Making Semiconductor Device Cool through HPC ab initio Simulations

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Oct. 1, 2017 to Sept. 30, 2019

Lawrence Berkeley National Laboratory

U.S. DOE Advanced Manufacturing Office Program Review Meeting
Washington, D.C.
June 11, 2019

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Overview

Project Title: Making Semiconductor devices cool through HPC ab initio simulations

Timeline:

Project Start Date: 10/01/2017

Budget Period End Date: 12/30/2018

Project End Date: 09/30/2019

Barriers and Challenges:

- Optimize the material and shape of interconnect, to reduce the heat generations
- Calculate the quantum transport for >1000 atom systems

AMO MYPP Connection:

- Advanced Sensors, Controls, Platforms and Modeling for Manufacturing

Project Budget and Costs:

Budget	DOE Share	Cost Share (in kind)	Total	Cost Share %
Overall Budget	$300,000	$60,000	$360,000	20%
Approved Budget (BP-1&2)	$300,000	$60,000	$360,000	20%
Costs as of 3/31/19	$300,000	$60,000	$360,000	20%

Project Team and Roles:

- Lin-Wang Wang (LBNL): Developing the code, and methods to be run on HPC
- Byounghak Lee (Samsung Inc): Using the code, and running jobs on HPC for interconnect systems

Project Objectives

- Electronics consumes more than 25% of the total electricity in U.S., and it is steadily increasing

- Interconnect on an semiconductor chip dominates the overall power consumption.

- As the size of the electronic device shrinks, the heat generation on an interconnect is getting worse.

- Current industrial used simulations package (TCAD) is based on continuous model, which cannot describe the atomic nature of the nanowire

- The goal of this project is to use atomistic, quantum mechanical simulations on HPC to investigate the electric conductivity on interconnect nanowires, and their heat generations, so they can be optimized.

Technical Innovation

Current practice:

- ❖ The current industrial device simulation tool (TCAD) uses continuous model, classical heat generation and transport equation.

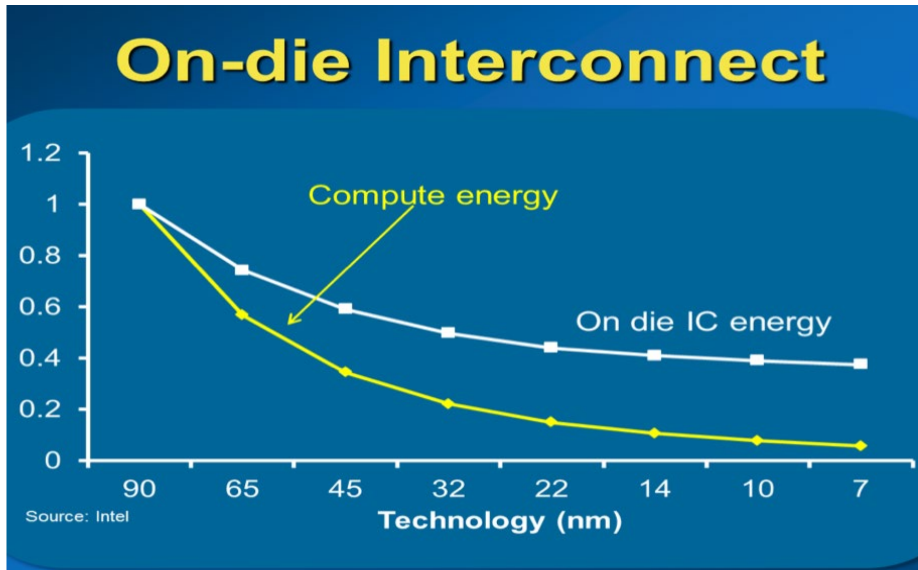
Limitations:

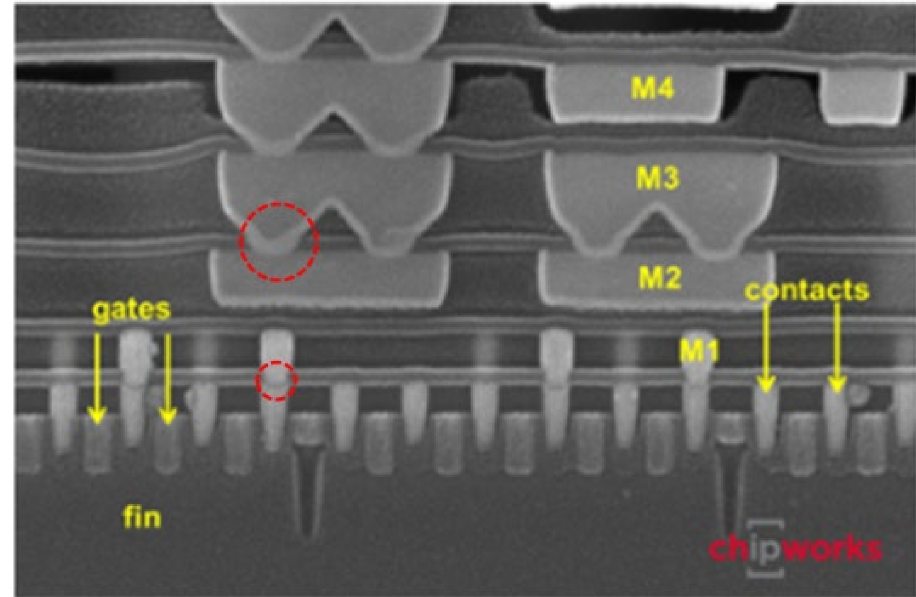
- ❖ When the interconnect nanowire size is in a few nm, the classical equation can fail, and realistic atomistic description becomes necessary
- ❖ For small nanowire, the quantum mechanical equation including wave function interference becomes necessary to describe the electron transport.

Approaches used in the current project:

- ❖ Using linear scaling ab initio quantum mechanics method to calculate the electronic structure and charge density in nanosize interconnect
- ❖ Developing linear scaling method to calculate the quantum transport in the interconnect
- ❖ Using the new methods, and simulations on HPC platform to understand and optimized the interconnect structure and material compositions

Technical Approach





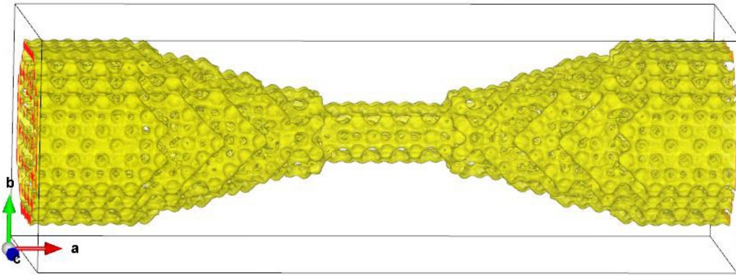
The total power consumption of an IC (white curve) versus the energies used by the computing unit (green curve). The difference between these two curves Represent the power consumption of the Interconnect.

A TEM cross section of a on die interconnect. The biggest heat generation happens at the smallest interconnect.

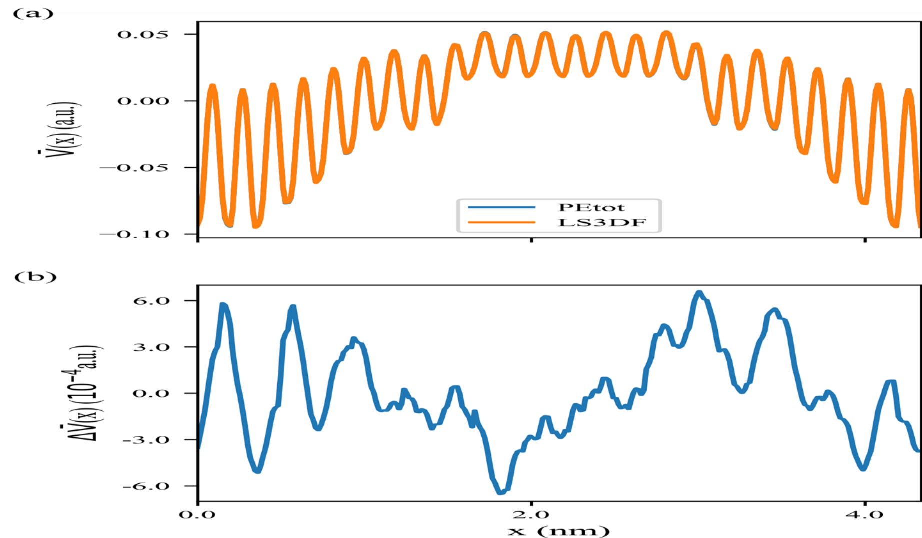
Technical Approach

A linear scaling 3 dimensional fragment (LS3DF) method for large system (>10,000 atoms) electronic structure calculations. The method divides a large system into many fragments, and uses many small groups of computer processes to calculate these fragments, then patch the charge densities of these fragments together to yield the charge density of the original system for Poisson equation solution.

Technical Approach

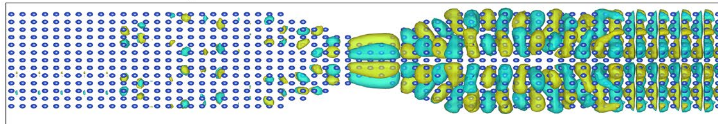


A >2000 atom Cu, self-consistent calculation using quantum mechanical density functional theory (DFT), with the linear scaling three dimensional fragment (LS3DF) method on Titan machine in ORNL

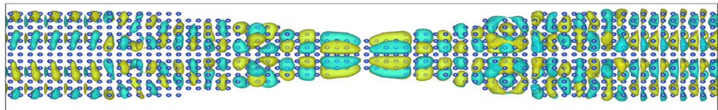


The cross section averaged potential (upper panel) and their difference between the LS3DF method and direct DFT method (lower panel), showing the accuracy of the LS3DF method. For large systems, the LS3DF method is hundreds of times faster than direct DFT method.

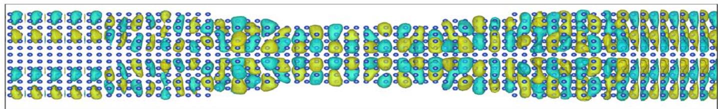
(a) system I ($T_n = 0.226$)



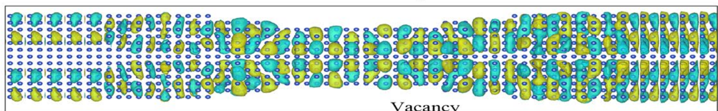
(b) system II ($T_n = 0.744$)



(c) system III ($T_n = 0.683$)

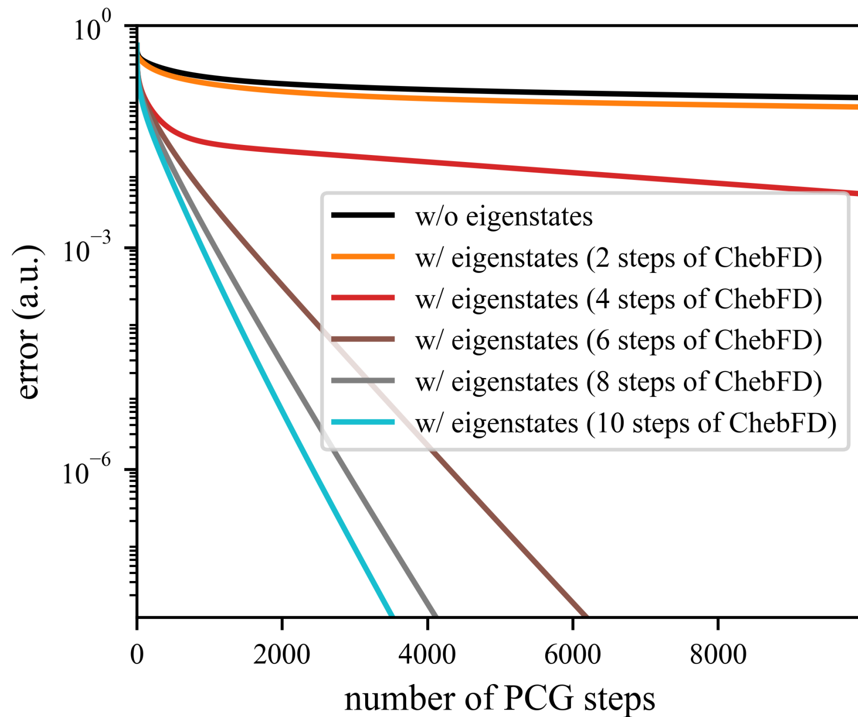


(d) system III with a vacancy ($T_n = 0.672$)



An electronic scattering state injected from the right hand side of the interconnect wire, passing through the bottlenecks of interconnects with different shapes. The initial incident wave function is the same for these cases. Tn is the transmission coefficient.

Technical Approach



A preconditioning method is used to accelerated the calculation of the scattering state. The acceleration depend on the steps of Chebyshev filter applications.

system	N_{Cu}	R (nm)	L (nm)	T
I	3996	0.5	2.0	0.187
II	3660	0.5	5.0	0.181
III	4140	0.75	5.0	0.349
III*	4139	0.75	5.0	0.353

The total transmission T (which is proportional to the conductivity) of different interconnect shapes. The R is the radius of the interconnect neck, while L is the length of the interconnect center part. The results like this can be used to help the design of optimal interconnect shapes.

Results and Accomplishments

- Successfully applied the LS3DF method on Cu system for interconnect simulation
- Developed an accelerated method to calculate the scattering states for large system quantum transport
- Simulated the Si nanowire interconnect for different shapes, provided data to optimize the interconnect
- Calculated the finite temperature effect, and the heat generation (will be finished within next two months).

Transition

- Technology Readiness (TR) level of 4 (for atomistic device simulations beyond the current continuous model) anticipated by project end.
- Will be used in future beyond Moore's law device simulations
- Samsung is interested in using this new approach to calculate quantum transports in some of their R&D.