Large Area SiC Gate Turn Off (GTO) Thyristor Development

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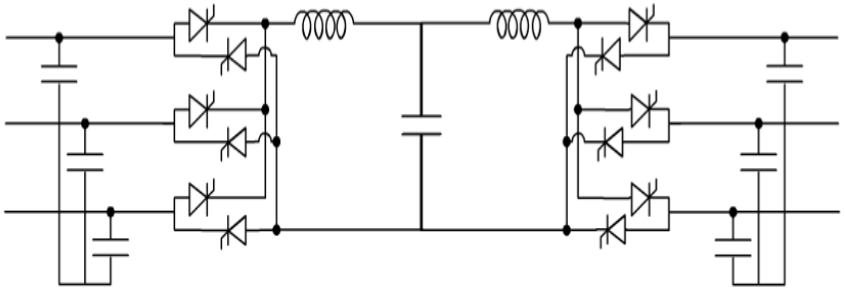
Why Silicon Carbide Power Devices?

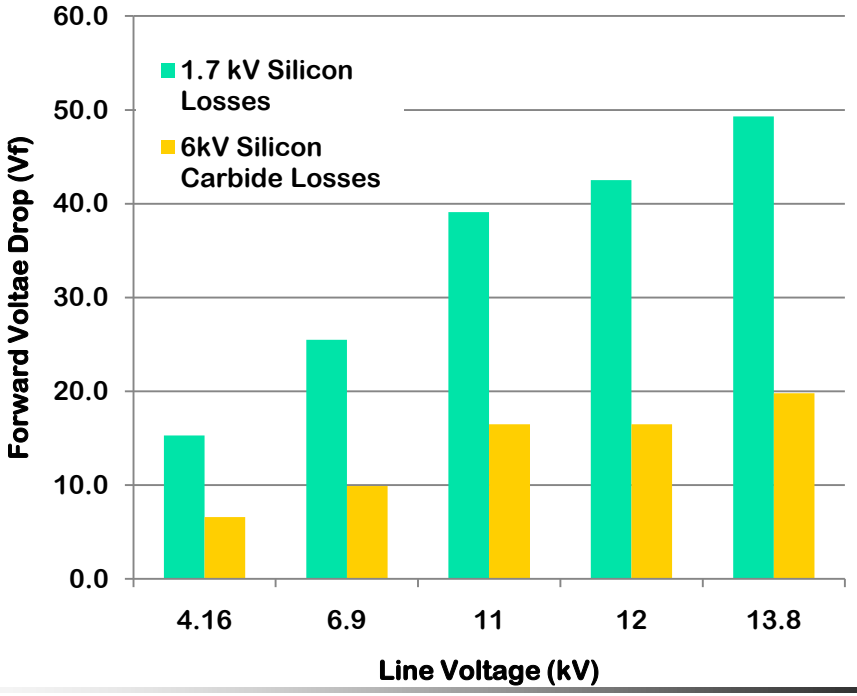
Property - Silicon Carbide vs Silicon	Performance of SiC Power Device	Impact AC-DC/ DC-AC circuits
Breakdown Field (**10X**)	Lower On-state Voltage drop for 5-20 kV Devices (**2-3X**)	Higher Efficiency of circuits
Smaller Epitaxial Layers (**10-20X**)	Faster Switching speeds (**100-1000X**)	Compact circuits
Higher Thermal Conductivity (**3.3-4.5 W/cmK vs 1.5 W/cmK**)	Higher Chip Temperatures (**250-300°C instead of 125°C**)	Higher continuous current densities, Higher pulsed power
Melting Point **(2X)**	High Temperature Operation (**3X**)	Simple Heat Sink
Bandgap **(3X)** (**10^{16}X** smaller n_i)	High Intrinsic Adiabatic Pulsed Current Level (**3-10X?**)	Higher Current Capability

SiC Thyristors – Wide Applicability

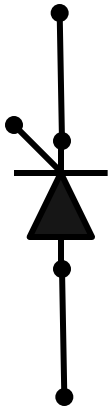
- Grid-Tied Energy Storage Power Conditioning – AC/DC; DC-AC; DC-DC
- FACTS Elements
  - Static VAR Comp.
  - STATCOM
  - TCSC (Series Comp.)
  - Static Sync. SC
  - Univ. Power Flow C.
  - Interline PFC
- HVDC



Courtesy: Princeton Power Systems

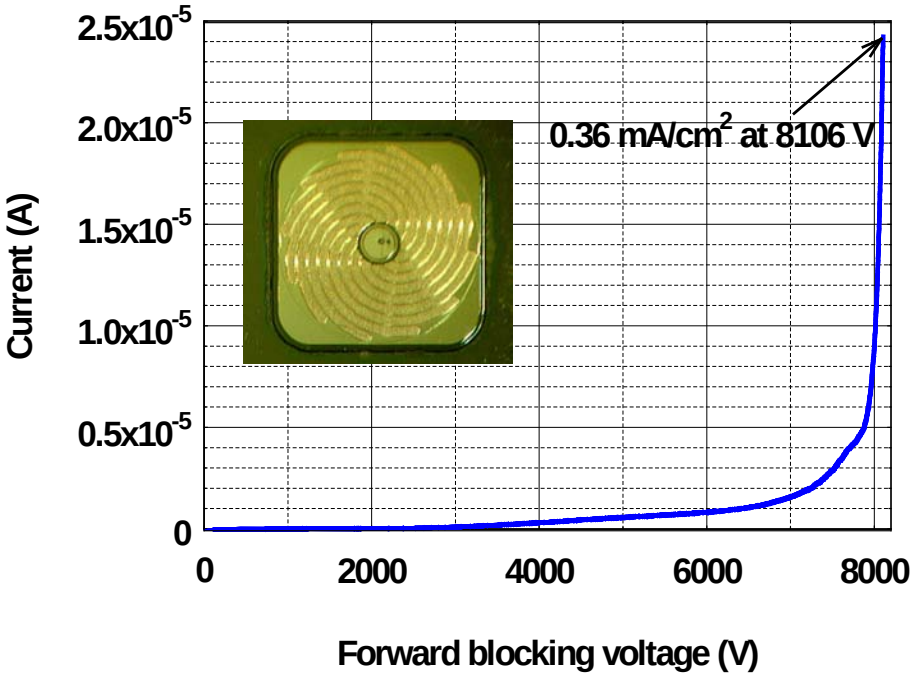


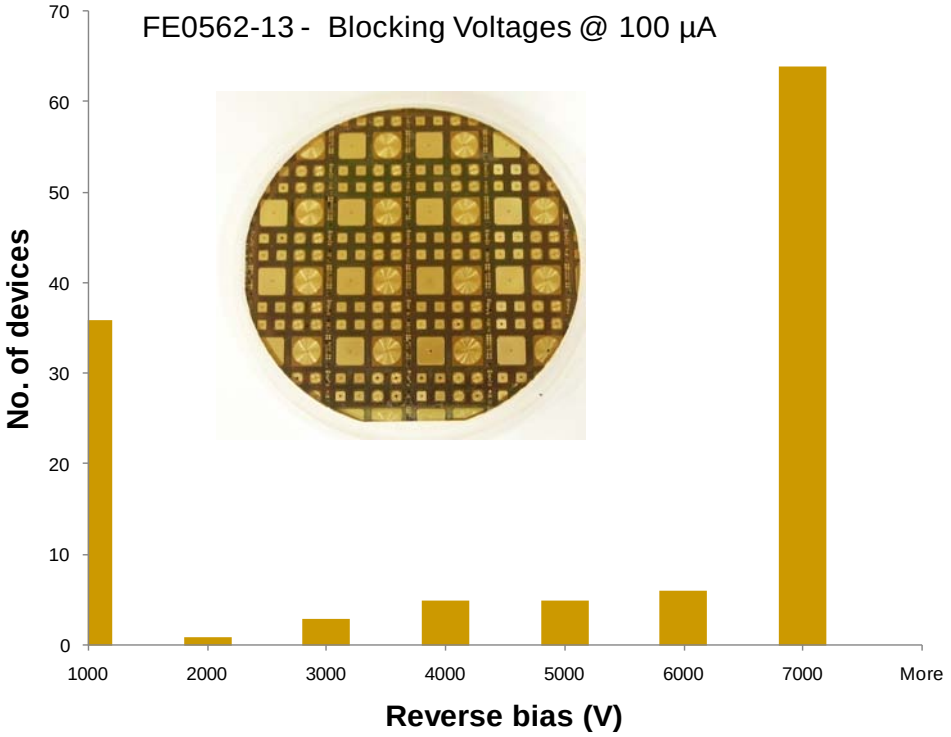
Goals: Specs for Devices/Modules



- Voltage 15 kV (Phase II Target)
- Current >100 Amp
- Frequency >20 kHz
- Fully Soldered Packaging on all terminals

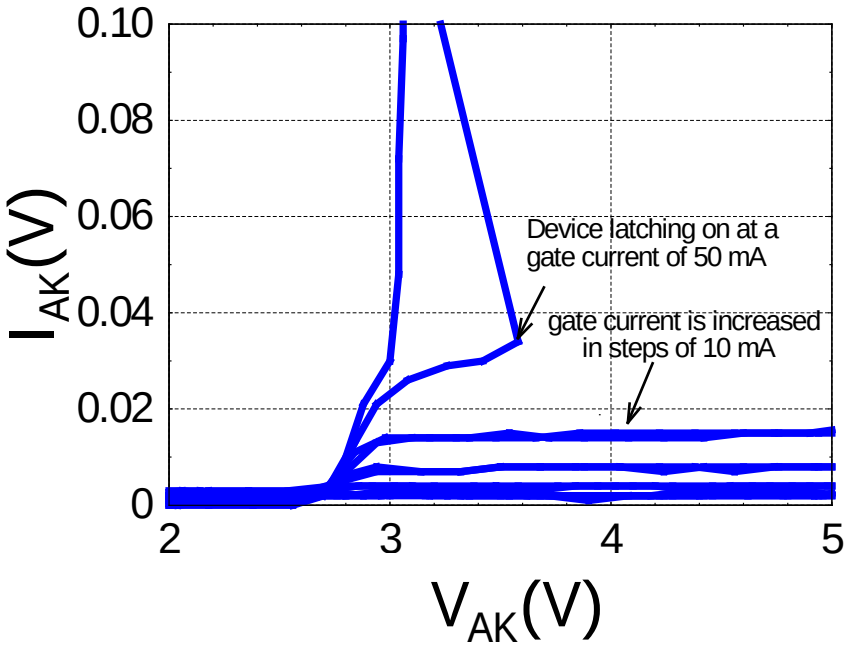
Forward blocking characteristics

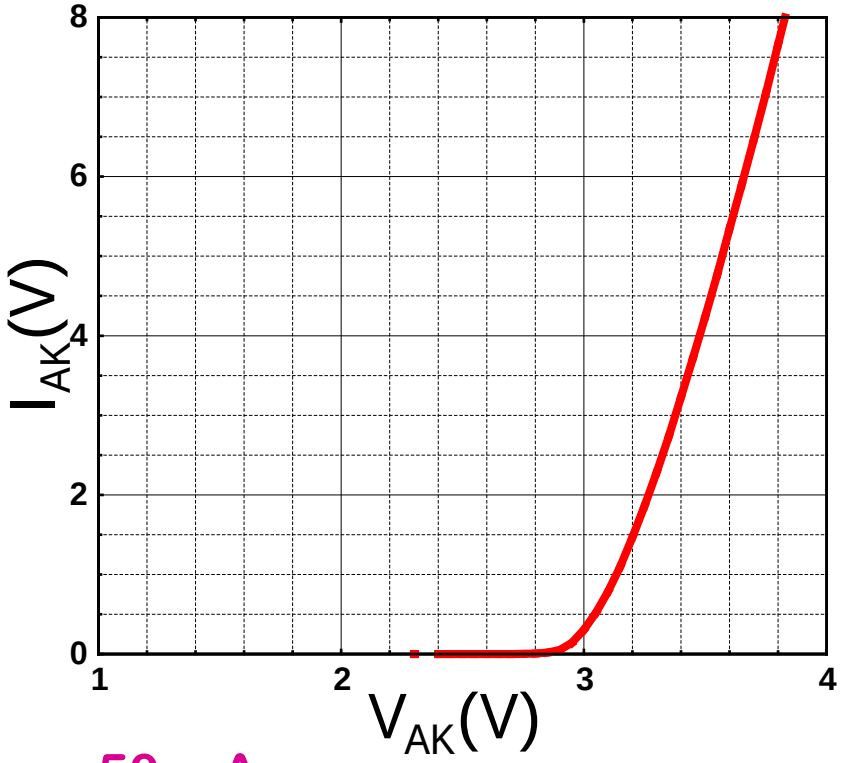




Forward blocking voltages in excess of 8000 V were achieved

On-state performance





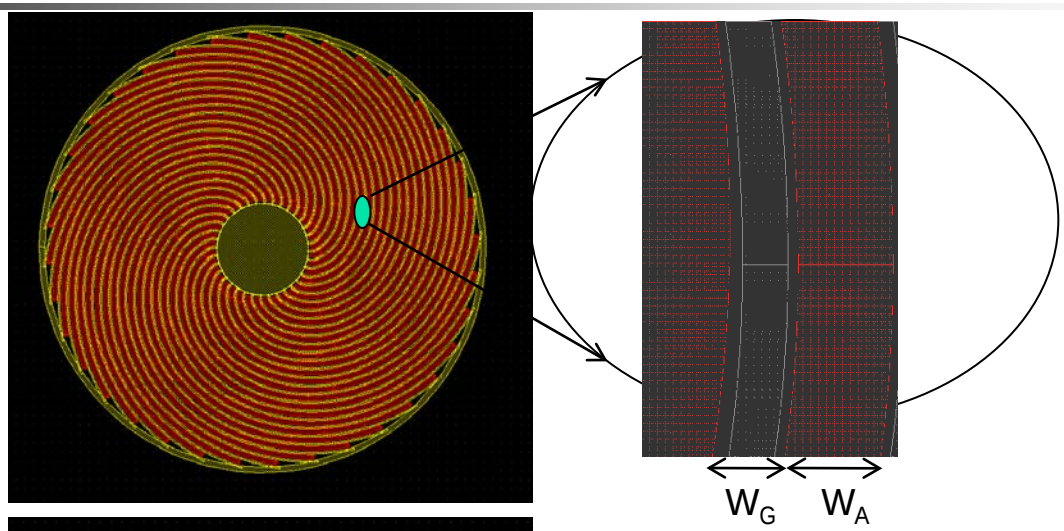
Gate trigger currents as low as 50 mA

Von as low as 3.8 V @ 100 A/cm^2

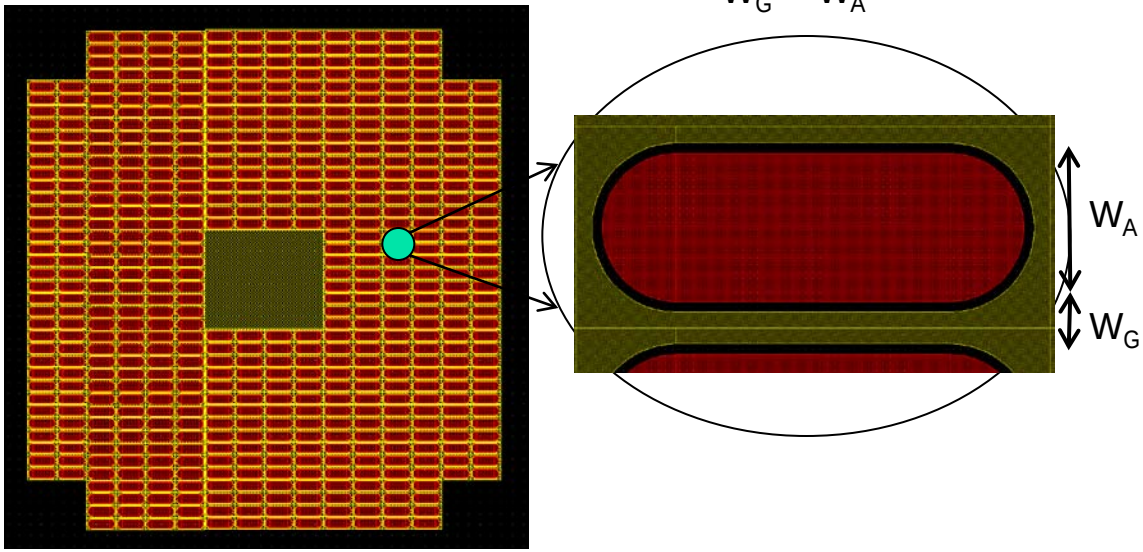
Differential Ron,sp as low as 5 mΩ-cm^2

Device Designs

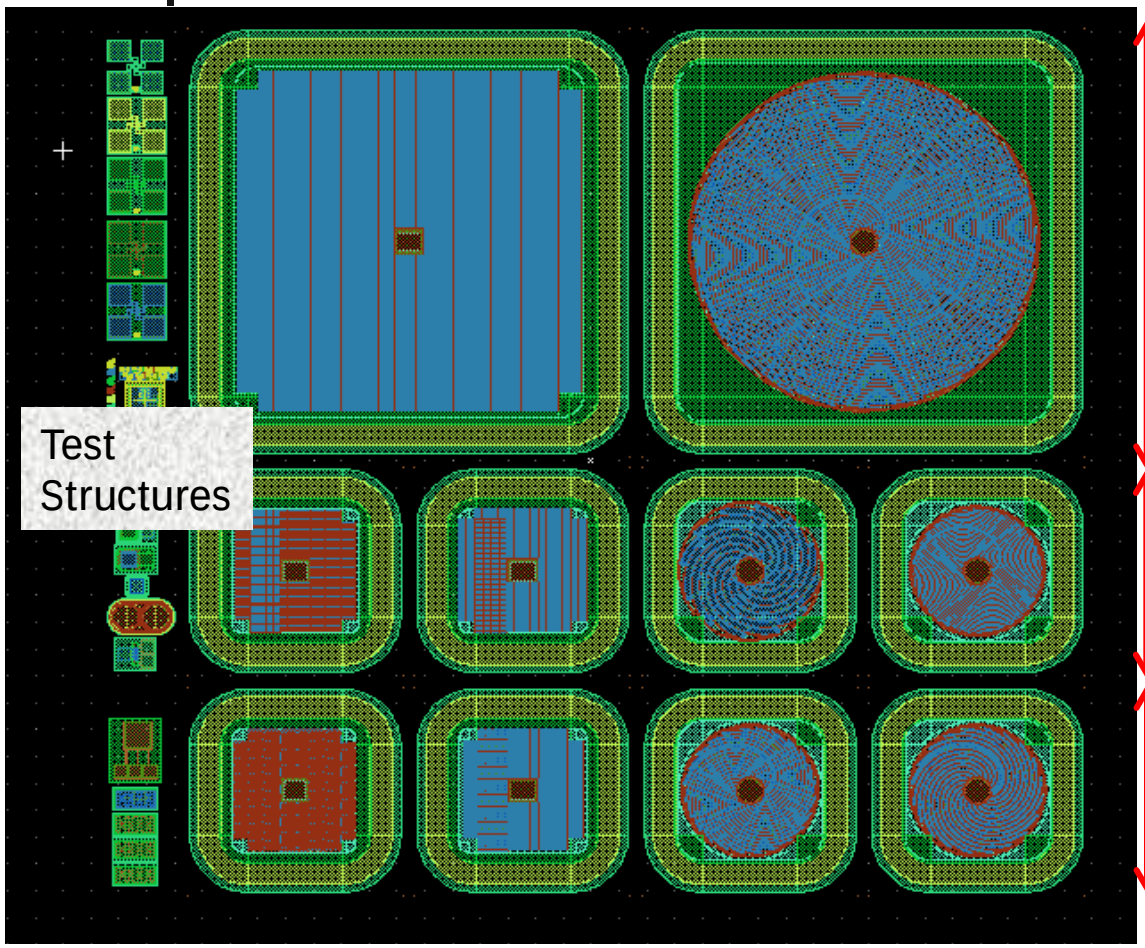
Involute



Cellular

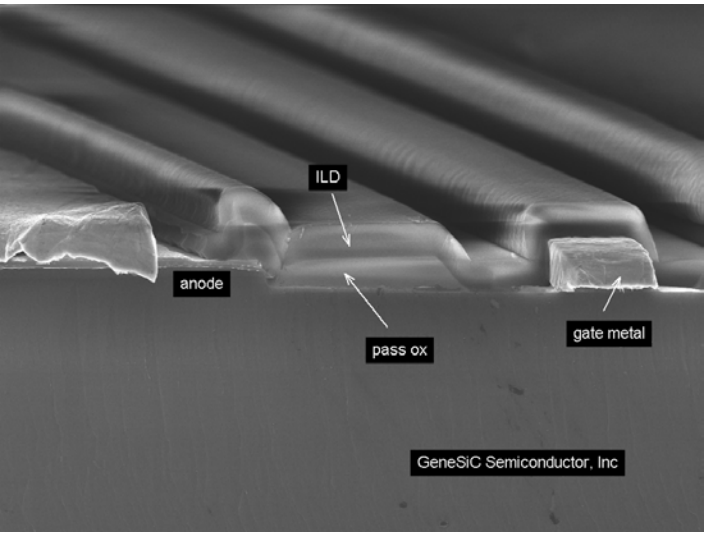


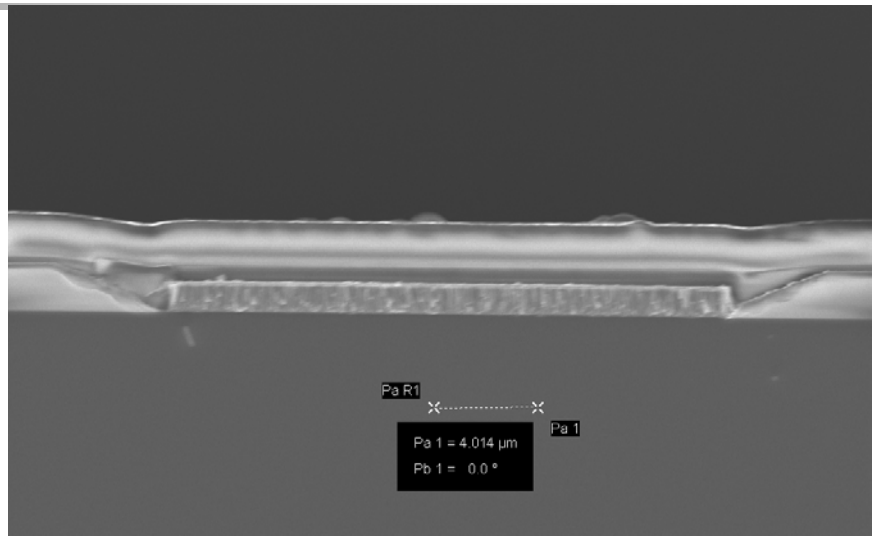
Device Layout



Pattern	W_A(μm)	W_G(μm)
Involute	24	21
Involute	48	21
Involute	48	34
Involute	117	21
Cellular	24	15
Cellular	24	24
Cellular	42	15

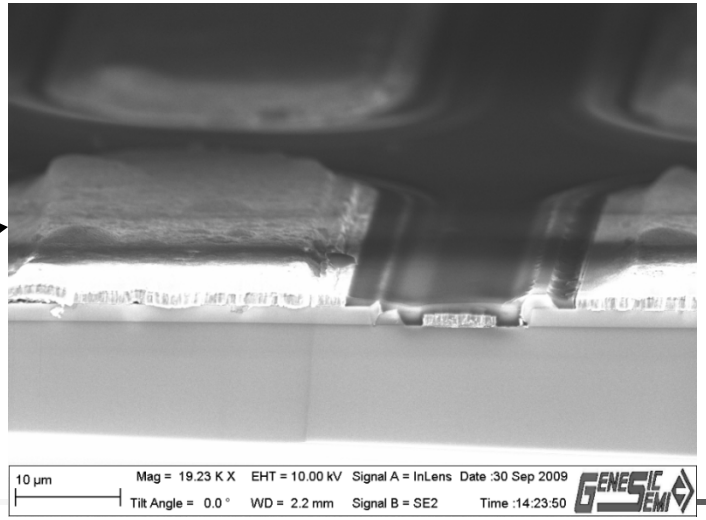
Device Processing – metallization, surface planarization



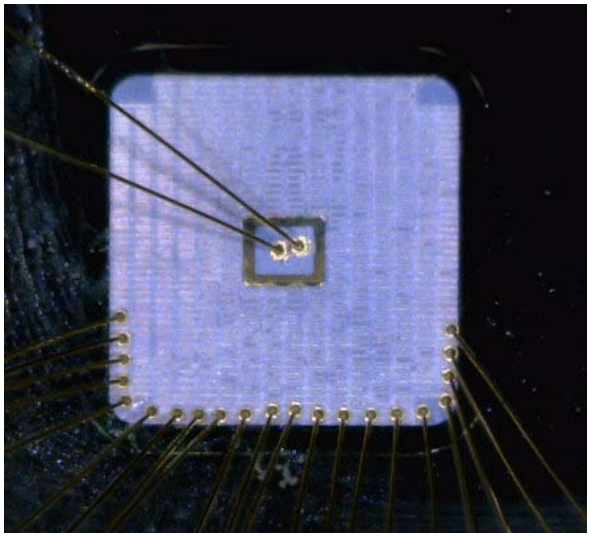


No surface planarization

With surface planarization



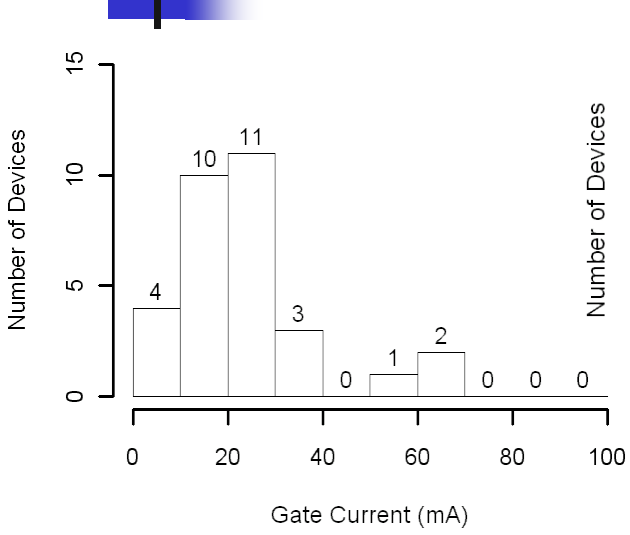
Device Packaging



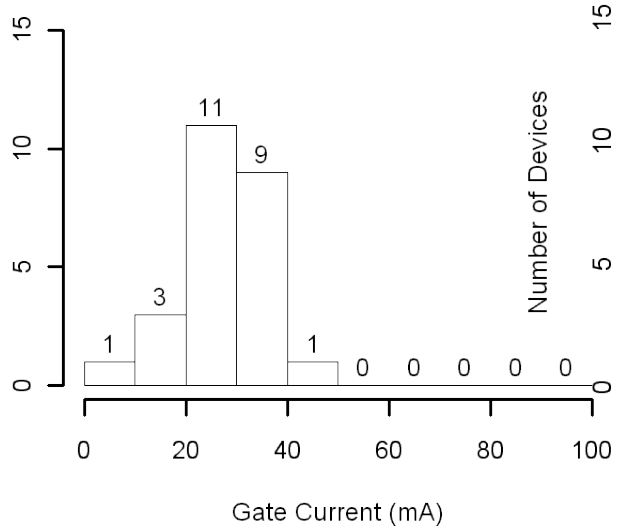
Custom designed package capable of >10kV operation

Soldered contacts are being worked upon, but Metallization integrity was good for multiple wire bonds

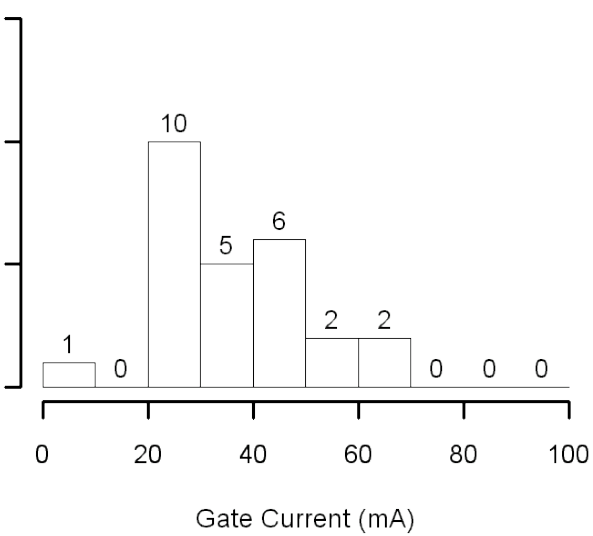
On-state performance – influence of anode width



117 µm wide anode, 21 µm wide gate
12 gate fingers



48 µm wide anode, 21 µm wide gate
24 gate fingers

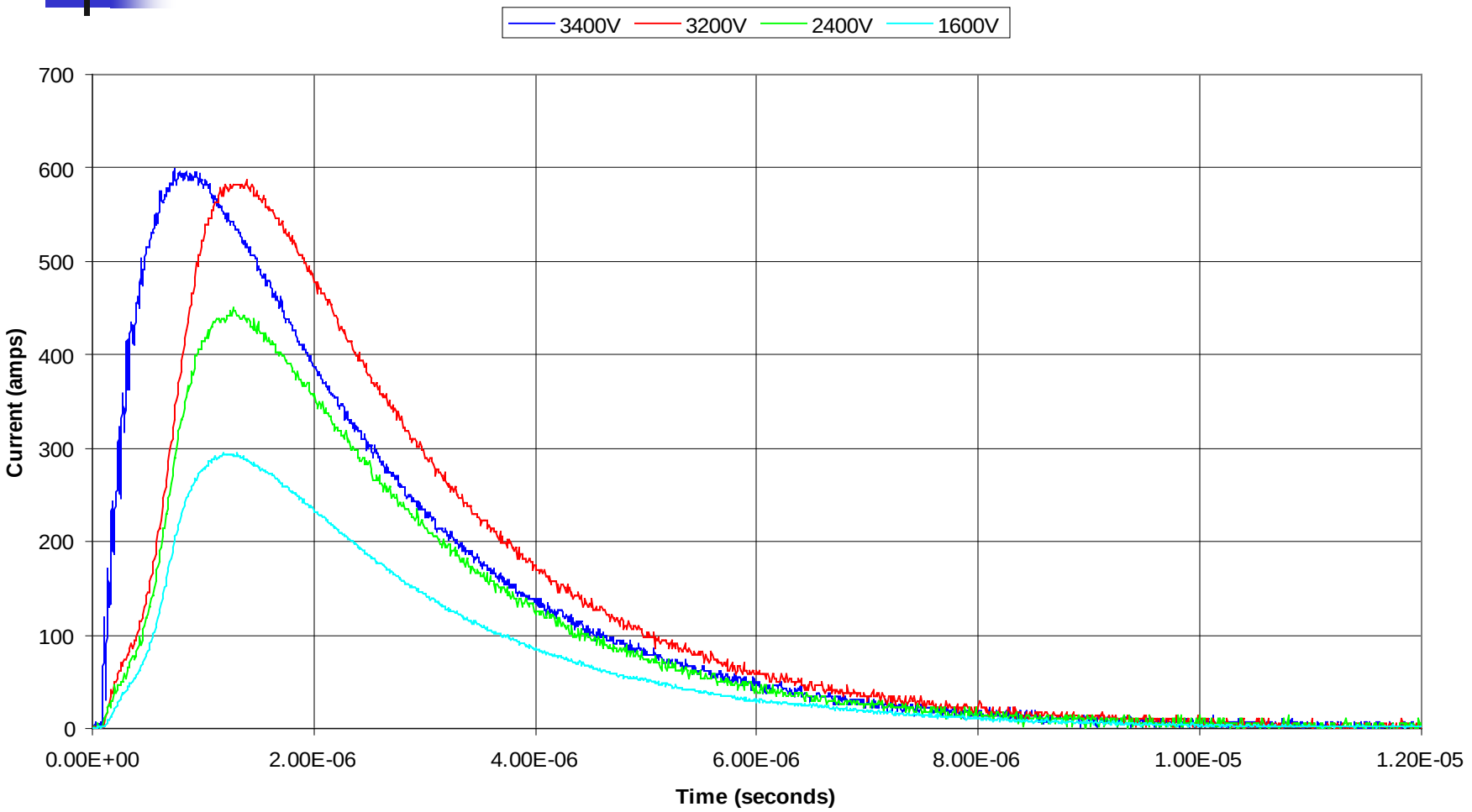


24 µm wide anode, 21 µm wide gate
36 gate fingers

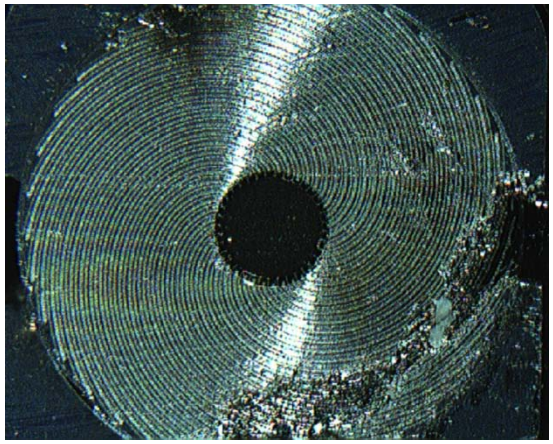
For involute devices, gate trigger current decreases with increasing anode width, due to smaller number of parallel gate fingers originating from central gate pad.

Ron,sp is the range of 5-6 mΩ-cm^2 for all designs implying negligible resistance contribution from ohmic contacts.

Pulsed Measurements conducted to test failure limits of Thyristors



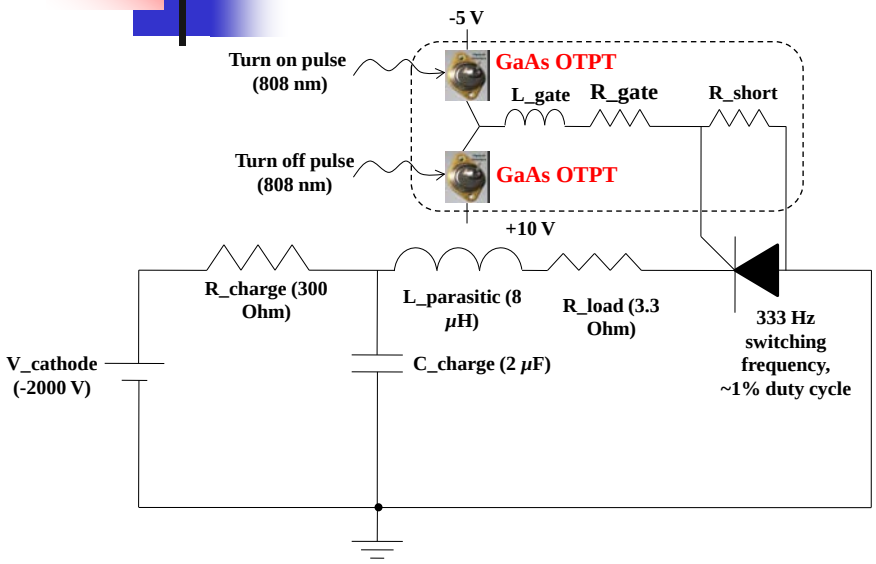
Optical micrographs after failure



With metallization intact

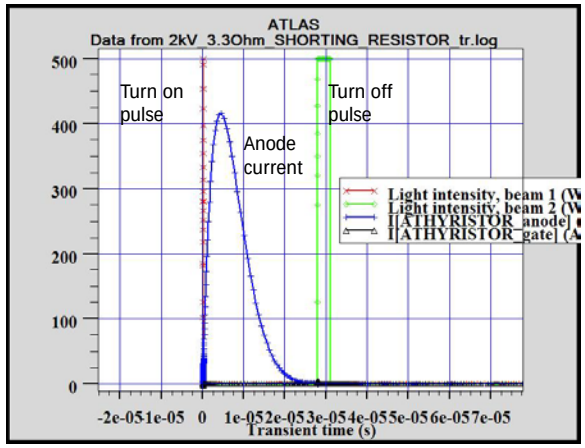
After metallization was etched off

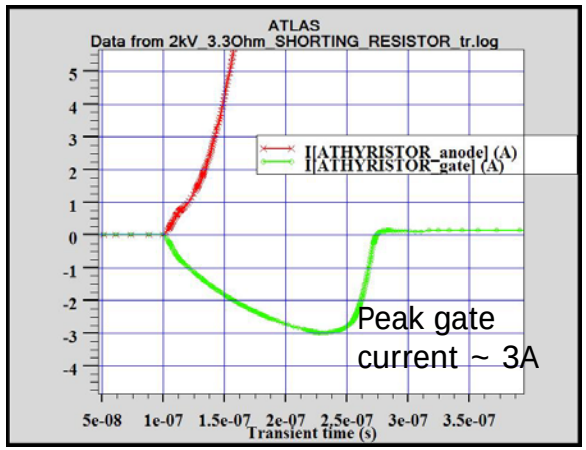
Optically Controlled SiC Thyristors for stacked serial operation

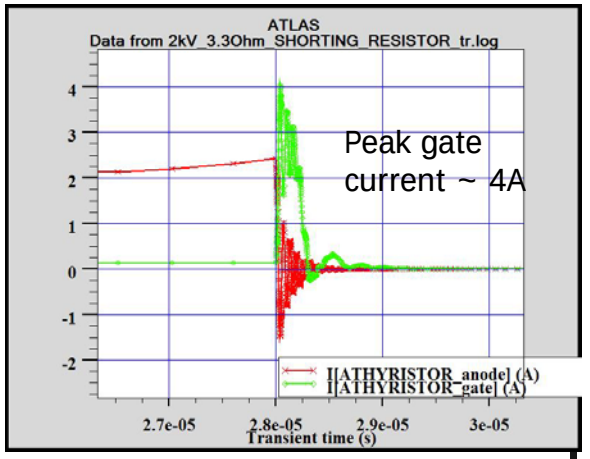


- Higher Electromagnetic Noise Immunity
- Enhanced Electrical Isolation
- Rapid Turn on due to Direct
- Photogeneration

Courtesy: Univ. Illinois (Prof. Mazumder)







Conclusions

- First Batch of 8000 V GTO Thyristors show exceptional performance – near theoretical blocking voltages and low on-state losses
- Significant device design, processing and characterization developed at UHV levels
- In pulsed mode, over 600 A of current was conducted through a single 4 x 4 mm device
- Next Steps:
  - Build 12 kV Thyristors
  - Finish switching characterization
  - Determine high temperature limits
- Find Strategic Partners for insertion for commercialization