U.S. DEPARTMENT OF ENERGY | OFFICE OF ELECTRICITY

PACE
ACCELERATING ELECTRIFICATION

IPS Hardware Prototype Development

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Project Status: Ongoing **Project Term: 07/20 - 09/23** **Partners: Oak Ridge National Laboratory**

Project Summary

The Objective of this project is to develop and demonstrate the intelligent power stage (IPS), which is an interoperable plug-and-play power stage with embedded intelligence and online health monitoring capability. Through the standardized communication interface, IPS can provide sufficient component level status information to interact with the Smart Universal Power Electronics Regulator (SUPER). The IPS developed in this project consists of an isolated DC/DC converter stage, a three-phase inverter stage, self-maintained auxiliary power supplies, sensors and a powerful control platform with communication channels. The UA IPS prototype is a 480-V grid-tied inverter rated at 50-kW. The performance of the IPS and its advanced features will be firstly demonstrated at UA and then at ORNL for additional testing and demonstration with SUPER.

Technical Approach

The advanced features of the IPS design include (1) the ability to identify the external parameter (e.g., LCL filter parameters); (2) online health monitoring and prognosis, e.g., DC link capacitance monitoring with capacitor end-of-life (EOL) indication; and (3) advanced gate driving with the ability to control the voltage overshoot, switching loss and dv/dt. In addition, the UA IPS has various innovations in the converter hardware design, such as the high-efficiency high-density silicon carbide (SiC) power stage and high frequency transformer.

Accomplishments

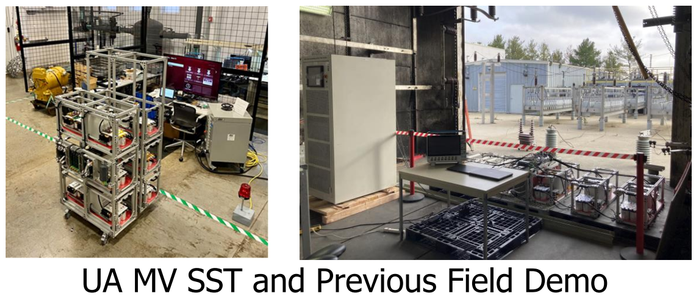
- External parameter identifications, such as LCL parameters, to enhance interoperability;
- Onboard health monitoring and prognosis to enhance reliability and resiliency;
  - Junction temperature estimation for the SiC power modules used in IPS
  - DC link capacitance identification and Capacitor end-of-life (EOL) indication
- Advanced gate driving with optimized multi-stage turn-off and reduced voltage overshoot
- Developed IPS controller platform with standardized communication interface
- Completed the IPS power stage hardware develop and validation at rated power.

Impact/Commercialization

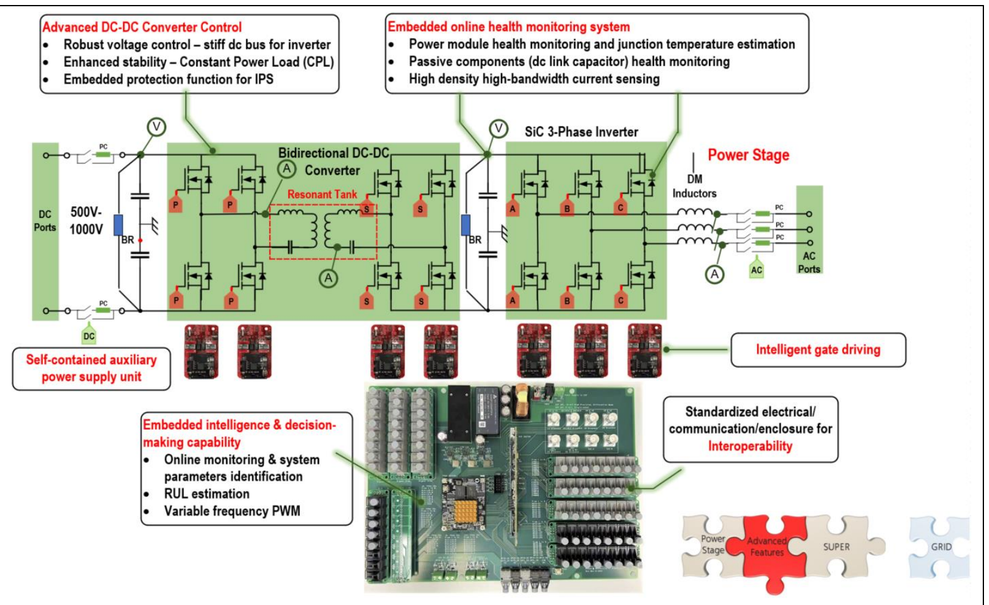
The advanced features developed for IPS will enable its situational awareness, enhance the interoperability and system reliability. Further with the standardized architecture, the IPS can be easily connected to the generic testing environment or standardized SUPER to demonstrate advanced grid functionalities.

Future Work

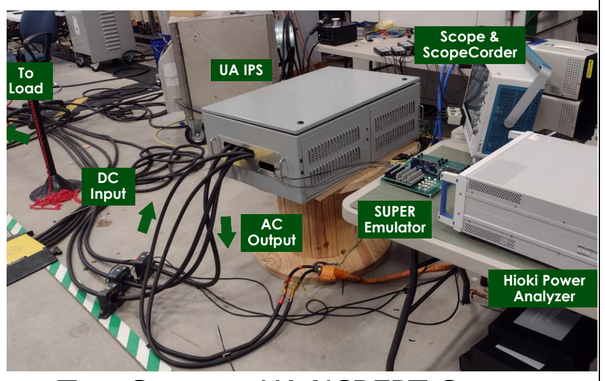
- IPS System TRL enhancement
- Seeking field demonstration opportunities for grid-tied inverters with advanced features.
- Develop and demonstrate medium -voltage (MV) IPS system with advanced features.



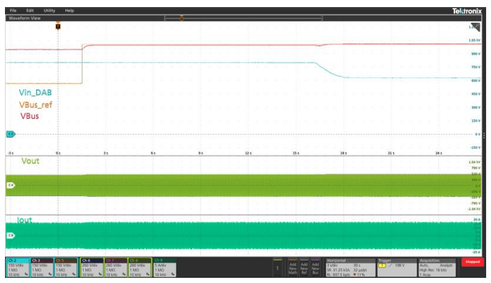
UA MV SST and Previous Field Demo



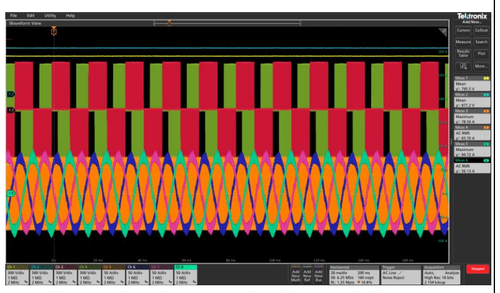
UA IPS Hardware



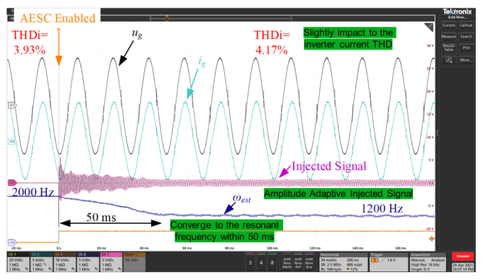
Test Setup at UA NCREPT Center



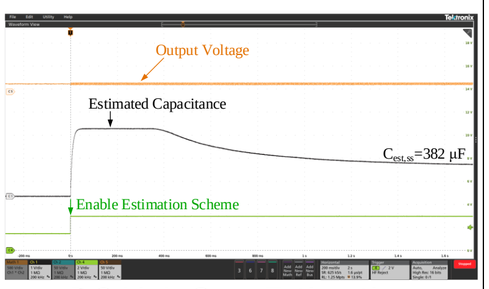
IPS Dynamic Performance



Steady State @ Rated Power



LCL Resonant Freq. Estimation



DC Link Cap. Estimation