High Voltage, High Power WBG Module Development

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Project Summary

WBG Devices enable next generation power converters

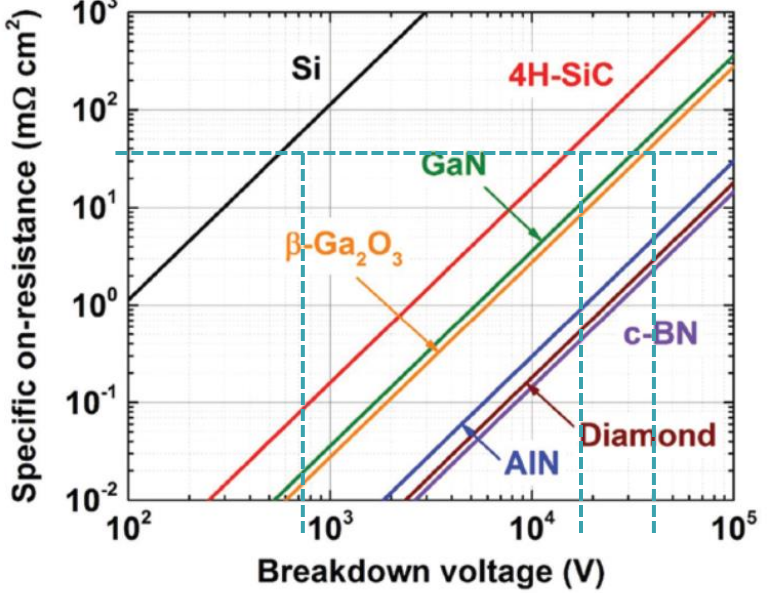
Wide Bandgap (WBG) materials (SiC, GaN) have benefits for power converters

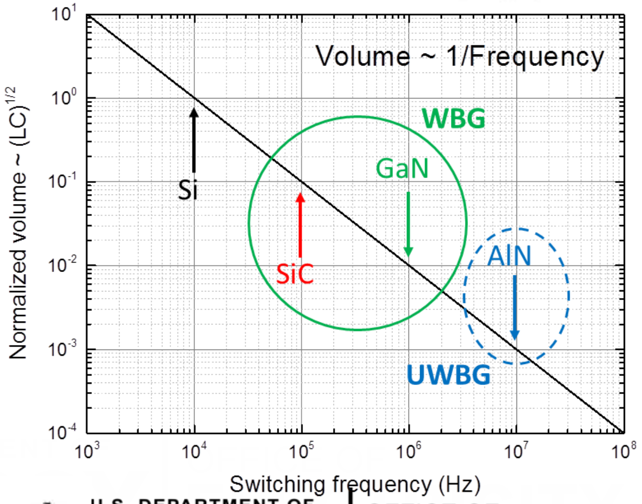
- ***High critical field***
    - High voltage hold-off for given resistance
        - Fewer cascaded devices
        - Significantly simplifies stack turn-off and synchronization
    - Low resistance for given voltage hold-off
        - Smaller devices → lower capacitance
        - Faster switching with fewer losses
        - Results in smaller converter passives → higher power density

- Over past 20 years, WBG die yield has ***rapidly improved***
    - Elimination of fabrication and growth defects
        - *e.g.,* micropipes, basal plane dislocations
    - Steadily increased ***operational voltages and current handling***
        - 10 kV engineering die available since ~2012
        - Current SOA: Single 3.3 kV devices

→ No 3.3 kV modules commercially available due to ***limitations in module packaging*** resulting in degraded ***performance and reliability***

Vertical unipolar device:
FOM = $V_B^2/R_{on,sp} = \varepsilon \mu_n E_C^3/4$





Project Summary

WBG Devices enable next generation power converters

- Traditional module packaging has multiple limitations
    - Limit wide-scale commercial availability of high voltage, high power SiC modules
        - Large parasitics, poor thermal management → limit converter power density
        - Packaging encapsulation, die/package interfaces → limit long-term reliability
        - High cost → limits widespread applicability
- ***Revolutionary module design improvements*** needed to target packaging limitations
- ***Enable high voltage/high power WBG packaging solutions for next-generation power electronics***
- ***This project will***
    1. Develop packaging solution that targets key limitations in WBG module packaging
    2. Demonstrate 3.3kV/120A multi-chip full-bridge module
    3. Evaluate performance and long-term reliability of modules

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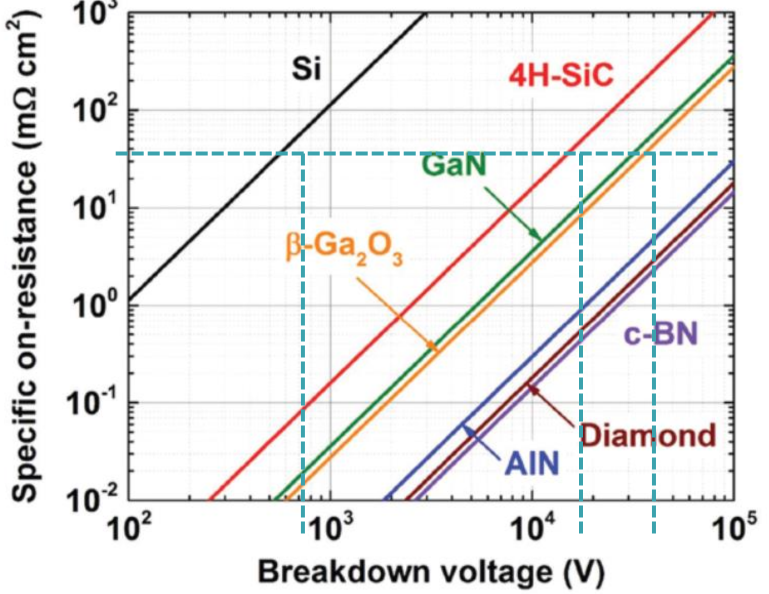
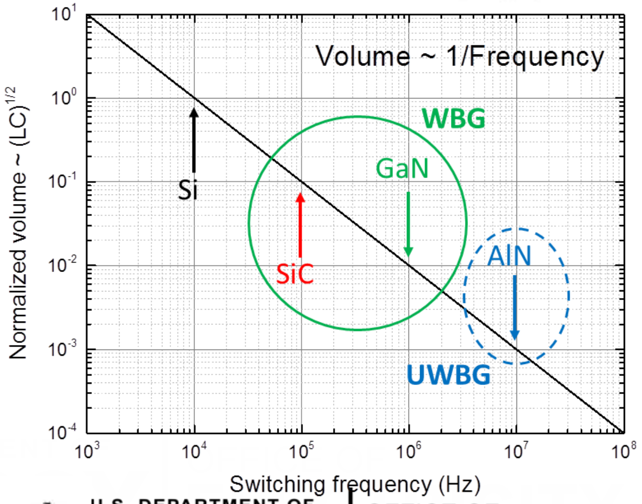




The Numbers

- DOE PROGRAM OFFICE:
  OE – Transformer Resilience and Advanced Components (TRAC)
- FUNDING OPPORTUNITY:
- LOCATION:
  Albuquerque, New Mexico
- PROJECT TERM:
  01/01/2023 to 01/01/2025
- PROJECT STATUS:
  Ongoing
- AWARD AMOUNT (DOE CONTRIBUTION):
  $500,000
- AWARDEE CONTRIBUTION (COST SHARE):
  $0,000
- PARTNERS:
  Sandia National Laboratories, Stonybrook University

Technical Approach

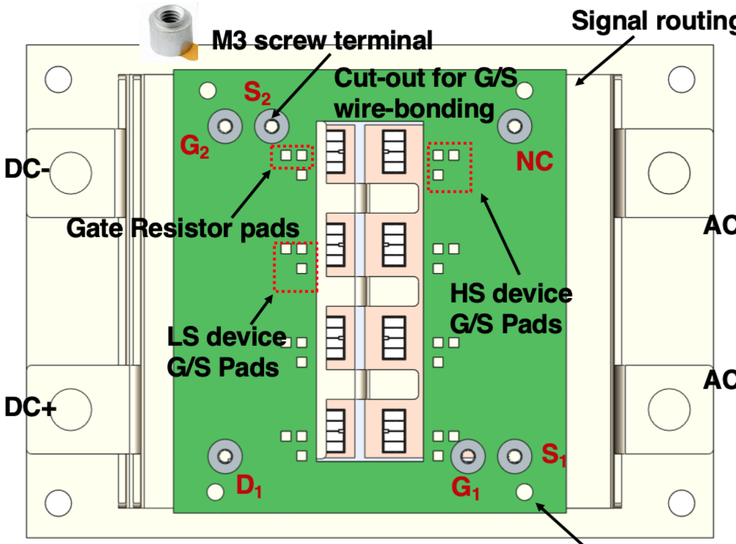
Task 1 (SUNY): High current bonded module (3.3 kV, 120A)

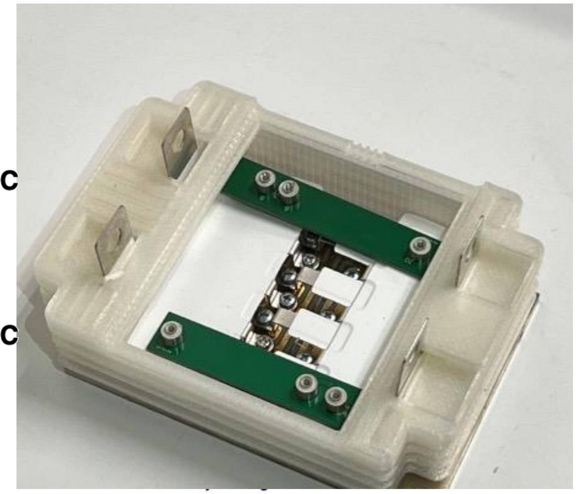
Goal: develop WBG-specific ***3.3kV, 120A multichip full-bridge module,*** compatible with current HV Si IGBT module (XHP) form factors

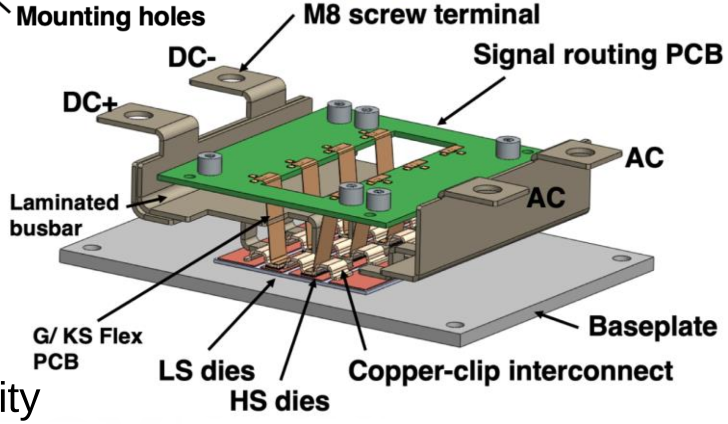
- Optimized multichip paralleling layout
- Flexible PCB for signal routing
    - ultra-low power loop inductance
        - Improves dynamic current sharing of paralleled devices
        - Reduces temperature differences among all devices

- Wire-bonded-less (Ribbon Bonded) interconnects
    - higher current capability
    - lower inductance
    - increased top-side cooling
    - increased reliability.

- Design for reliability
    - AlN substrate with AlSiC baseplate → closer CTE mismatch
    - Pressure-less nanosilver paste for die → high thermal conductivity and low void content
    - Pressure-assisted nanosilver sintering substrate-to-baseplate → high thermal conductivity







Technical Approach

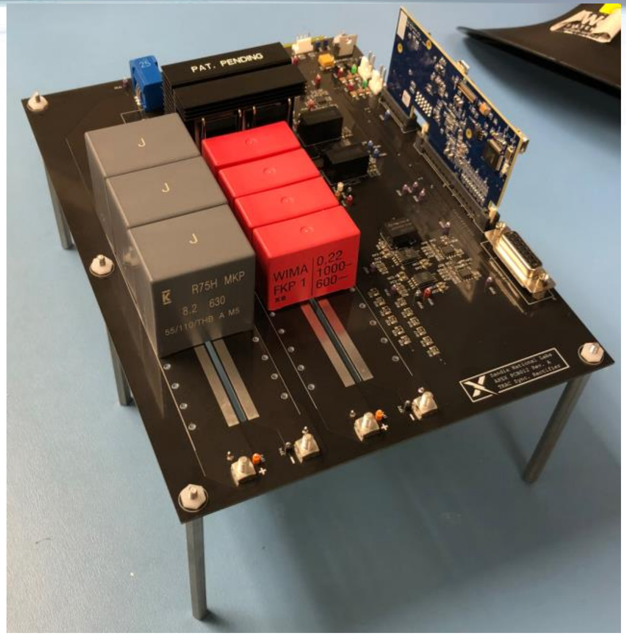
Task 2 (Sandia): Module Reliability and Performance Evaluation

Evaluate module performance and long-term reliability

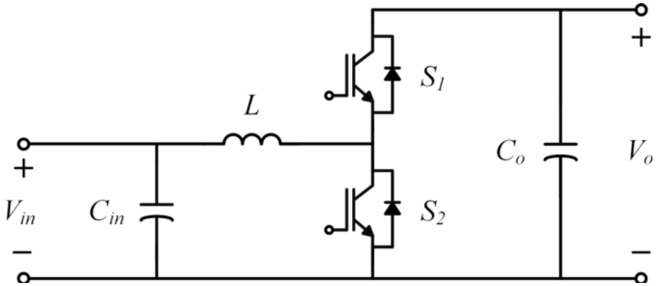
- High temperature reverse bias
  - Evaluate E-field driven failure mechanisms
- Inductive Switching/Double Pulse
  - Switching Time/Energy

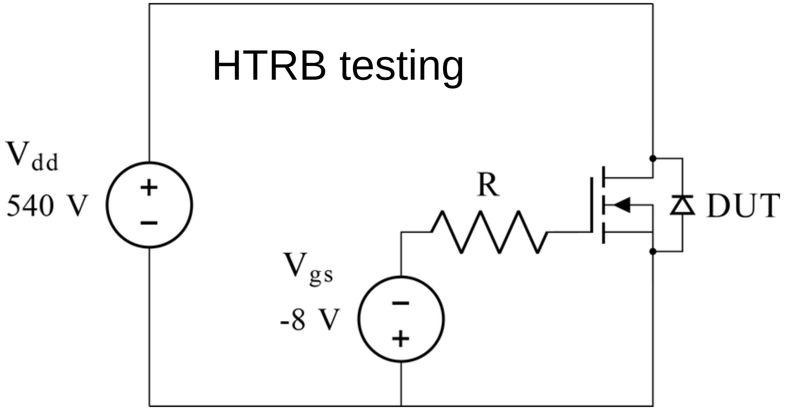
Evaluate dynamic performance of the modules in operational converter

- Simplified DC/DC converter to be fabricated
  - Scale 10kW synchronous rectifier board (previous TRAC project)
  - Switching characterization under realistic switching schemes in exemplar circuit.

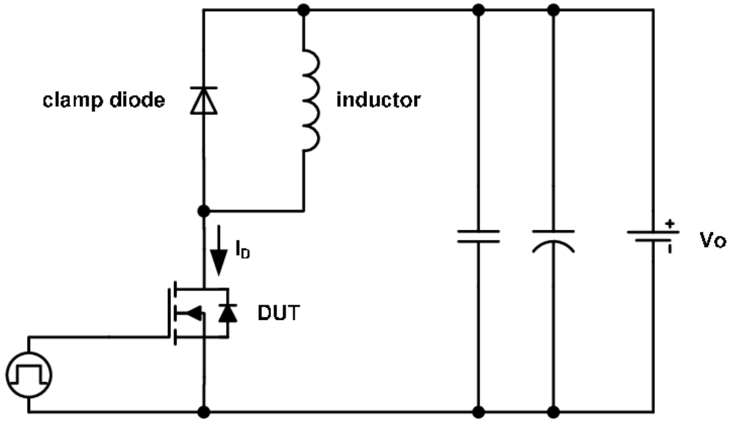


Synchronous Rectifier





HTRB testing



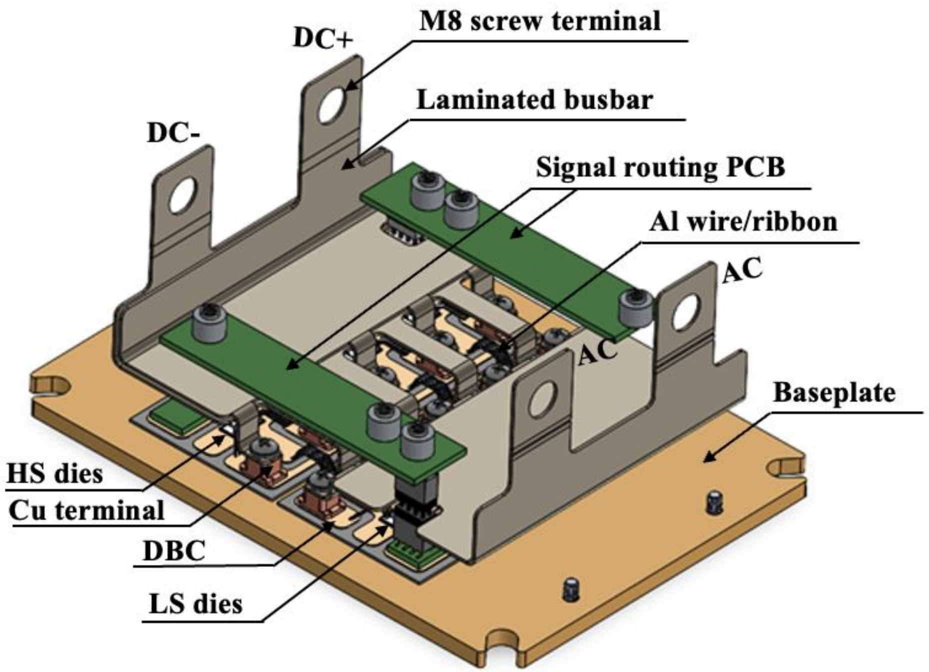
Inductive Switching

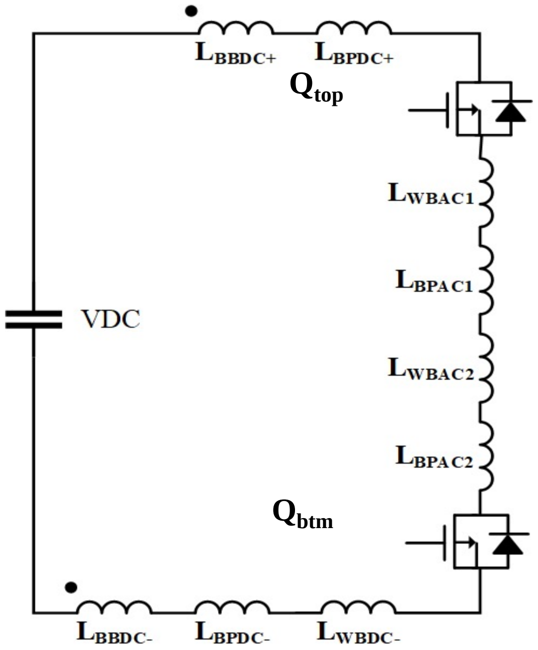
Accomplishments

- **Preliminary design for a 3.3 kV SiC module**
  - Industrial standard XHP 3 packaged
  - 3.3 kV/400A half-bridge configuration
  - 4 SiC MOSFETs paralleled at each switching position

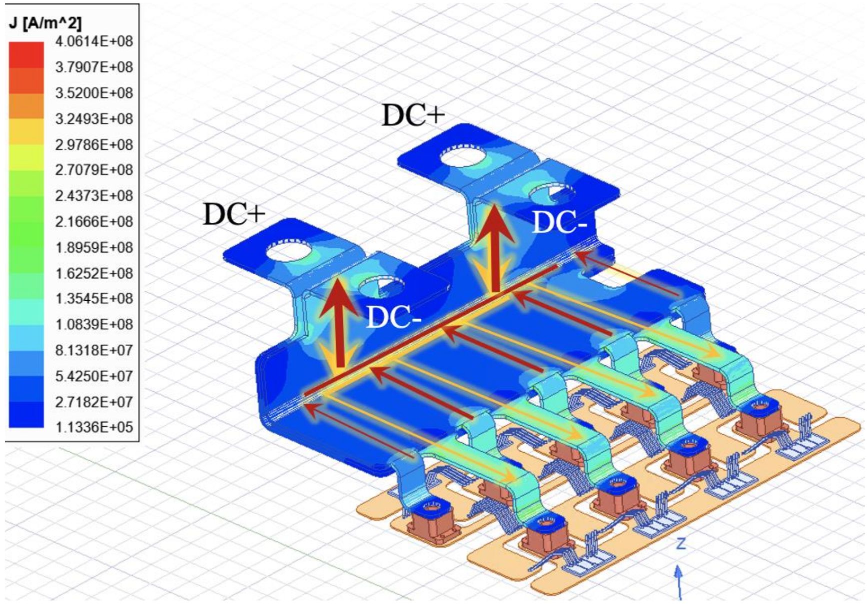
- Power loop inductance calculated by ANSYS Q3D
  - DC bus bars
  - DBC copper
  - SiC devices
  - Al bonds included in calculation

- **Power loop inductance:** 9.0 nH
- 149.1 W per die (100 kHz @ 4 kW/m^2·°C convection)





Extracted parasitic network



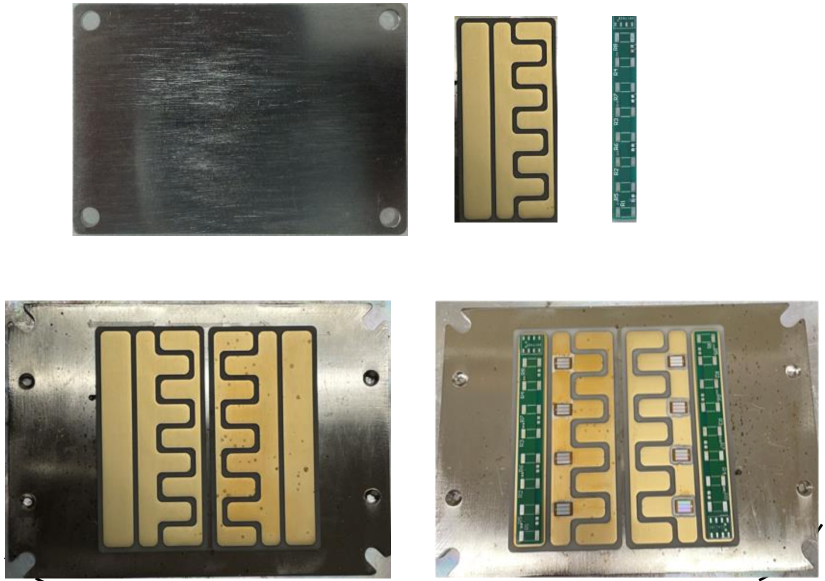
Vertical commutation loop

Accomplishments

- Preliminary module design fabricated with ceramic chips
- Fabrication of all the mechanical and electrical interconnections
  - DBC, bottom PCB, ribbon bonds, Cu terminal attachment, laminated busbars, encapsulation, housing

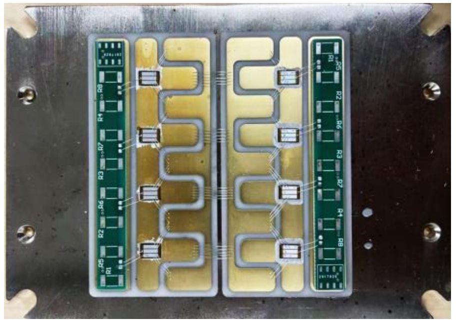
Attaching DBC, Die and bottom PCB

- ➢ Stencil
- ➢ SAC305 solder paste reflow x3



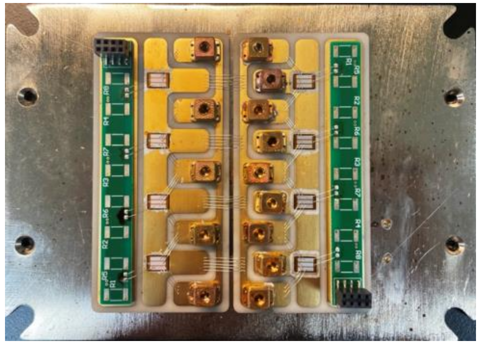
Ribbon bonding

- ➢ 5mil wire for gate
- ➢ 12mil wire for power routing

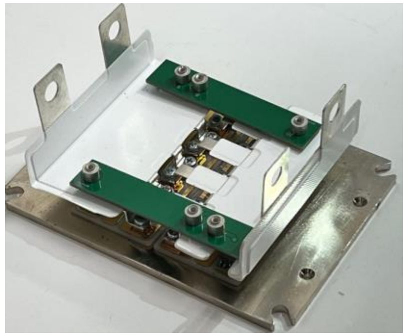


Cu terminal attachment

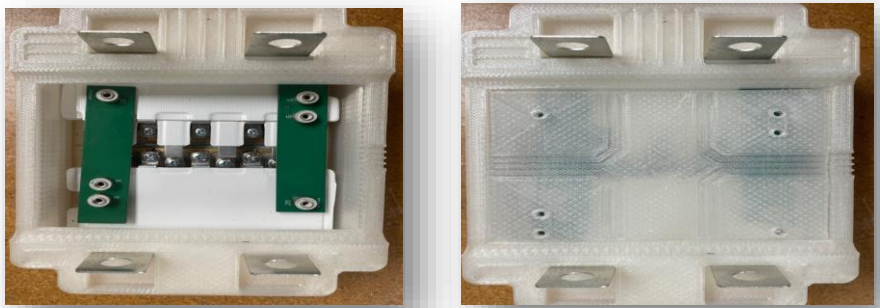
- ➢ SAC305 solder paste reflow



Laminated busbar attachment



Housing



Accomplishments

- Partial discharge test, staircase ramp in voltage up to 4.95 kV
- Thermal test to evaluate DBC crosstalk
  - 12W thermal dissipation with no heatsinking and passive dissipation

- Future work devoted to fabrication of a full 3.3kV module
  - Actual SiC devices

	PN#	Description	Distributor	Status	Remarks
1	732-5240-ND	M3 screw terminal	Digikey	Arrived	Gate terminal
2	92000A076	M3 pan head screws	Mc-Master	Arrived	For fastening busbar
3	TW-04-03-T-D-245-145	Pin connector	Digikey	Arrived	For gate routing
4	SQW-104-01-F-D-VS	Pin connector	Digikey	Arrived	For gate routing
5	SAC305	Solder paste	Digikey	Arrived	
6	Nusil R-2188	Silicone encapsulation	Nusil	Arrived	
7	Custom	SMT Chip resistor	CX Thin Films	Arrived	For thermal characterization
8	Custom	DC and AC laminated busbar	Hiconics	Arrived	
9	Custom	DBC (AlN)	Best Tech	Arrived	
10	Custom	Level-1 PCB	AllPCB	Arrived	
11	Custom	Level-2 PCB	AllPCB	Arrived	
12	Custom	Cu terminals	AllPCB	Arrived	For connection b/w busbar and DBC
13	Custom	Cu baseplate	AllPCB	Arrived	
14	Custom	3D printed housing	SBU	5 Ready	
15	G2R50MT33-CAL	3.3 kV SiC bare die	GeneSiC	Ordering	In stock
16	NTC020N120SC1	1.2 kV SiC bare die	GeneSiC	Ordering	Lead time: 4 months

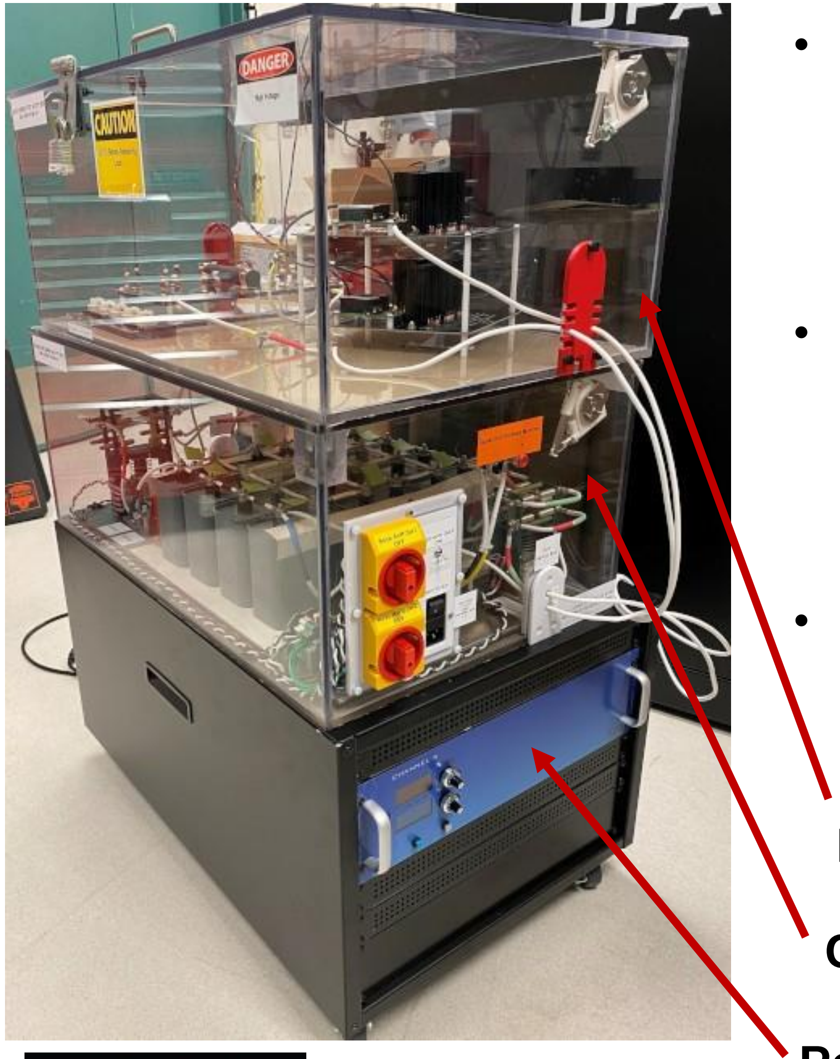
Accomplishments

- Gate driver design adapted for 20kV isolation

- HV power supply
  - Ultravolt DC power supply
  - 2x 20C24-P250-I5 modules in parallel configuration)
  - max output 20kV/25mA

- Capacitor bank
  - 12x 50uF/2.5kV capacitors
  - Cornell Dubilier S00590 in a series/parallel configuration,
  - 66.67uF at 7.5kVdc

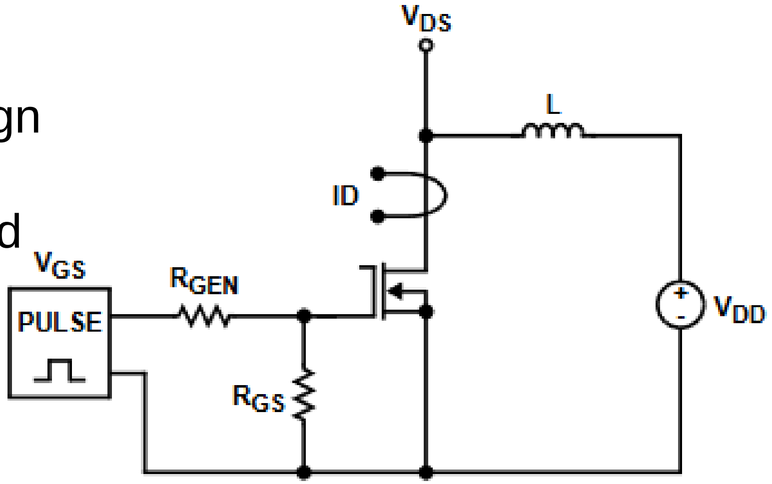
- Inductive bank (L) has been design
  - Cores have been ordered
  - Wiring of cores once received



Protection Equipment

Capacitive Bank

Power Supply



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Timeline

MILESTONE LOG

Milestone	Task#	Completion Date		Verification Method	Status
		Planned	Actual		
Full module design	1	09/30/2023	04/01/23	Simulation of thermal/insulation performance	**Completed**
Fully functional 3.3 kV, 120A module	1	11/30/2023		Evaluated in double pulse testing	**On Schedule**
Module evaluation circuit fabricated and commissioned	2	11/30/2023		Dynamic module characterization results	**On Schedule**
Reliability and performance testing of module	1	11/30/2024		Module evaluation at different voltage/current/power levels	**On Schedule**
In-circuit evaluation of high-current bonded module	2	11/30/2024		Demonstration of module operation in power converter	**On Schedule**

Impact/Commercialization

- List of innovations
  - None to Report

- IP status
  - None to Report

Future Work

- List of future work (CY 2023)

  a. Module design and fabrication

    i. Fabricate 3.3kV module with SiC devices

  b. Module characterization

    i. Wind inductor bank for double pulse testing
    ii. Commission double pulse testing
    iii. Evaluate 3.3kV module
    iv. Commission thermal chamber for reliability testing

THANK YOU

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Backup Slides

Acronyms

Insert any acronyms used and the associated definition here.

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