Scalable Smart Lighting Platform

Microchip “ink”

Scalable new manufacturing process

Optimized Light Efficiency

PARC, InnoSys, Inc, Wendy Davis
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New Project: Agreement DE-EE0009693, BENEFIT2020

Project Summary

A Smart Lighting Platform Goal

Save >50% building lighting energy.
Dynamic, customized, directional light fields.
Integrated, chip-based sensing and control.
Thin, large area, flexible format

Key Barrier:

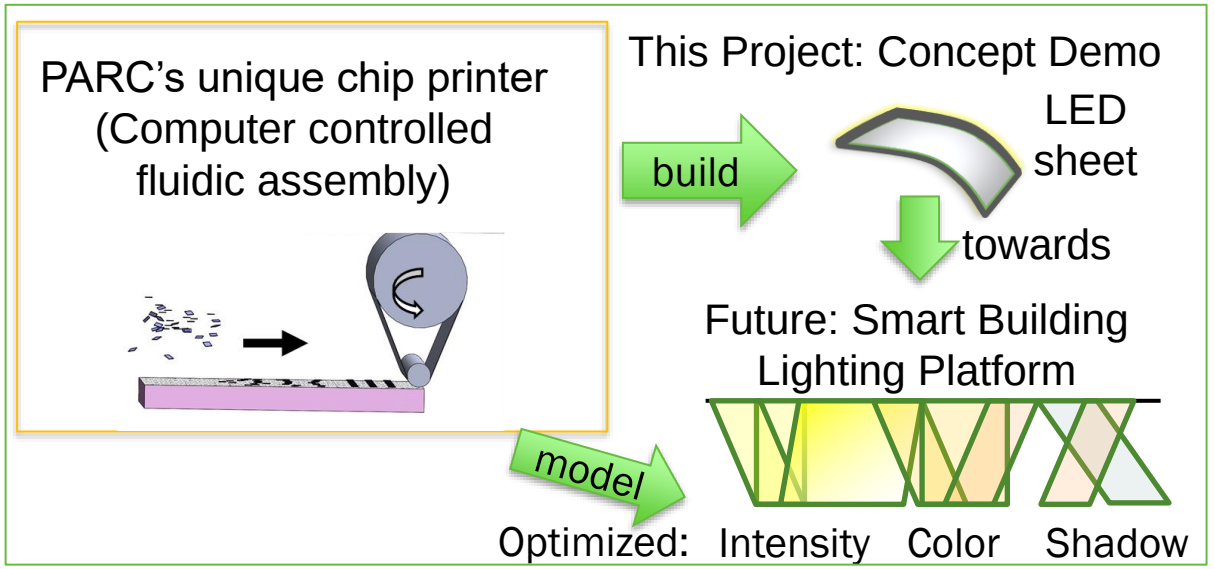
Fabrication cost. Need high chip count heterogeneous systems of millions of LEDs and other semiconductor chiplets.

This project:

1) Model energy, performance cost tradeoffs.

2) De-risk cost by showing *scalability* of new chip printer process. Demo a thin flexible LED light sheet.

PARC	Project lead. Fab process, demo, modeling
Innosys	Support demo design, phosphor
Wendy Davis	Advise modeling, market



Performance Period: 2022-2025

DOE budget: $1310k Cost Share: $328k

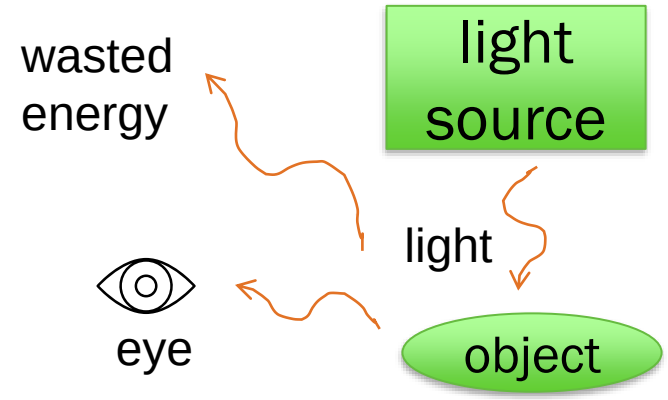
Milestone 1: New fab process can assemble and interconnect (200 chips).

Milestone 2: 1st LED light sheet (1000 chips)

Milestone 3: Full LED strip, testing (10,000 chips). Modeling shows >50% energy savings with market acceptable performance and cost.

Problem – Light Application Efficiency (LAE) Unrealized

- Lighting consumes 18% of building electricity but most generated photons wasted as do not reach eyes
- 3x energy reduction gain possible through light application efficiency with smart directional/timed sources.[1] Gaze dependent most energy savings potential, but hardest to implement. Need new capability.



Modest energy savings
Easier to implement
Incremental changes

Potentially large energy savings
Harder to implement
Radical changes

Convenient switches | Occupancy-based | Activity based | Adaptation responsive | Absorption-minimizing | Gaze dependent

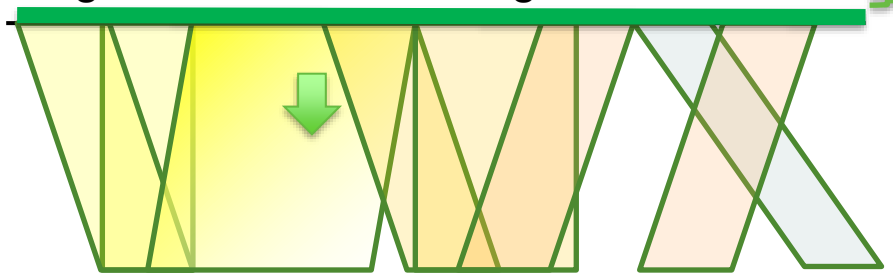
J.Y. Tsao, M.H. Crawford et al., Adv. Optical Mater. 2 (2014), 809.

Vision - New Smart Lighting Building Platform

meters

Thin, flexible, large area, customizable, poster-like

Digital Large Area 2D Thin Sheet
High-Resolution Full Light Field Control



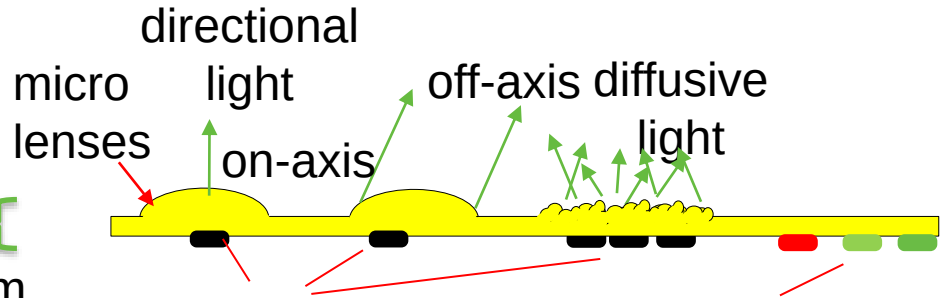
Graded Intensity optimization

Color optimization

Shadow optimization

Dynamic, directional, high resolution, tunable diffuse

1 mm



Cross section zoom in view, <1mm size chips

Millions of addressable light sources & distributed sensing

Current

Future

Optimized light application efficiency
New platform
50% less energy for office case

Alignment and Impact

Achieving Project Goals Enable Much Future Building Energy Savings

- **Advance smart light sheet concept (LAE)**
  - Build 1st concept demonstrator
  - 2-3x energy reduction possible for 18% of building electricity (lighting)
- **More LED adoption by enabling attractive, thin, diffuse, flexible form factor**
  - >2 quads saved if remaining non-LED linear & low/high bay fixtures convert to LED
  - >5 quads saved if rest of lighting markets also converts to LEDs
- **Future cost reduction, mass adoption possible**
  - PARC printer 1000x lower cost potential than current approaches

Success Definition

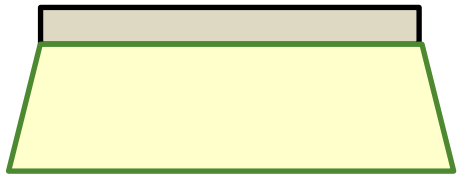
- **Show >50% energy savings, cost tradeoff**
- **Show scalable high chip count fab possible with basic LED light sheet demo.**

Broader DOE Impact Potential

- ***Smart building platform extendable to new functionality with heterogeneous IC chips***
  - ***Sensing people, environment…***
- **PARC's microchip printer beyond lighting. High part count heterogeneous systems/materials.**
  - Semiconductor/photonics, computation, large area sensors (solar etc), microstructured materials, 2D materials, energetics…

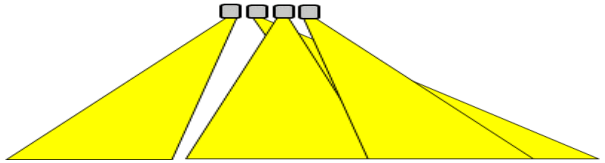
Approach: Current Light Sources Limited

Linear Fixture



- No direction control
+ low cost, current market leader

Point Source Directional



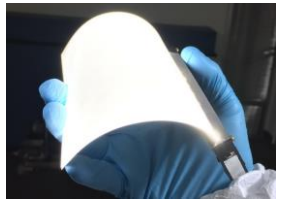
- High glare
- Bulky
- Not diffuse
+ Directional

OLED

LumiCurve

- No direction control
- No sensors
- Poor robustness
- Poor customization
- Not tunable
- High cost
+ Diffuse, thin, flexible

LightPipe



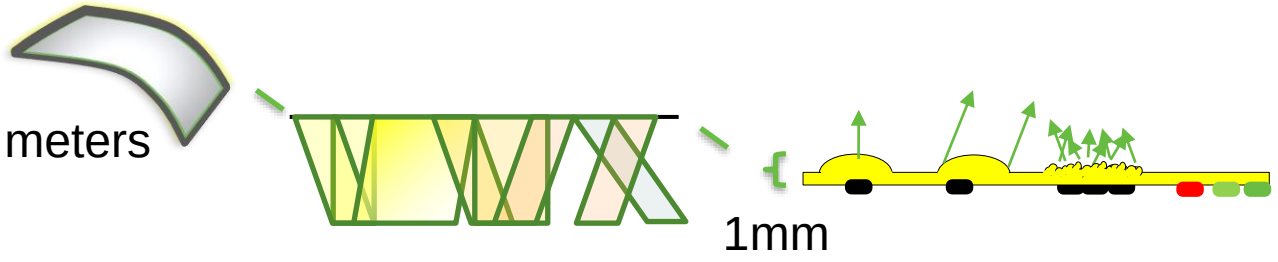
LucentOptics

- No direction control
- No sensors
+ Diffuse, thin, flexible
+ Low cost

Proposed New Platform Combines Best Properties

+ large area, thin, flexible sheet
+ directional, high resolution
+ sensors, tunable diffusivity
+ customizable

low cost ? Need to show scalable high chip count possible.

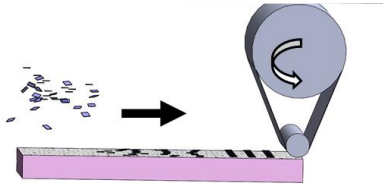


Approach: Manufacturing Cost Key Barrier

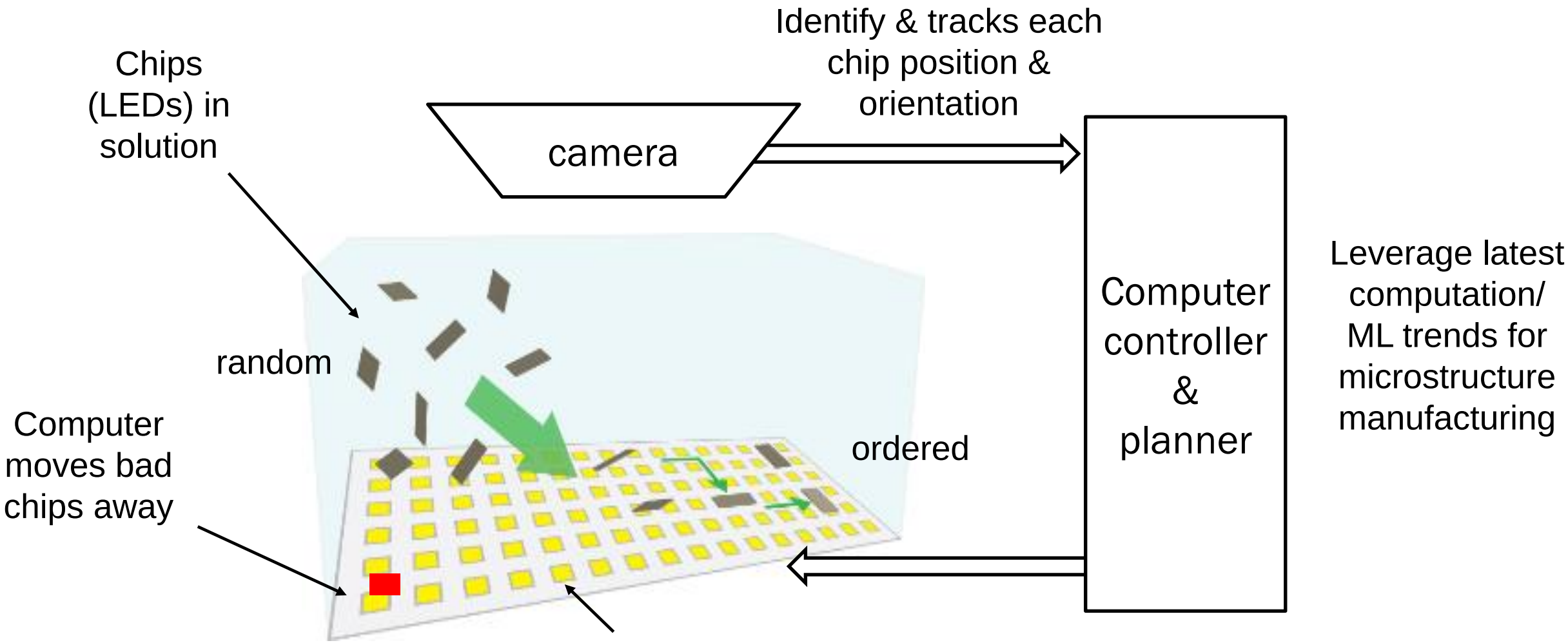
- **Need millions of heterogeneous semiconductor microchips (per square meter) on thin flexible substrates**
  - Current million chip systems >10^5
  - Assembly costs >>10^4 should reduce to ~$1 for lighting market mass adoption
- **Existing fabrication not scalable to low cost**
  - High chip count approaches are high cost & slow (robotic pick/place, laser, stamp)
  - Other (non-PARC) fluidic assembly approaches have low-cost potential but low yield, not heterogenous.

- **PARC's new chip printer process has low-cost scaling potential**
  - Designed for chip "ink"
  - Xerographic printing $1/m^2

PARC's chip printer (Computer controlled fluidic assembly)

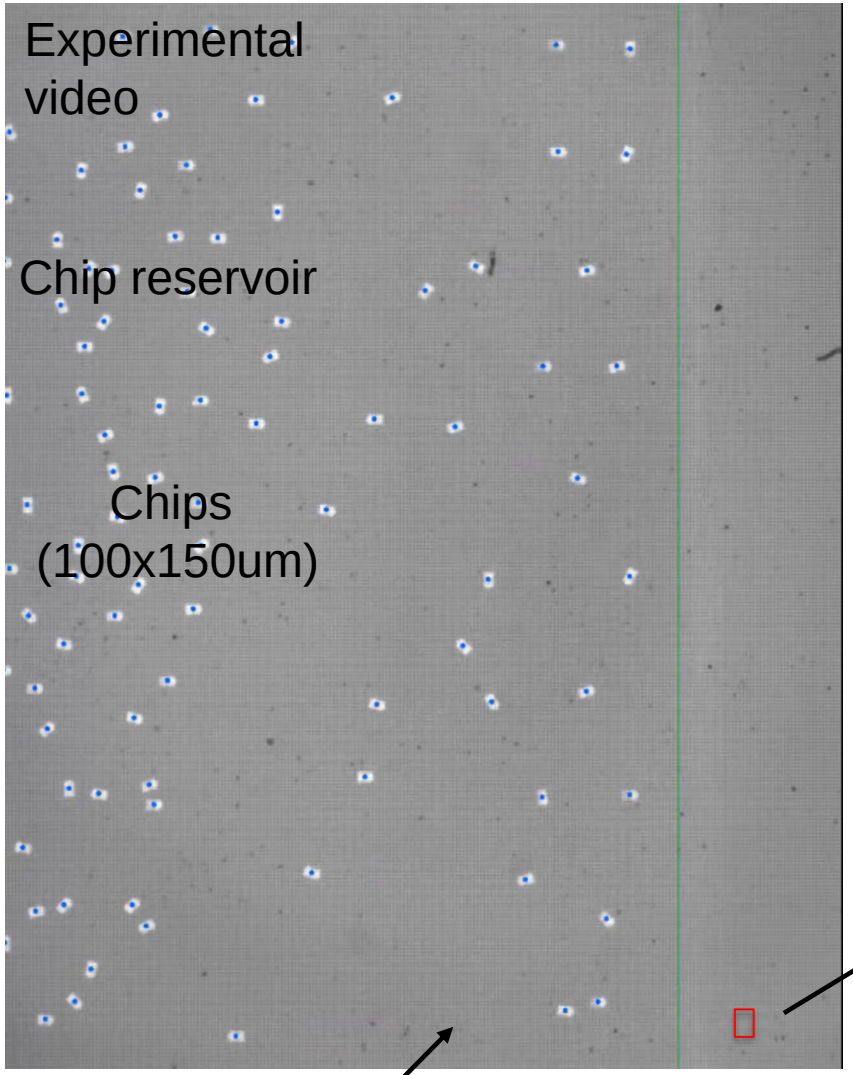


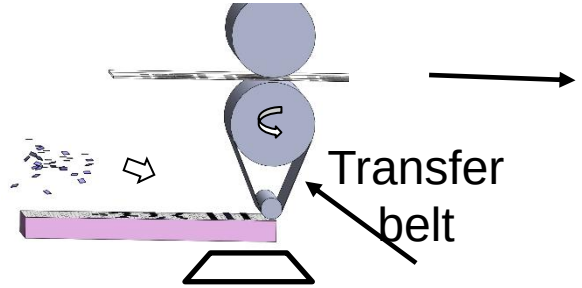
New : Software directed electrostatic microassembly



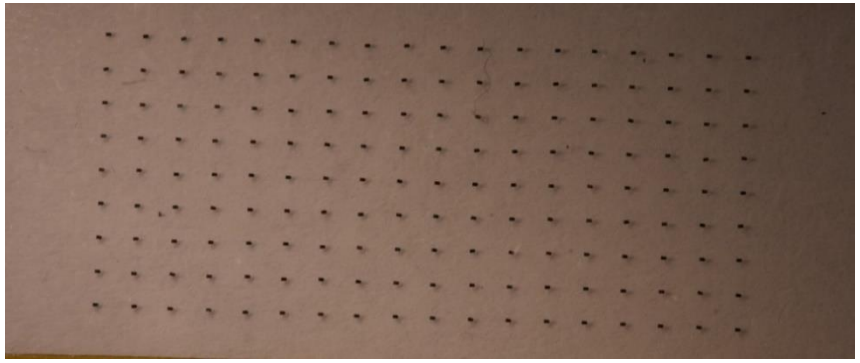
Active matrix electrode array generates dynamic electric force fields to individually direct chips in parallel to target locations, enabling sorting, defect healing, heterogeneous.

Computer Assembly Integrated With A Transfer Belt



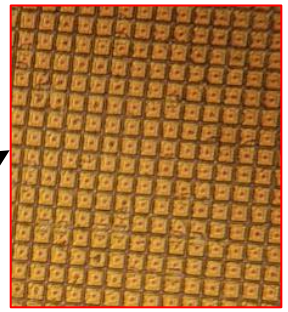


Camera view under row transfer nip



Continuous Feed Assembly & Transfer “printout” (162 chips, 150x250um, on pdms, 1mm pitch)

Electrostatic Non-contact Lab setup 1in wide



50um actuator grid

High throughput potential

- Scalable software & physics (cm/sec)
- Wide printer
- Heterogeneous with 1 transfer

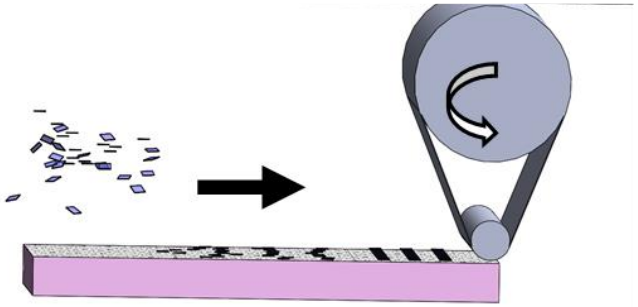
Approach: Project Plan & Goals

#	Goal Type	Goal	Budget Period 1	Budget Period 2	Budget Period 3
1	Experimental	Improve assembly printer system to show scalability for low cost. Demo thin, white light LED sheet.	200 chips (interconnect process)	1000 chips (white light sheet)	10,000 chips (full LED strip & testing)
2	Modeling	Show large energy savings of new directional light sheet, customizable platform, and cost tradeoffs.	light output model	energy savings for key use cases	cost sensitivity versus energy savings

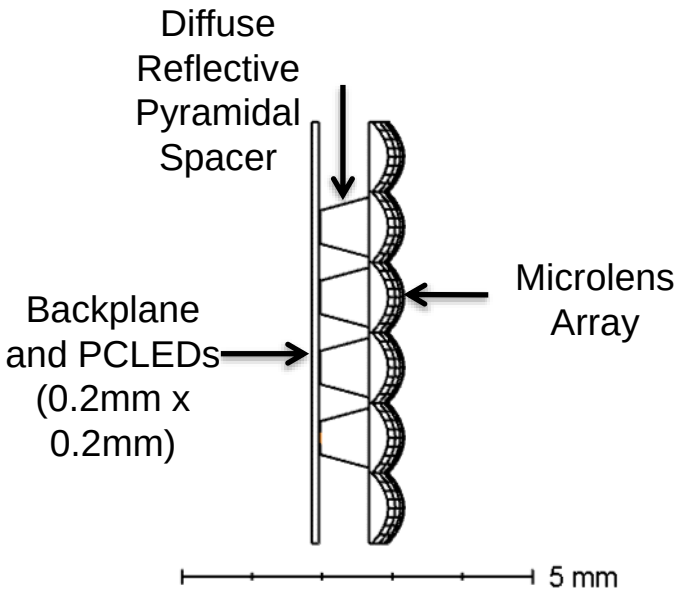
- **Majority of resources planned for experimental goals (#1)**
- **Improve process to scale # of chips key challenge**
  - 100x more assembly and 1000x more interconnects than PARC's prior work

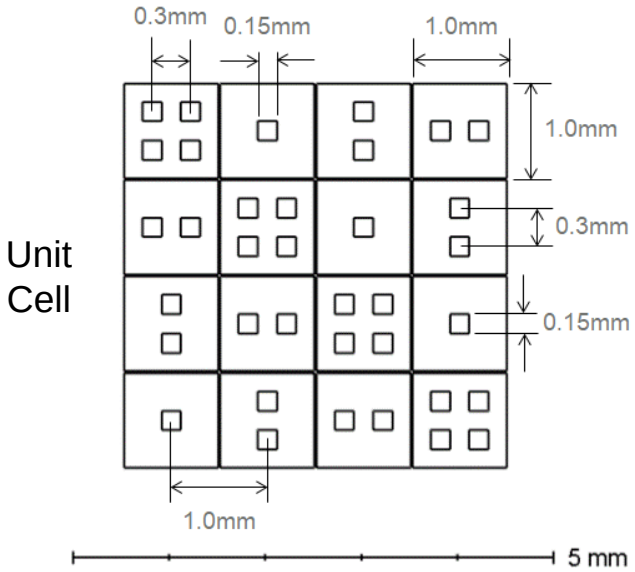
Approach: Challenges & Strategy

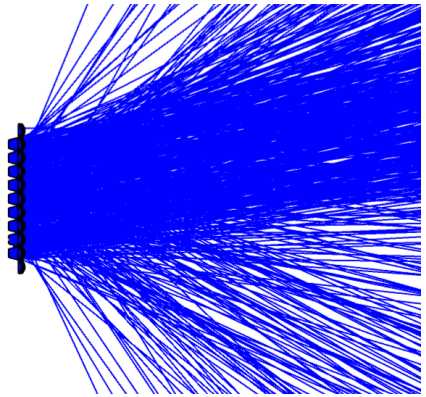
- Challenges
  - Low-cost with high chip count system and yield
  - Mitigation: Prioritize yield understanding early
- Business strategy
  - Build manufacturing tool, sell smart lighting sheet
  - Engage investors/customers in lighting/display with modeling, demos
  - Leverage LED display hot trends
- How will demonstrate benefit
  - Modeling shows energy savings and cost tradeoffs
  - Experiments show low-cost potential with new chip printer process.

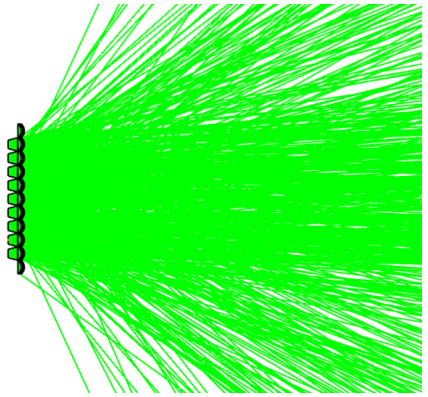


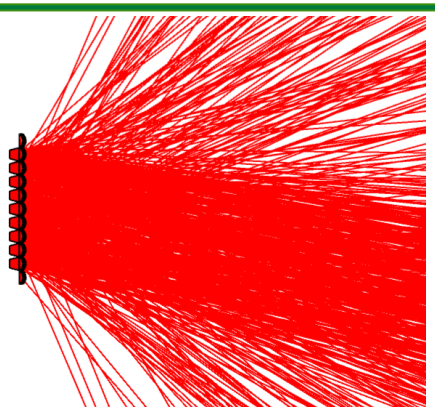
Progress - Modeling a Dynamic LED Light Sheet

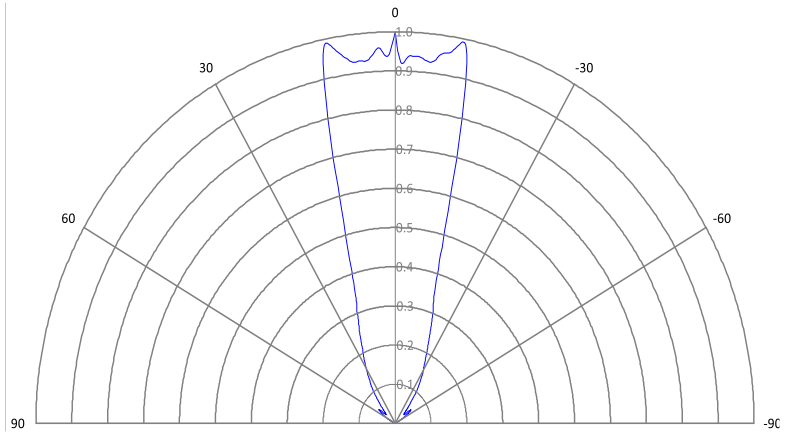


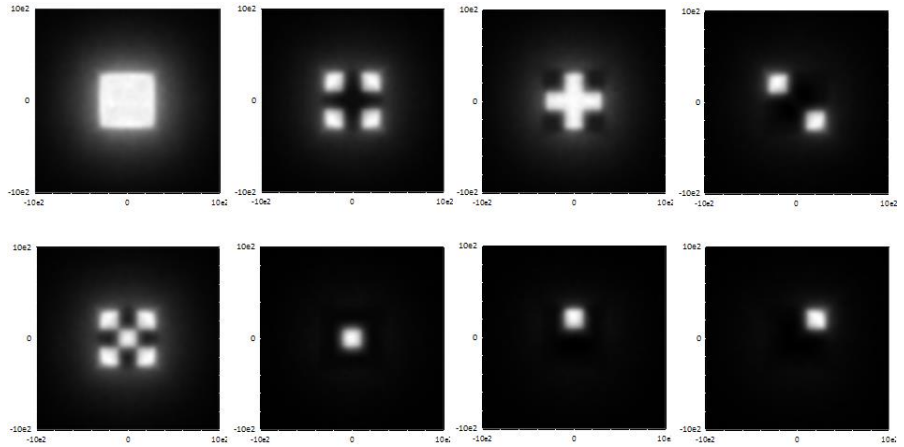








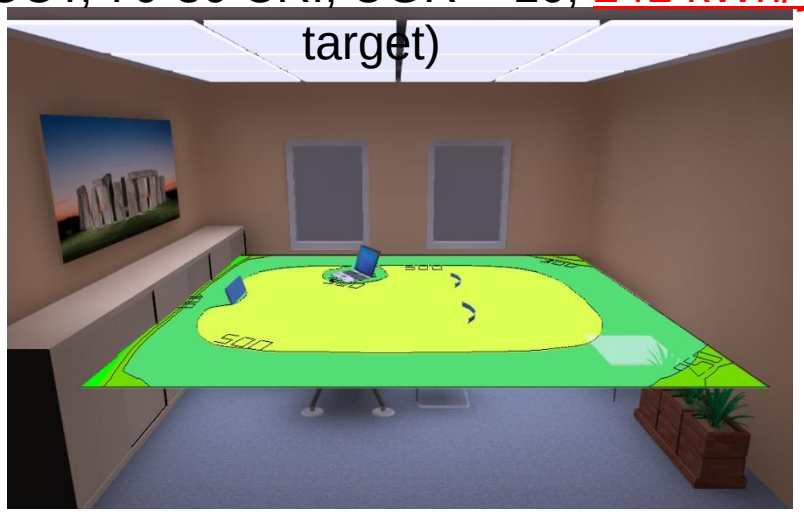


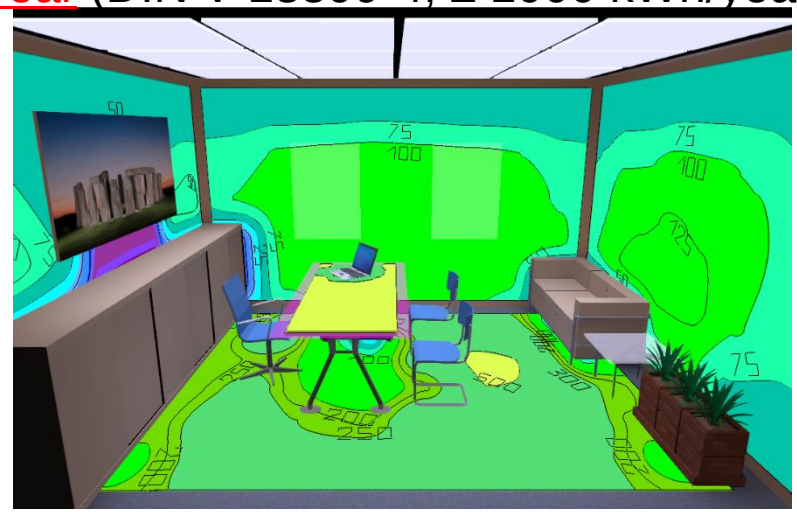


White PCLED Output (lm) (min)	0.7188	Unit Cell Light Output (lm)	21.9
White PCLED Power (mW)	4.382	Unit Cell LED Power (W)	0.158
White PCLED Efficacy (lm/W)	164.0	Unit Cell Efficacy (lm/W)	138.9
LEDs per Unit Cell	36	Electronics and Thermal Droop Efficiency	0.80
Optical System Efficiency	0.847	Luminaire Unit Cell Efficacy (lm/W)	111.1

Modeling Shows 50% Energy Savings for Office Example

CASE 1: 500 lx task plane illum, 3991°K CCT, 70-80 CRI, UGR < 10, 241 kWh/year (DIN V 18599-4, ≤ 1000 kWh/year target)

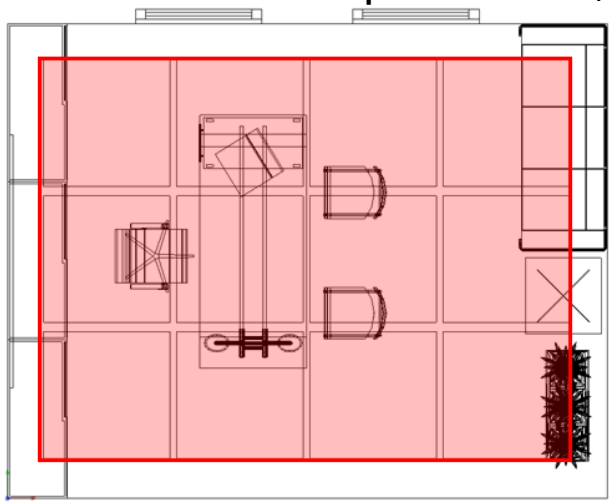


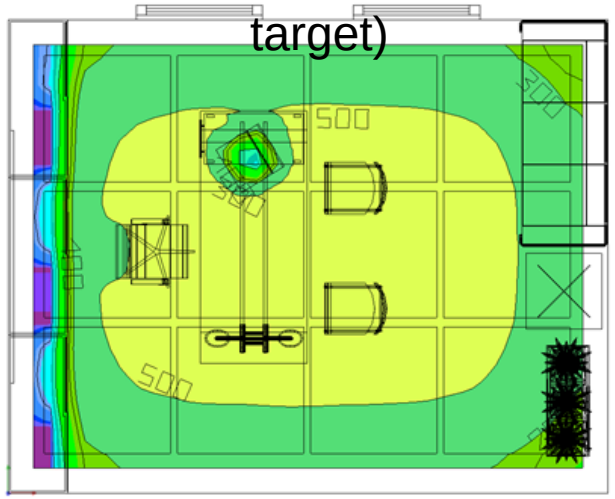


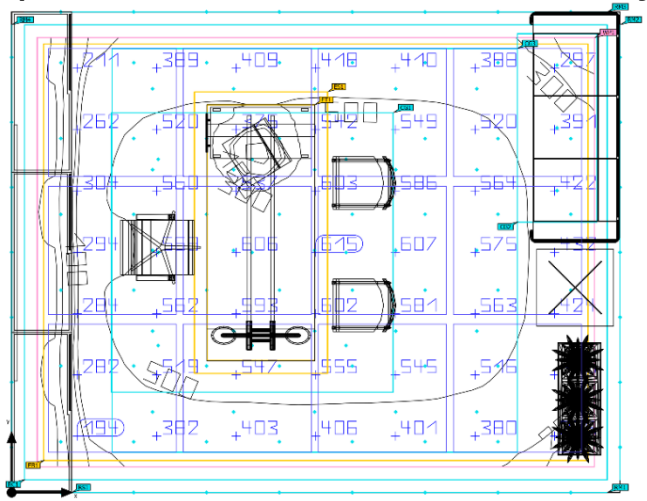
CASE 2: 500 lx task plane illuminance, 3991°K CCT, 70-80 CRI, UGR < 10, 122 kWh/year (DIN V 18599-4, ≤ 1000 kWh/year max. target)

Comparison: 5m x 4m x 2.8m Basic Office Space Example

CASE 1: 500 lx task plane illum, 3991°K CCT, 70-80 CRI, UGR < 10, 241 kWh/year (DIN V 18599-4, ≤ 1000 kWh/year target)







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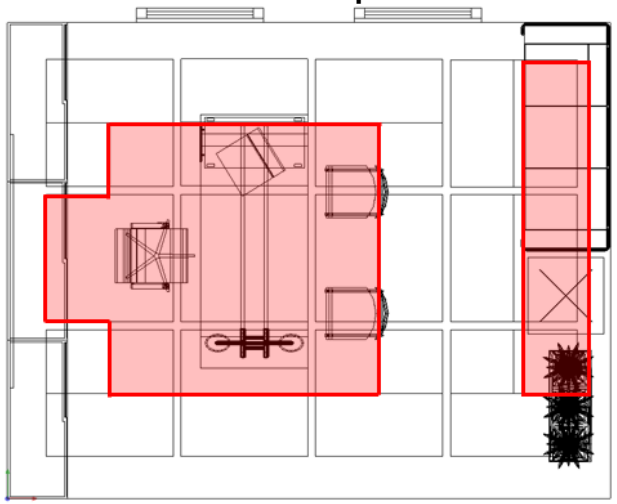
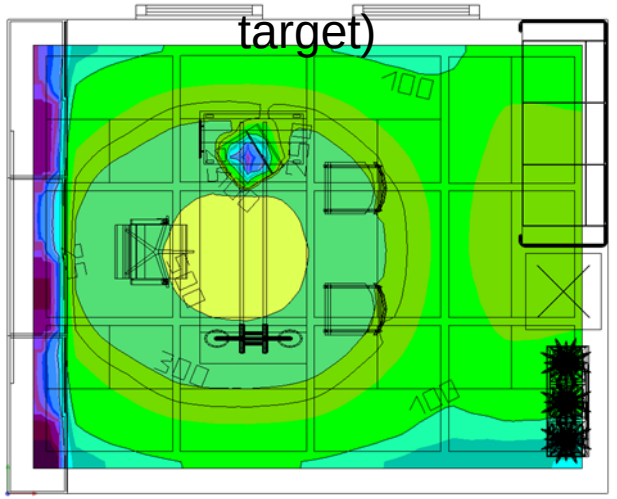
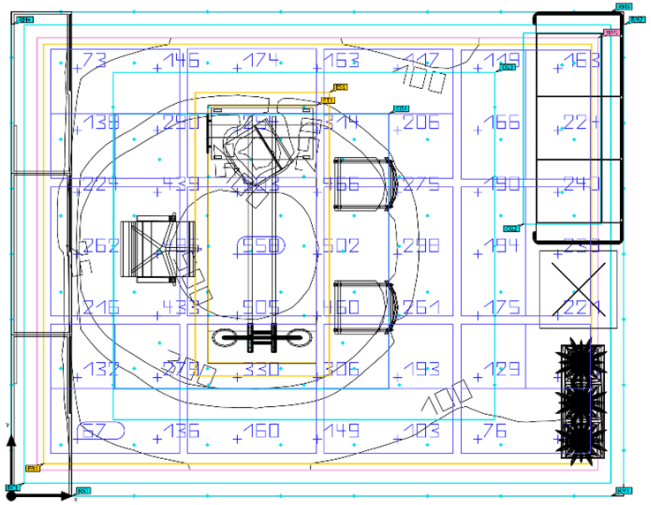
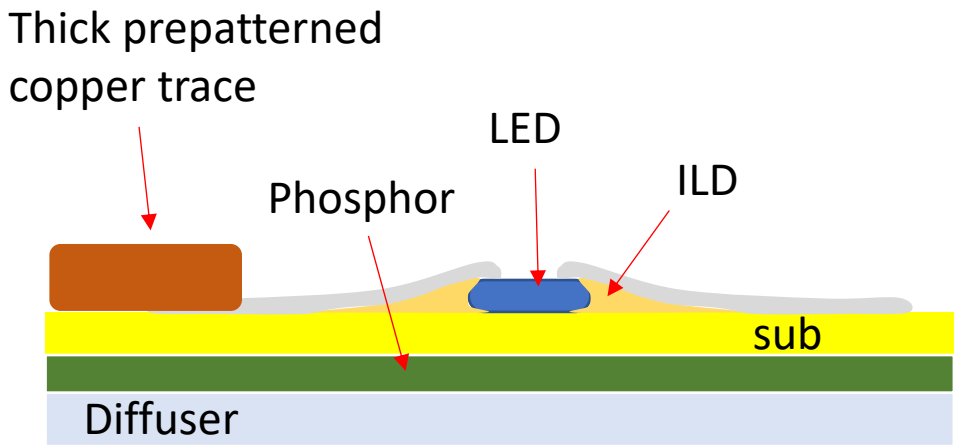






Progress and Future Work

- 3 of 4 milestones for BP1 (of 3) achieved
  - Designed final demonstrator
  - Improved chip printer loading
  - Modeled directional light sheet
    - showed 50% energy savings, office case
- Unexpected Issues/Lessons
  - NCE for support tool failure
  - HW/SW system challenging



Light sheet demonstrator cross section

- Remaining Project Plans
  - Build 1st electrically interconnect LED array, 1st white light sheet, final demonstrator.
  - *Increase # chips 100x, # interconnects 1000x over PARC's prior work*.
  - No new project changes anticipated
- Plans beyond end of the project
  - Raise funds, mature tech, start company.
  - Build production tool, high chip count product based on LED light sheets

THANK YOU

Microchip “ink”

Scalable new manufacturing process

Optimized Light Efficiency

PARC, Innosys and Wendy Davis
PI Eugene Chow, PhD, PARC Principal Scientist & Strategy Leader
650-812-4181, echow@parc.com

New Project: Agreement DE-EE0009693, BENEFIT2020

REFERENCE SLIDES

Project Execution

	21	FY2022				FY2023				FY2024				FY2025			
Planned budget ($k)	11	292				442				529				364			
Spent budget ($k)	11	292				84				0				0			
	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
Past Work Milestones																	
Q1 Design demonstrator																	
Q2 Loader																	
Q4 Light output model																	
Current/Future Work Milestones																	
Q3 1st interconnect run																	
Q1 Interconnected LEDs																	
Q2 1st white light sheet																	
Q3 1000 chips interconnected																	
Q1 Full LED test strip																	
Q2 LED test strip testing																	
Q3 Improve yield																	

- NCE
- Did 1st modeling milestone early

Go/No-Go:

- 200 chips (1st interconnects)
- 1000 chips (1st light sheet)
- 10,000 chips (final demo)
- Performance/ Cost Model

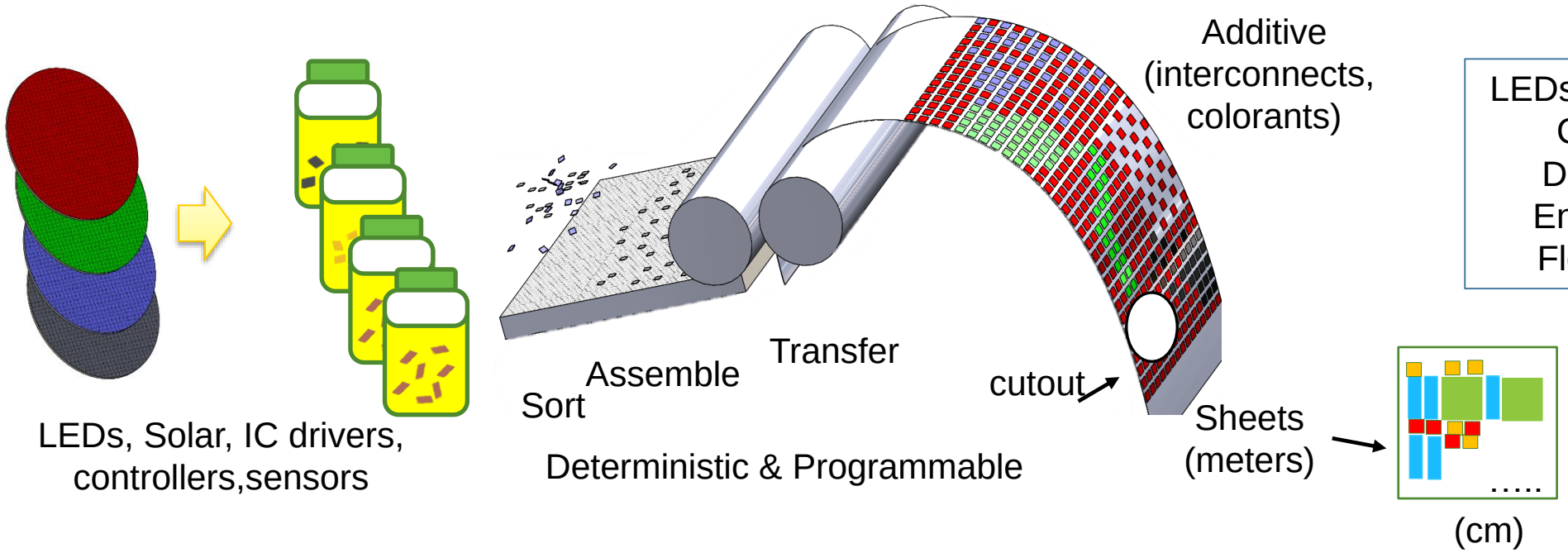
◆ planned date

Team

Who	Org Type	Project Role
PARC	50 yr old industrial research lab, 1st laser printer & 1st personal computer	Lead project, Improve chip printer process to demonstrate 1st light sheet. Perform modeling.
Innosys	Small minority owned company	Support light sheet design, phosphor integration
Wendy Davis	Consultant, lighting application expert	Guide modeling specs for market acceptance
Lumileds, others	LED vendors	Supply LEDs

Vision: Microassembly Printer for Smart Systems

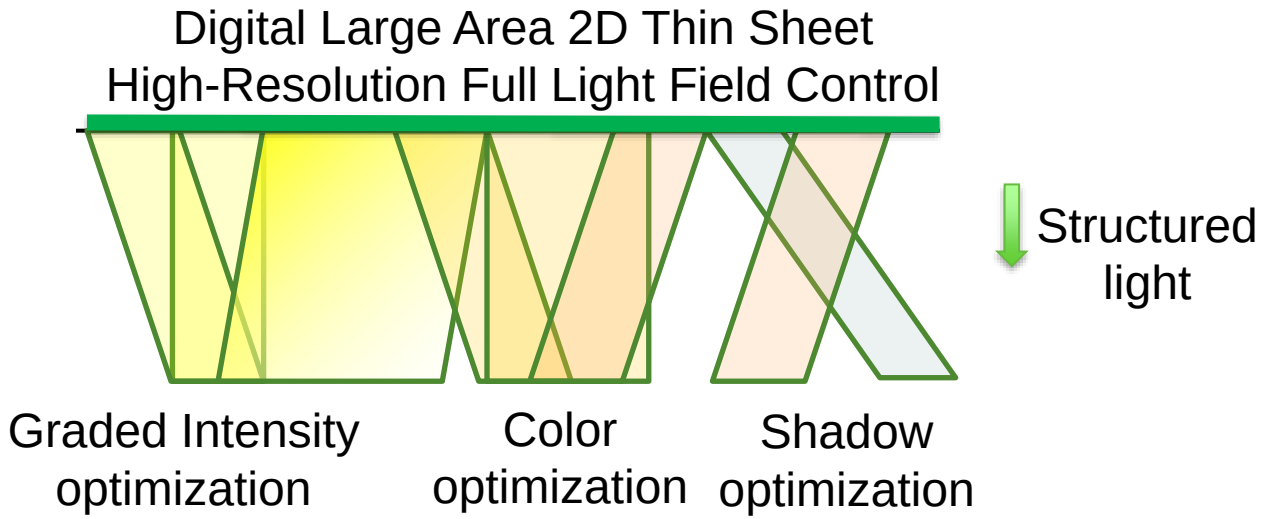
Wafers | Chiplets | Digital Printer | Smart Building Systems



- High throughput & low cost, heterogeneous of small chips (10-500um). Millions of chips.
- Digital – sort chips, custom patterns, rapid prototyping
- Goal – disruptive low cost of printing ($2/m^2 for assembly & interconnect), *independent of number of devices*
- Smart Light Sheet Cost – design, chips, substrates/optics & testing (assembly & interconnects negligible)

Vision – A New Smart Building Lighting Platform Enabled by High Chip Count Systems

- **Ideal source: light field generator**
  - Arrays of LEDs/lenses with programmable directional, fine scale control
  - Diffuse, low glare desired for market adoption – large area source
  - Sensing, control, drivers..
  - Thin, flexible – adaptable form factor
  - Customizable & Low cost



- **Need high chip count system platform**
  - Millions of heterogeneous semiconductor chiplets on a flexible substrate. Current tools can't build.
  - Need a new assembly integration manufacturing method