DOE Office of Electricity TRAC

Peer Review

U.S. DEPARTMENT OF ENERGY | OFFICE OF ELECTRICITY

PROJECT SUMMARY

Intelligent Power Stages (IPSs) at OSU

The project aims to improve the reliability of grid-tied power converters with advanced monitoring circuits and intelligent algorithms. In detail, an advanced detection circuit has been built and integrated into an adaptive gate drive for power modules. Because of the inherent noisy measurement environment of power converters, on-state device voltage drop together with several other measurements are fused together to provide accurate descriptions of the stress and degradation of at both device and converter levels.

An 80 kVA grid-tied converter prototype with the most popular circuit topology for grid-tied converters have been built to validate the proposed the advanced gate drive circuit designs and sensor fusion algorithms.

PRINCIPAL INVESTIGATORS

Dr. Jin Wang, Professor

Dr. Mahesh Illindala, Professor

WEBSITE

https://hvpe.osu.edu (High Voltage and Power Electronics Laboratory at the Center of High Performance Power Electronics at OSU, established in 2007)

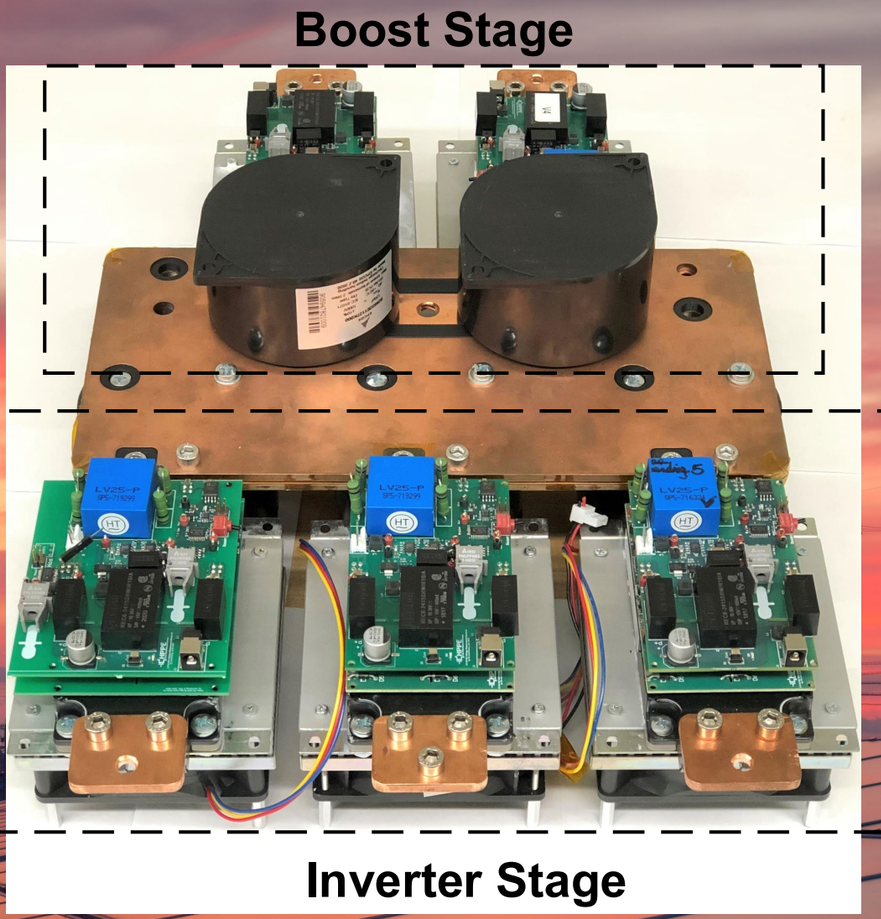
Primary Innovations

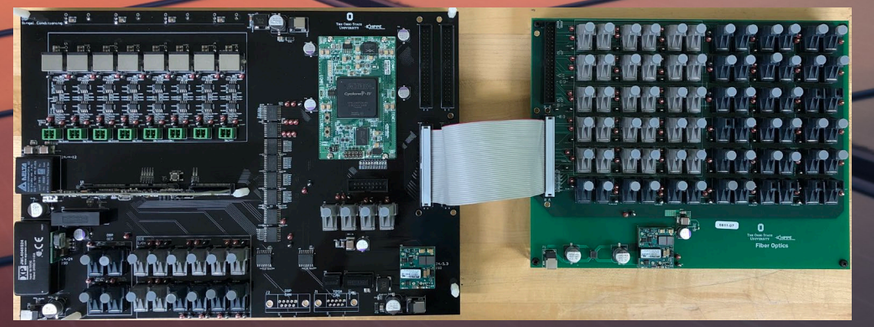
Main Challenges

- Noisy measurement environment for health monitoring due to the high-speed switching of SiC devices
- High power density requirement in urban settings

Primary Innovations

- Advanced power device on-state voltage measurement with high noise immunity
- Sensor fusion algorithms to accurately report the stress and degradation of devices and power converters
- Adjustable gate drive that helps to reduce device degradation
- Liquid metal-based power converter cooling with the inductor in the boost converter functioning as the pump

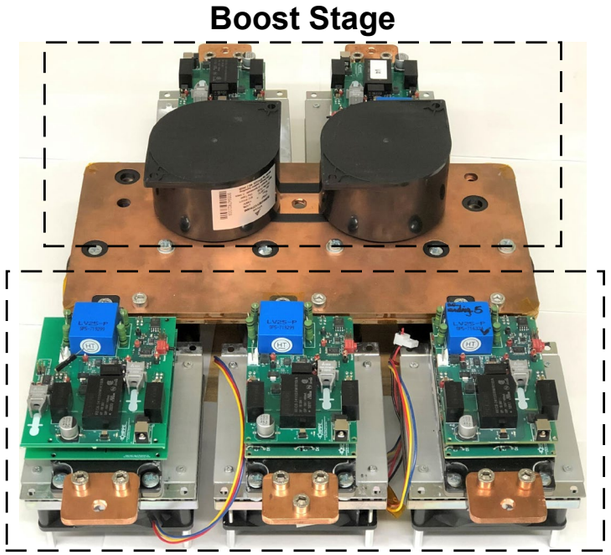




Hardware Development/Innovation Update

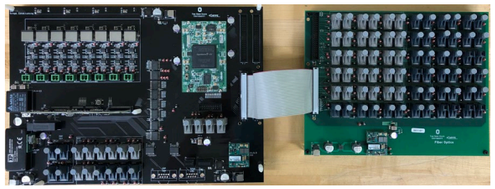
- Main circuits, controller boards, and thermal simulation
- Vds_on and temperature measurements
- Sensor fusion-based Stress Index and Health Index
- Gate voltage adjustment
- Liquid metal-based cooling

Main Circuit, Controller Board, Busbar, Thermal Design

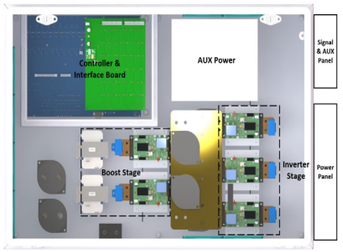


IPS Power Stage Prototype

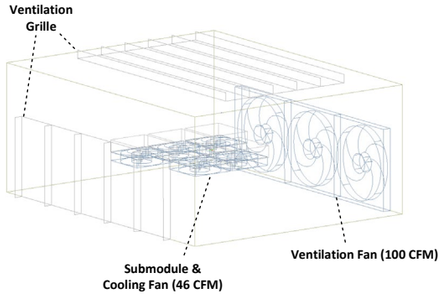
	DSP	FPGA
P.N.	TMS320f28379D	Cyclone IV EP4CE40F29C8

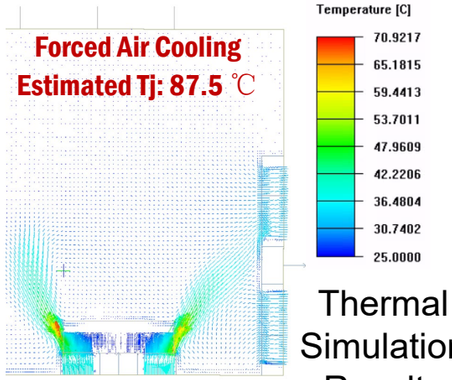


Controller and interface board

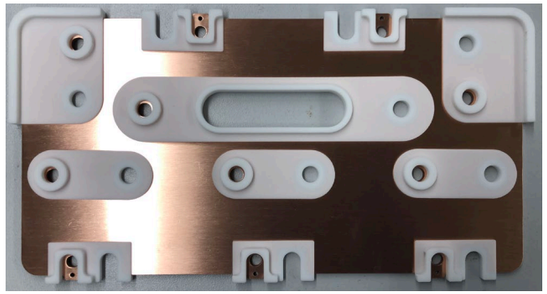


Final Assembly Design





Thermal Simulation Results



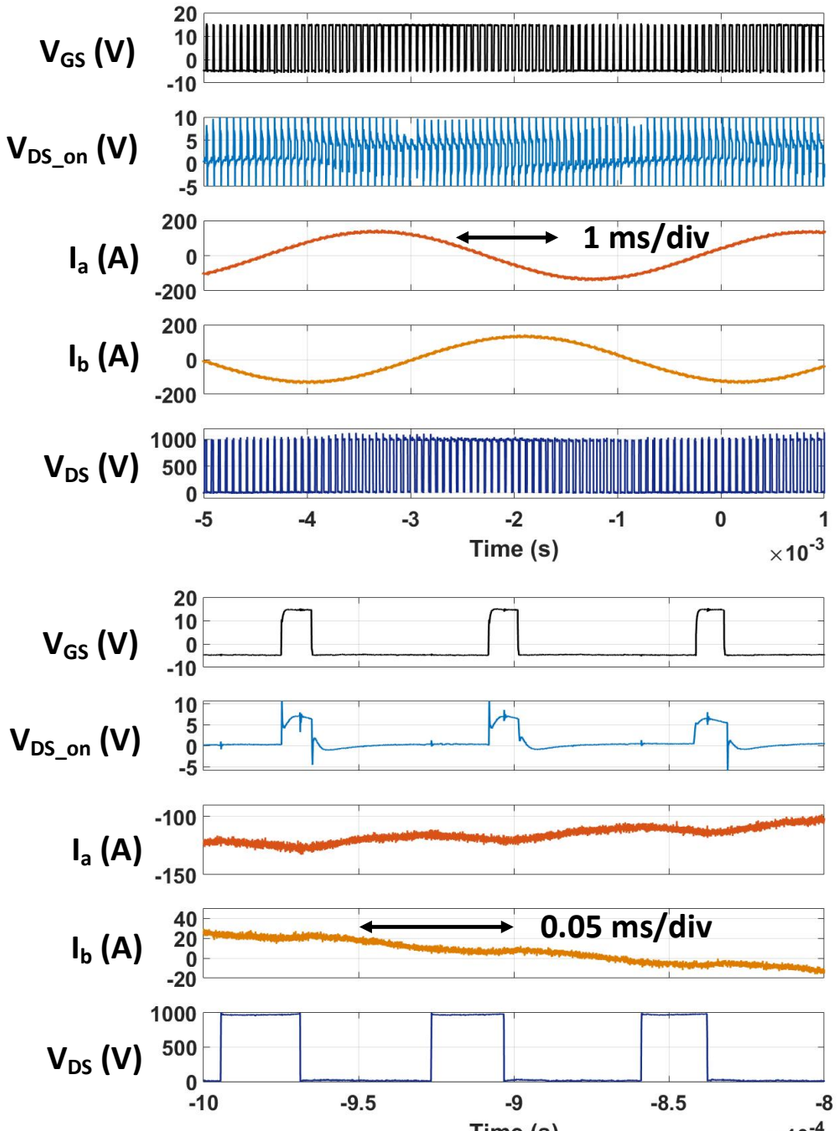
Busbar FEA Simulation Specifications and Results				
Busbar Configurations	Current Path	AC Resistance	AC Inductance	Voltage Overshoot
Copper Material, 4 mm Thickness	Between Submodules	1.31 mΩ	23.65 nH	<15% (Switching at 1000 V with 5 A/ns)
	Between DC-Link Caps and Submodules	0.96 mΩ	10.2 nH	

Power Stage Test Results: DC/AC Stage

Inverter Full Power Tests

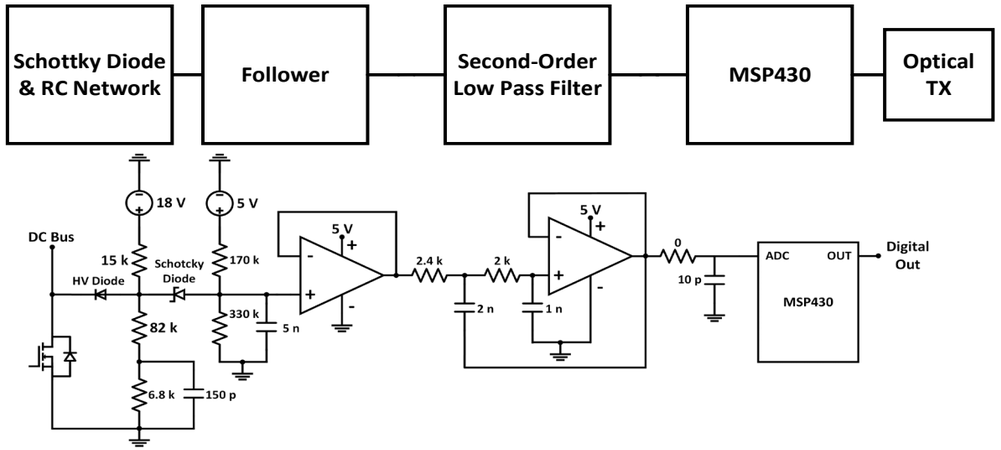
Testing Condition	
Input DC Voltage	970 V
Output RMS Current	97 A (for 80 kVA)
Switching frequency	15 kHz
Load	RL Load (provided by Vertiv)

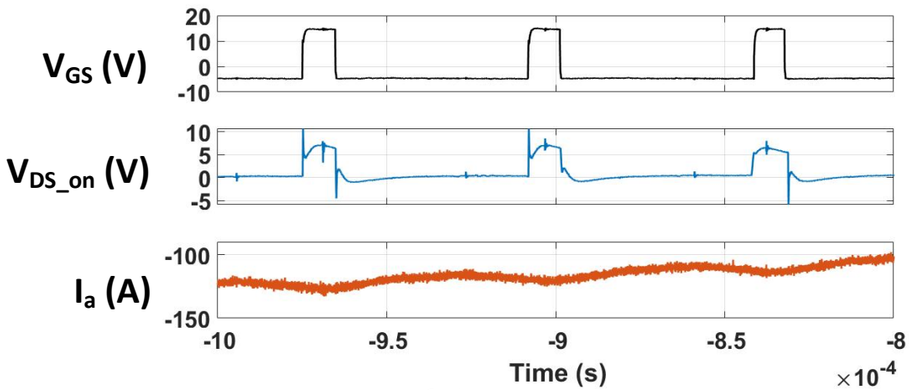
- The inverter behaves well at full voltage and full current
- The gate drive has very clean gate voltage waveform (V_{GS})
- The device voltage (V_{DS})overshoot is within 5%.
- The on-state voltage measurement (V_{DS_on}) is almost noise free



Test waveforms

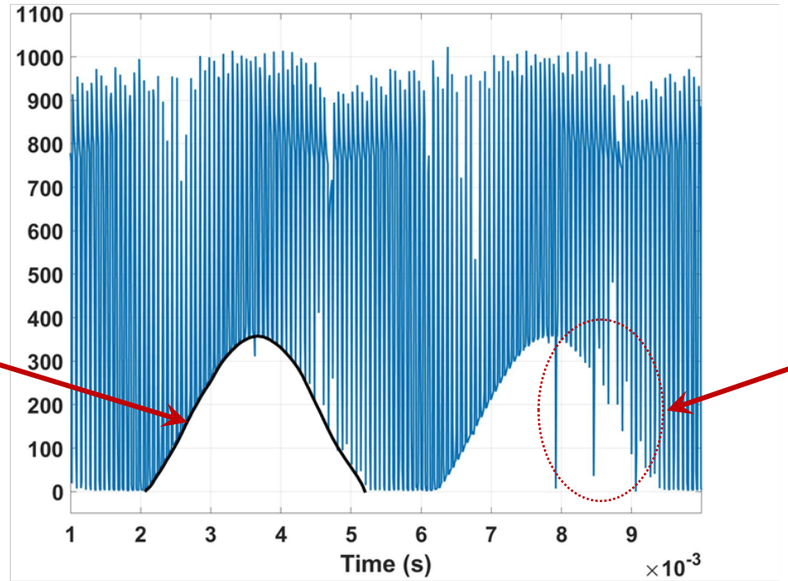
On-State Voltage Drop Measurement in the DC/AC Stage





Analog output of the V_{DS_on} measurement

The black profile shows device on-state voltage change during half fundamental cycle



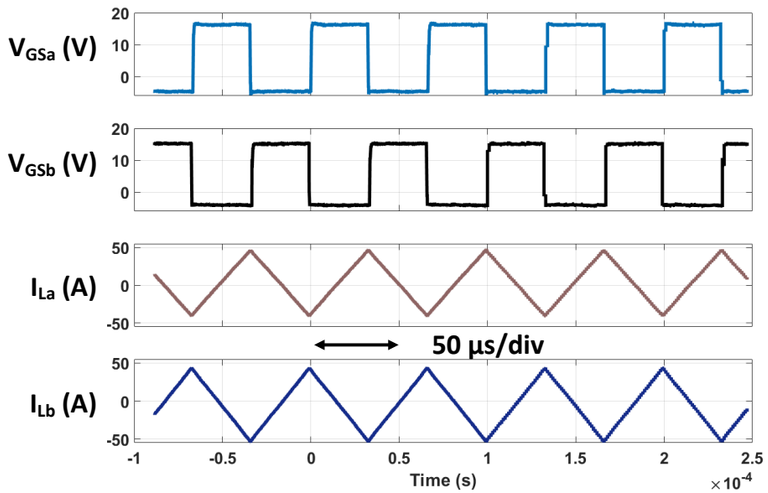
The occasional noise in the digital read-out highlight the need of sensor fusion

FPGA reading of the V_{DS_on} measurement

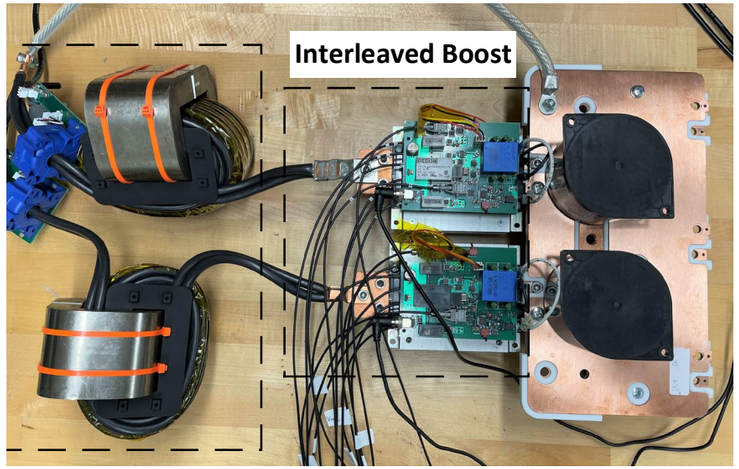
Power Stage Test Results: Boost Converter

Interleaved Boost Stage Tests

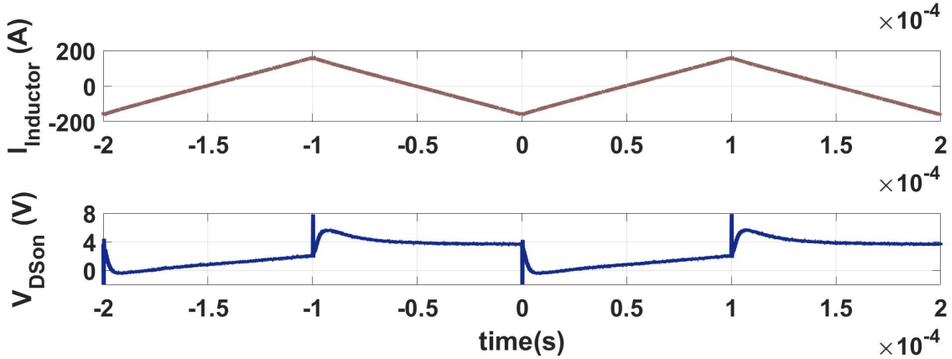
Testing Measurements	
Input DC Voltage	500 V
Output DC Voltage	995 V
Switching frequency	5-15 kHz
Boost Inductor Value	170 µH



Test Waveform at 15 kHz



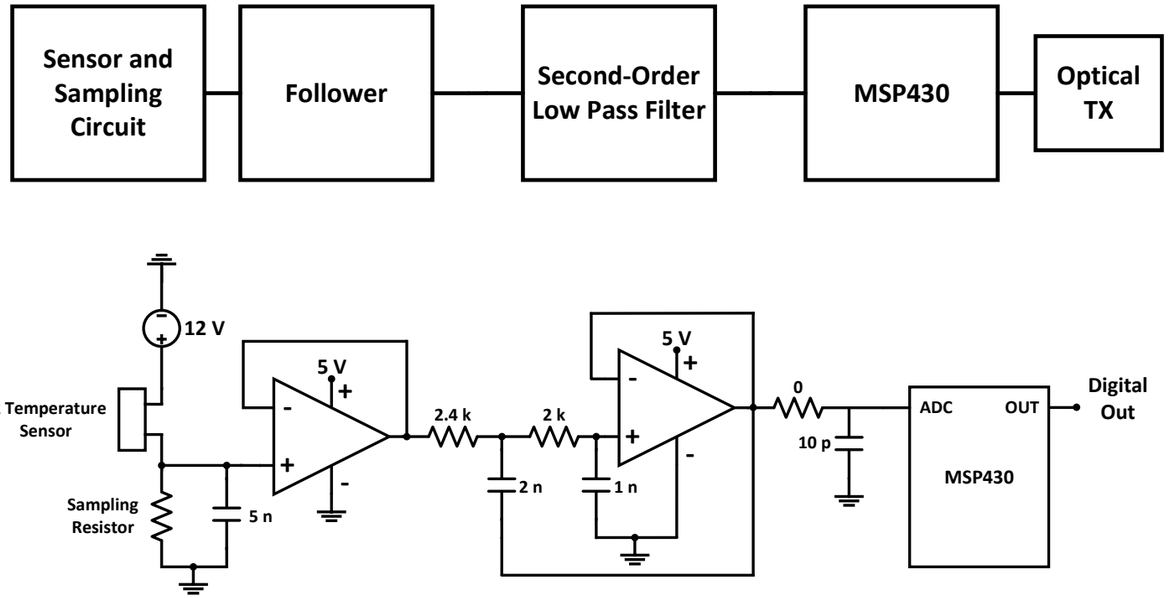
Test Setup



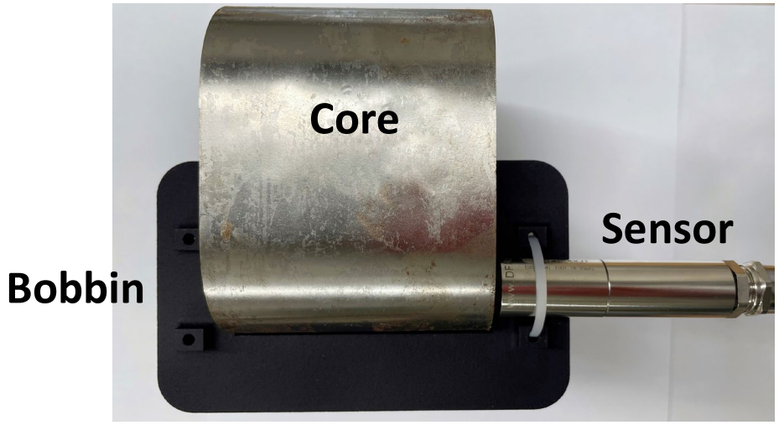
Current and ON-state voltage measurement test Waveform at 5 kHz

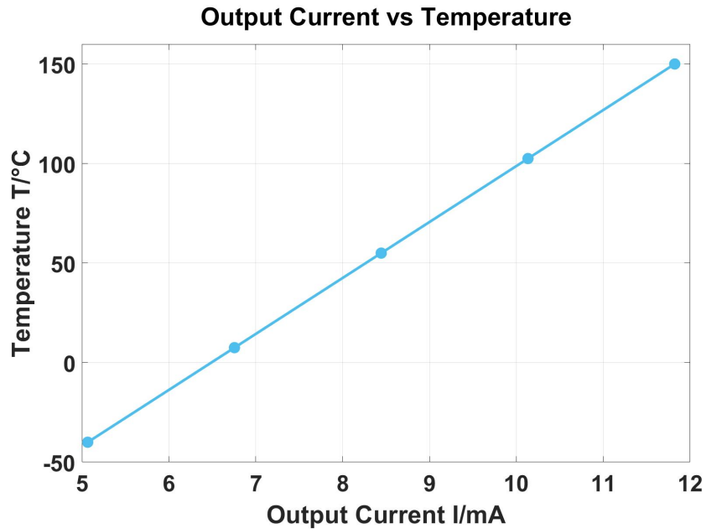
- The boost stage behaves well at full voltage and high current
- The gate drive waveforms (V_{GS}) are very clean
- The on-state voltage measurement (V_{DSon}) is noise free

Inductor Core Temperature Measurement



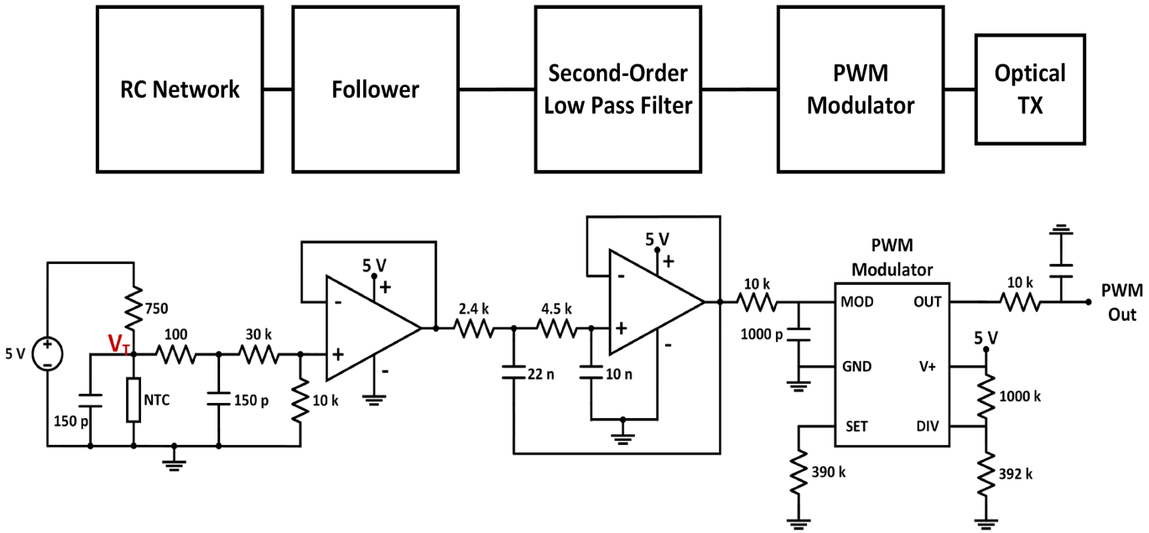
- IR sensors are mounted close to the cores of the interleaved inductors for noise free core temperature measurement.



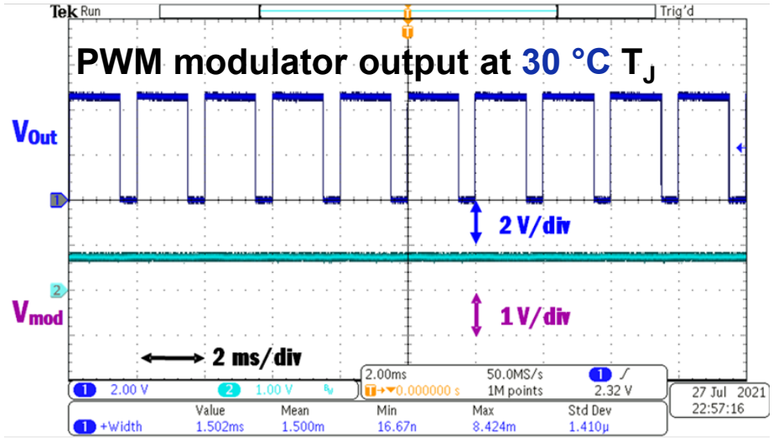


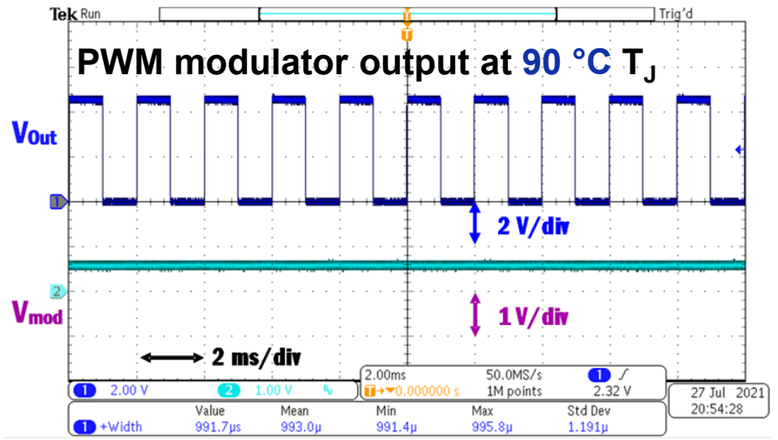
Sensor output current vs. temperature

Junction Temperature Measurement



- The duty cycle of the PWM modulator output decreases when the junction temperature rises.
- The sensor is on the substrate. Thus, the measurement does not accurately reflect the real junction temperature.



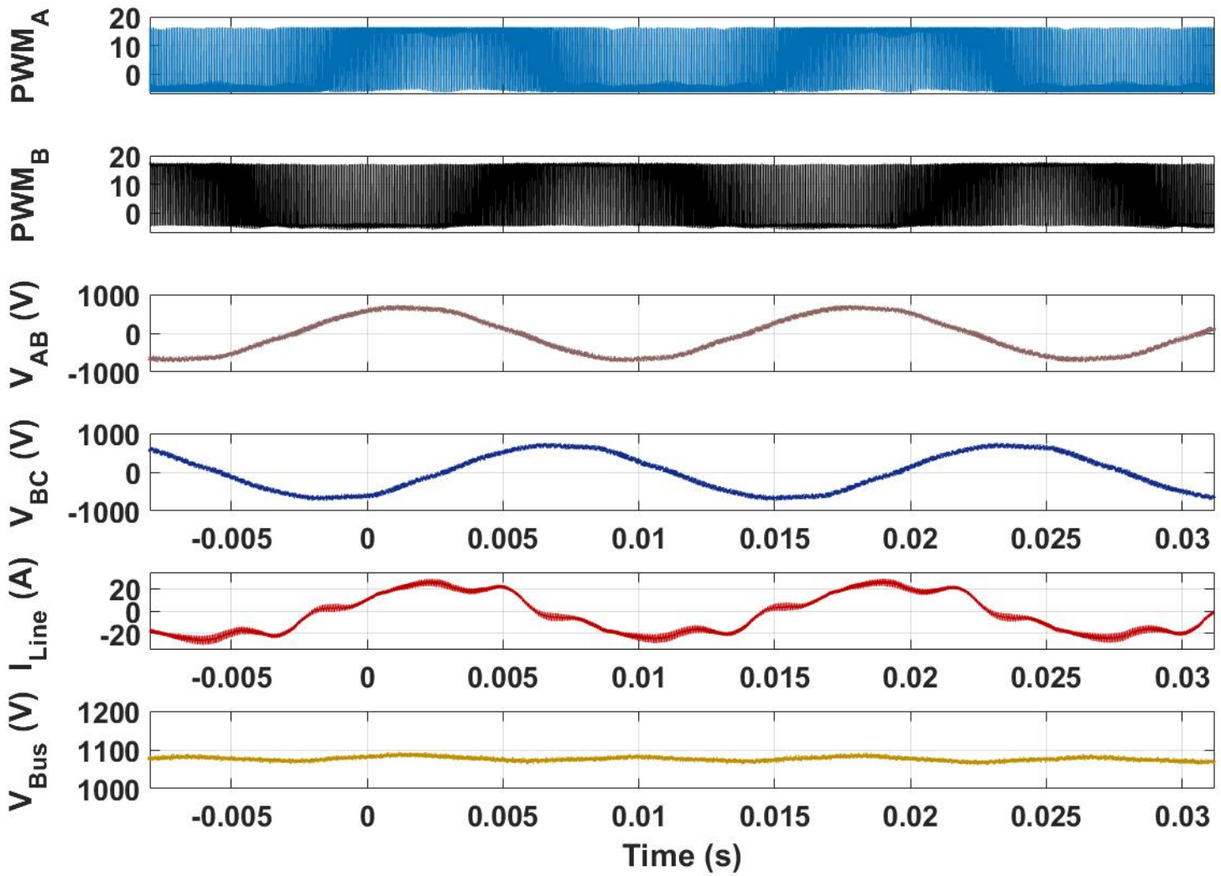


PWM Modulator Output Waveforms

Power Stage Test Results: Grid-tied Tests at 15 kVA

Grid-Tied Test Condition	
Grid Side V_{Line}	480 V
Input Dc Bus Voltage	1070 V
Modulation Index	0.784
Line Filter	1.2 mH (0.03 P.U.)
Switching Frequency	15 kHz
Power	15 kVA
Power Factor*	0.7

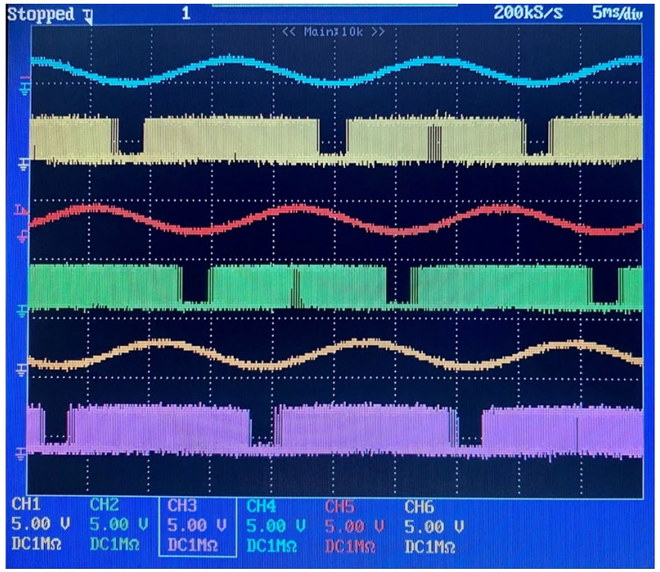
*** The power factor is limited by the active power capability of the power source that has been used during the experiment.**



Grid-tied test waveforms

CHIL Validation of Grid-tied Algorithm at Full Power

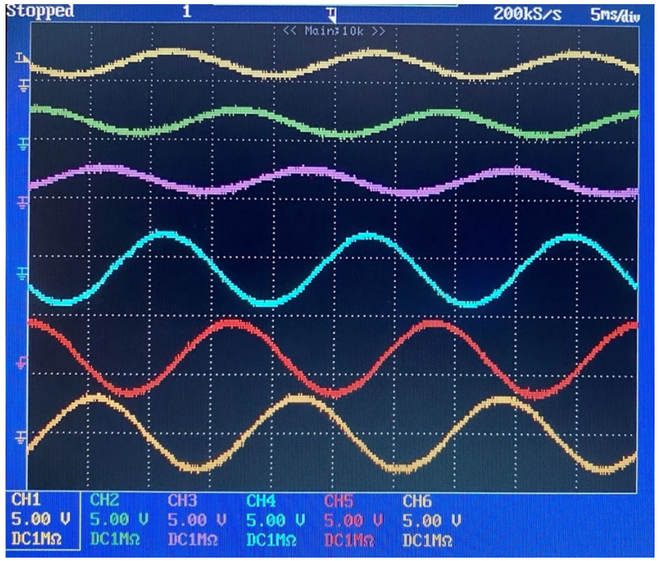
Grid 3-ph Voltages

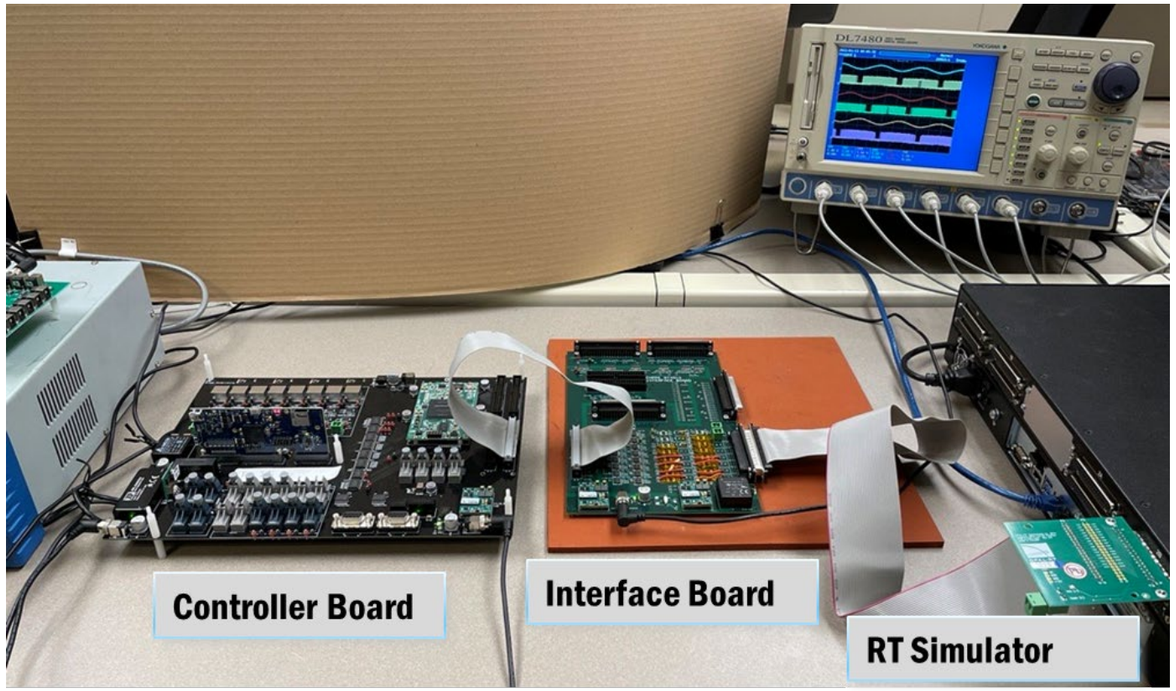


PWMs from the IPS controller

Grid 3-ph Voltages

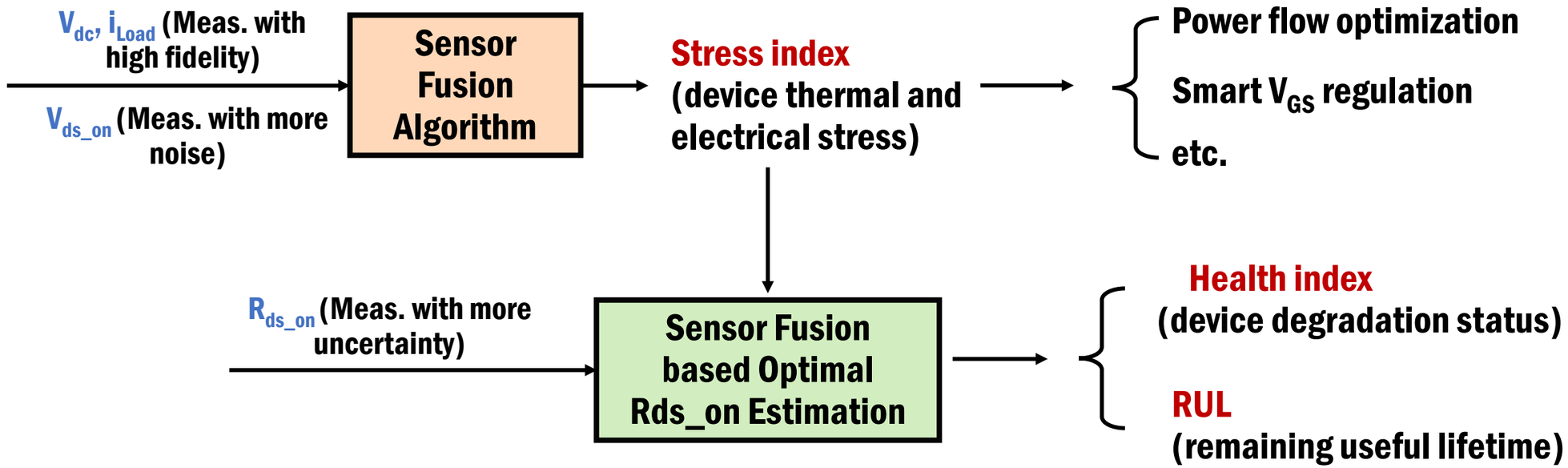
3-ph Line Currents (-100 A, +100 A)



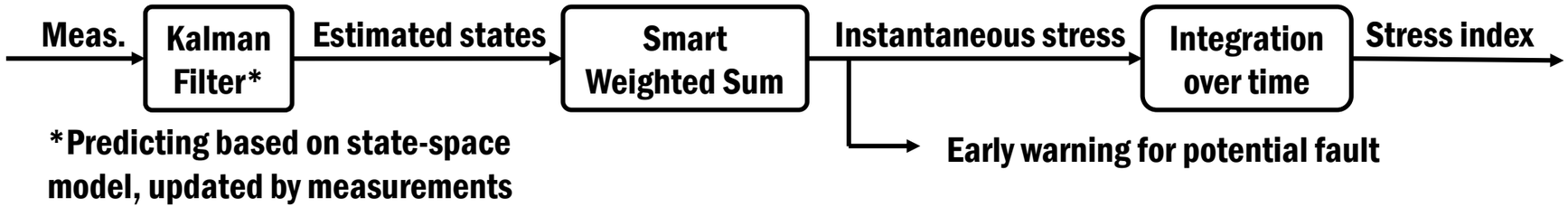


Stress Index and Health Index

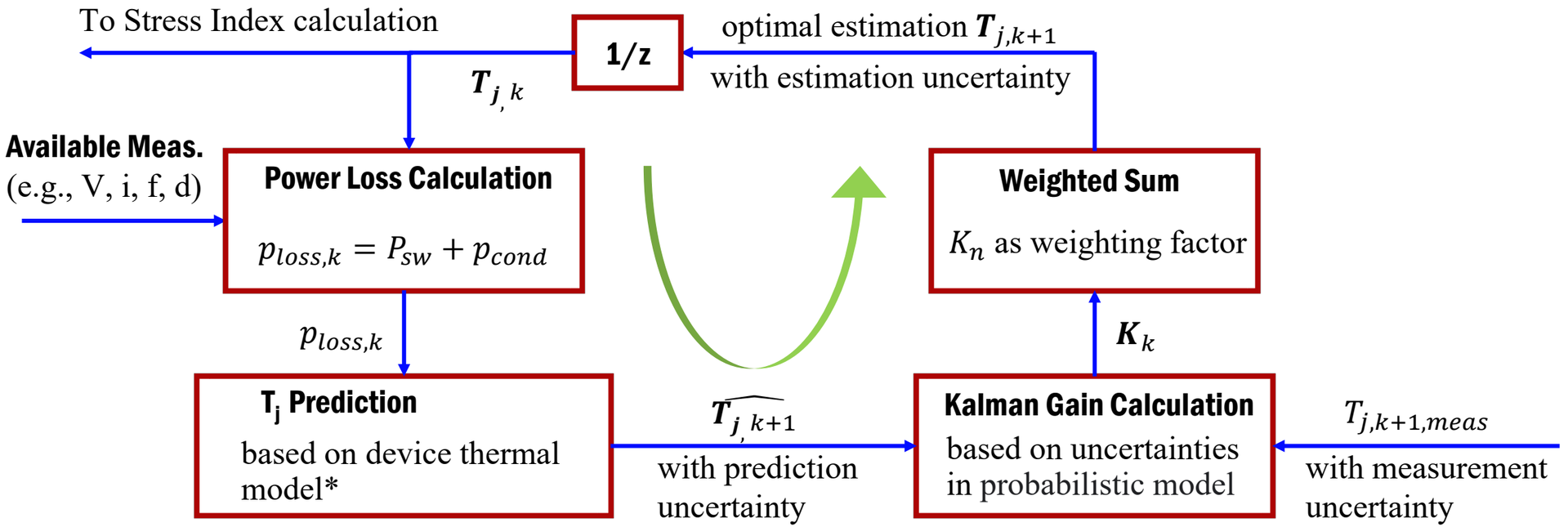
- Stress index indicates thermal and electrical stress level of power devices
- Health Index indicates device degradation status



Stress Index Generation



With Kalman filter, Tj could be estimated optimally based on available measurements



* A proven device thermal model of the Rohm power module is made available to the project team.

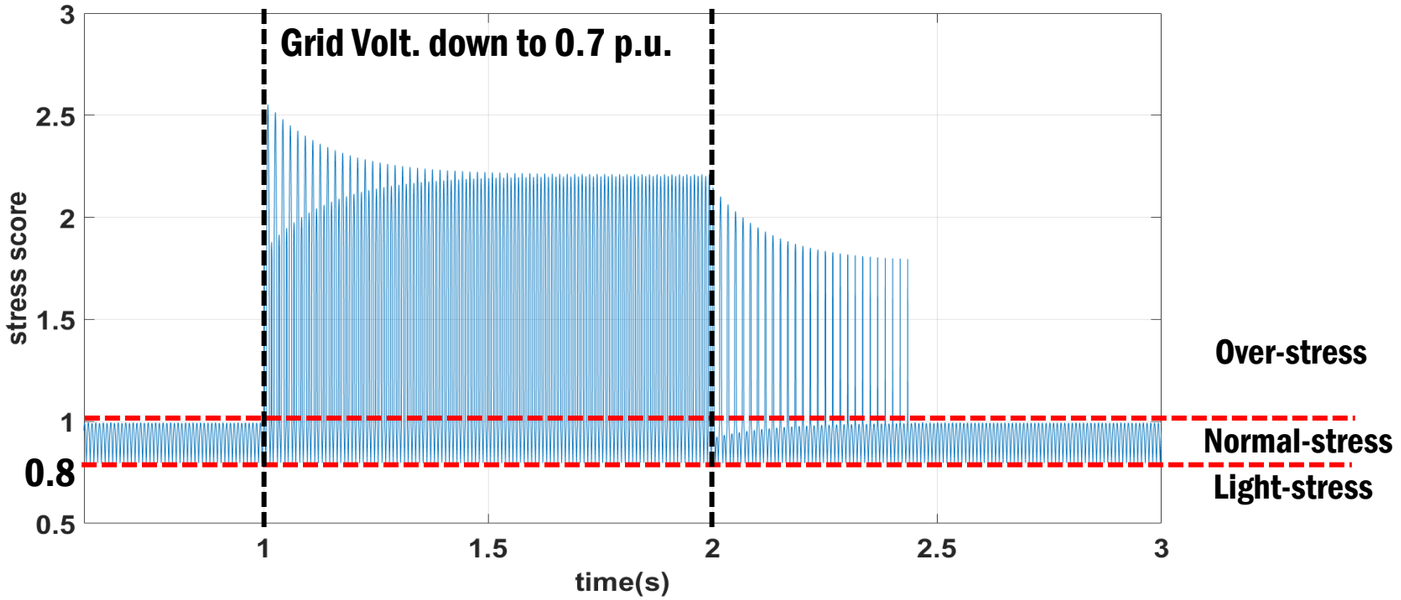
Stress Index Generation and Case Study

$$\textbf{Stress Index} = K_i \cdot \frac{i_{load}}{I_{ac\_Nom}} + K_v \cdot \frac{v_{dc}}{V_{dc\_Nom}} + K_T \cdot \frac{T_j}{T_{j,Nom}}$$

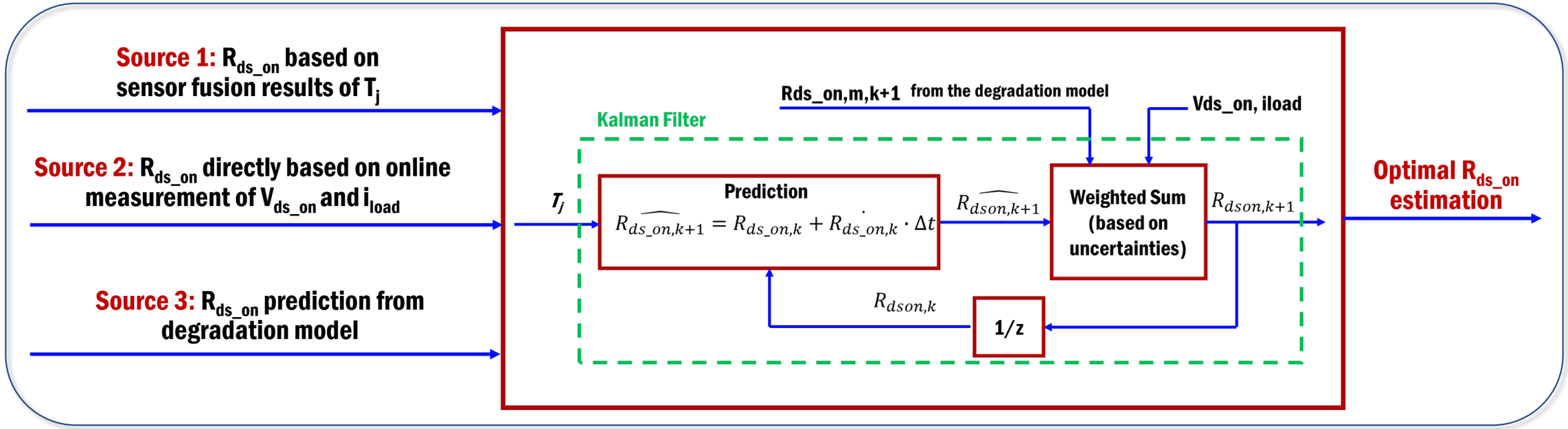
$$\begin{cases} K_v = 0.5 \\ K_T = 0.3 \\ K_i = 0.2 \end{cases} \qquad \begin{cases} V_{dc\_Nom} = 1010\ V \\ I_{ac\_Nom} = 60.5\ A \\ T_{j,Nom} = 56\ ℃ \end{cases}$$

CHIL Test Results of Stress Index Generation during a Voltage Sag Event

When the grid voltage is reduced to 0.7 p.u., the stress index of the device goes up significantly if the inverter is still controlled to output the rated power.

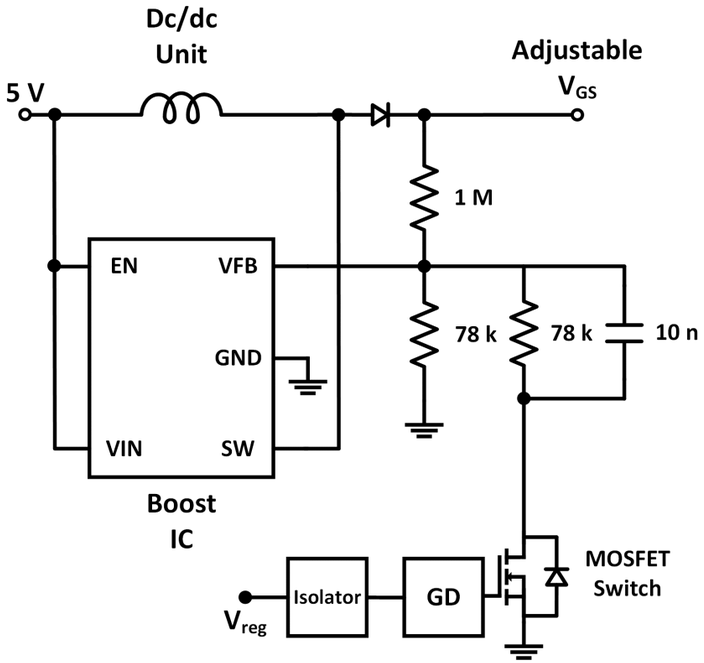


Health Index

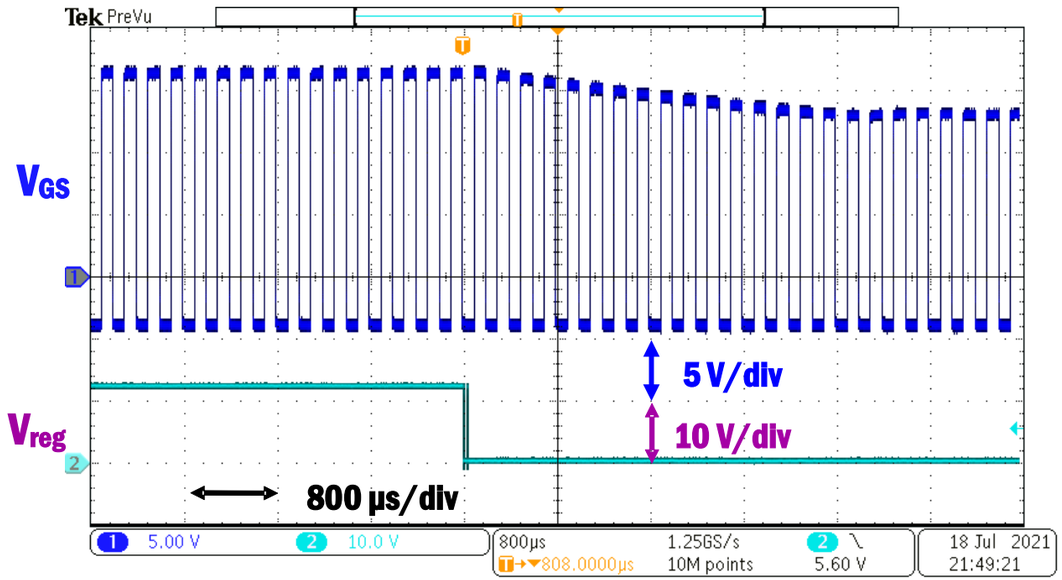


Health index will be mainly based on the degradation of on resistance (Rds_on) of the SiC MOSFET over time.

Gate Voltage Regulation



V_{GS} Regulation Circuit

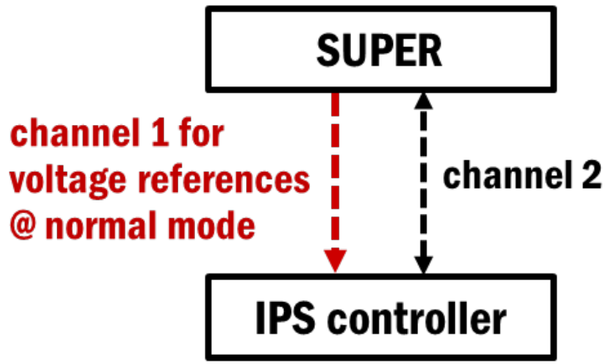


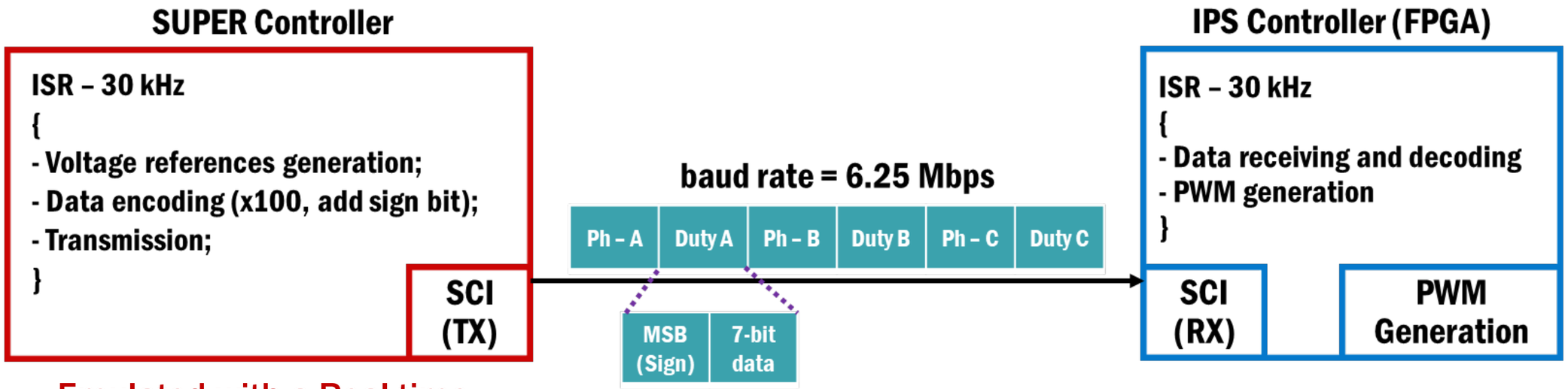
VGS_on Regulation Test Waveform

The gate voltage regulation capability provides SUPER one more knob for load sharing and reliability improvement.

Communication Validation Test Setup

- ❑ **Channel 1 is used for 3-ph voltage references transmission**
  - **SCI (UART) protocol**
  - **Communication in every switching cycle**
- ❑ **Hardware test validation**



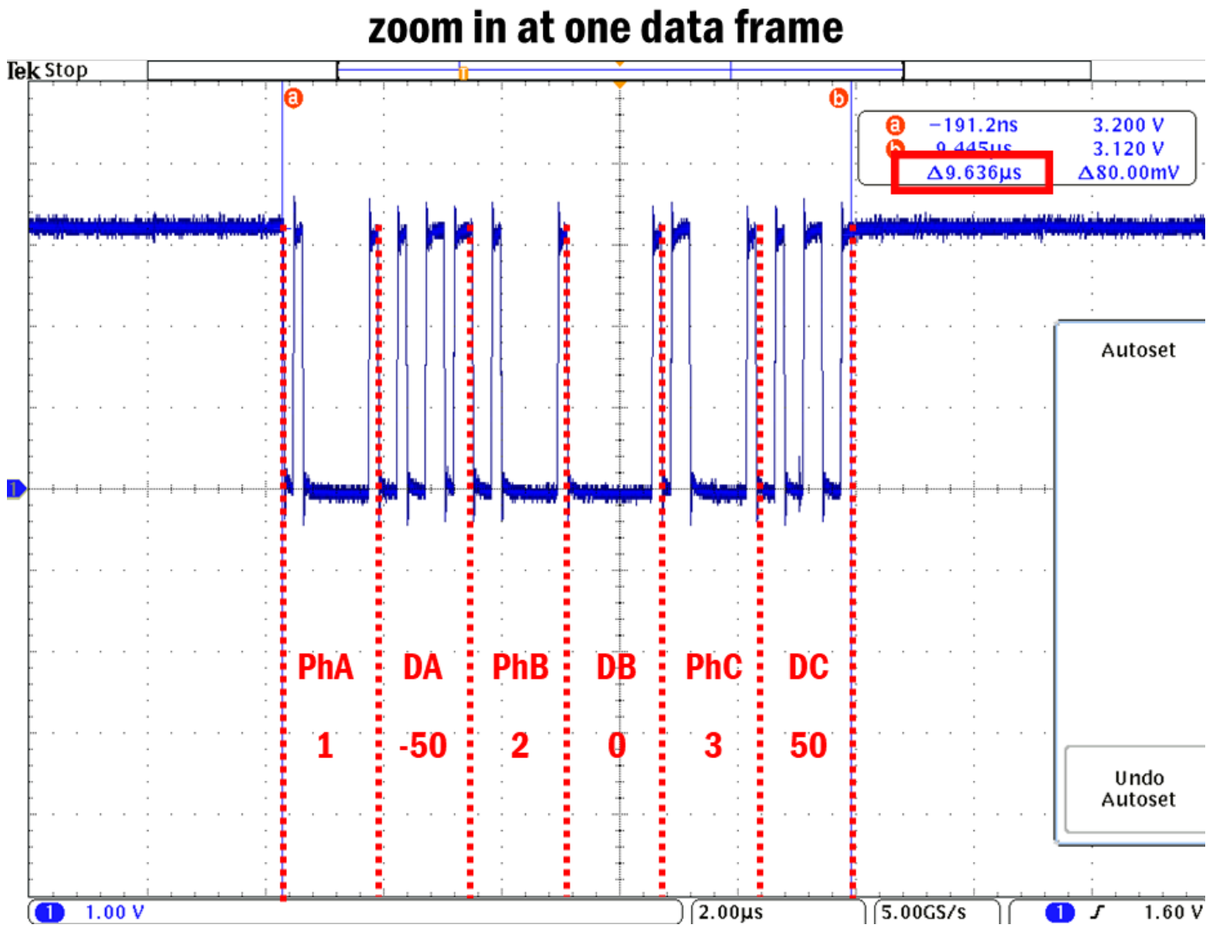


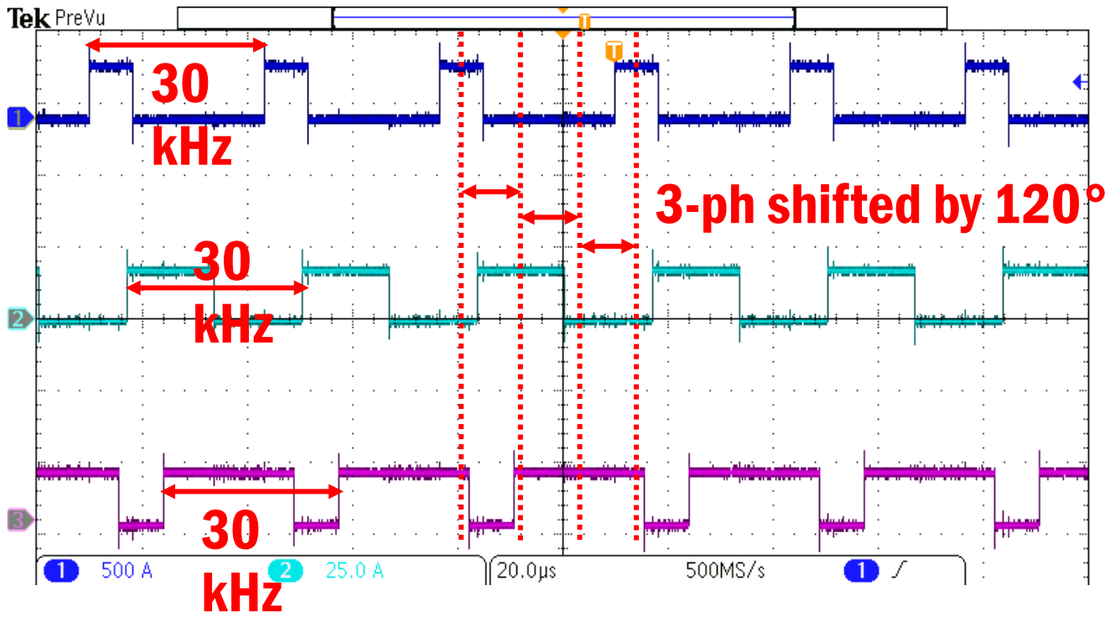
Emulated with a Real-time Simulator

Communication Validation Example

Data receiving from SUPER: for 6.25 Mbps baud rate, the 6 consecutively transmitted data (10-bit each) take 9.6 µs

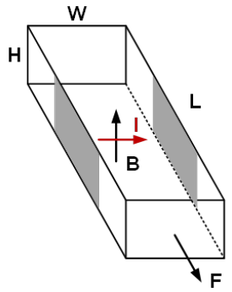
data decoding		duty cycle
Phase A	-50	25%
Phase B	0	50%
Phase C	+50	75%

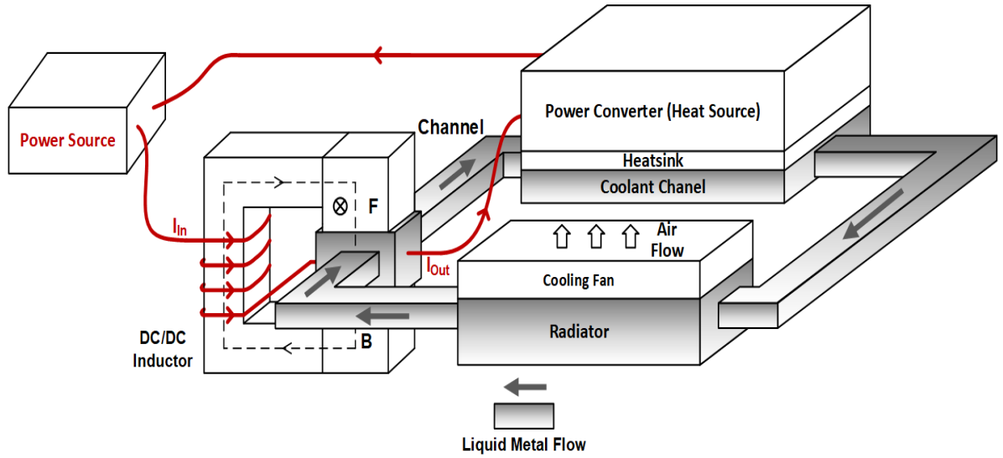


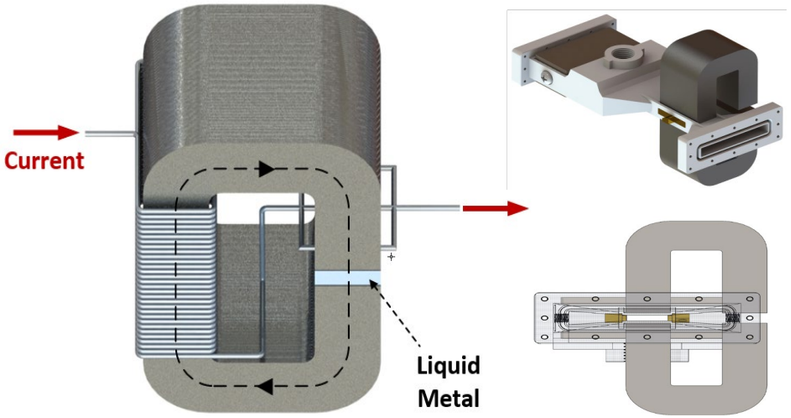


Inductor Integrated Liquid Metal Pump

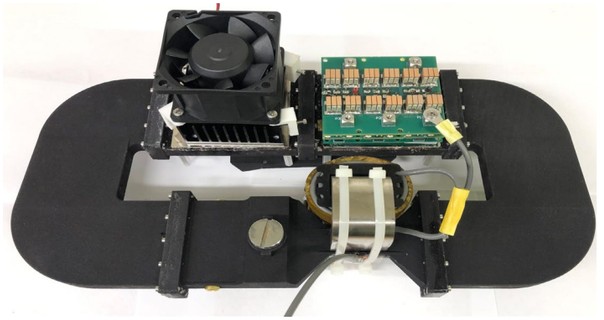
Liquid metal-based cooling with the electromagnetic pump integrated into the inductor of the boost converter *







- Low steady thermal impedance that enables higher power density
- Low transient thermal impedance that enables high over current capability
- Eliminate rotatory pumps
- Great for grid-tied inverters in urban and commercial settings where space is limited, e.g. fast charging stations in lower Manhattan



Concept Validation with a 10 kW Prototype

This concept has been demonstrated separately with a boost converter inductor in a 10 kW prototype.

The IP is solely credited to the IPS project.

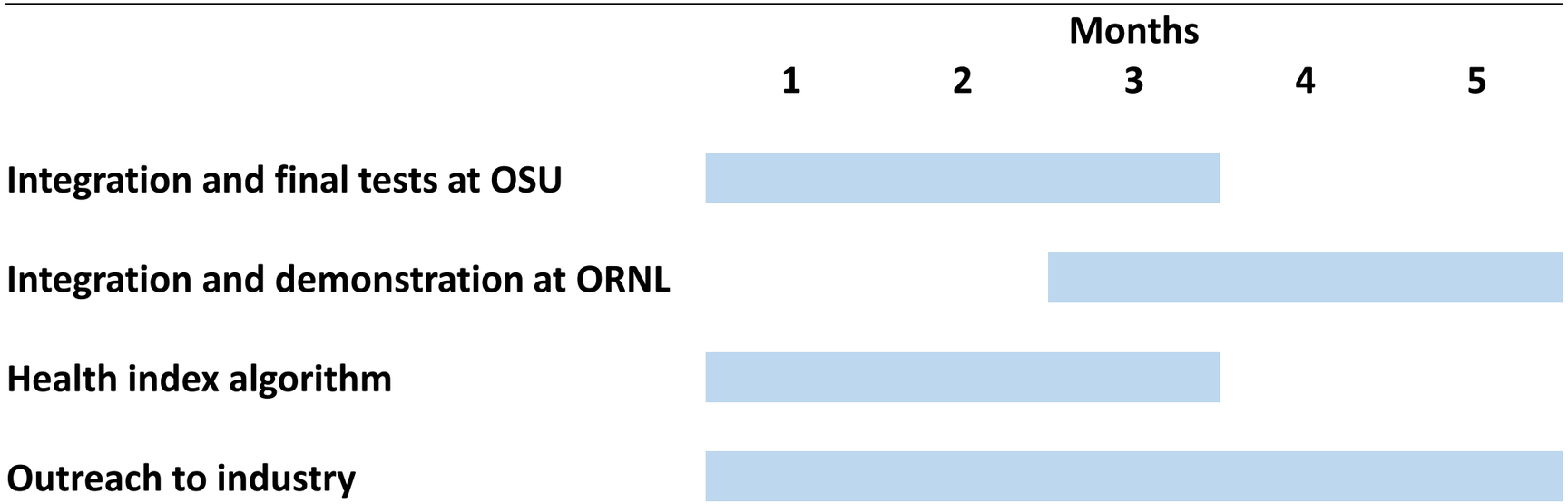
Junchong Fan Won the 2nd Place Award at IEEE ECCE 2021 Student Demonstration Competition.

The concept will be implemented into other projects soon. The team is also in discussion with CoFan on commercialization.

Milestones

Milestones	Description	Status	Expected Finishing Date
M1	Literature Review, circuit analysis	Finished	
M2	Circuit design, detailed schematic	Finished	
M3	PCB design, bus bar design, cooling design	Finished	
M4	Function demonstration of all sub-components	Finished	
M5	Assembly of the IPS and full system validation	In progress	02/01/2022
M6	Demonstration of basic functions at ORNL	Planned	05/30/2022
M7	Demonstration of advanced functions at ORNL	Planned	07/30/2022
M8	SUPER level system demonstration	Planned	09/30/2022

Timeline


Months
1
2
3
4
5
Integration and final tests at OSU
Integration and demonstration at ORNL
Health index algorithm
Outreach to industry

Risk and Mitigation Strategy

Anticipated Delays, Risks

- Covid caused delays in lab work
- Potential damage during transportation
- Difficulties in communication during onsite tests at ORNL due to travel or visit restrictions

Mitigation Strategy

- Streamline test plans
- Start to work on transportation and hand-off plan
- Start to work on a plan on how to remote support the tests at ORNL (video feed, remote monitoring panel, HMI, possible remote control, etc…)

Impact/Commercialization

Technology Impact:

- Advanced sensing hardware and software for health monitoring of grid-tied power converters
- Advanced thermal management of grid-tied power converters by improving heat transfer coefficient

Publications, Presentations and Student Training

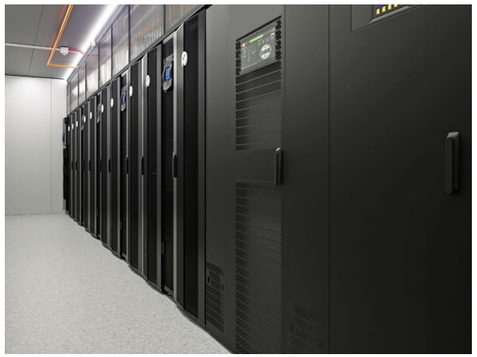
- One MS Thesis: Jesse Pakula, Development of Control and Health Monitoring for a Grid-Tied Three-Phase Inverter Within a Group of Coordinated Inverters
- One paper published; two more planned to be submitted in 2022
- Won the 2nd Place Award at the IEEE ECCE 2021 Student Demonstration
- Four graduate students trained

Impact/Commercialization

Industry Outreach on Health Monitoring for Power Converters

In discussions with Vertiv (previously known as Liebert/Emerson Network Power) to seek collaborations between the SUPER/IPS project team and the leading grid-tied inverter manufacturer.

Vertiv (Revenue 2020: $4.4 Billion) is one of the leading manufacturers of industry-scale uninterrupted power supplies (UPS). Many U.S. data centers are powered with Vertiv's grid-tied UPSs. Vertiv has developed multiple platforms for health monitoring of power converter fleets. After initial discussions and lab tours, Vertiv has expressed great interest in collaborating with the project team.



https://www.vertiv.com/en-us/

Link for the brochure of the Vertiv™ Power Insight

https://www.vertiv.com/4a3cb9/globalassets/products/monitoring-control-and-management/software/trellis-power-insight-data-sheet_243365.pdf

Impact/Commercialization

IP Status

One patent has been filed for the liquid metal-based cooling (solely credited to this project).

- CoFan, one of the largest thermal management company in the United States had reached out for further product and development (https://www.cofan-usa.com)
- The technology will be integrated into other Federal and industry sponsored projects soon.

Three patent applications under preparation: two on monitoring and cooling hardware designs and one for the sensor fusion algorithm.

Three out of four above mentioned IPs will be solely credited to this project. The follow-up IP on liquid metal will be partially credited to this project.

THANK YOU

U.S. DEPARTMENT OF ENERGY | OFFICE OF ELECTRICITY

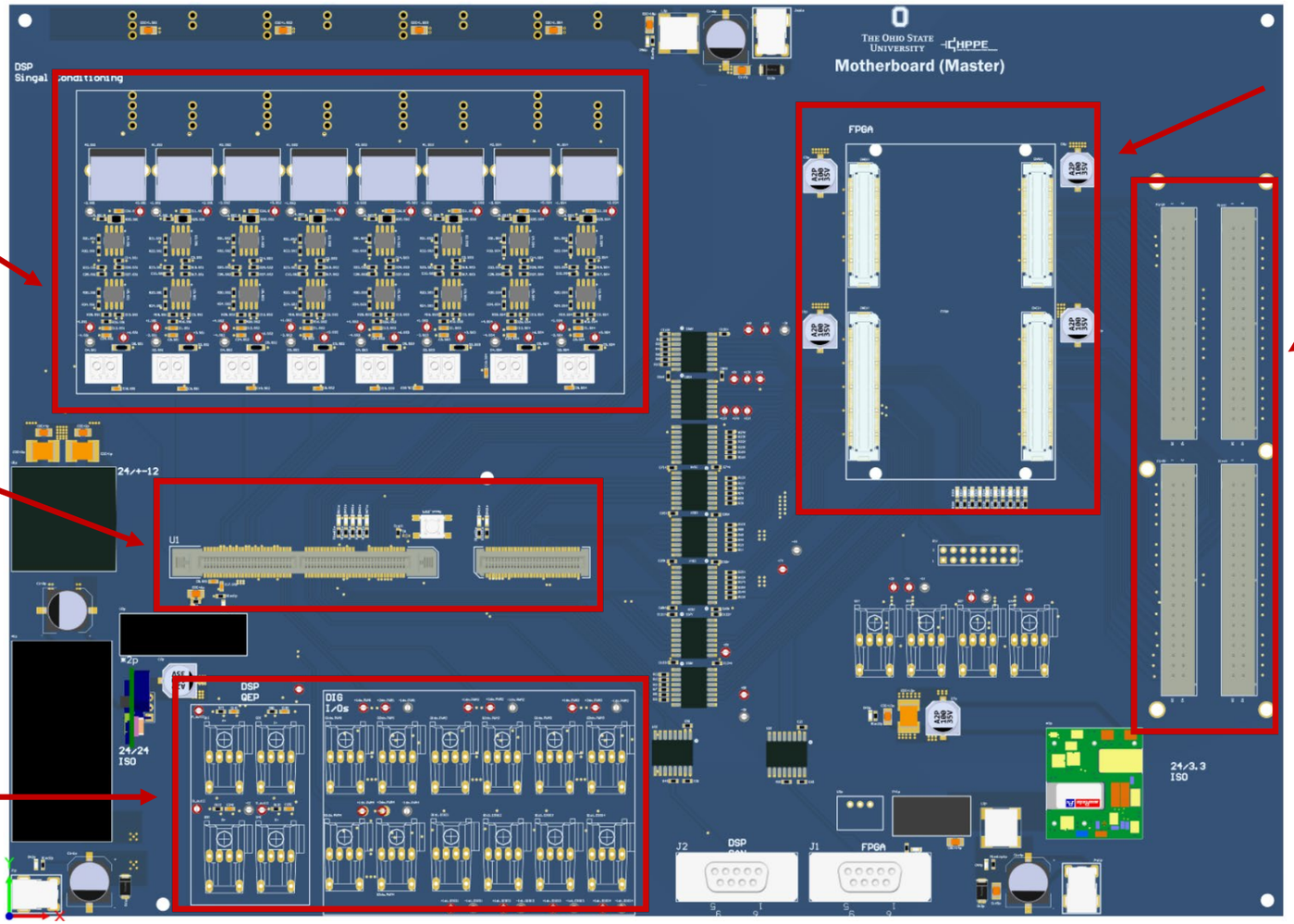
IPS Controller Board Architecture

	DSP	FPGA
P.N.	TMS320f28379D	Cyclone IV EP4CE40F29C8

ADC ports of DSP

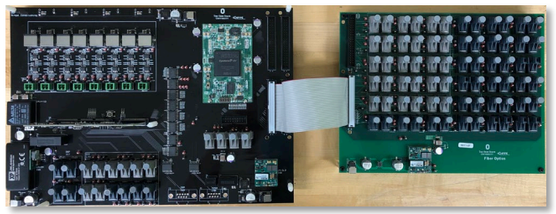
Socket for DSP card

Fiber connectors to DSP GPIO pins



Socket for FPGA board

Connectors to FPGA pins



Controller and interface board