DOE Office of Electricity TRAC

Peer Review

U.S. DEPARTMENT OF ENERGY | OFFICE OF ELECTRICITY

SSPS 1.0: Hardware Development

Smart Universal Power Electronics Regulators (SUPERs) & Intelligent Power Stages (IPSs) for SSPS 1.0

PRINCIPAL INVESTIGATOR
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ORNL

PROJECT SUMMARY

Demonstration of advanced and standardized power electronics interfaces (SUPER & IPS) for the grid

- ❑ **Universal design for grid interfaces – Interfaces that can be tied to assets or loads with changes only to the software layer**
- ❑ **Grid interfaces with advanced & intelligent features – Autonomous operation, online health monitoring & decision-making capability**
- ❑ **Scalable and interoperable design with standardized interfaces**
- ❑ **IPSs with advanced sensing techniques, algorithms capable of estimating the health of at least 2 components**

The Numbers

DOE PROGRAM OFFICE:
OE – Transformer Resilience and Advanced Components (TRAC)

FUNDING OPPORTUNITY:
AOP

LOCATION:
Knoxville, Tennessee

PROJECT TERM:
07/01/2020 to 09/30/2022

PROJECT STATUS:
Ongoing

AWARD AMOUNT (DOE CONTRIBUTION):
$9,000,000

AWARDEE CONTRIBUTION (COST SHARE):
$0

PARTNERS:
Consortium of University Partners

Team - ORNL

ORNL - SUPER architecture, functionalities & advanced algorithms, IPS (developed by ORNL), integration of IPSs from partners

Madhu Chinthavali
Power Electronics System Architecture

Brian Rowden
Hardware design and prototyping

Steven Campbell
System Integration & Testing

Rafal Wojda
Magnetics Design

Jonathan Harter
Hardware development

Radha Sree Krishna Moorthy
Project Lead & Software framework development

Aswad Adib
SUPER and IPS simulation

Jang Euk
Fiber Optic Interface Development

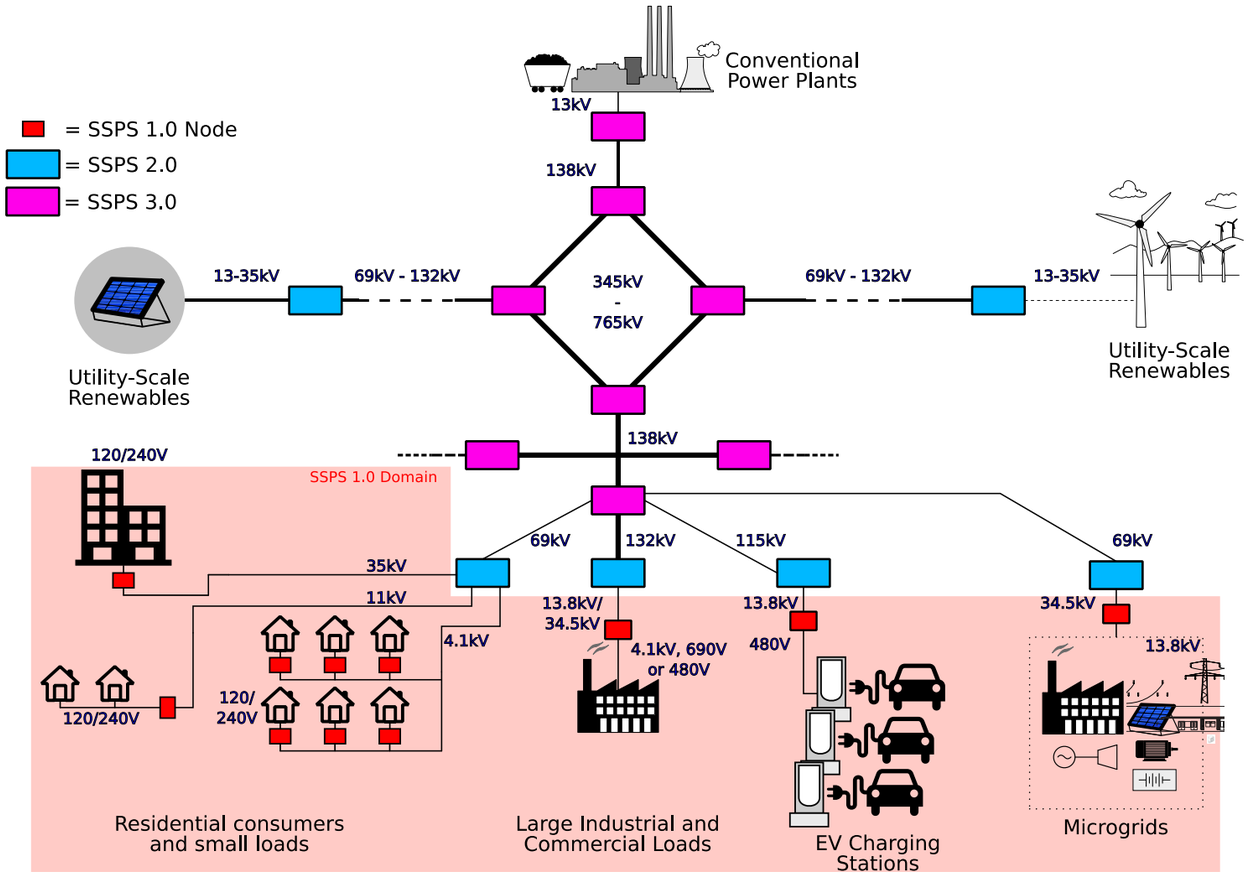
University Partners – Library of IPSs

14 Professors/PIs, 6 Postdocs, 26 Students

- The Ohio State University, Columbus, Ohio: Dr. Jin Wang
- Virginia Polytechnic Institute and State University (Vtech), Blacksburg, Virginia: Dr. Rolando Burgos
- Florida State University (FSU), Tallahassee, Florida: Dr. Helen Li
- The University of Texas at Austin, Texas: Dr. Alex Huang
- The University of Arkansas (UARK), Fayetteville, Arkansas: Dr. Yue Zhao
- The State University of New York (SUNY) at Stony Brook, New York: Dr. Fang Luo
- The University of North Carolina at Charlotte (UNCC), North Carolina: Dr. Babak Parkhideh

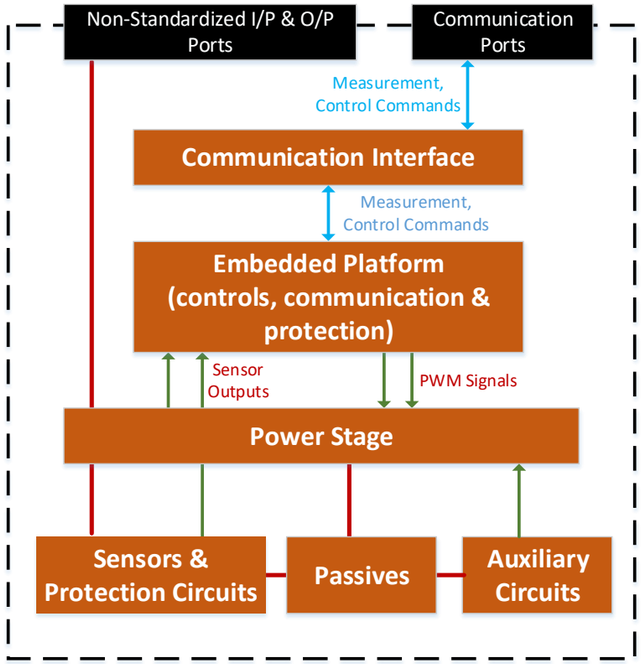
Innovation: SSPS 1.0 Implementation

- SSPS Hubs & Nodes – An autonomous grid entity capable of power and information exchange serving as an interface between the grid and end user.
- SSPS concept will enable hierarchical control, communication, optimization, protection and intelligence
- Architecture realized by fundamental building blocks – modular, interoperable, scalable, autonomous & intelligent grid tied systems

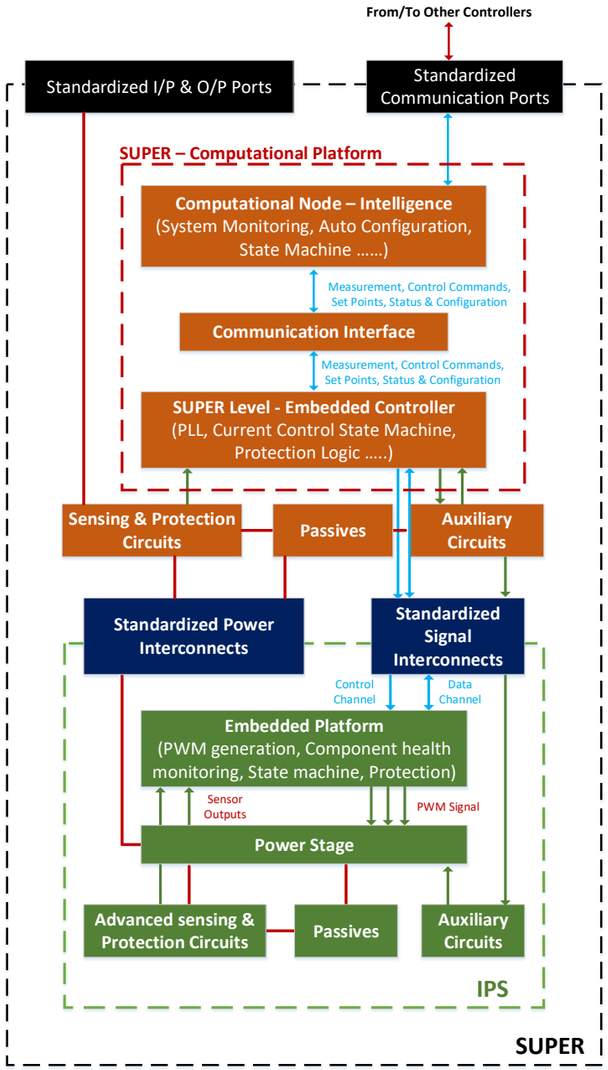


** “Solid state power substation Technology Roadmap”, U. S DOE Office of Electricity, Transformer Resilience and Advanced Components (TRAC) Program, Jun. 2020.

Innovation: SUPER



State of the Art

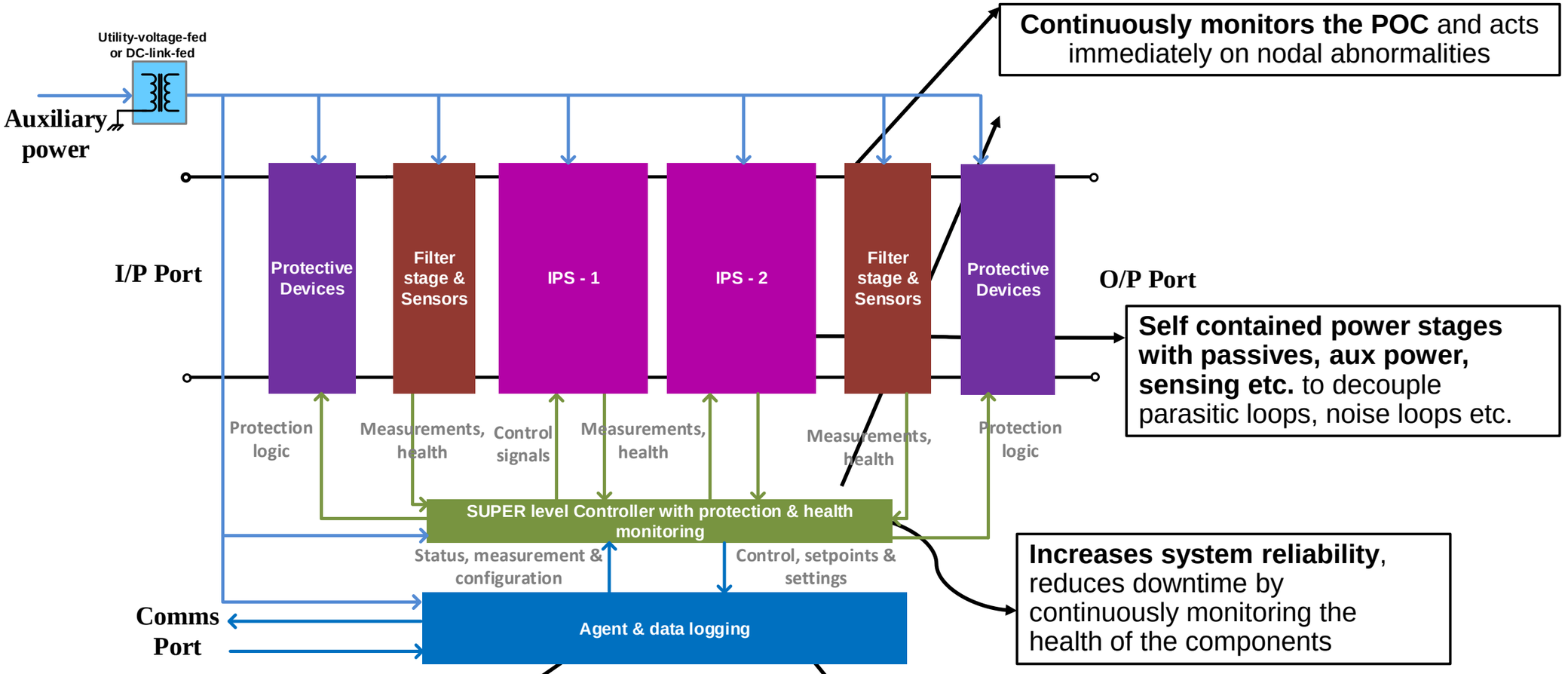


SUPER

SUPER Features	System level impact
1. Interoperability ☑	• Easy integration & reduction in BOS costs
2. Embedded intelligence & decision-making capability with a flexible scalable platform ☑	• Improved voltage profile at the point of connection (POC) • De-rated/continuous operation during failure events
3. Embedded online health monitoring system – Diagnostics/Prognostics ☑	• Allows maintenances to be pre- planned • Can prevent the loss of the inverter from affecting the overall system • Increases lifetime • Data for offline learning algorithms
4. Cyber-physical security	• Improved protection against cyber threats
5. Self contained intelligent power stages ☑	• Decouples parasitics and noise loops • Additional sensing & processor can be utilized for internal health monitoring of IPS

Innovation: Fundamental Building Blocks - SUPER

Smart Universal Power Electronics Regulators (SUPERs) – Modular, interoperable entities that are for fundamental blocks of SSPS



Continuously monitors the POC and acts immediately on nodal abnormalities

Self contained power stages with passives, aux power, sensing etc. to decouple parasitic loops, noise loops etc.

Increases system reliability, reduces downtime by continuously monitoring the health of the components

Enables transactive function for P & Q
Embedded intelligence for fault tolerant operation etc.

Enables **autonomous operation** & **maximizes grid support**. Enables dynamic voltage & frequency regulation etc.

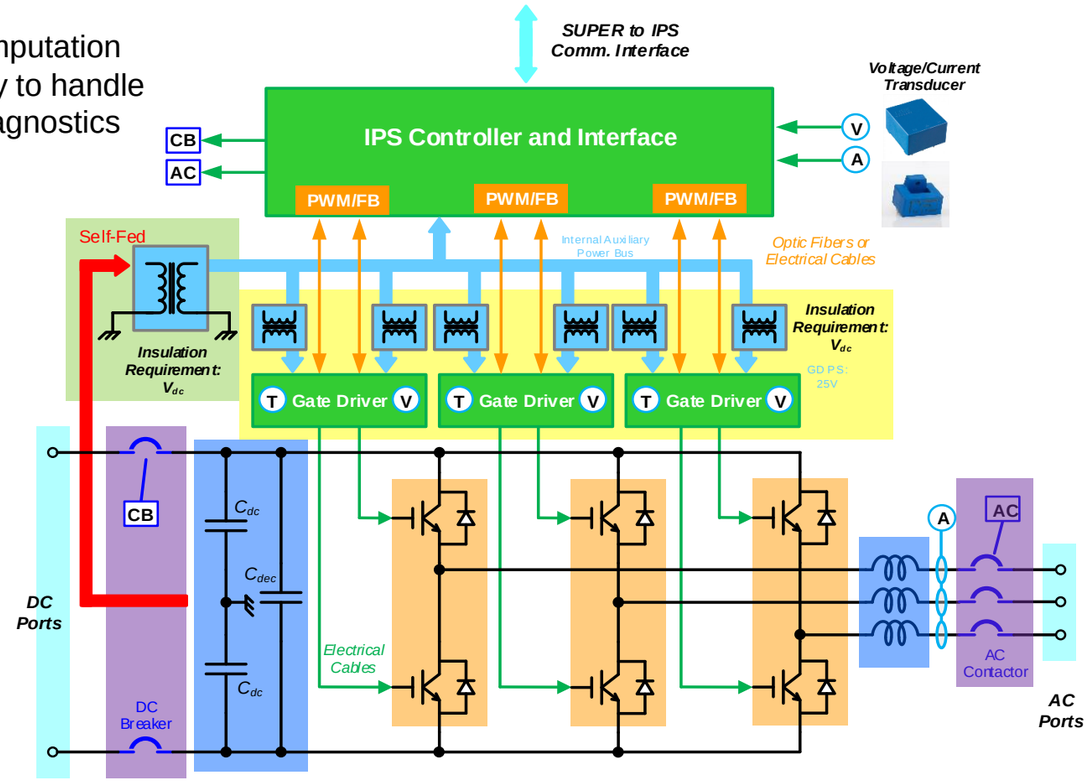
Innovation – Fundamental Building Blocks – IPS

Controller: More powerful computation and communication capability to handle data processing to enable diagnostics and prognostics

Auxiliary power supply: Self-maintained power supply provides safe shut-down during system crash and minimize the Interconnection between SUPER and IPS

Integrated passives: Ensure safe and reliable performance with the minimum required parameters, so the

Device: Advantage packaging to shrink overall SUPER and IPS form factor



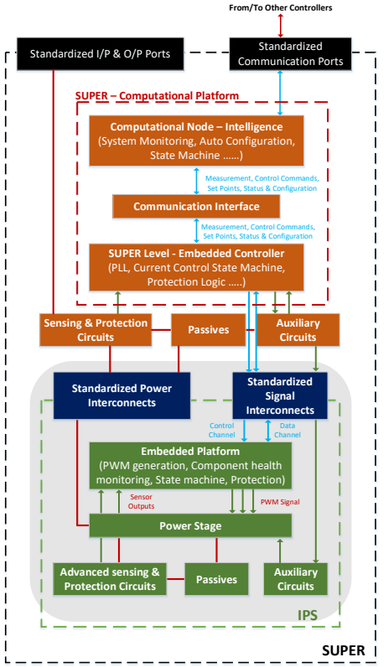
IPS Critical Features Desired by SUPER:

- **Interoperable plug-and-play power stage**
- **Provide sufficient component-level status information to enable accurate SUPER-level diagnostics and prognostics**

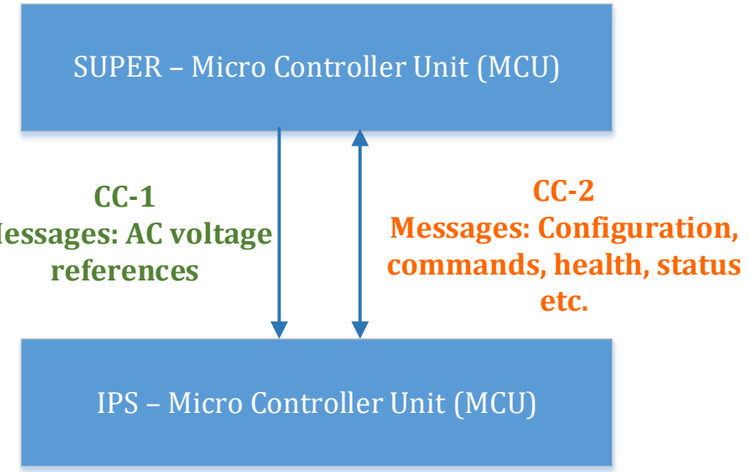
Sensors: Several sensors can be integrated into gate drivers to improve the overall form factor and mitigate noise interference

Interconnectors between components within IPS: More optical interconnections involved to improve the noise immunity capability, especially at higher switching frequency of utilized WBG devices

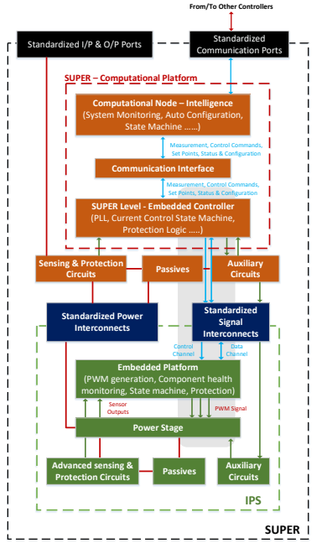
Gate driver: Integrated and intelligent gate driver (i2GD) enables integrated sensing (e.g., dc link voltage, device or phase current), active gate driving, and initially enable diagnostics and prognostics features for SUPER

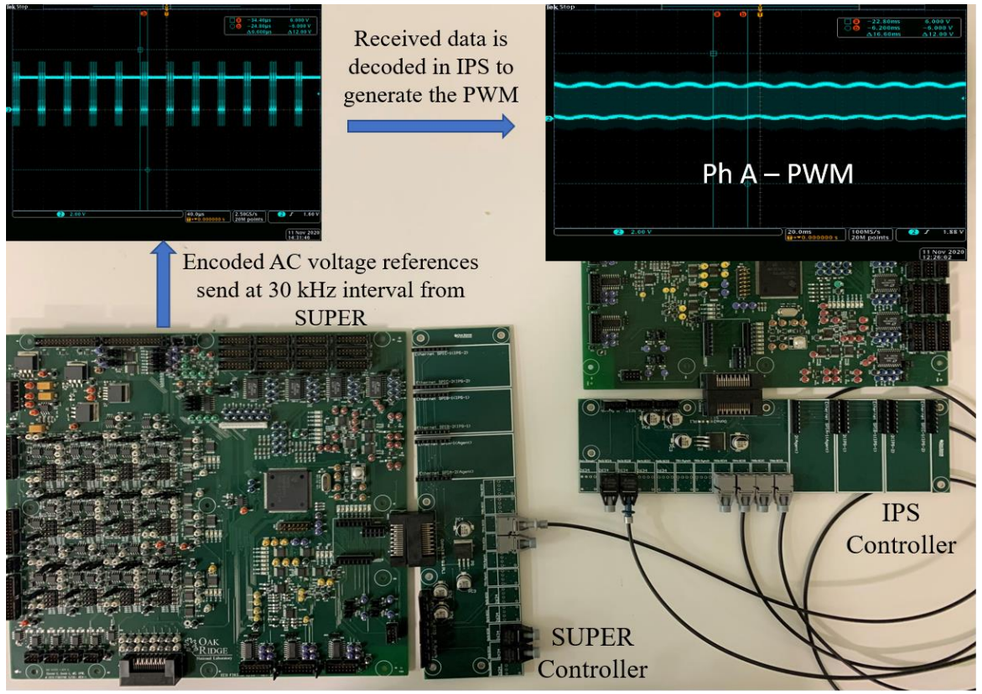


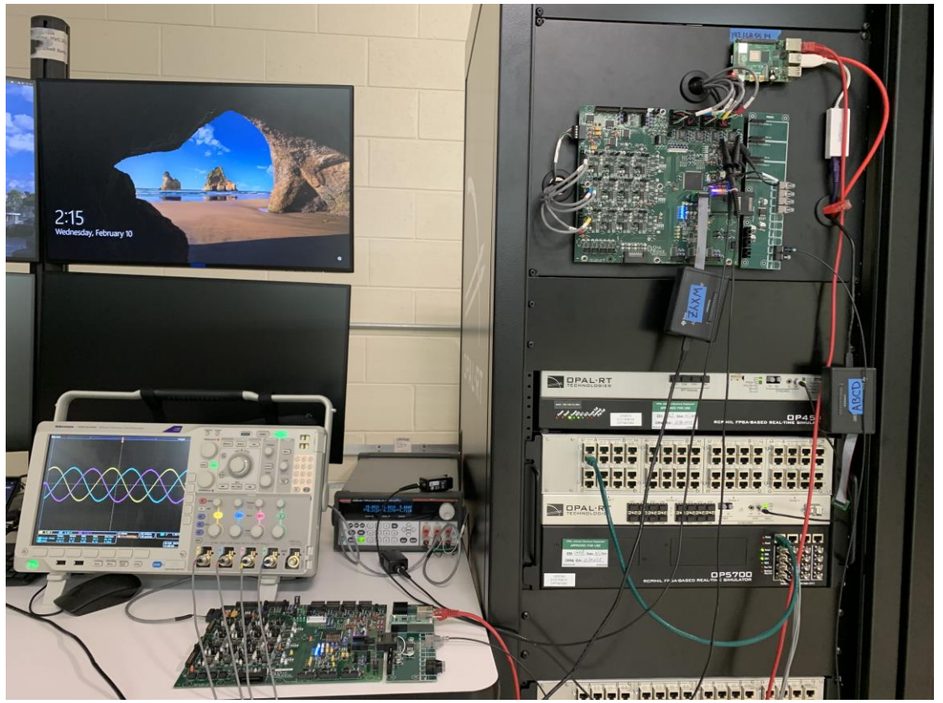
Innovation Update #1: Communication Validation



- Validation of SUPER & IPS control architecture with a high-speed communication link (6.25 Mbps)
- The communication architecture was validated by all partners



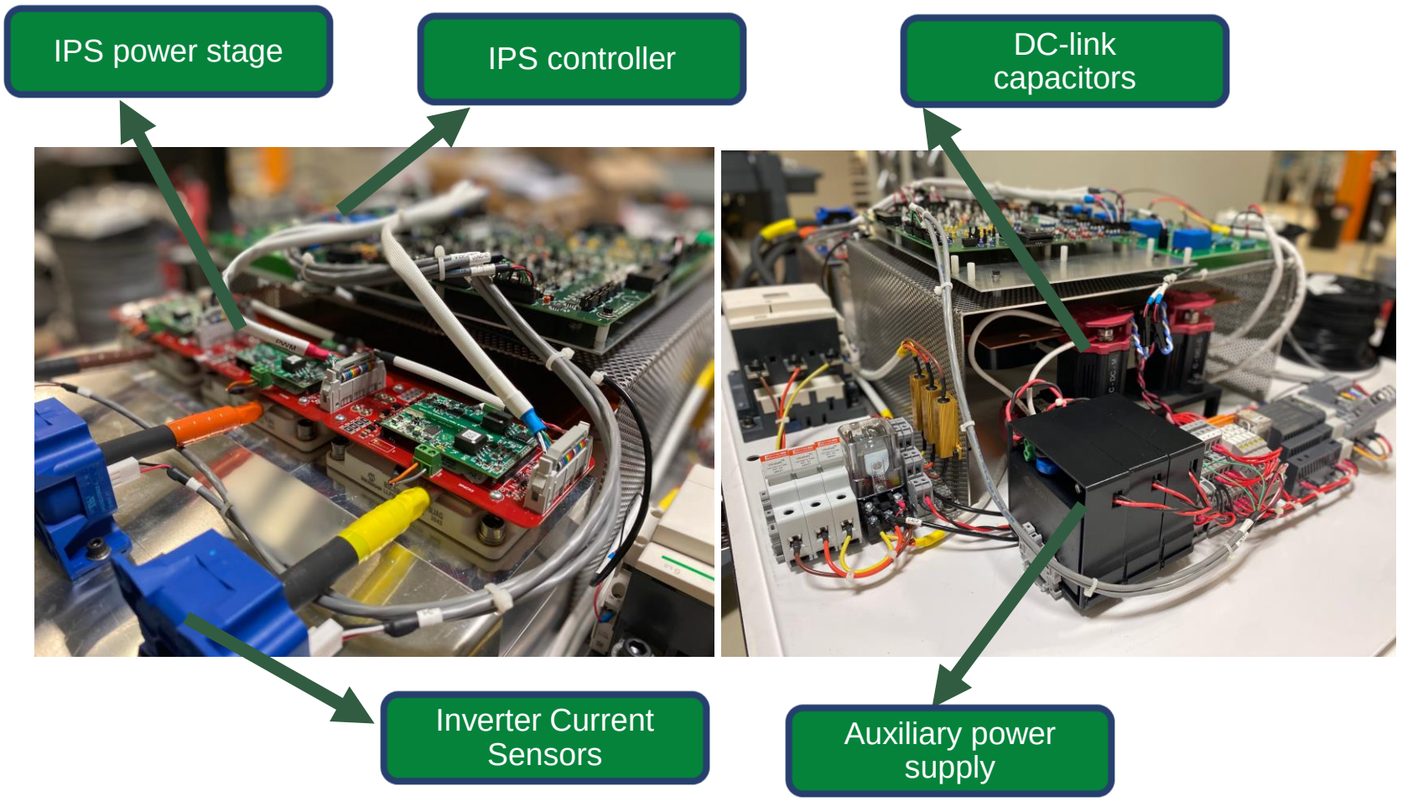


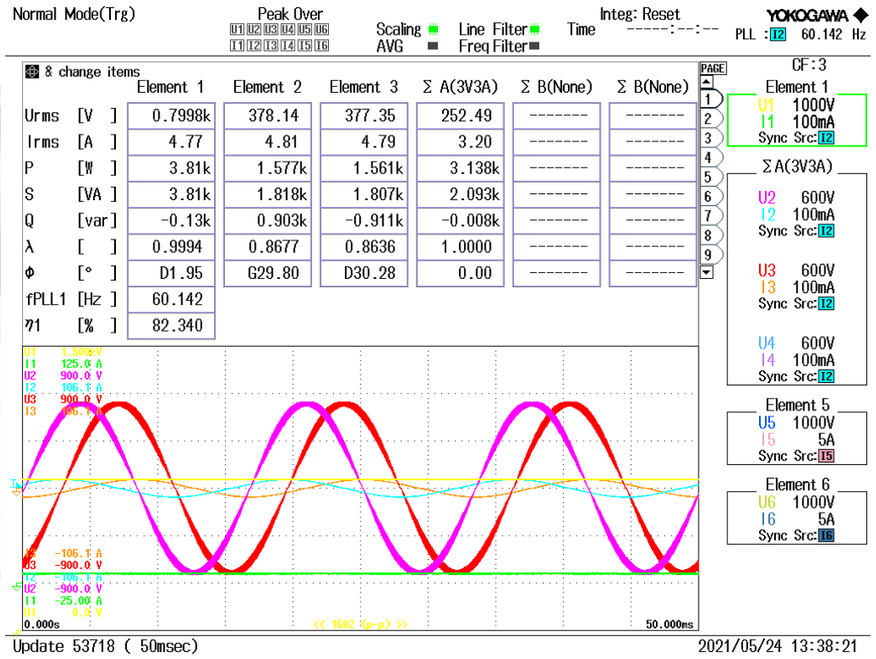


CHIL Setup for SUPER validation in Grid-C

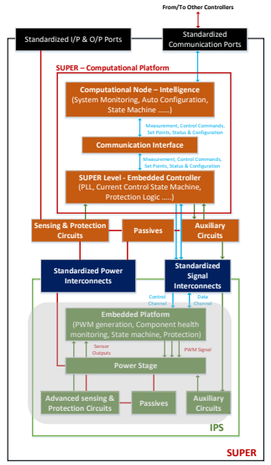
Innovation Update #2: Baseline IPS Validation

Components of the baseline IPS including contactors, gate drivers, IPS controller, communication expansion board were tested extensively during integration



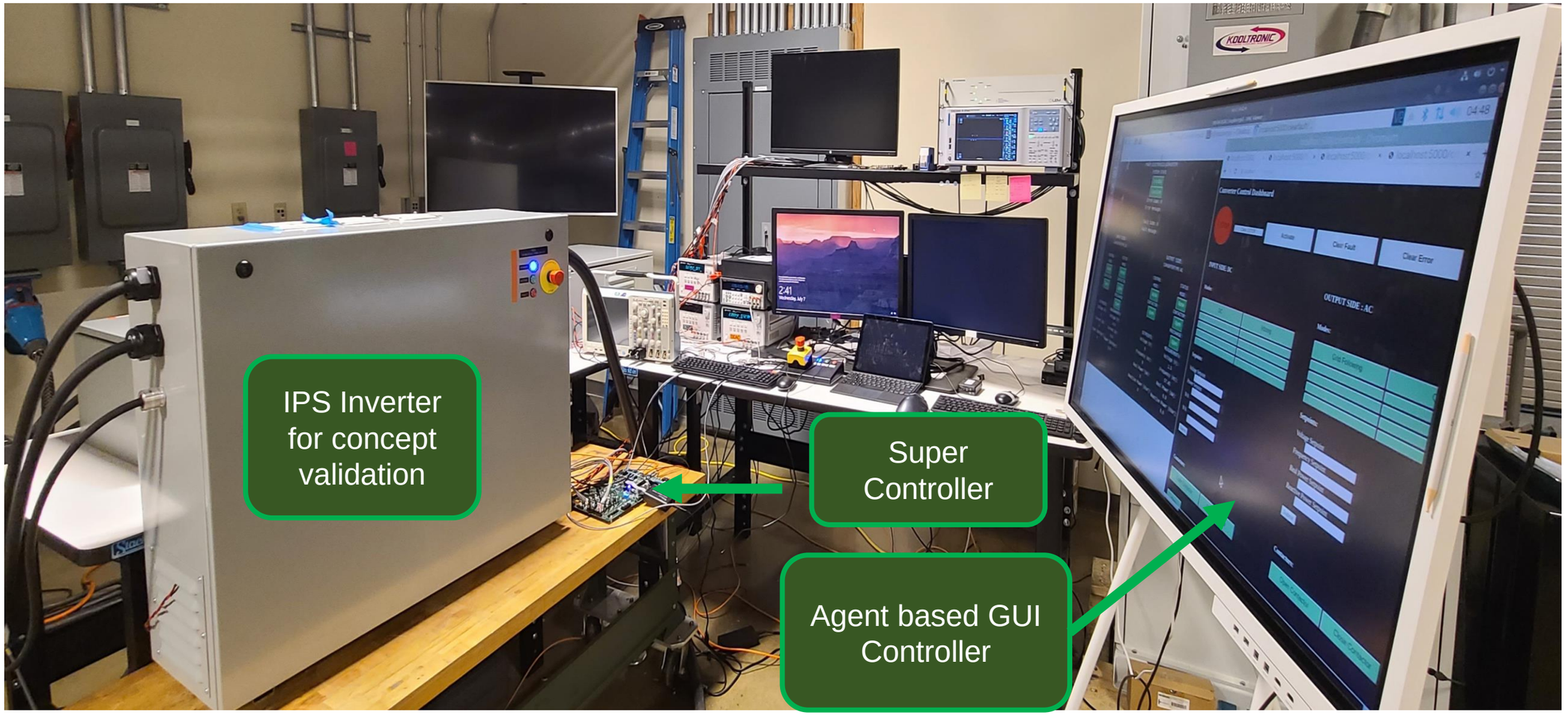


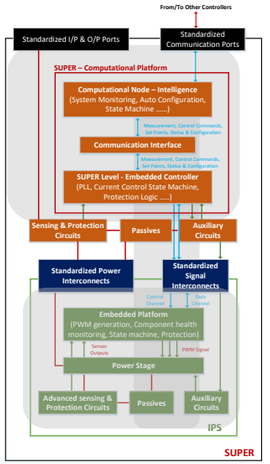
IPS testes at 800 V, 3.8 kW, 30 kHz in open loop configuration



Innovation Update #3: Overall Architecture Validation

Validation of SUPER & IPS architecture with high-speed communication links, controls, protection and standardized interfaces for grid functions

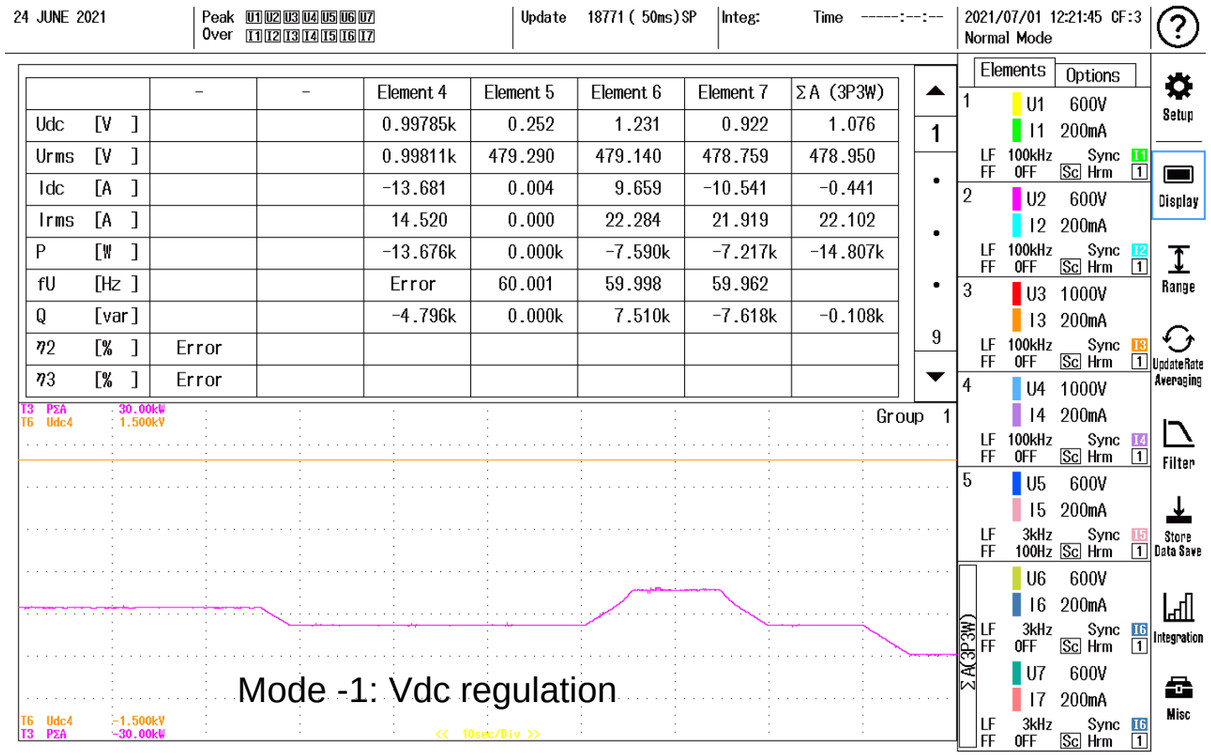




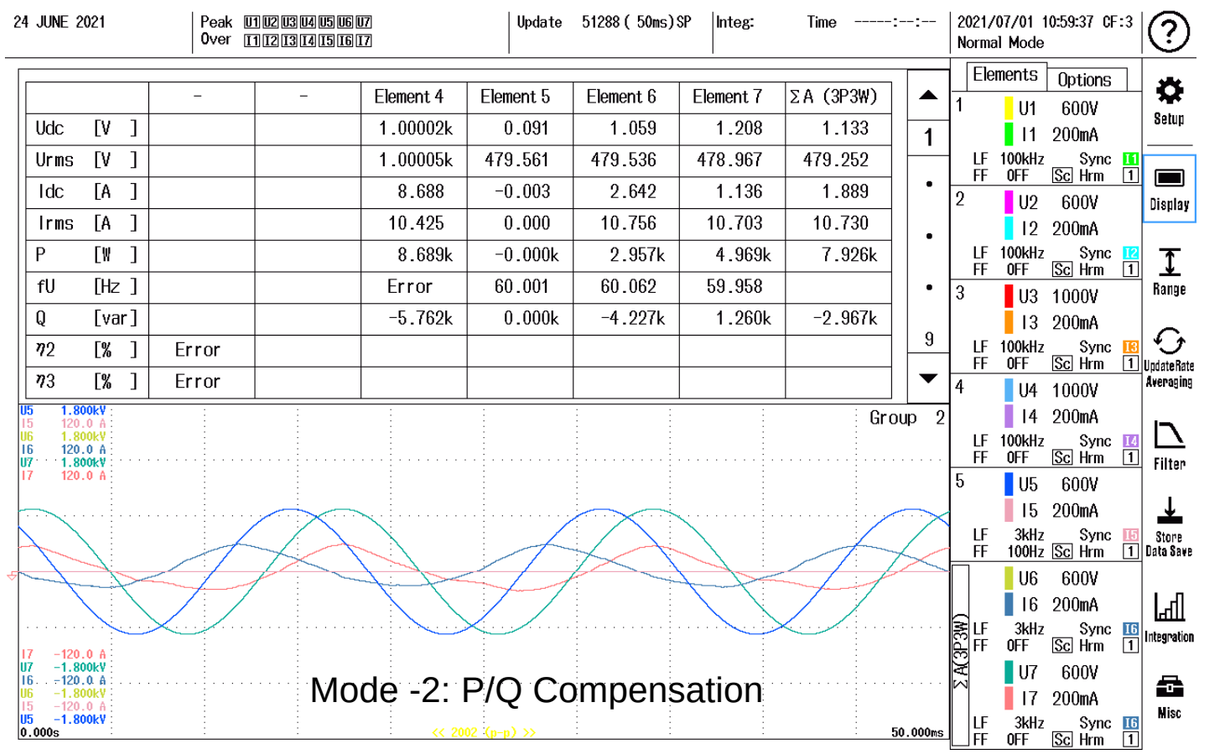
Innovation Update #2: Overall Architecture Validation

- ❑ Vdc regulation (GI): The SUPER maintained the dc-link at 1-kV & real power P (up to 15 kW), was injected/absorbed using battery test system

- ❑ P/Q Compensation (DCSI): SUPER injected/absorbed P/Q from/to the grid (Tested up to 10 kW & -5 kVAR)



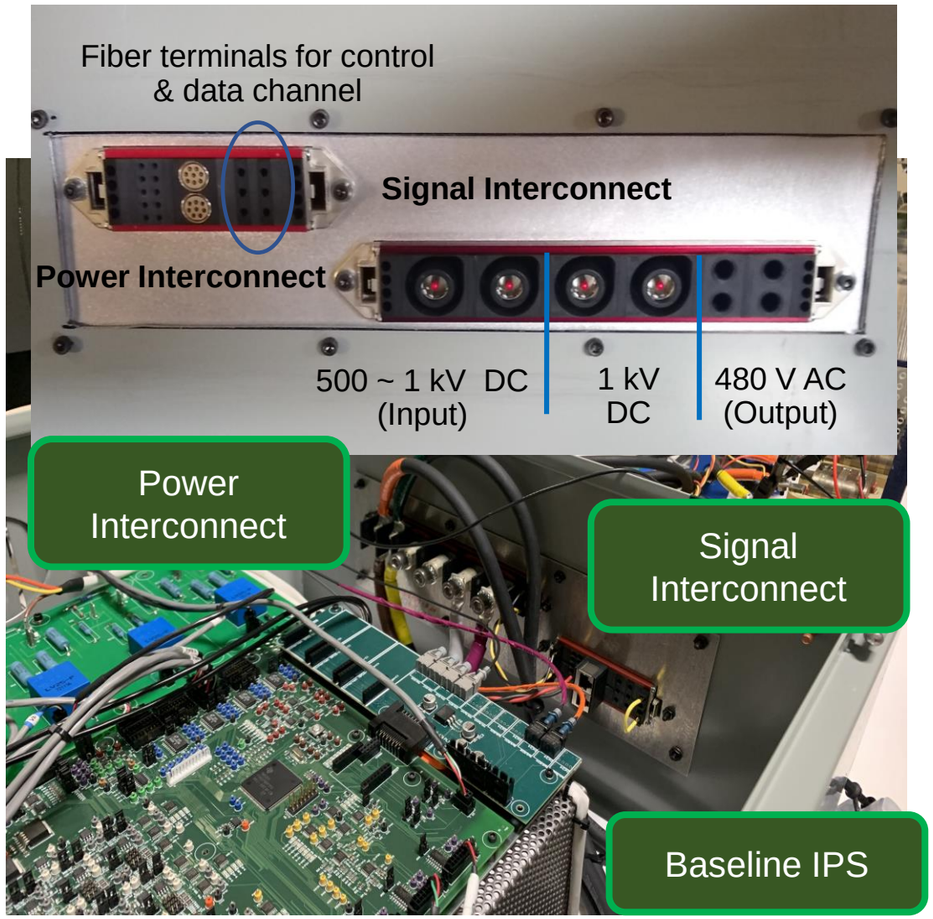
	-	-	Element 4	Element 5	Element 6	Element 7	ΣA (3P3W)
Udc [V]			0.99785k	0.252	1.231	0.922	1.076
Urms [V]			0.99811k	479.290	479.140	478.759	478.950
Idc [A]			-13.681	0.004	9.659	-10.541	-0.441
Irms [A]			14.520	0.000	22.284	21.919	22.102
P [W]			-13.676k	0.000k	-7.590k	-7.217k	-14.807k
fU [Hz]			Error	60.001	59.998	59.962	
Q [var]			-4.796k	0.000k	7.510k	-7.618k	-0.108k
η2 [%]	Error						
η3 [%]	Error						

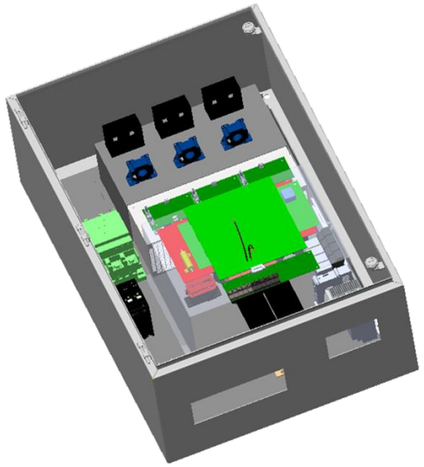


	-	-	Element 4	Element 5	Element 6	Element 7	ΣA (3P3W)
Udc [V]			1.00002k	0.091	1.059	1.208	1.133
Urms [V]			1.00005k	479.561	479.536	478.967	479.252
Idc [A]			8.688	-0.003	2.642	1.136	1.889
Irms [A]			10.425	0.000	10.756	10.703	10.730
P [W]			8.689k	-0.000k	2.957k	4.969k	7.926k
fU [Hz]			Error	60.001	60.062	59.958	
Q [var]			-5.762k	0.000k	-4.227k	1.260k	-2.967k
η2 [%]	Error						
η3 [%]	Error						

Innovation Update #3: Standardized Interconnects & Enclosure

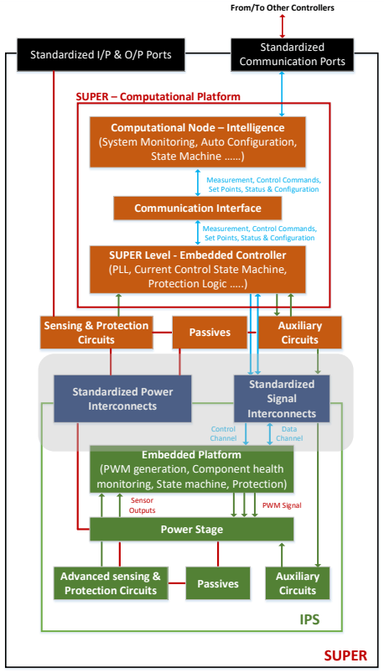
- Modular test cell configuration to show interoperability between IPSs from university partners
- Test cell designed to operate at 1kV, 480 V & 150 kVA and be agnostic to IPS design and non-idealities & support parallel operation.





Parameters	Fiber Optic
POF Diameter (core)	980/1000 um
Protective Covering Diameter	2200 um
Insertion Loss	< 3dB @ 650nm (socket/pin depends on assembly) <6 dB@ 650nm (common lens)
Mating cycles	500 (socket/pin) 100,000 (lens)

Parameters	AC Terminals	Intermediate DC-Link Access / DC Terminals
Rated voltage	600 V ac	5 kV dc (line – line) 2.9 kV (phase – neutral)
Rated current/contact	150 A	20 A (2 poles) / 32 A (1 pole)
No. of poles	2	1 or 2
Contact diameter	8 mm	3 mm
Contact resistance	< 150 µΩ	< 1.1 mΩ
Mating cycles	100,000	100,000
Type of termination	Screw	Crimp



Innovation Update #4: Standardized SUPER Test Cell

- Modular test cell configuration to show interoperability between IPSs from university partners

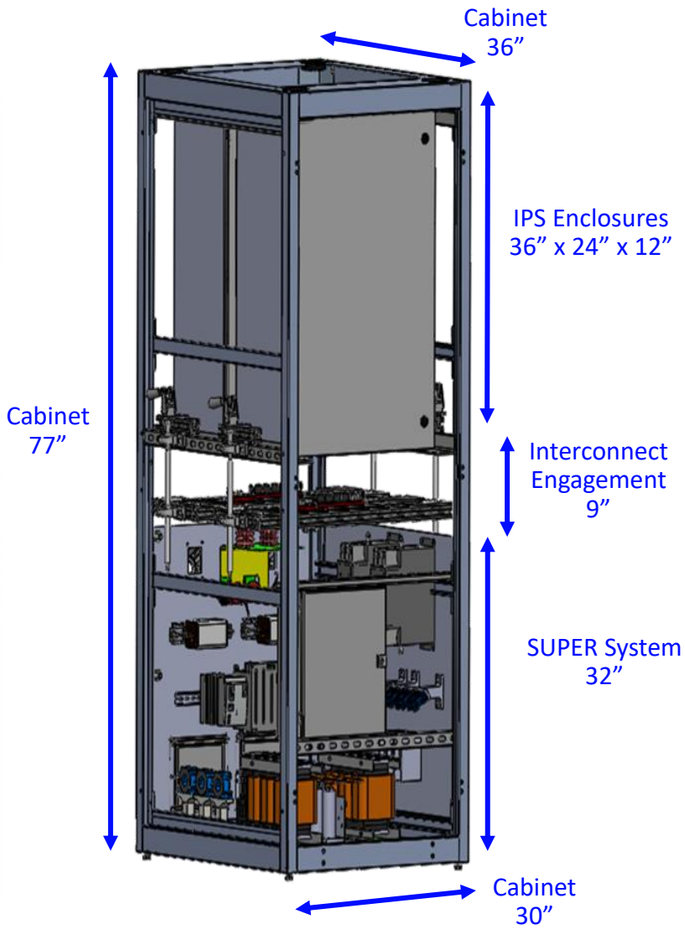
Power Routing
- DC Bus, Intermediate DC Bus, Precharge circuits
- DC Fusing, and DC Main Interconnects
- AC Routing, Filters, to LCL Interface

SUPER Auxiliary Supply Routing
- 480Vac to 24V Supply and Battery backup
- SUPER 15V and 5V Supply
- Wide range DC input to 24V supply
- Interconnect Switch

LCL Interface
- LCL (configurable for 1 or 2 IPS test positions) and Sensors
- AC Bus, Fusing and Grid Interconnect

Shielded Control Cabinet
- Houses the controller & the communication interfaces
- Receives the signals through the standardized signal interfaces from IPS

Engaging & Disengaging Mechanism for the Interconnects



Innovation Update #5: IPS Library & Features

❑ Library of IPSs from university partners to validate **vendor agnostic design** of SUPER

IPS from University Partners	Topologies		Features
	DC/DC	DC/AC	
Florida state university (FSU)	Interleaved buck boost converter with coupled inductor	3-ph 2-level voltage source inverter (VSI)	Interleaved configuration reduces the Input current ripple. Ideal for BES applications
Ohio State University (OSU)	Traditional boost converter	3-ph 2-level VSI with carrier frequency modulation	Capability to integrate the inductor with the liquid metal cooling
University of Arkansas (UARK)	Soft-switching CLLC Bidirectional dc/dc converter	3-ph 2-level VSI	Resonant configurations for power transfer at higher frequencies and with soft switching
University of New York, Stony Brook (NY-SB)	Interleaved boost converter	3-ph 2-level VSI with redundant half bridge legs & coupled ac inductors	Capitalizes on P & N cell layout to optimize switching speeds
University of North Carolina, Charlotte (UNCC)	-	4-leg 3-ph 2-level VSI	4-leg configuration is suitable for harmonic filtering applications
University of Texas, Austin (UT-Austin)	DC/DC stage with parallel devices	3-ph 2-level VSI with parallel devices	Parallel devices for current handling capability
Virginia Polytechnic University (Vtech)	3-level dc/dc converter	3-ph 2-level VSI	3-level configuration reduces the EMI

*green color text highlights IPS with discrete devices

Innovation Update #5: IPS Library & Features

IPS Features	University Partners
1. Interoperability - Standardized electrical ports and communication interface - Enclosure scalability and standardization - Compliance to standards & protocols	• Execution by ORNL with al university partners
2. Embedded intelligence & decision-making capability with a flexible platform **-** Interoperable/scalable with different embedded controllers - Monitors the point of connection continuously - Easy transition between control mode required by SUPER - Immediate response to IPS internal faults with least impact to the SUPER	• Framework is developed by ORNL and will be communicated with all university partners
3. Embedded online health monitoring system – Diagnostics/Prognostics **-** Embeds temperature sensors in IPS to enhance thermal monitoring for prognostics - Monitors the health and degradation status of critical components in IPS - Captures/maps faults to their corresponding signatures - Robust/retrievable events recording and reporting system	• In-situ on-state resistance measurement (Vtech, UT-Austin & UNCC) • In-situ junction temperature measurement (UARK & UT-Austin) • In-situ gate leakage current measurement (FSU) • Estimation of passive components (UARK) • DC-link capacitance health estimation (NY-SB, UNCC, Vtech & UARK)
4. Integrated minimum passive, intelligent gate driving, sensing and protection - Standardized minimum integrated passives - Intelligent and robust gate driving scheme - Integrated sensing and protective device	• Intelligent gate driver (Vtech & FSU) • Advanced current sensors (UNCC) • Fusion algorithms for sensed signals (OSU) • Digital twin for prognostics/diagnostics (NY-SB)
5. Cyber-physical security **-** Hardware and software mechanisms to secure power electronics systems	-
6. Self-contained auxiliary power supply - Draws the required power from IPS itself and power all the contained components	• All universities

Innovation Update

Milestone Update

Milestone Description (or Go/No-Go Decision Criteria)	Period	Status	Accomplishments/Notes
1.1.1 - Validation of SUPER design, operation and controls through simulation and establishing the major IPS design requirements.	BP1 – Q1	Completed	❑ Identified the hardware, controls, communications, interface requirements for SUPER & IPS considering the project objectives
1.2.1 - CHIL validation of the agent framework, the control modes & protection logic and strategy. 1.2.2 - 3D layout of the SUPER 1.0 with all its subcomponents.	BP1 – Q2	Completed	❑ The entire agent framework with the control, protection & communication were validated in CHIL. ❑ The passives for SUPER have been designed and validated through simulations. ❑ The 3D layout of the SUPER with all its subcomponents has been developed.
1.3.1 - Preliminary results from open loop testing of SUPER 1.0	BP1 – Q3	Completed	❑ Magnetics prototyping and testing has been completed. ❑ Standardization details for IPS including constraints were articulated to the university partners. ❑ Open loop testing of SUPER has been completed.
1.4.1 – Experimental results of autonomous operation of SUPER functioning as G with IPS 1.0.	BP1 – Q4	Completed	❑ Closed loop operation of SUPER has been validated experimentally with the agent.

Innovation Update

Milestone Update

Milestone Description (or Go/No-Go Decision Criteria)	Due	Status	Accomplishments/Notes
2.1.1 - Complete the development of testbed for experimentally validating IPS 2.0 and its subcomponents.	BP2 – Q1	Completed	❑ The SUPER test cell development has been completed
2.2.1 - Complete the performance evaluation and validation of IPS 2.0 power stage from university partners.	BP2 – Q2	In Progress	
2.3.1 - Experimental results validating the response of IPS 2.0 for a grid function. 2.3.2 – Demonstration of advanced featured of IPS 2.0.	BP2 – Q3	Not Started	
2.4.1 - Demonstration of autonomous operation of SUPER 2.0 functioning as G with IPS 2.0s 2.4.2 - Demonstration of SUPER 2.0 operating as L 2.4.3 - Demonstration of scalability of SUPER 2.0 with two non-identical IPS 2.0s Complete the final report with the summary of the results.	BP2 – Q4	Not Started	

Innovation Update

Risks

- Anticipated delays in validation of IPS in the SUPER test cell owing to the pandemic
- Anticipated delays in the integration of IPS from university partners in the SUPER test cell

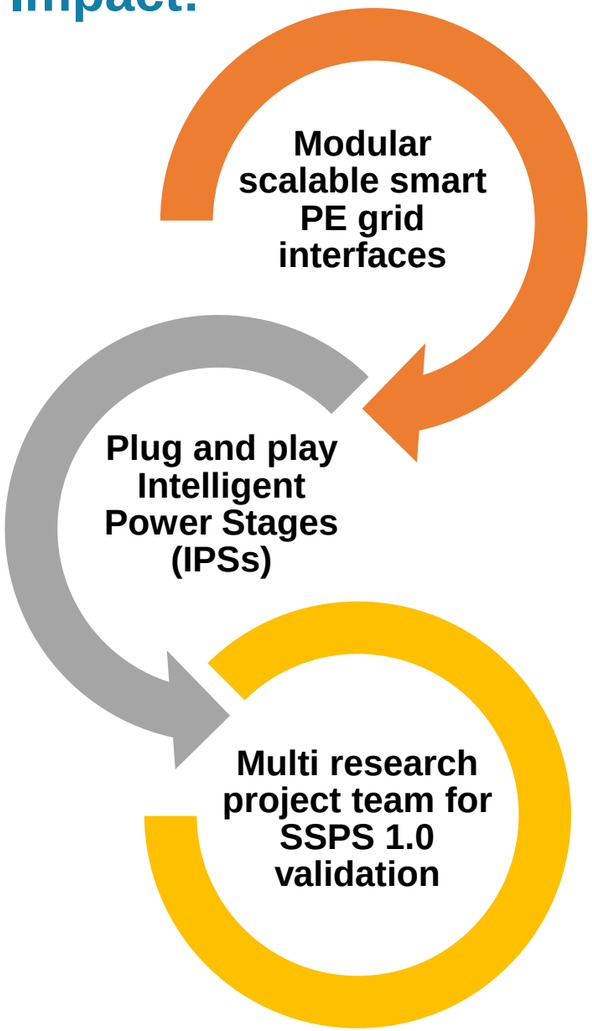
Innovation Update

Future Work

- Validate advanced features like online health monitoring in SUPER with IPSs from partners
- Validate advanced algorithms in SUPER for grid support
- Demonstrate the grid support capabilities of SUPER

Impact/Commercialization

Impact:



- Provides a pathway to develop power electronics interfaces with well defined hierarchy in controls, communication, protection, intelligence and optimization for scalability & modularity
- Provides a pathway to develop a library of power converters for SSPS 1.0
- Provides a pathway for interface, communication, protection standardization
- Provided a pathway to develop holistic systems with embed intelligence & advanced features systematically and strategically in fundamental blocks
- Helps emulate the different vendor scenario to access interoperability & standardization

Impact/Commercialization

Invention Disclosures Filed:

- M. Chinthavali and R. S. K. Moorthy, “Fundamental Building Block Concept and Architecture to Support Solid State Power Substations at the Consumer End”.
- M. Chinthavali, M. Starke and R. S. K. Moorthy, “Solid State Power Substation (SSPS) Distribution and Consumer End Grid Infrastructure”.

Publications:

- M. Chinthavali, R. S. K. Moorthy and A. Adib, “Standard Modular Architecture for Consumer End Plug and Play Interfaces”, in *Proc. 2021 IEEE Applied Power Electronics Conference and Exposition (APEC),* Jun. 2021, Phoenix, AZ, USA.

THANK YOU

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