DOE Office of Electricity TRAC

Peer Review

U.S. DEPARTMENT OF ENERGY | OFFICE OF ELECTRICITY

PROJECT SUMMARY

High Temperature Capacitor Development

This project focuses on the development of material and component-level knowledge of ceramic capacitors for DC-Link for high performance power electronics, including development of new high temperature and lifetime dielectrics and understanding device-level and DC-Link level characterization and modeling of Ceralink capacitors.

PRINCIPAL INVESTIGATORS

Dr. Jonathan Bock, Materials R&D

Dr. Sean Bishop, Materials R&D

Dr. Jacob Mueller, Power Electronics R&D

WEBSITE

www.Sandia.gov

Sandia National Laboratories

Exemptional Service in the National Interest

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The Numbers

DOE PROGRAM OFFICE:
OE – Transformer Resilience and Advanced Components (TRAC)

FUNDING OPPORTUNITY:

LOCATION:
Albuquerque, NM

PROJECT TERM:
10/01/2019 to 10/01/2022

PROJECT STATUS:
Incomplete

AWARD AMOUNT (DOE CONTRIBUTION):
$1,000,000

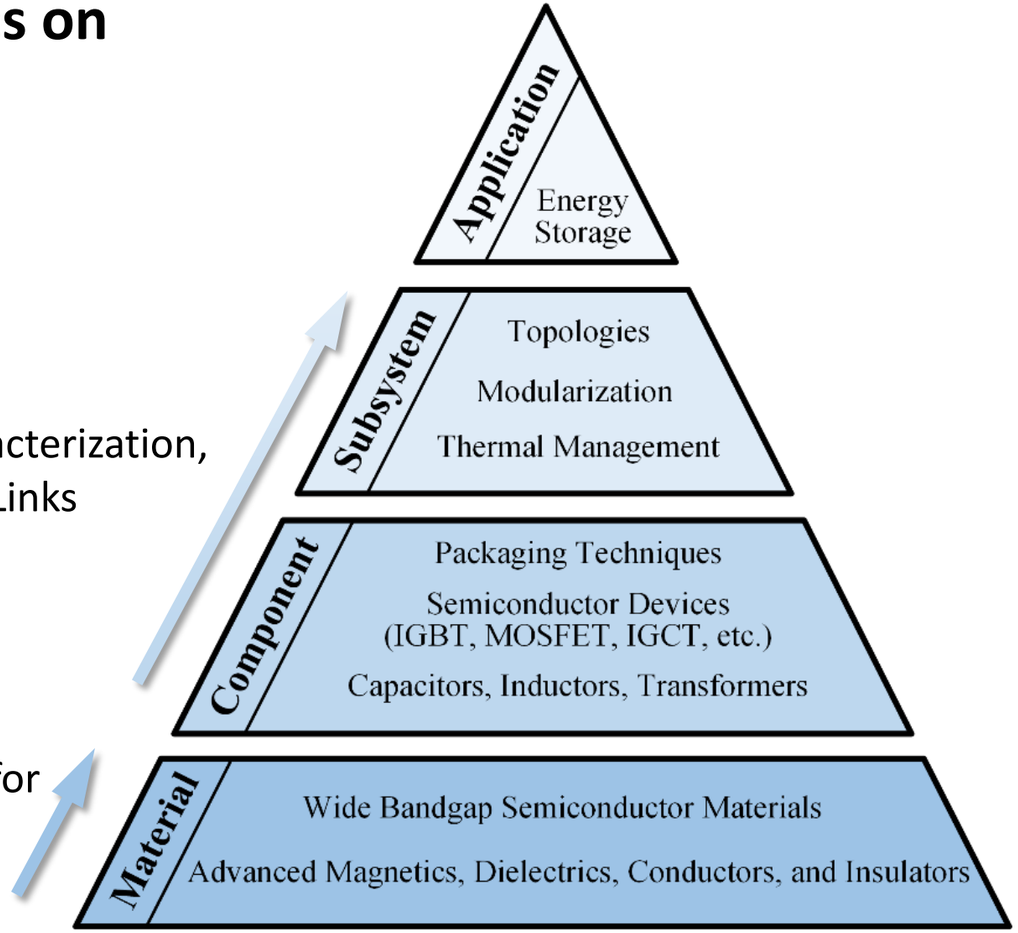
AWARDEE CONTRIBUTION (COST SHARE):
$0

Power Electronics At Sandia National Labs

Our DC-Link Capacitor Development Program focuses on moving from materials up to application.

TRAC Task 2– Ceralink Capacitor Characterization, from individual piece-parts to full DC-Links

TRAC Task 1 - Development of Candidate Dielectrics for Next-Gen MLCC's (BZT-BT: $Bi(Zn,Ti)O_3$-$BaTiO_3$)



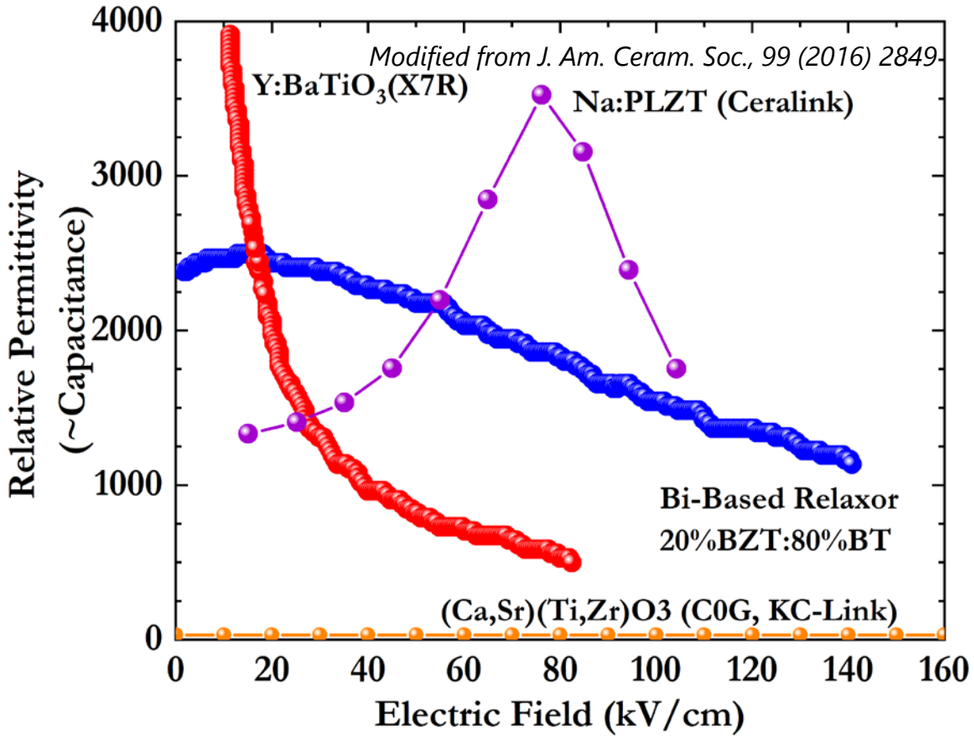
Primary Innovation – Task 1

- A candidate dielectric material for high volumetric efficiency DC-Link capacitor dielectrics, $Bi(Zn,Ti)O_3$-$BaTiO_3$, shows promising initial degradation mechanics. Our data suggest high-lifetime devices may be obtainable, but concern exists in reducing environments necessary for a low-cost product.

Innovation Update

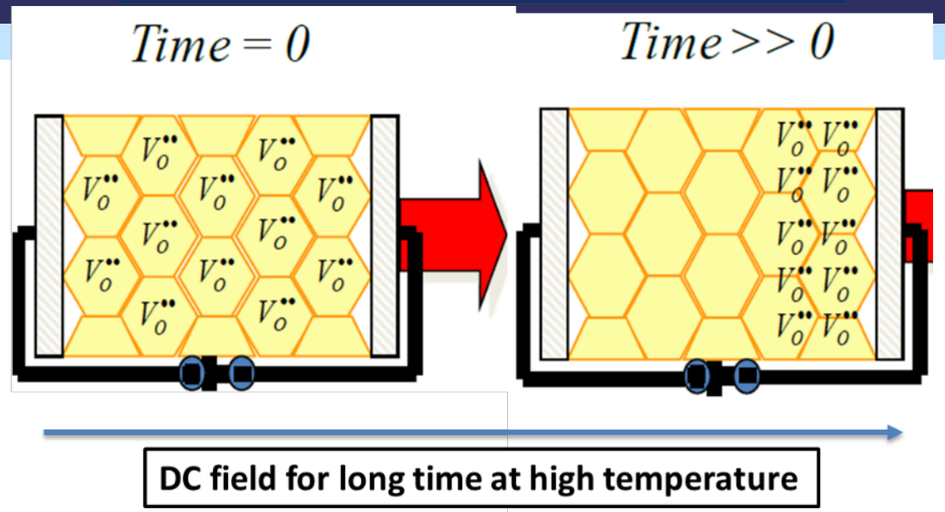
$Bi(Zn,Ti)O_3$-$BaTiO_3$ Dielectrics – "X7R" Modified for High Temperature and High Field Performance

High Capacitance Density at high DC Voltage

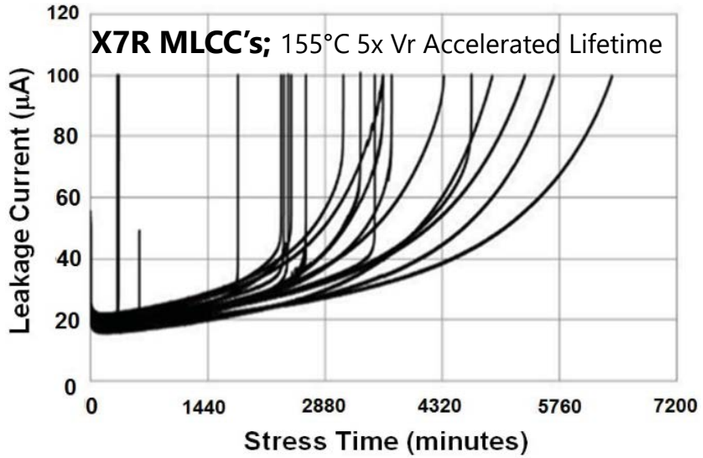


- Retains capacitance at high E-field/High applied voltages
- Can be designed w/ low loss at high temp (regulate Self-heating)
- All benefits of MLCC's: Low ESR/ESL, little/no practical dV/dT limit

Known Failure Mechanism Concerns



Modified from R. Maier, Penn. State PhD Thesis (2014)

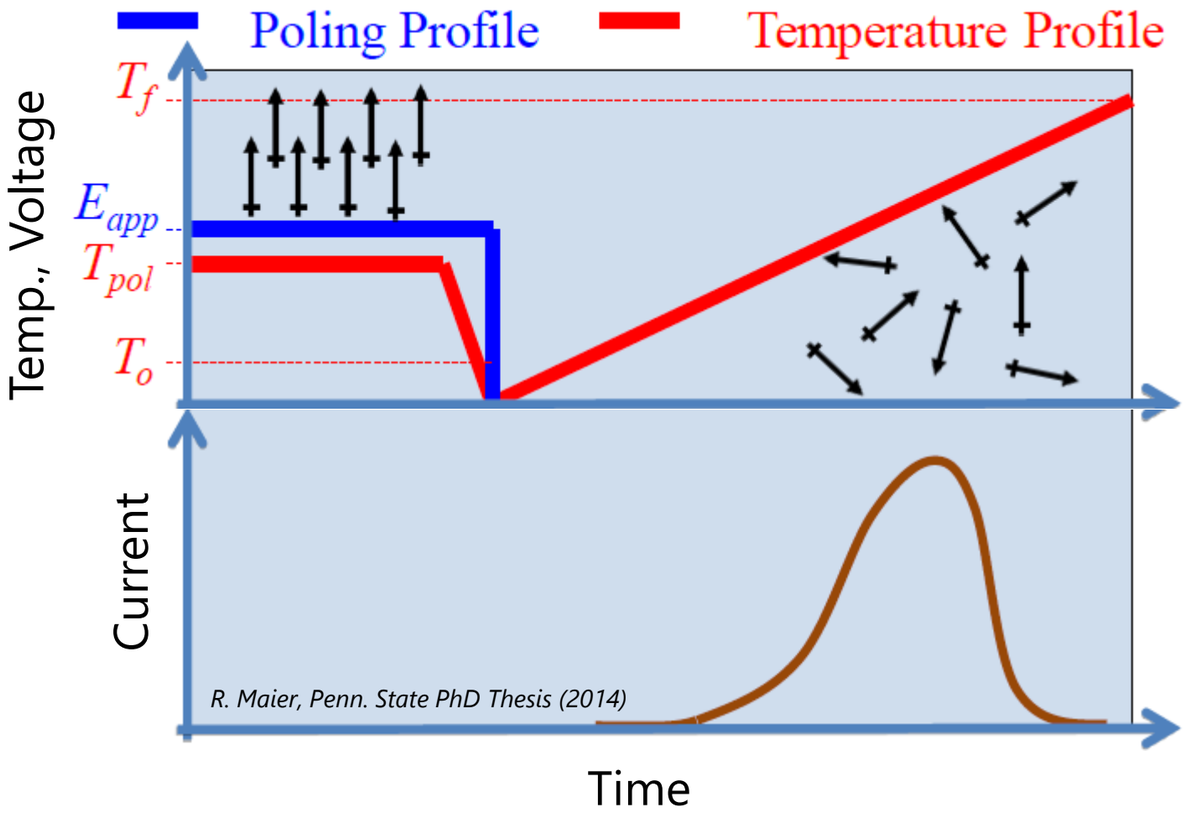


Modified from D. Liu. IEEE Trans. On Comp., Pack., and Manf., 5 (1), pg 40 (2015)

Despite Promising Properties, No Lifetime/Degradation Analysis Exists for BZT-BT Materials

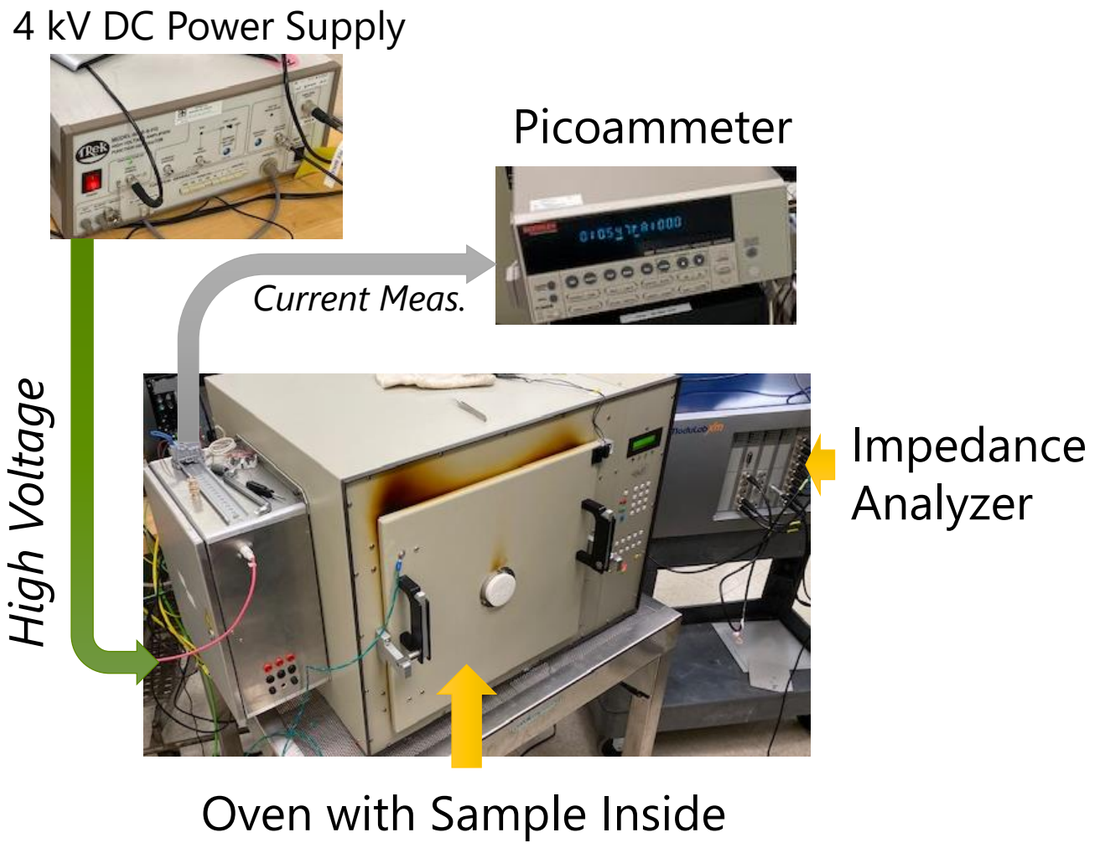
Measuring Electromigration

Thermally Stimulated Depolarization Currents



Measuring Degradation

Highly Accelerated Lifetime Tests

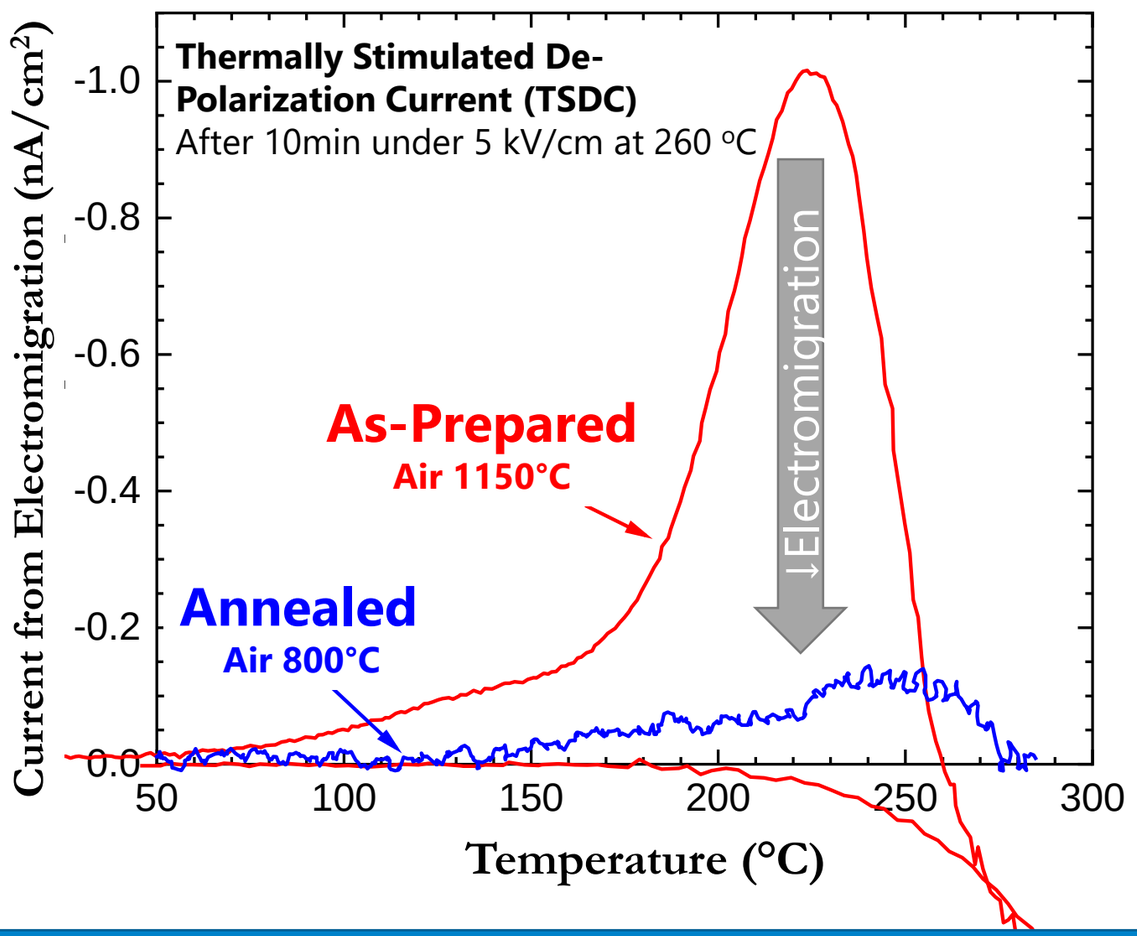


Tools were developed to allow direct comparison of Failure mechanism (Electromigration) to Failure mode (IR Degradation)

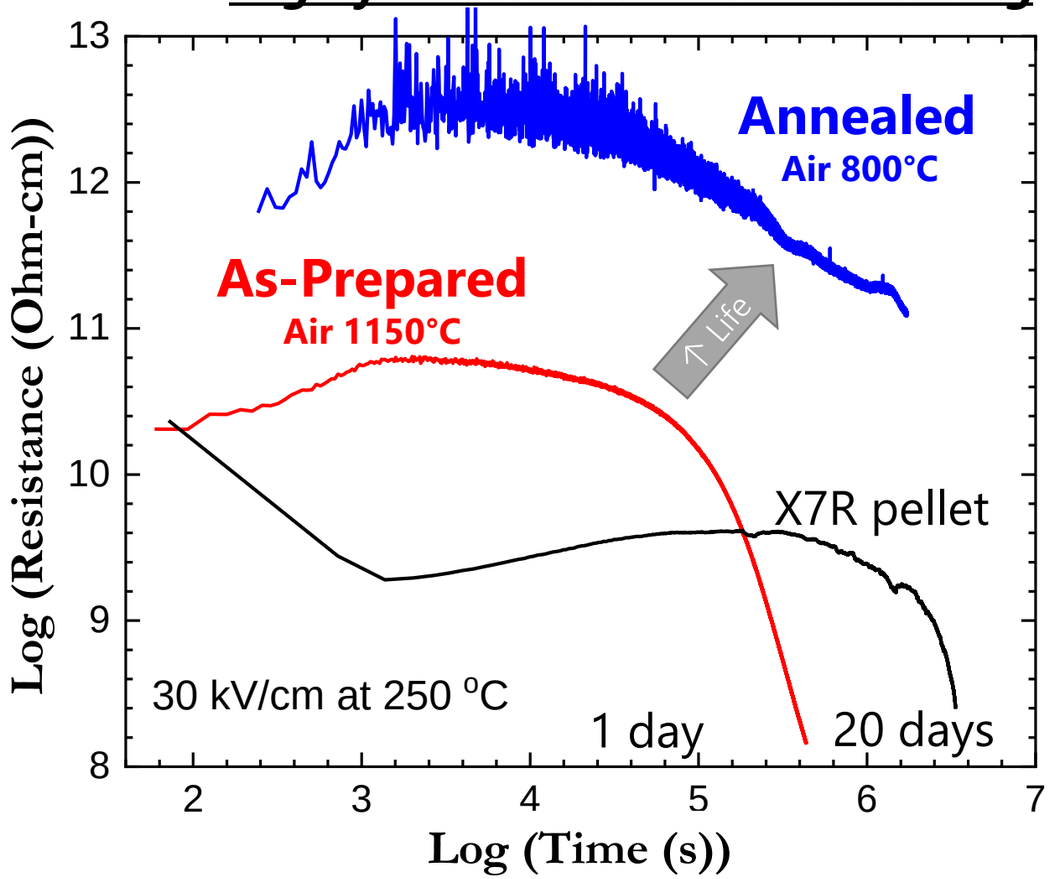
Innovation Update

Degradation Measurements
Samples: $(Bi_{0.22}Ba_{0.78})(Zn_{0.1}Ti_{0.9})O_3$

Electromigration (TSDC) Testing



Highly Accelerated Lifetime Testing



High resistances and low degradation are found, but only after air annealing.
The material may be significantly reduceable – a concern for low-cost production

Impact/Commercialization

- This work shows that BZT-BT can show promising high resistance and low degradation behavior needed for high temperature capacitors

- Observed ease of reduction for this material adds to the challenges of commercialization of low-cost product:
  - Reducing environments needed for processing MLCC's w/ Ni or Cu electrodes
  - BZT-BT shows potentially high reducibility and (from other work) low thermodynamic stability in these environments.

- As more evidence points toward increasing barriers for commercialization, the dielectrics community must reflect on the path forward…

IP STATUS

No IP is expected from this work.

Materials Path Forward For FY22

Finish Electromigration and Degradation Experiments for 2 Journal Publications

- Impact of thermal annealing
  - Focuses on Bi-Rich samples (Donor doped)
  - Finalize TSDC work, activation energy of electromigration, degradation statistics.
- Impact of chemistry (Acceptor/Donor Doping)
  - Comparison to Ba-Def (Acceptor doped) samples

Stretch: Utilize Tools for component-level work

- TSDC and In-situ Impedance-Spec techniques, developed for this work, will be fantastic tools for understanding physics of failure and lifetime predictions in commercial $CaZrO_3$ (KC-Link) and Na:PLZT (Ceralink) capacitors.

Power Electronics At Sandia National Labs

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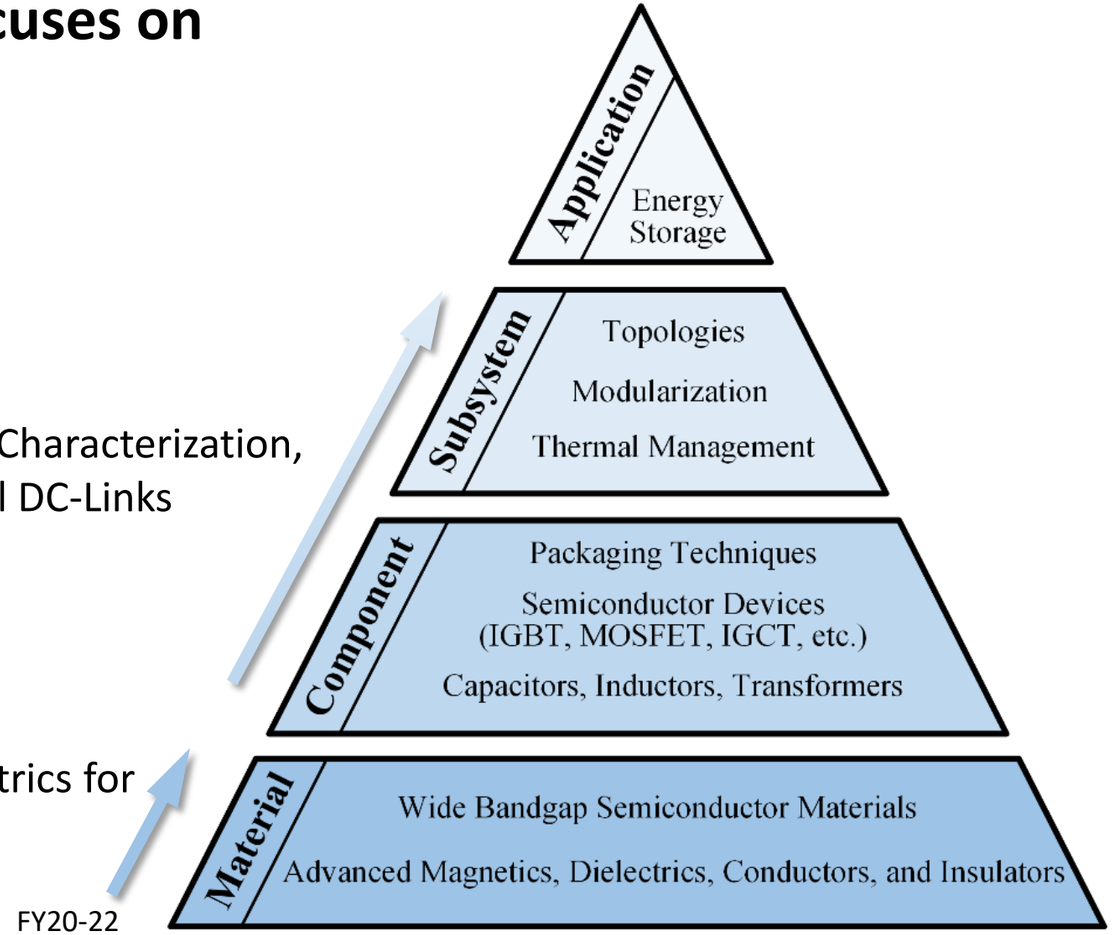
TRAC Task 1 - Development of Candidate Dielectrics for Next-Gen MLCC's (BZT-BT: $Bi(Zn,Ti)O_3$-$BaTiO_3$)

FY20-22



Primary Innovation – Task 2

- Device-level characterization of Ceralink capacitors, measured in this program, suggest favorable performance for DC-Link applications; however, their complex behavior may create difficulties in modeling DC-Link behavior. Accurate and accessible design tools are needed maximize the impact of these converters in practical power conversion applications.

Innovation Update

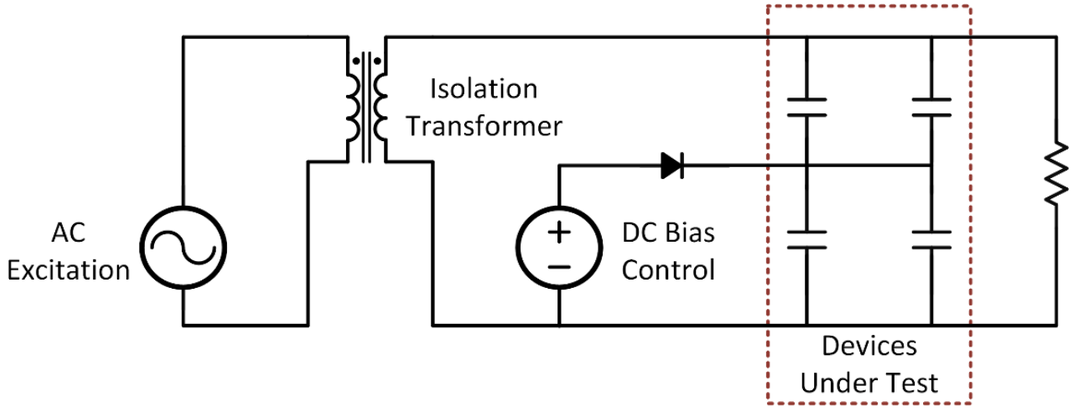
Piece-part Characterization of Ceralink Capacitors (TDK B58031I5105M062, 1uF/500V)

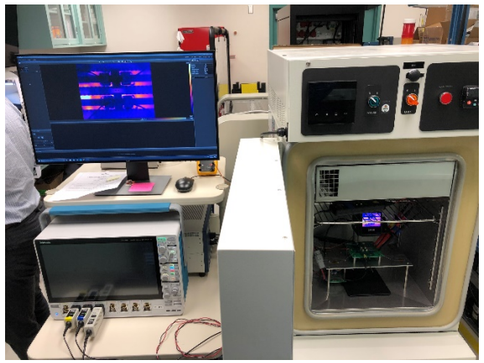
Characterization Experiments

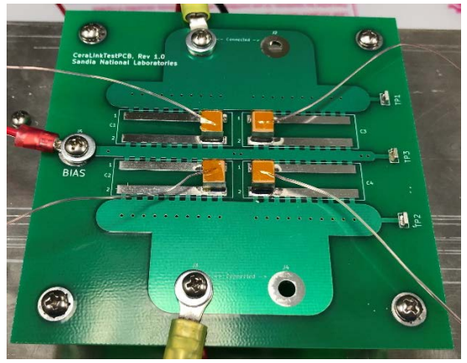
- Apply AC current excitation for 30 minutes with controlled DC bias and ambient temperature
- Measure device temperatures, voltages, currents
- Calculate effective capacitance, ESR, dissipation factor, loss

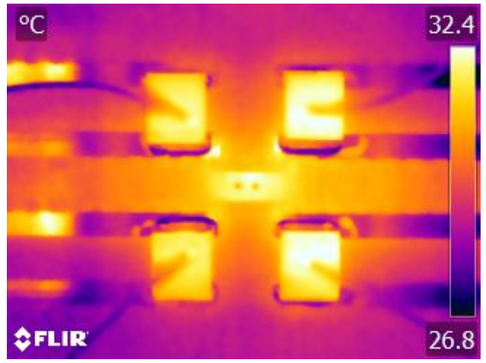
Range of Operating Conditions

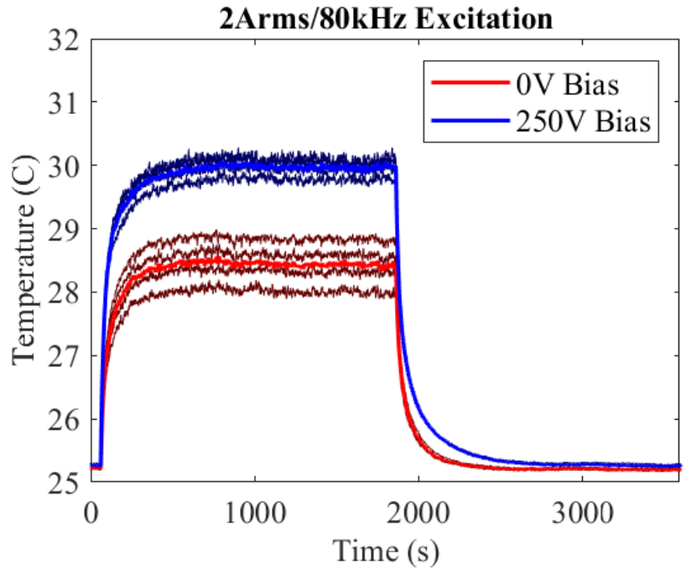
- Sinusoidal current excitation at $3A_{RMS}$/cap
- AC excitation frequency – 80kHz, 120kHz, 160kHz, 200kHz
- DC voltage bias – 0V, 300V, 400V, 500V
- Ambient temperature – 25C, 55C, 85C







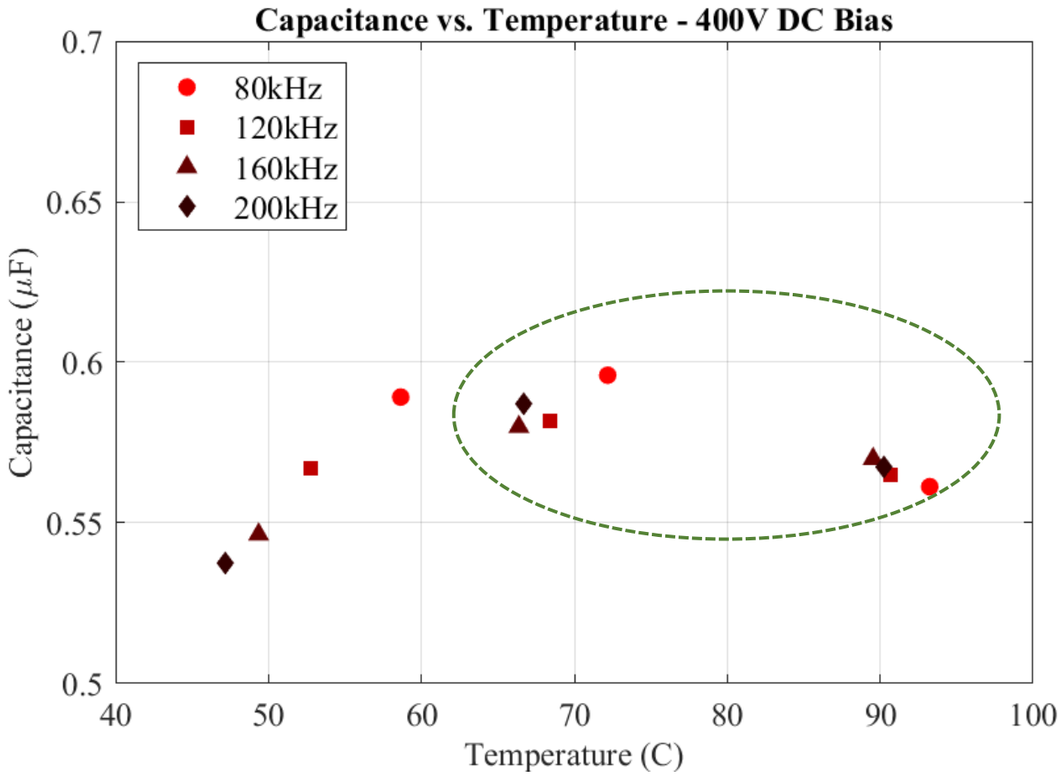




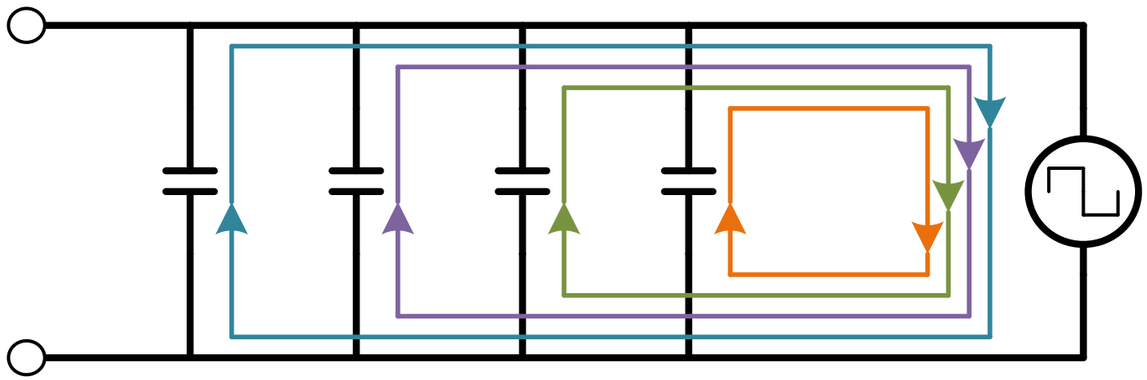
Individual device characterization looks favorable for DC Link applications:
High ripple current capability, Stable capacitance w/ DC Bias, Low loss at high temperature.

Innovation Update

Complex Behavior Of Ceralink Capacitors: Important for Subsystem Design and Modeling



In capacitors, $|Z| = 1/(2\pi fC)$, so operating regions in which *capacitance decreases with temperature are advantageous* for performance and reliability.



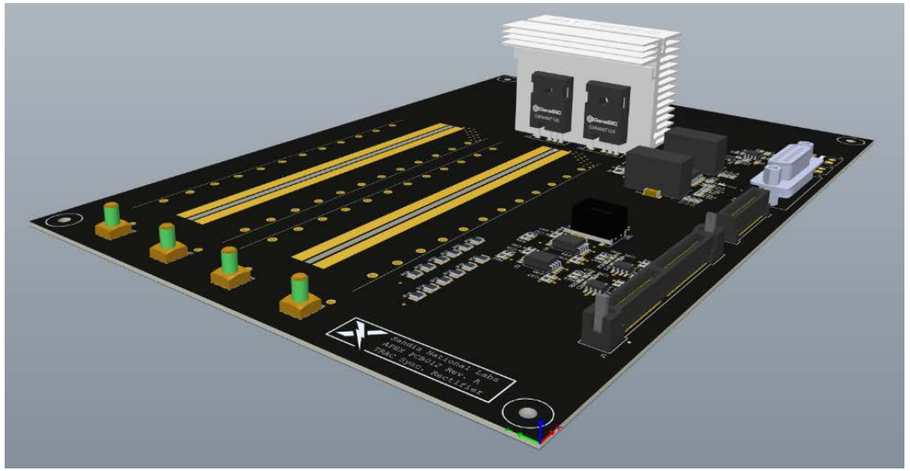
- C vs T relationship is critical for DC link applications
- Balanced distribution of current stress between parallel capacitor elements in the DC-Link is important to prevent thermal runaway.
- If impedance increases with temperature, the hottest element receives the least current, creating a negative feedback loop that should work against thermal runaway.

Complex but potentially advantageous device-level behavior exists.
Assuring advantageous behaviors carry to the subsystem level is non-trivial

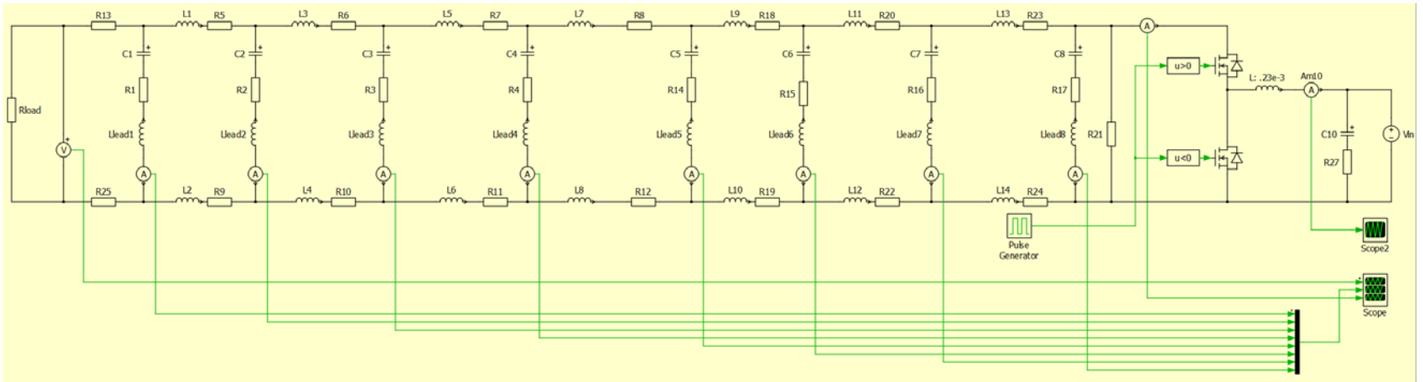
Ceralink Path Forward FY22

- **Goal**: Understand device and subsystem performance in a practical power conversion application, including parasitic impedances and temperature-dependent behaviors.
- Characterization data are gathered in a hardware platform designed to match target applications for Ceralink caps, i.e. wide bandgap-enabled power converters
- Custom converter platform provides high flexibility in DC link circuit composition, ability to control parasitic impedances between parallel cap branches
- Data gathered from converter platform will be used to develop models that accurately describe device operation within the DC-link system
- Intent is to generate accessible models and design tools power electronics engineers

Stress Ceralinks in Actual Converters



Model Ceralink DC-Links:
Device Model Validation and Parasitic Adjustments



Impact/Commercialization

- Characterization of capacitor behavior within a DC link as a function of system structure and operating conditions helps build an understanding of devices' potential for performance improvement and suitability for key power conversion applications

- Accessible models and design methodologies accelerate the adoption of advanced capacitor technologies by reducing engineering effort and risk involved in new power conversion system designs

IP STATUS

No IP is expected from this work.

Summary

- A candidate dielectric material for high volumetric efficiency DC-Link capacitor dielectrics, $Bi(Zn,Ti)O_3$-$BaTiO_3$, shows promising initial degradation mechanics. Our data suggest high-lifetime devices may be obtainable, but concern exists in reducing environments necessary for a low-cost product.
- Device-level characterization of Ceralink capacitors, measured in this program, suggest favorable performance for DC-Link applications; however, their complex behavior may create difficulties in modeling DC-Link behavior.
- Future work will focus on publishing annealing and chemistry impacts in BZT-BT work while simultaneously pivoting to Ceralink-focused work utilizing power electronics staff and degradation investigation tools for BZT-BT.

THANK YOU

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