DOE Office of Electricity TRAC

Peer Review

U.S. DEPARTMENT OF ENERGY | OFFICE OF ELECTRICITY

IPS Hardware Prototype Development

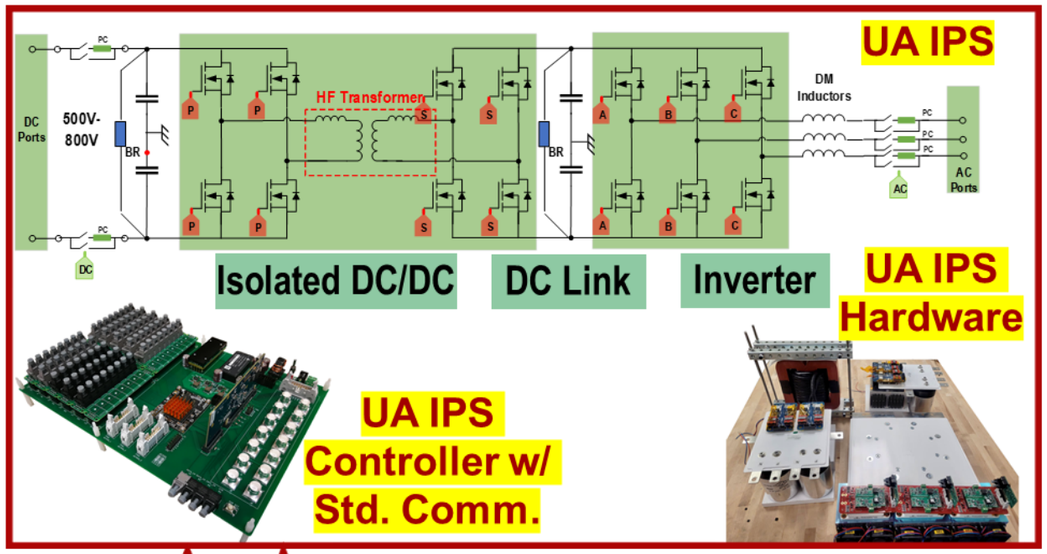
PRINCIPAL INVESTIGATORS
Dr. Yue Zhao, Associate Professor
Dr. Juan Carlos Balda, University Professor
University of Arkansas

UNIVERSITY OF ARKANSAS | College of Engineering
Electrical Engineering

PROJECT SUMMARY

The Objective of this project is to develop and demonstrate the intelligent power stage (IPS), i.e., an interoperable plug-and-play power stage with embedded intelligence and online health monitoring capability. Through the standardized communication interface, IPS can provide sufficient component level status information to interact with the Smart Universal Power Electronics Regulator (SUPER). The IPS developed in this project consists of an isolated DC/DC converter stage, a three-phase inverter stage, self-maintained auxiliary power supplies, sensors and a powerful control platform with communication channels.

Innovations – Overview



AC voltage references (m_a, m_b, m_c)

SUPER (w/ LCL filter)

IPS status/health, & commands, contactor status, measurements

- IPS: Intelligent Power Stages
- SUPER: Smart Universal Power Electronic Regulators

External Parameter Identifications ✓

Interoperability, Situation Awareness

- External LCL parameter estimation.

Onboard Health Monitoring and Prognosis ✓

Reliability, Resiliency (Internal)

- Junction temperature estimation for the SiC power modules used in IPS;
- DC link capacitance identification.
- Capacitor end-of-life (EOL) indication using estimated DC link capacitance.

Advanced Gate Driving (AGD) ✓

Reliability, Efficiency, Performance

- AGD with optimized multi-stage turn-off;
- Capability to manipulate voltage overshoot, switching loss and dv/dt.

IPS Controller Platform ✓

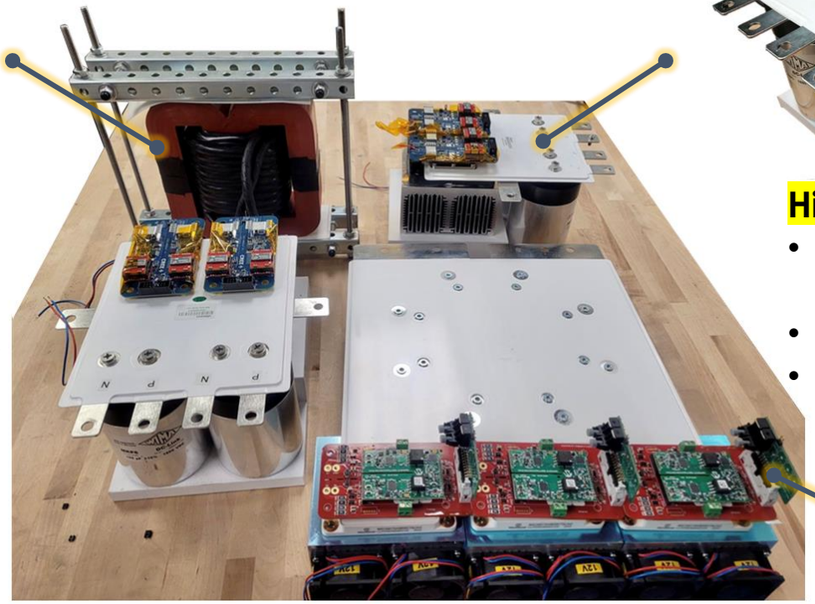
Interoperability, Performance

- Standardized communication interface;
- Optimized layout w. enhanced noise immunity.

Innovations – Overview

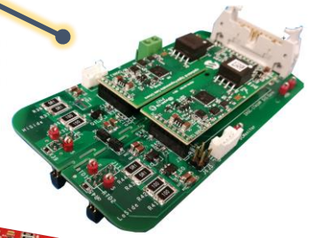
- In addition to the **validation & demonstration** of the advanced features …

High-Efficiency Transformer
- Custom nanocrystalline core;
- Optimized litz wire arrangement;
- Designed peak efficiency 99.6%.



High-Efficiency All SiC Power Stage
- Standardized topology (H-bridge converter & 3-Phase 2-L inverter)
- Ultra-low inductance bussing;
- Embedded current/voltage sensing.

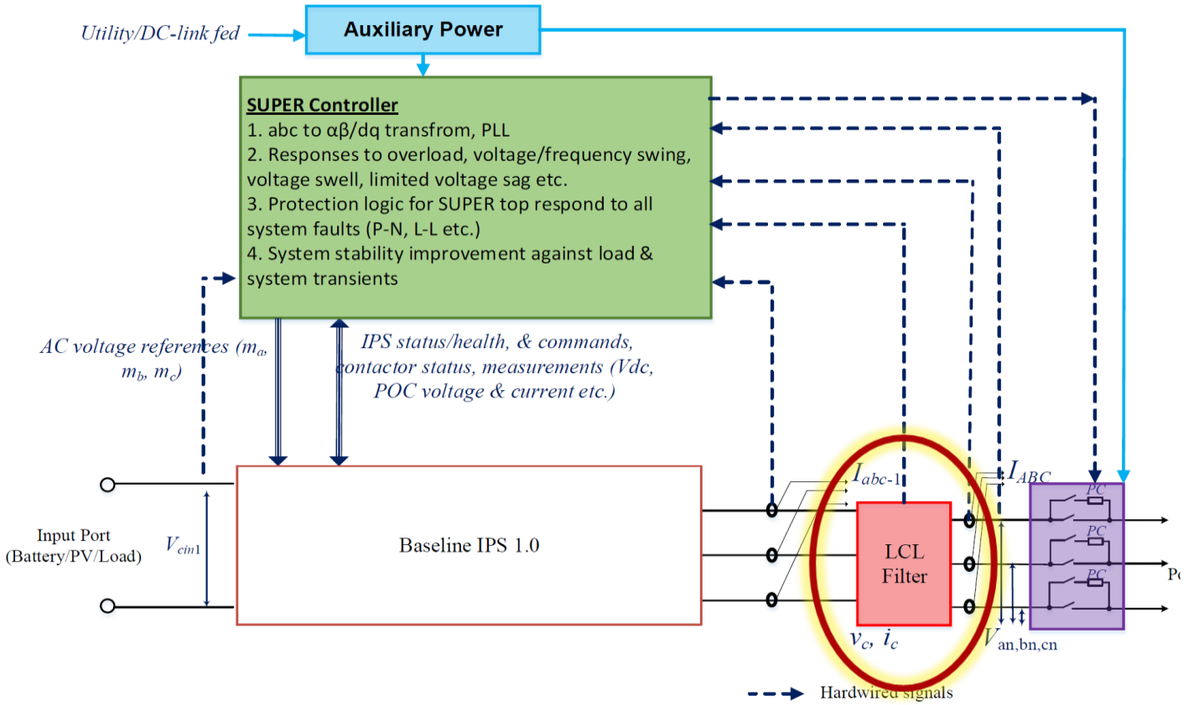
UA IPS Controller Platform
- DSP + FPGA architecture;
- Standardized comm. interface;
- Scalable/expandable I/O array.

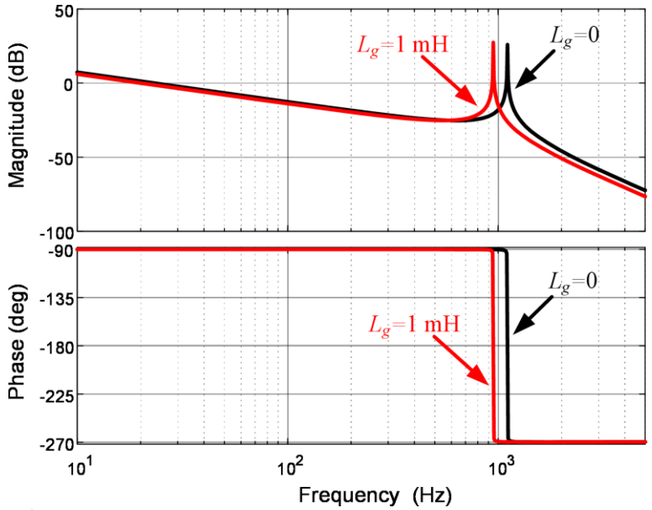


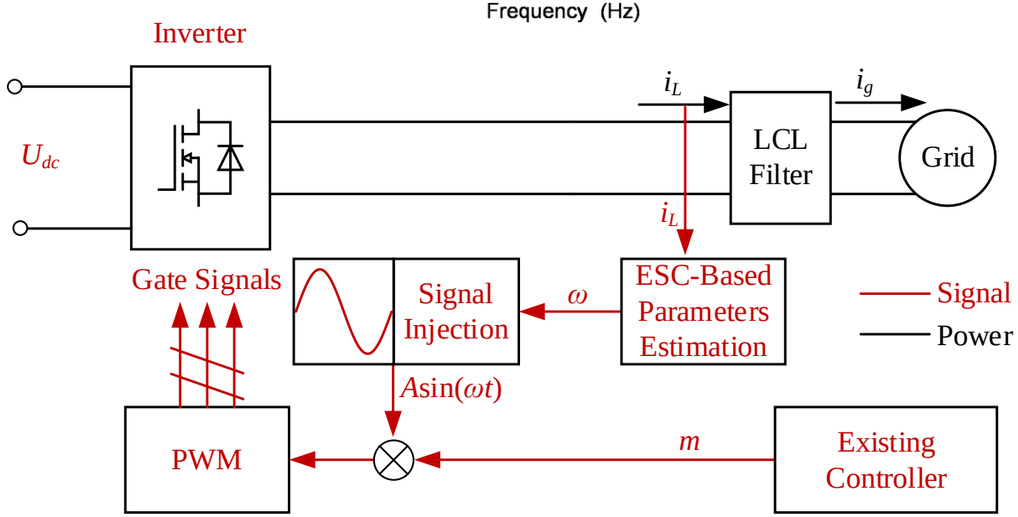
Intelligent Gate Driver
- Augmented 2-stage turn-off;
- Standardized fiber Rx/Tx;

Innovation Update

- LCL Parameter Identification





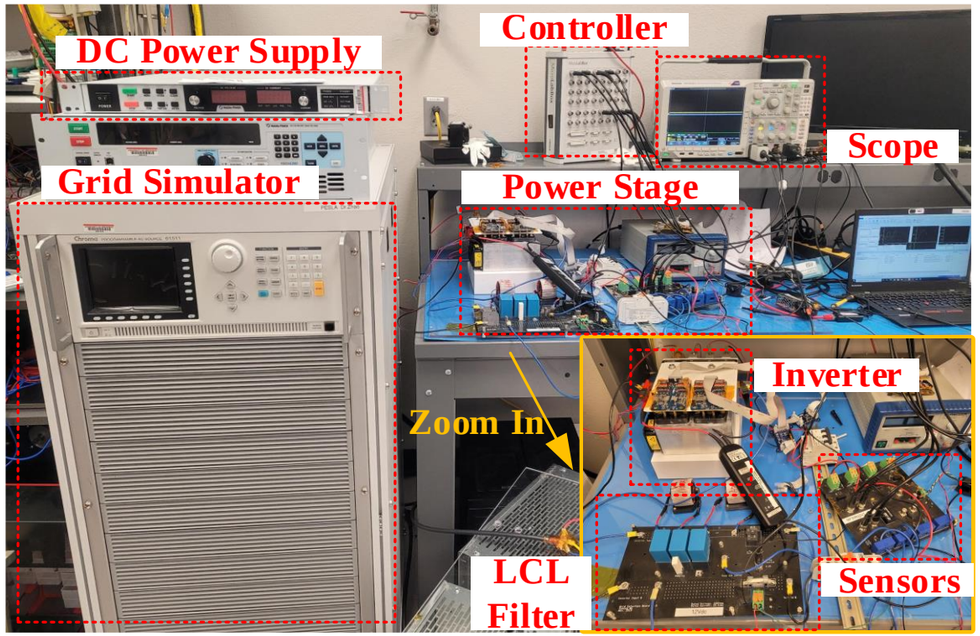


Block Diagram of Proposed ESC Based LCL Parameter Identification Scheme

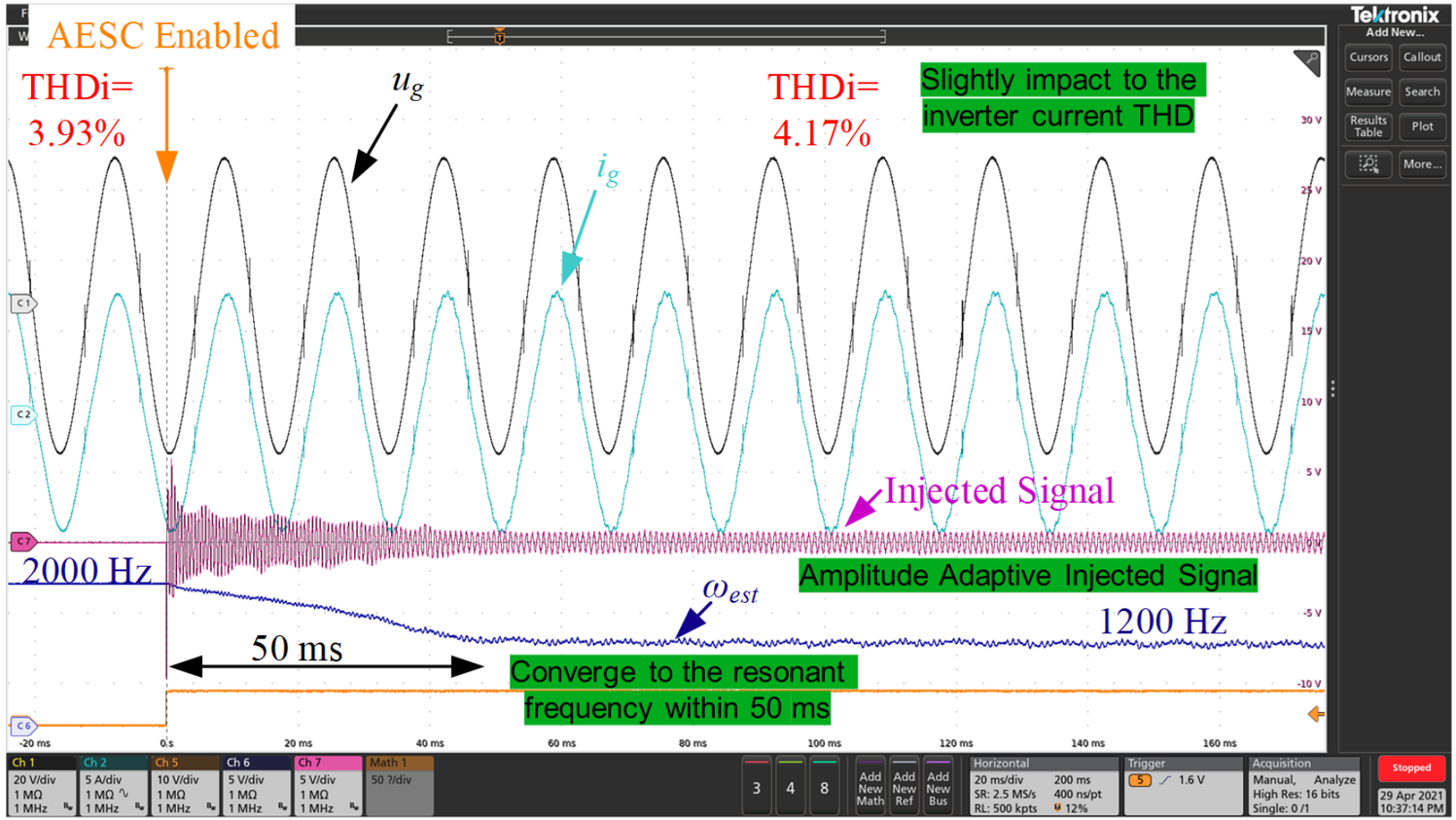
- LCL filter is critical to the performance of the IPS;
- LCL filter, which is part of SUPER, is external to the IPS;
- The knowledge of LCL parameters can be used to enhance the control performance and for the purpose of state estimation

Innovation Update

- LCL Parameter Identification – Experimental Studies



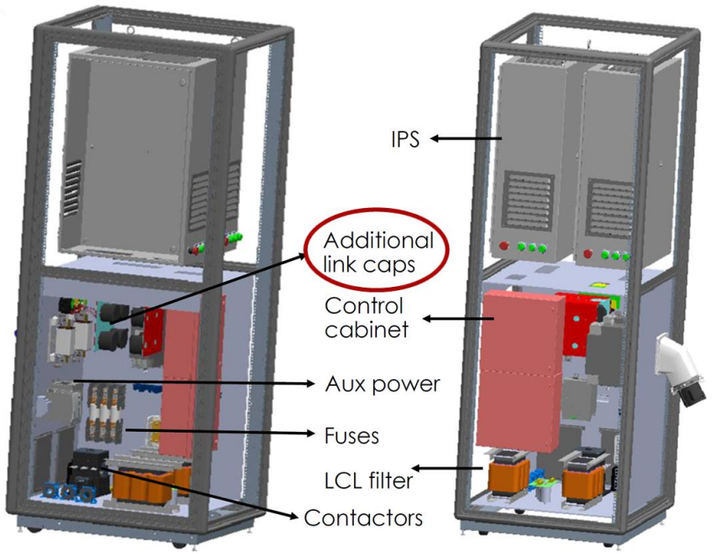
Grid-Tied Inverter Testing Setup

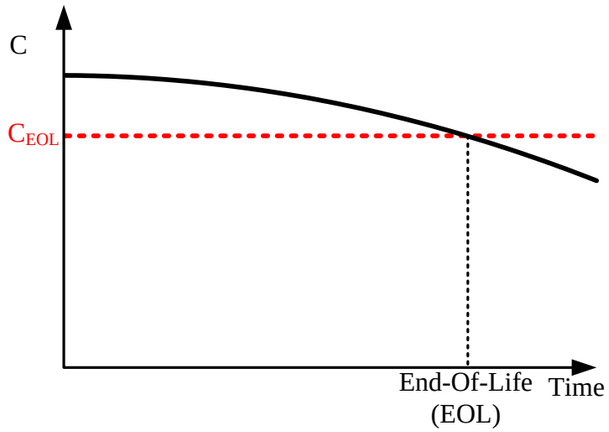


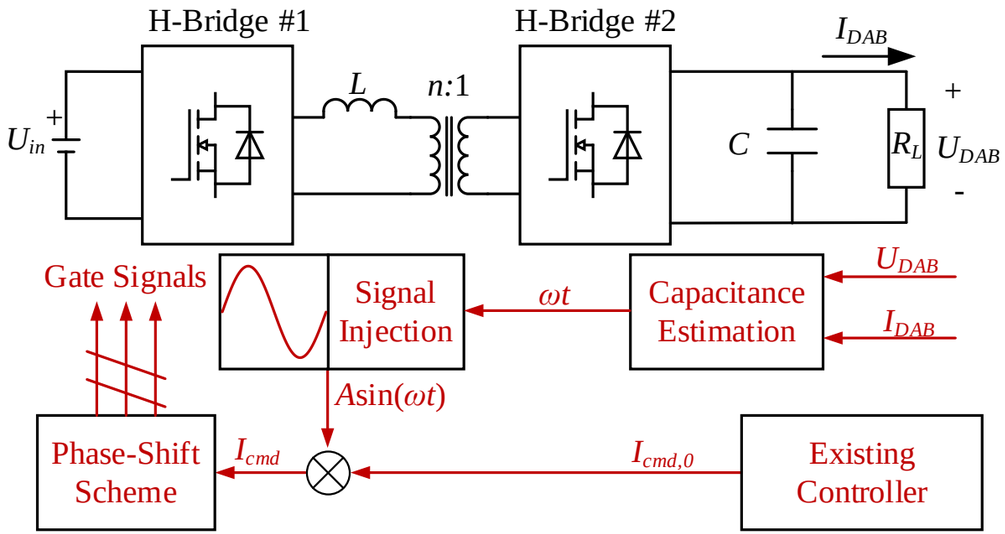
- Y. Wu, M. Mahmud, F. Diao, Y. Zhao, R. K. Moorthy and M. S. Chinthavali, "Extremum Seeking Control based Resonant Frequency Estimation for a Grid-Tied Inverter with LCL Filter," 2021 IEEE Energy Conversion Congress and Exposition (ECCE), 2021, pp. 882-886.
- Y. Wu, M. H. Mahmud, R. S. Krishna Moorthy, M. Chinthavali and Y. Zhao, "Adaptive Extremum Seeking Control Based LCL Filter Resonant Frequency Online Estimation," in IEEE Transactions on Power Electronics, vol. 37, no. 1, pp. 59-64, Jan. 2022, doi: 10.1109/TPEL.2021.3102063.

Innovation Update

- DC Link Capacitance Estimation



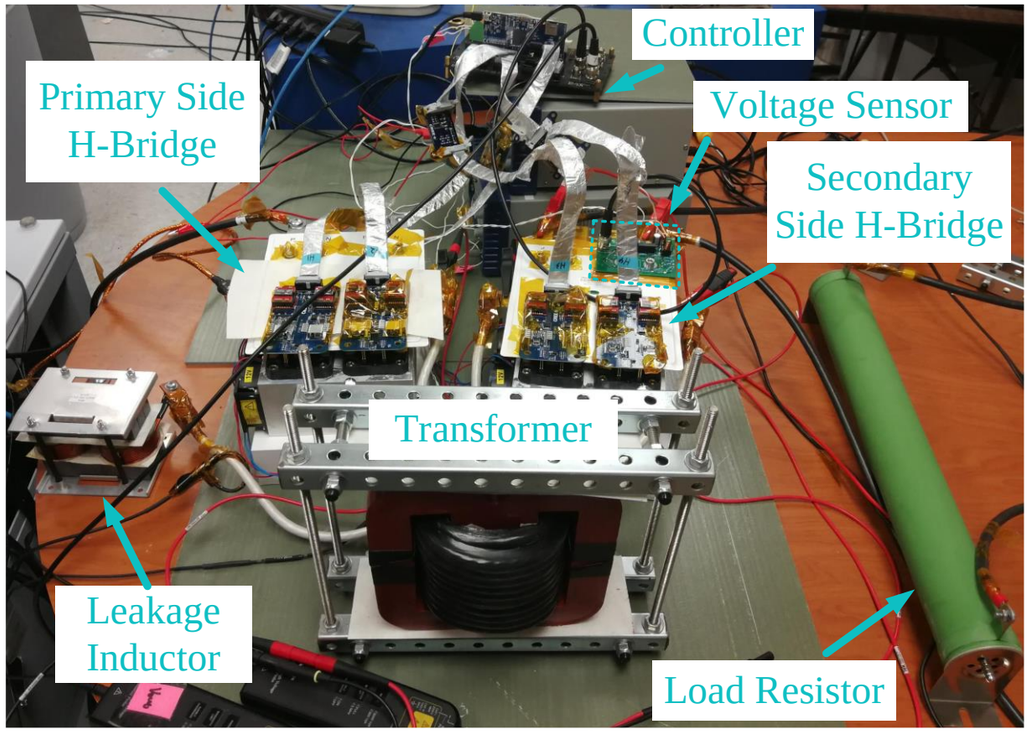




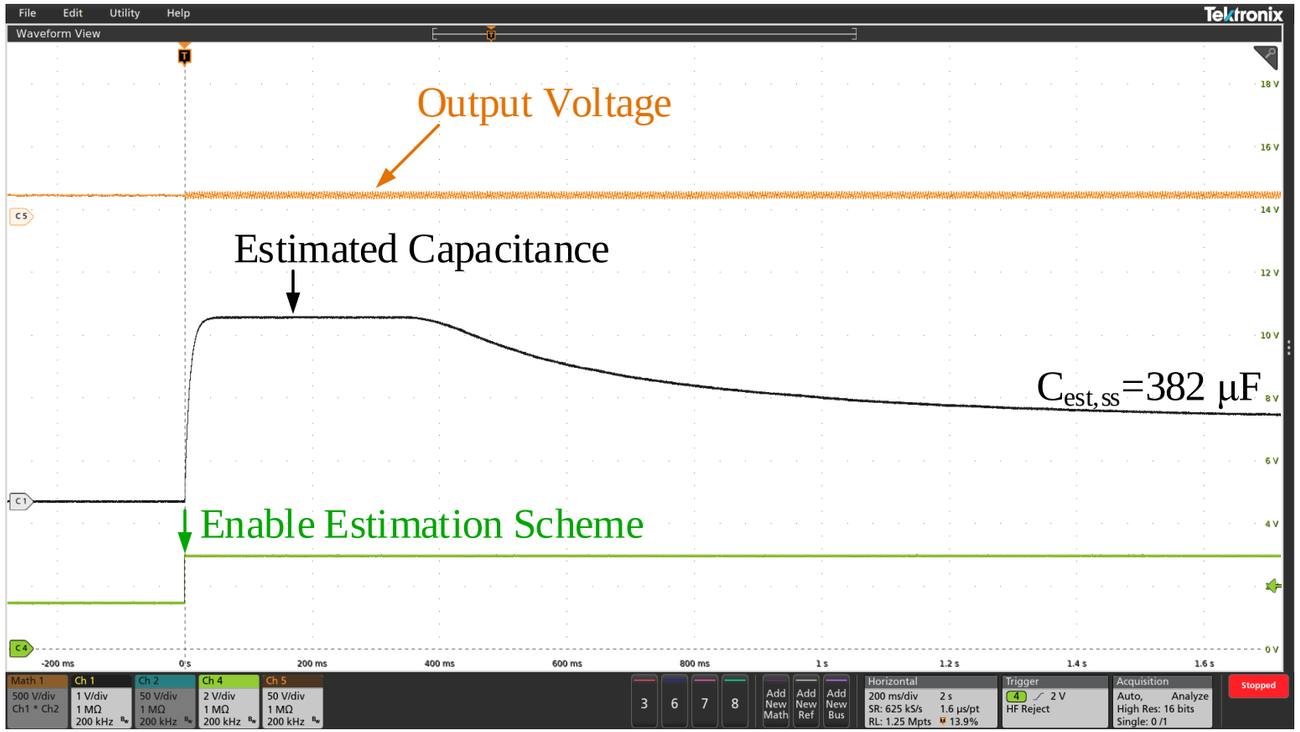
- ❖ The control gains of the DC/DC stage are designed based on the capacitance in the HV DC link;
- ❖ SUPER may add additional capacitance to the HV DC link to enhance the system stability;
- ❖ If DC link capacitance (IPS internal + SUPER external) can be estimated, the control gains can be updated online to improve the DC bus voltage regulation;
- ❖ The estimated capacitance can be used as an indicator for the end-of-life (EOL) of the capacitors.

Innovation Update

- DC Link Capacitance Estimation – Experimental Studies



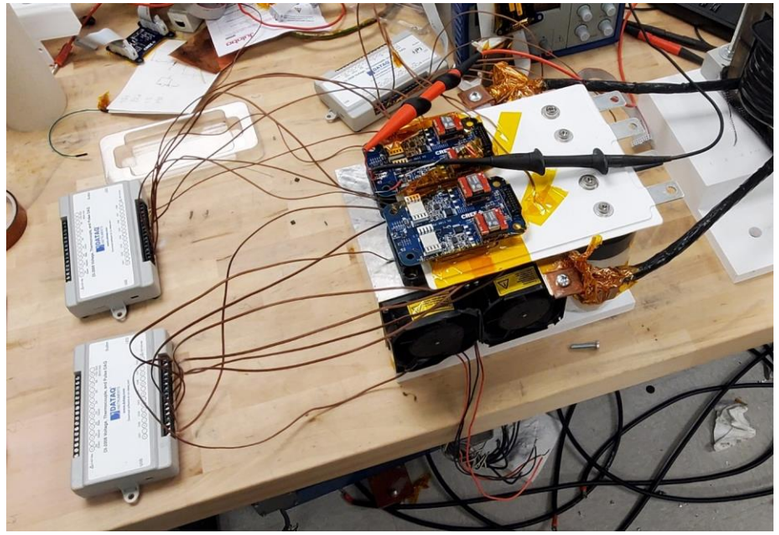
DC/DC Converter Testing Setup



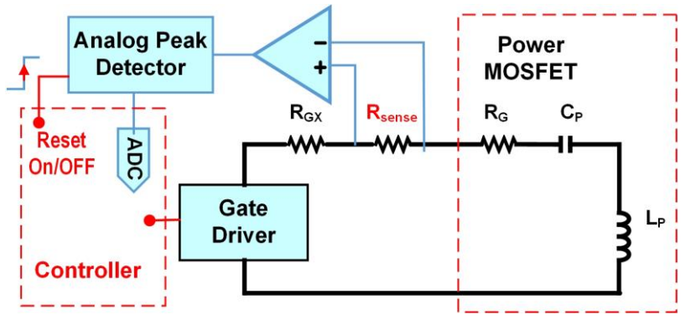
Typical Results for Capacitance Estimation

Innovation Update

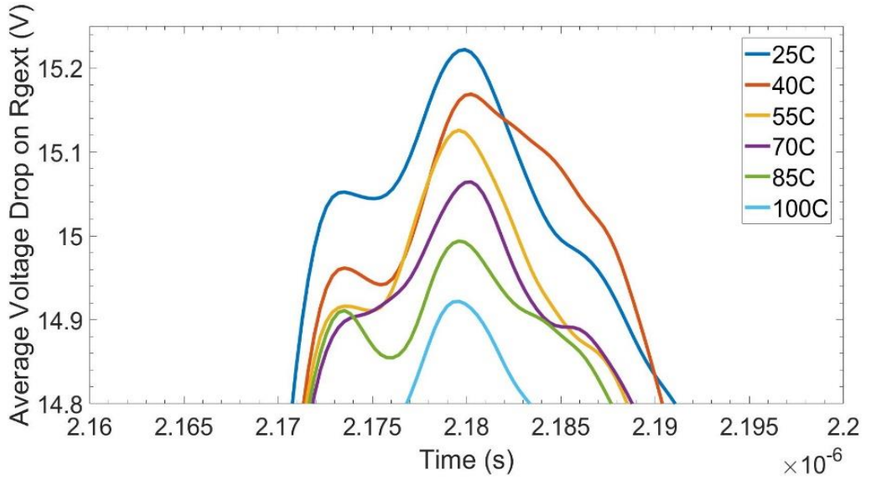
- Module Junction Temperature Estimation



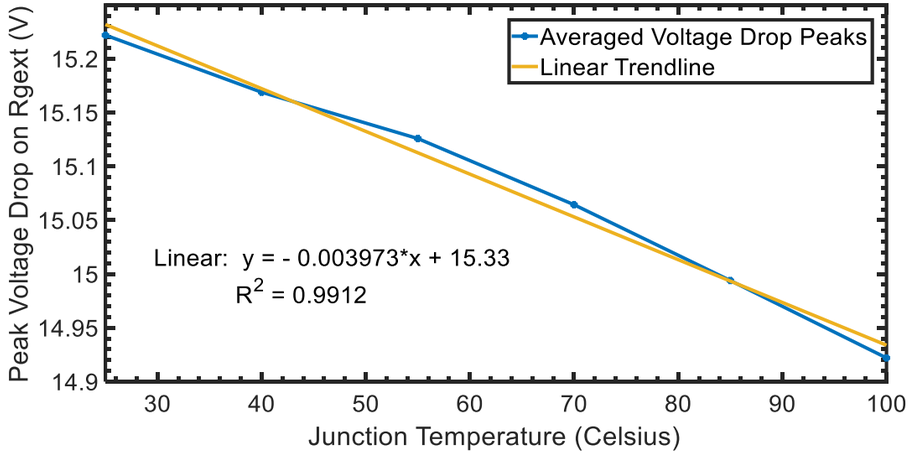
Power Stage Thermal Characterization Setup



Block diagram for Tj estimation



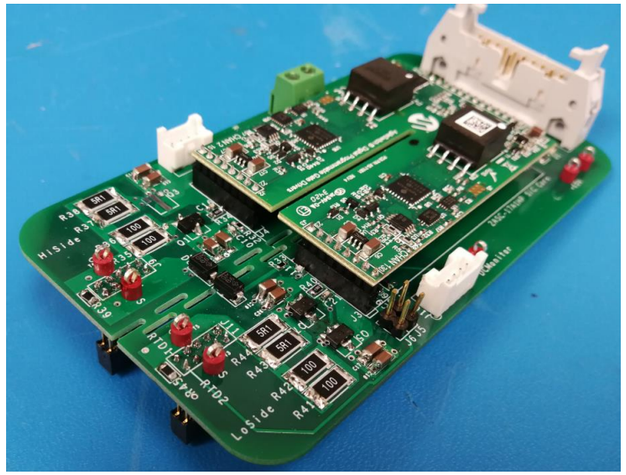
Voltage drop across external gate resistance



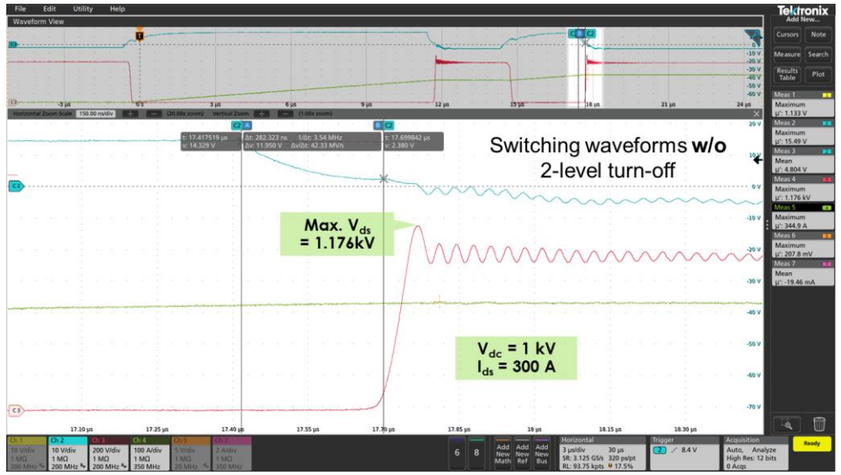
Volt./Temp. (°C) sensitivity analysis

Innovation Update

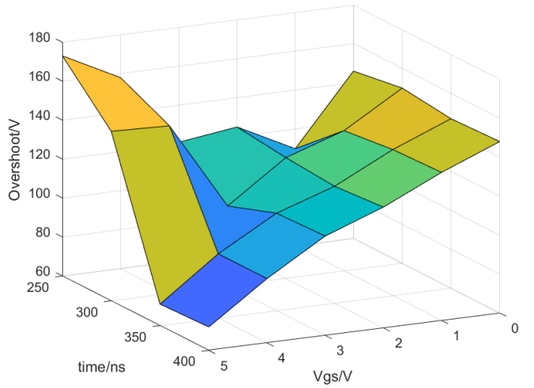
- Digital Gate Driver Demonstration for 1.7kV SiC Modules



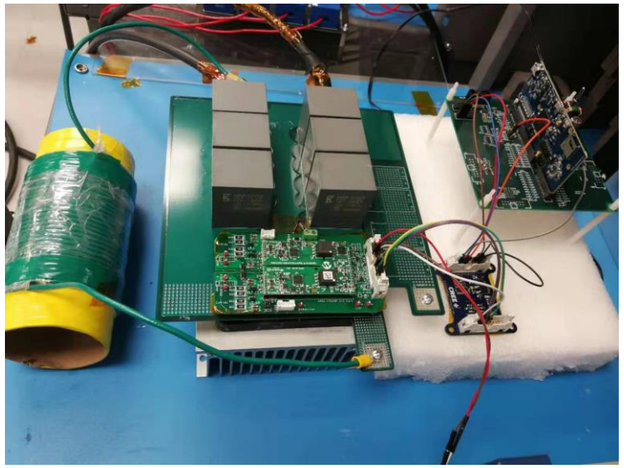
DGD Core with Custom Adaptor Board



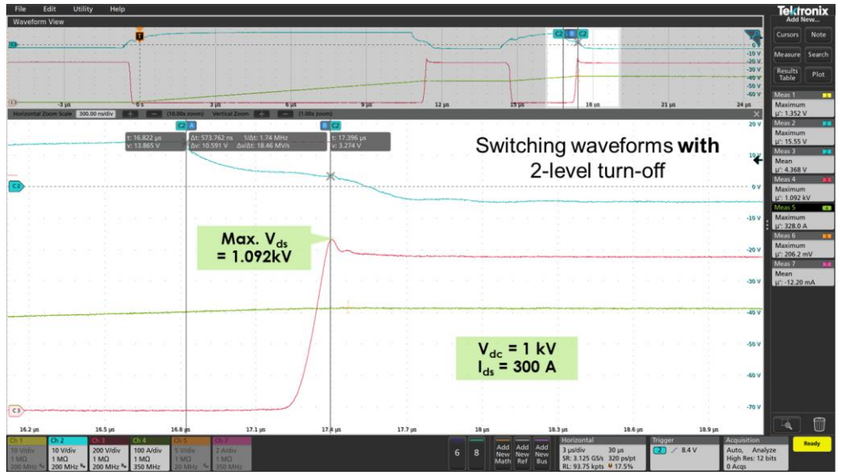
Typical Results without 2-level turn-off



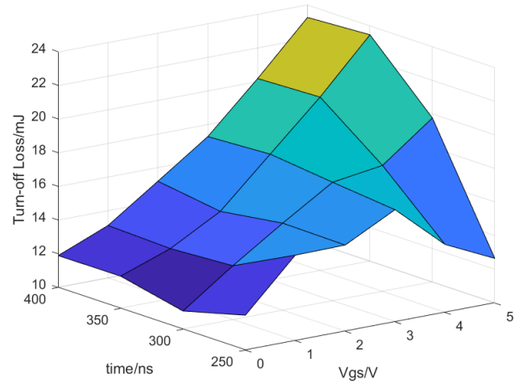
Impact to Voltage Overshoot



CIL Setup for 1.7kV CREE Module



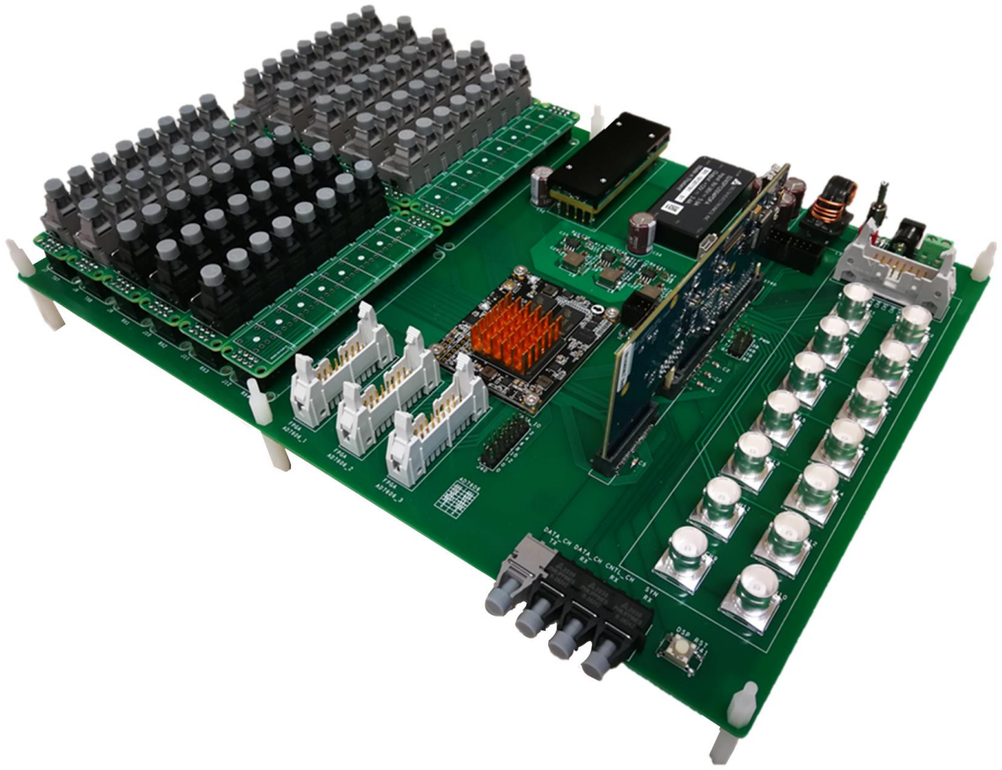
Typical Results with 2-level turn-off

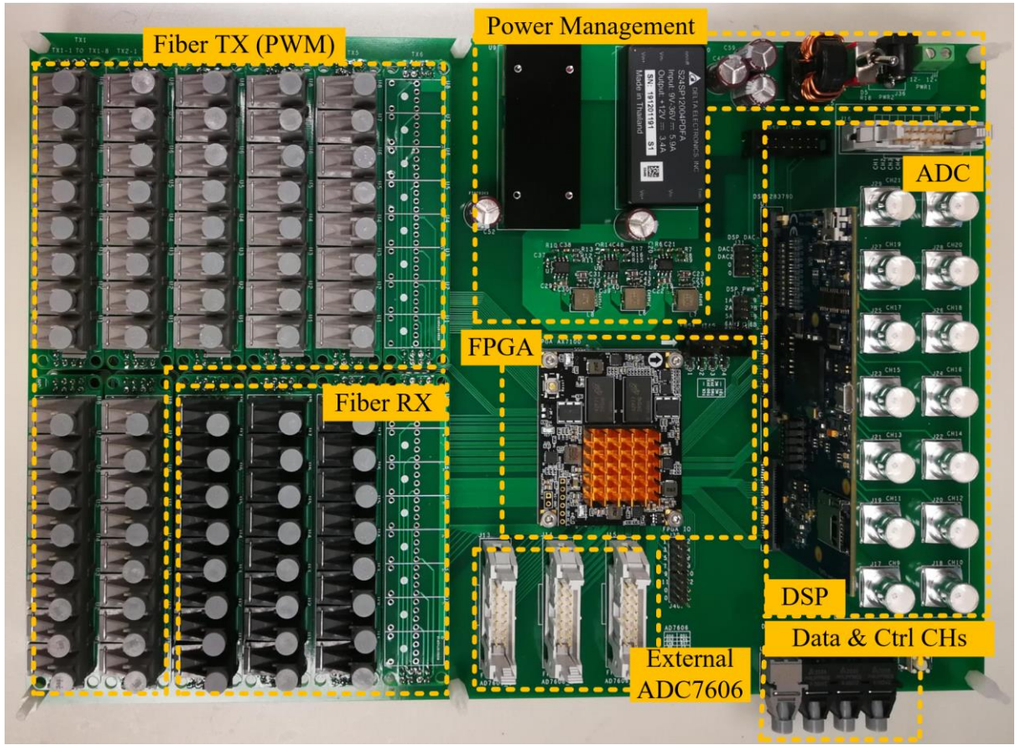


Impact to Turn-off loss

Innovation Update

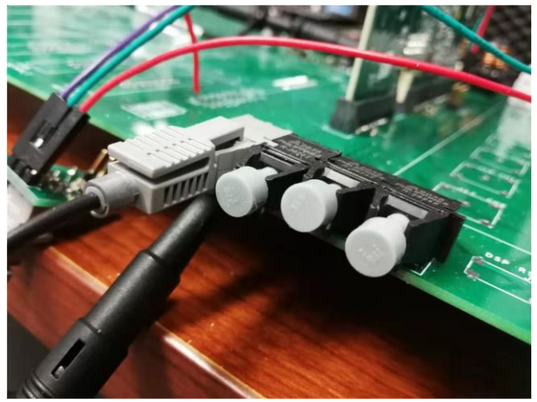
- IPS Controller Platform



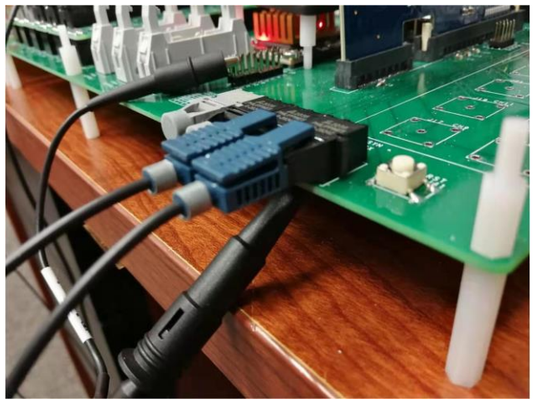


Innovation Update

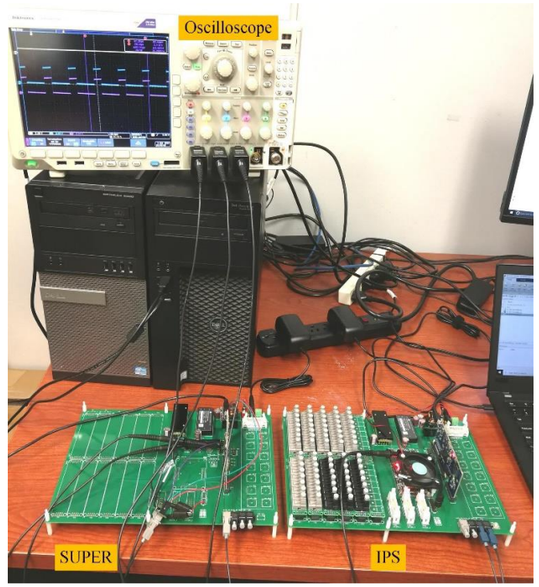
- IPS Control and Data Architecture Validation with Emulated SUPER controller



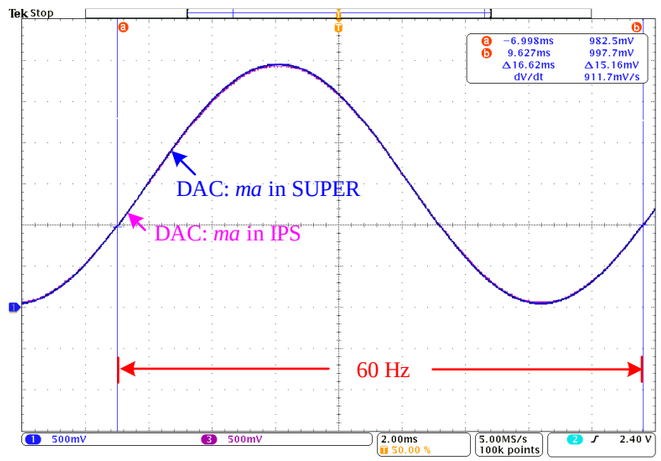
SUPER TX



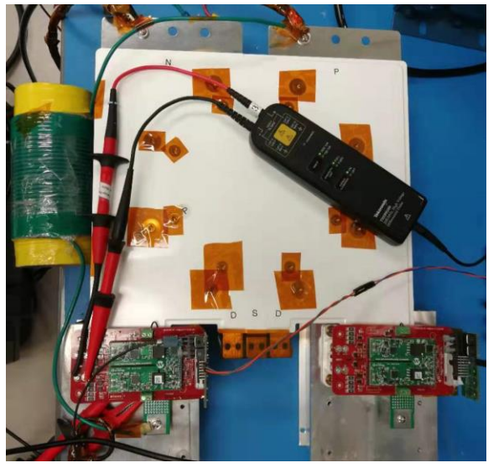
IPS RX



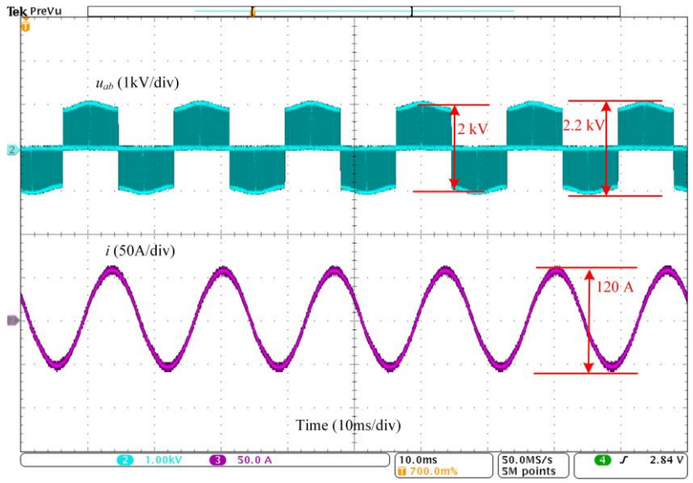
Controller Test Setup



Tx/Rx Modulation Index Profile



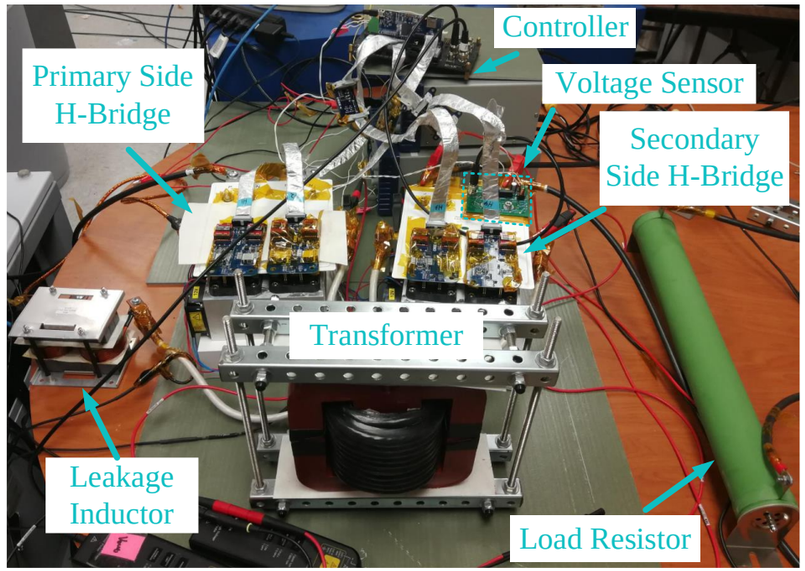
Inductive Load Test Setup for UA IPS



60 Hz line voltage under 1 kV DC bus

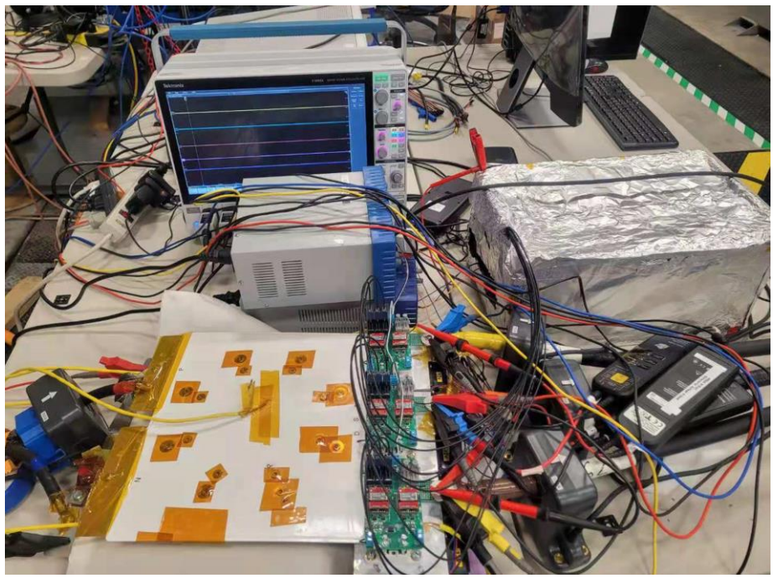
Innovation Update

- Status of the IPS Hardware Development & Testing



Test Setup for DC/DC Converter

1 MW
1.5kV Supply

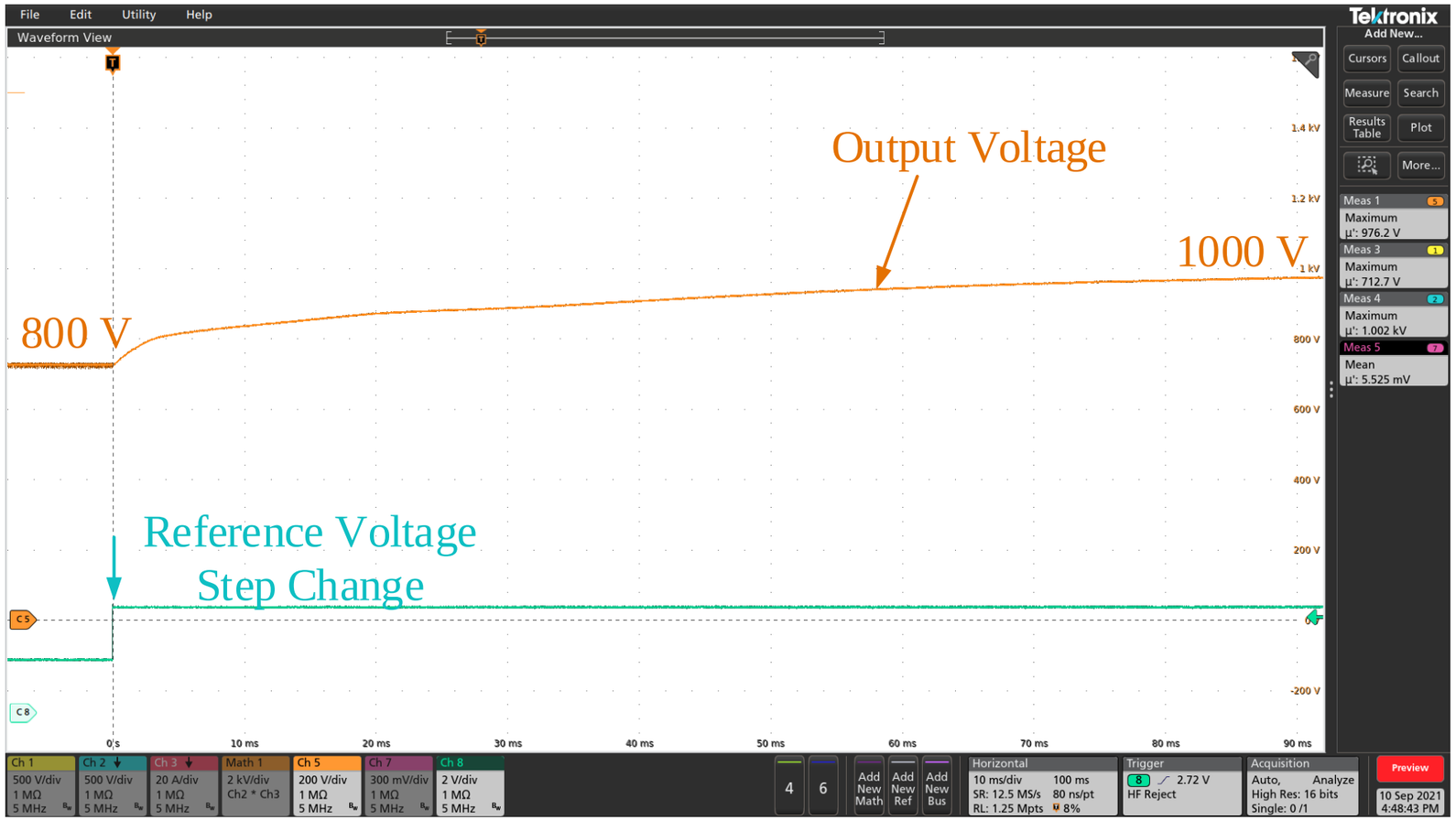


Test Setup for Inverter Stage

750 kW
Load Bank

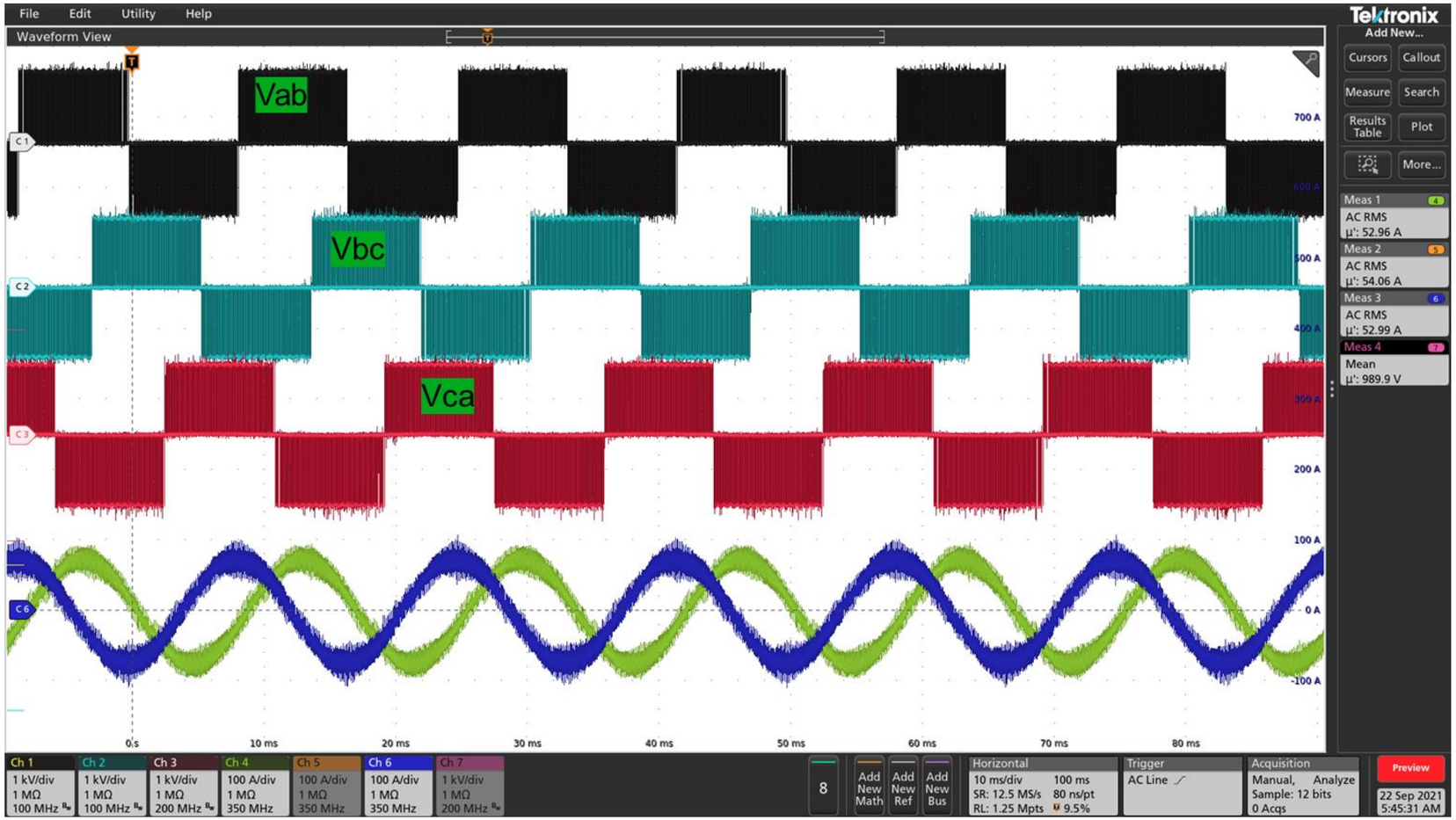
Innovation Update

- Close-loop control for DC/DC Converter



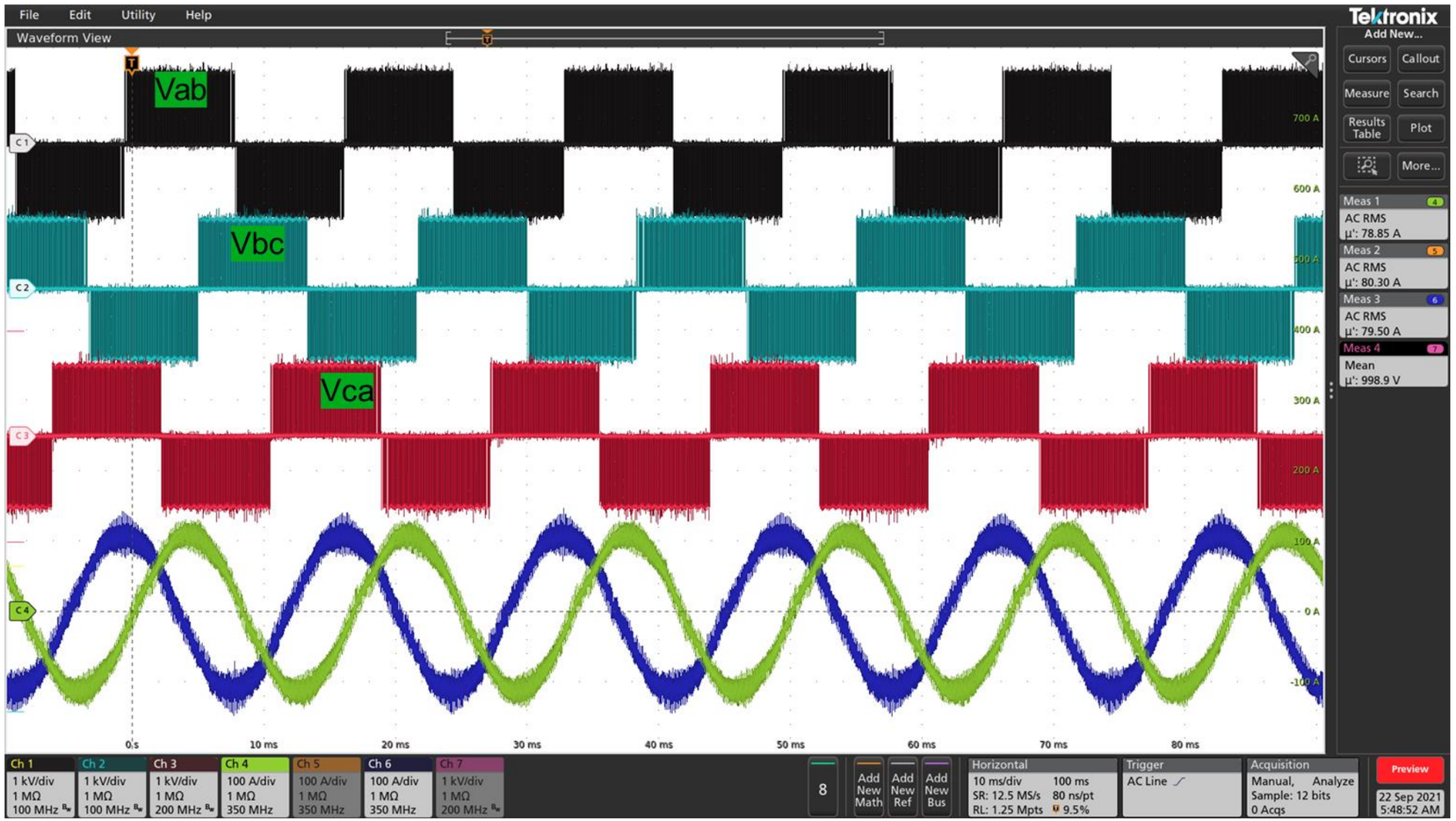
Innovation Update

- Continuous Power Testing for Inverter Stage @ 50kW (1kV DC bus, 480V AC)



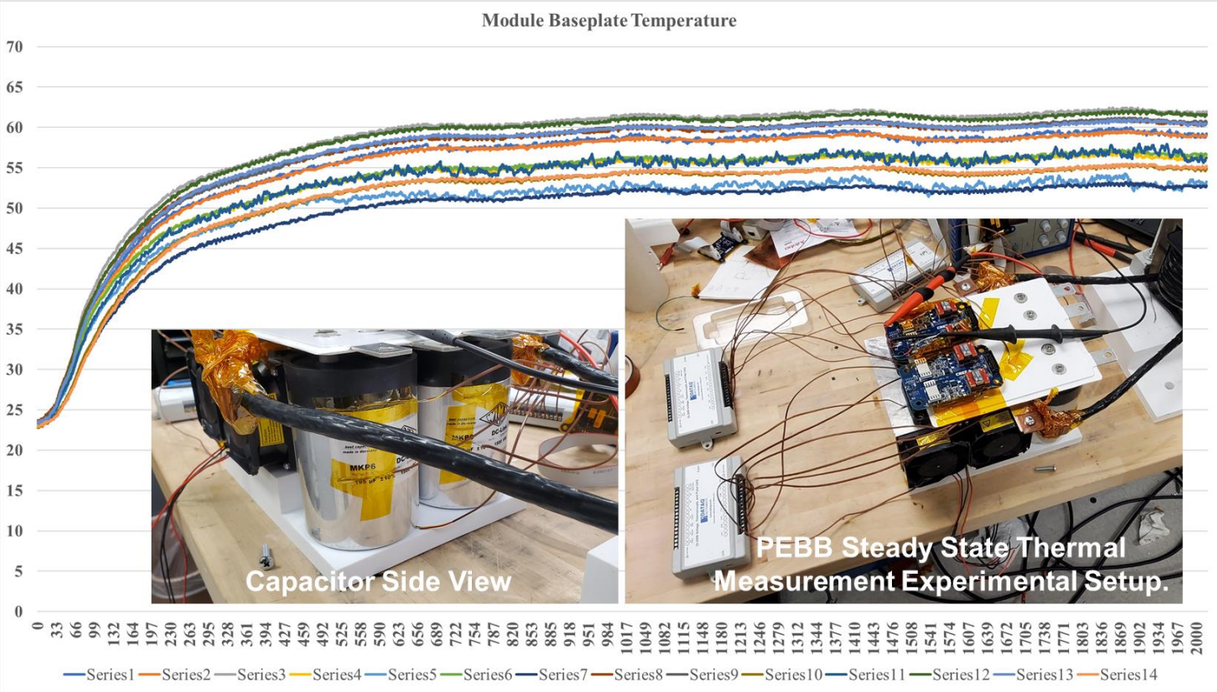
Innovation Update

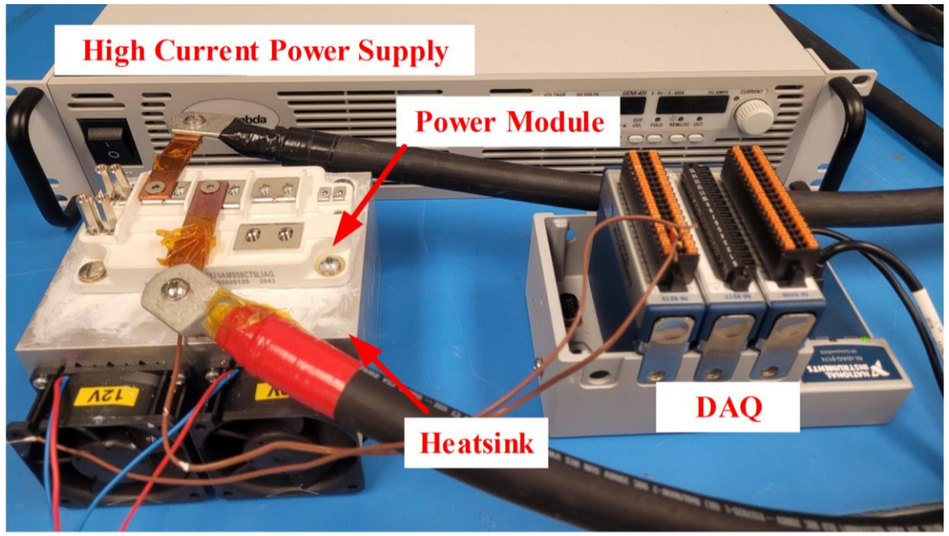
- Continuous Power Testing for Inverter Stage @ 75kW (1kV DC bus, 480V AC)

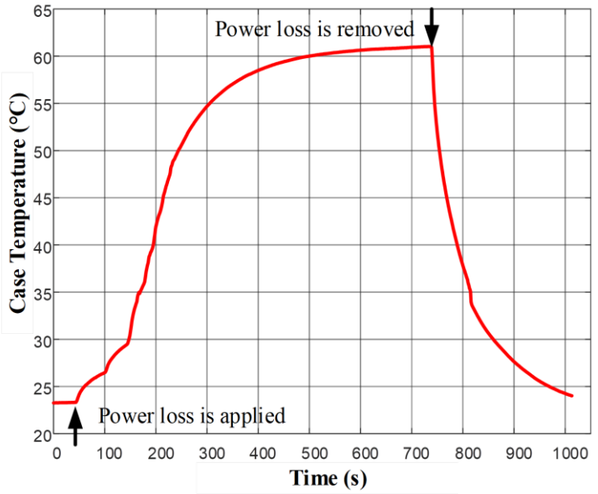


Innovation Update

- Thermal Validation

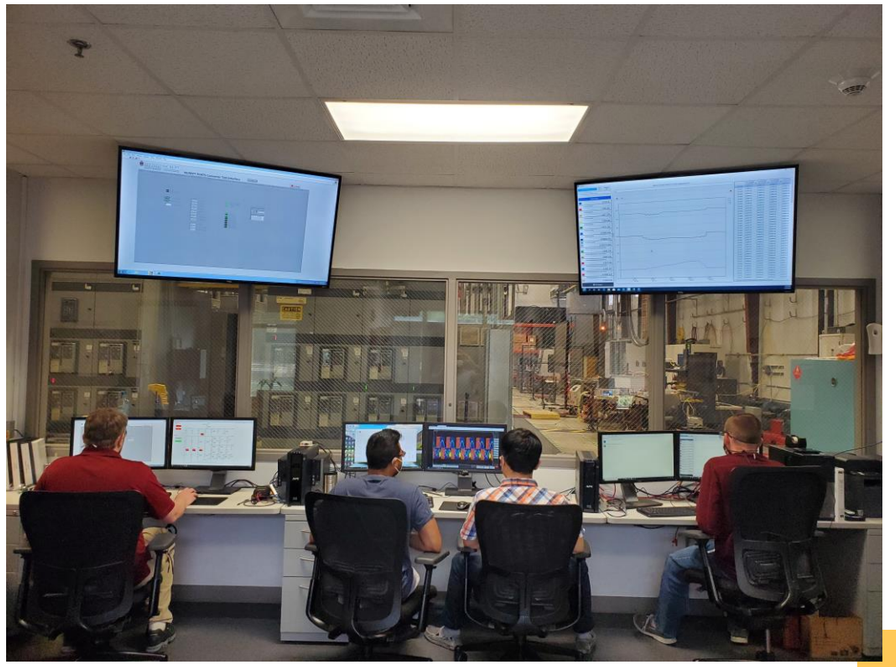






Innovation Update

- Milestone update
  - Completed the design and validation of hardware subcomponents in IPS, including DC/DC, Inverter, Gate Drivers, and Controller.
  - Implemented and validated various advanced features using the IPS hardware, including LCL parameter identifications, DC link capacitance estimation, module junction temperature estimation, communications, etc.
- Summarize the risks and mitigation strategy
  - COVID
  - Components long lead time



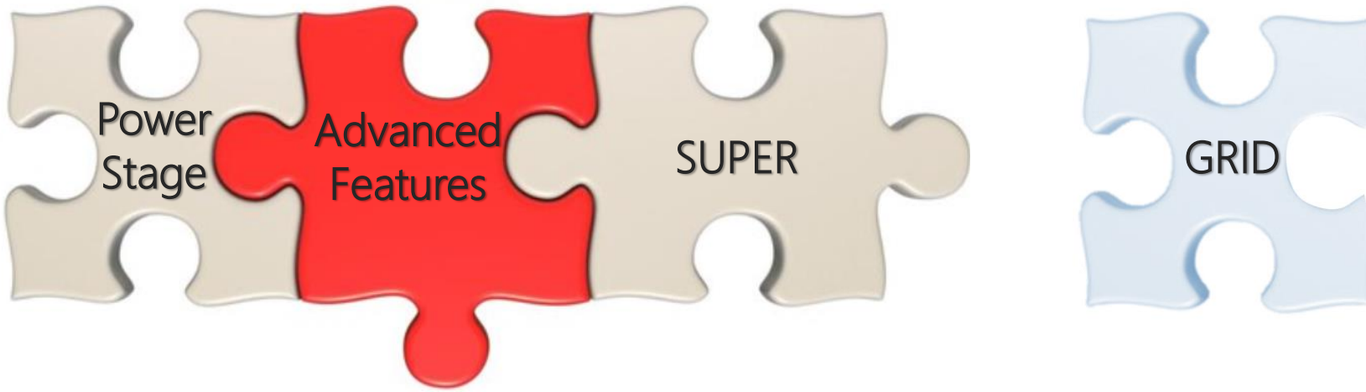
Innovation Update

BP2 Tasks

- Task 2.1 – IPS System Integration
    - Cabinet level integration
- Task 2.2 – IPS System Demonstration at University of Arkansas
    - Basic and advanced inverter functionalities
- Task 2.3 – Testing and Demonstration with ORNL
    - Grid functions
    - Integration and demonstration with SUPER

Impact/Commercialization

- The advanced features developed for IPS will enable its situational awareness, enhance the interoperability and system reliability.
- Further with the standardized architecture, the IPS can be easily connected to the generic testing environment or standardized SUPER to demonstrate advanced grid functionalities.



THANK YOU

This project was supported by the Department of Energy (DOE) - Office of Electricity's (OE), Transformer Resilience and Advanced Components (TRAC) program led by the program manager Andre Pereira & Oak Ridge National Laboratory (ORNL)

U.S. DEPARTMENT OF ENERGY | OFFICE OF ELECTRICITY

Acronyms

IPS: Intelligent Power Stages

SUPER: Smart Universal Power Electronic Regulators