U.S. Department of Energy
Advanced Manufacturing Office

Workshop on Ultra Precision Control for Ultra Efficient Devices—

Second Workshop in AMO Series on Semiconductor R&D for Energy Efficiency

April 21–23, 2021

Read-Ahead Document

Preface

The purpose of this document is to provide background information for those individuals who will be participating in the U.S. Department of Energy, Office of Energy Efficiency and Renewable Energy, Advanced Manufacturing Office Workshop on Ultra Precision Control for Ultra Efficient Devices on April 21–23, 2021. This is the second workshop in the AMO Series on Semiconductor R&D for Energy Efficiency. The first workshop was on January 25–26, 2021 and was focused on Integrated Sensor Systems. Like the readahead for that workshop, this brief document is structured to match the upcoming agenda. Please try to review the relevant sections prior to each day of workshop.

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1 Workshop Overview and Purpose

1.1 Advanced Manufacturing Office

The U.S. Department of Energy (DOE) Advanced Manufacturing Office (AMO) collaborates with manufacturers, small businesses, national laboratories, universities, and other stakeholders to catalyze research, development, and adoption of energy-related advanced manufacturing technologies and practices to drive U.S. energy productivity and economic competitiveness[1] as part of the Departmental priorities to combat the climate crisis, create clean energy jobs, and promote energy justice.[2] AMO uses a matrix approach to managing its research, development, demonstration and deployment (RDD&D) portfolio, which is funded at $396 million in fiscal year 2021 (FY 21). This holistic top-down and bottom-up systems approach identifies national needs, while leveraging AMO's fundamental and applied science foundations in materials, processes, energy systems, and the manufacturing enterprise to shape an AMO portfolio with the highest potential for impact. AMO supports research and development (R&D) projects, R&D consortia, and technical partnerships with national laboratories, companies (for-profit and not-for-profit), state and local governments, and universities through competitive, merit-reviewed funding opportunities designed to investigate new manufacturing technologies.

1.2 Workshop Purpose

On April 21 through 23, AMO will host the second workshop in a series focused on different topics related to semiconductor RDD&D. This workshop will focus on ultra-precise manufacturing (UPM) processes and next-generation control and metrology technologies needed to enable ultra-energy-efficient devices. Semiconductor industry products are critical to all manufacturing sectors, and greatly improving the energy efficiency of these products will provide lasting benefits for manufacturing, in both reducing environmental impact and increasing international competitiveness. The workshop will leverage recent AMO investments in atomic precision for microelectronics, as well as DOE Office of Science investments in microelectronics co-design (simultaneous design of hardware, software, and manufacturing processes). AMO aims to collect stakeholder input to further expand its portfolio related to UPM techniques to significantly reduce energy consumption of non-traditional devices.

Over the course of three days, attendees will explore and discuss ultra-energy-efficient devices through three topics:

1. Ultra-energy-efficient semiconductor devices
2. UPM processes for semiconductors
3. UPM tools (including next-generation metrology) for semiconductors

The information gathered at this workshop will inform AMO's future R&D portfolio investments; provide perspectives on trends, drivers, and challenges for ultra-energy-efficient devices and enabling technologies; and help the stakeholder community understand the opportunities on the horizon. For each topic, the workshop will include a panel discussion and a facilitated breakout session. The panel discussions will consist of academic, national laboratory and industry subject matter experts to discuss the research needs in the three topic areas. The

[1] U.S. Department of Energy, "Advanced Manufacturing Office," energy.gov. https://www.energy.gov/eere/amo/advanced-manufacturing-office [accessed 2021].
[2] U.S. Secretary of Energy Jennifer Granholm, "Deploying the Clean Energy Revolution," U.S. Department of Energy, February 25, 2021. https://www.energy.gov/articles/deploying-clean-energy-revolution.

facilitated breakout sessions will be used to further explore and refine the ideas presented in the panel discussions.

2 Motivation for Ultra-Energy-Efficient Semiconductors

Semiconductor industry products power nearly every aspect of our lives, and their use is expected to continue to grow exponentially with the rapid digitization of our modern economy in a post-pandemic world. Large industries such as telecommunications, the Internet of Things (IoT), and manufacturing are integrating more advanced semiconductor products into their products and processes. At the same time, we are approaching the inevitable end of Moore's Law efficiency increases due to device miniaturization. Due to these trends, semiconductor energy use is on track to become a major fraction of planetary energy use. As shown in Figure 1, computational energy use has doubled nearly every three years since 2010.[3] Ultra-energy-efficient semiconductor devices and architectures must be commercialized before 2030 to curb this unsustainable use of energy.

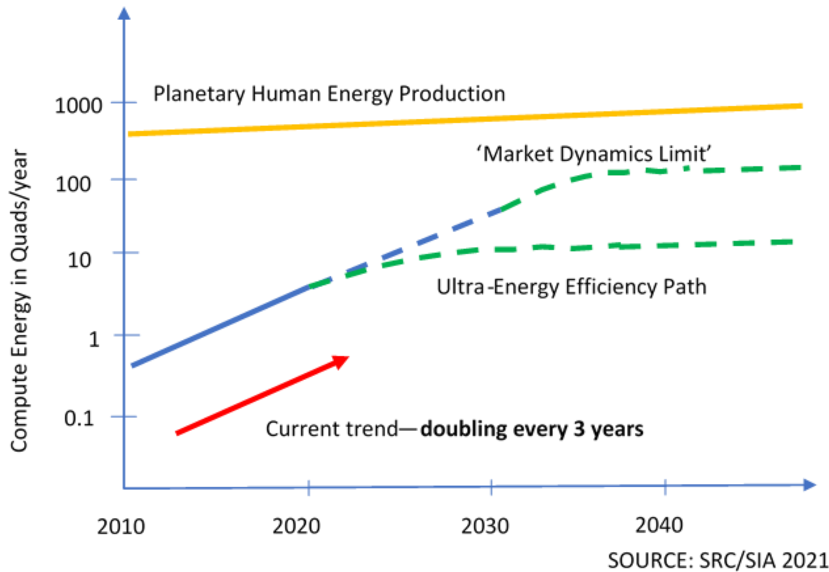

Figure 1. At current growth rates for computational energy use, the "Market Dynamics Limit" will be reached by 2035, limiting the world's computing capacity and economic growth. Alternatively, prioritizing ultra-energy-efficiency in semiconductor products can achieve a trajectory in which computing/economic growth and energy use are decoupled.

The looming semiconductor energy impact also comes at a time when the Biden–Harris Administration is accelerating the U.S. response to the climate crisis. The Nation is at an inflection point where federal investment in joint R&D for semiconductors—including the underlying manufacturing technologies for the next generation of devices—could accelerate our transition toward a sustainable path that avoids planetary energy impacts, while revitalizing a key domestic industry that offers high-paying jobs. In this unique generational moment, AMO seeks advice on how the federal government might best partner with domestic industry in identifying R&D needs to drive ultra-precise (and even atomic-level) control of manufacturing for ultra-energy-efficient (i.e., >10x reduced energy usage) semiconductor devices. By partnering with U.S. industry to further develop UPM technologies, AMO hopes to increase the competitiveness of domestic device

3 The Semiconductor Research Corporation (SRC) and the Semiconductor Industry Association (SIA), "The Decadal Plan for Semiconductors: a pivotal roadmap outlining research priorities." January 25, 2021. https://www.src.org/about/decadal-plan/.

and chip manufacturing, spur domestic job creation in this growing field, and combat the climate crisis by flattening the curve of semiconductor energy consumption across all sectors that use semiconductors by 2030.

3 Ultra-Precise Manufacturing

Ultra-precision manufacturing is the next step in a long history of manufacturing at ever-smaller scales. Figure 2 shows a subset of Norio Taniguchi's chart that plots, and accurately predicted, the capability of what he referred to as ultra-precise manufacturing (UPM).[4] Note that Taniguchi, in 1983, accurately predicted that we would achieve commercial atomic-scale accuracy in roughly 2020 (in thin film deposition). While important manufacturing technological advances will continue at larger scales, much that is cutting edge is at the nanoscale, or even the atomic scale. For example, at the micron scale, recent developments in electron-beam powder bed fusion have surpassed the additive manufacturing precision of laser powder bed fusion; but both techniques are important parts of AMO's current portfolio. AMO began its atomically precise manufacturing program in 2015 based on the hypothesis that increasing control at the atomic scale yields greater energy efficiency. As manufacturing technology has become more advanced, manufacturing precision has similarly developed, from the millimeter scale to the sub-nanometer. Semiconductor manufacturing is only one of the many application areas that will benefit from ultra-precision manufacturing, but it is probably the application area within AMO's Atomically Precise Manufacturing portfolio closest to commercialization.

Precision is not the only consideration when choosing a manufacturing method. Factors such as cost, throughput, and process intensity must be considered in conjunction with the desired precision when choosing the appropriate manufacturing technique. We will explore such trade-offs in our discussions throughout the workshop.

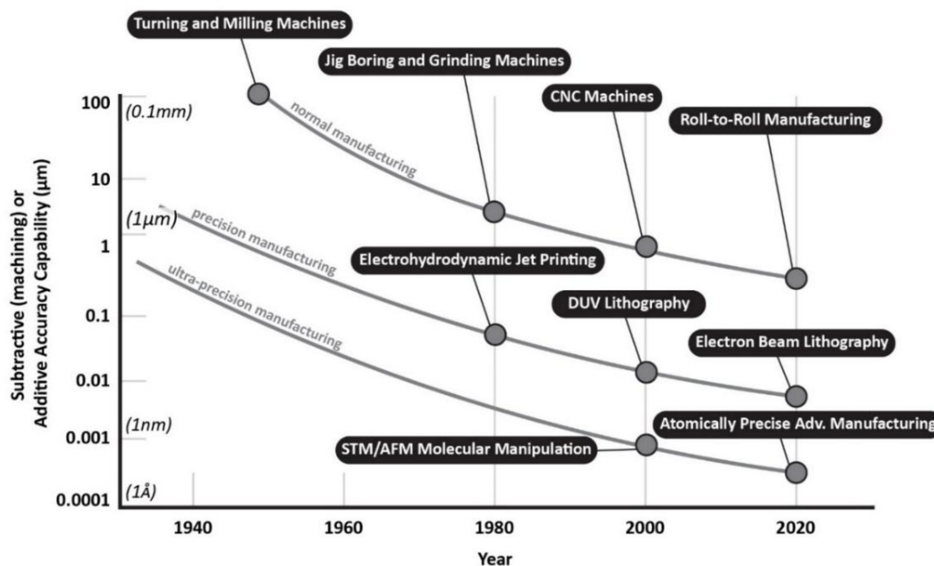

Figure 2. An adaptation of Taniguchi's plot showing the improvements in manufacturing precision over the 20th and 21st centuries. Modified with permission from P. Shore.[5]

[4] N. Taniguchi, "Current status in, and future trends of, ultraprecision machining and ultrafine materials processing," *CIRP Annals*, 32(2) (1983): 573–582. https://doi.org/10.1016/S0007-8506(07)60185-1.
[5] Paul Shore and Paul Morantz, "Ultra-Precision: Enabling Our Future," *Philosophical Transactions of the Royal Society A: Mathematical, Physical and Engineering Sciences* 370 (1973) (2012): 3993–4014. doi:10.1098/rsta.2011.0638.

4 Ultra-Energy-Efficient Devices

The metal–oxide–semiconductor field-effect transistor (MOSFET), which functions via thermionic emission of charge carriers, is the basis for logic, memory, and radio frequency (RF) device architectures and has stood as the flagship transistor for decades. As complementary metal–oxide–semiconductor (CMOS) transistors reach the fundamental (atomic) limit of scaling (according to Moore's Law), these devices can no longer offer enough improvements in energy efficiency to offset the energy consumption associated with their increasing use. New device designs, materials, and architectures must be harnessed to provide continuing energy efficiency gains. In this section, we emphasize devices, using new materials and device physics, that have the greatest chance of exceeding current MOSFET-based devices in energy efficiency and that may have near-term commercialization potential through integration with CMOS fabrication lines.

For computational devices, minimizing the physical size and increasing the precision of critical dimensions are the primary methods for reducing the energy and time per computation. This notion leads to a general need for ultra-precision research and manufacturing techniques. The 2020 Institute of Electrical and Electronics Engineers (IEEE) International Roadmap of Devices and Systems (IRDS) provides ranked lists of the most promising devices for logic and memory applications using non-traditional materials, physics, and structures (see Figure 3). These lists are the starting point for two of the three sections that follow. This document examines only the subset of devices that have been shown to have the potential for ultra-precision manufacturability and ultra energy efficiency. Some categories on the list (e.g., carbon nanomaterials) have been further divided into subcategories (e.g., one-dimensional [carbon nanotubes (CNTs)] and two-dimensional [graphene] devices) that have different manufacturability issues. The lists provided in the following sections are not exhaustive of potential ultra-energy-efficient devices, but simply serve as starting point for workshop discussions of devices whose commercialization, with additional research, is achievable by 2030. Some guiding questions to consider before the workshop include the following:

- Which promising or emerging devices are the most energy efficient?
- Are there device parameters that will suffer when designing for ultra-energy-efficiency?
- What is the connection between device energy efficiency and overall chip or system energy efficiency?
- What are the primary challenges hindering the integration of ultra-efficient devices into commercial products by 2030?

4.1 Logic for Potential Ultra Energy Efficiency

AMO is already conducting ultra-precision manufacturing research supporting 7 of the top 14 logic devices identified in the IRDS (Figure 3).

Generally, there are three types of emerging devices—with significant overlaps as new materials properties emerge. The first type relies on electric charge; the second and third types use state variables other than charge. The tunneling field-effect transistor (TFET) one-dimensional (1D) devices (CNT-based and nanowire FET devices) and 2D materials-based devices listed below are the first type. The TFET, tied for first in the IRDS as the most promising emerging logic devices, is first on our list for energy efficiency because it relies on quantum tunneling rather than thermionic emission to switch charge states. Logic devices based on charge appear to be the most straightforward to integrate with CMOS for near-term commercialization and are therefore emphasized here.

Emerging logic devices that use state variables other than charge as the effective carrier for logic operations are most likely to be important for energy efficiency beyond 2030. These devices are divided into two additional categories: those based on spin and magnetism and those not based on spin or magnetism. Devices in the first category can use an extraordinary variety of materials that have not yet been fully explored; any

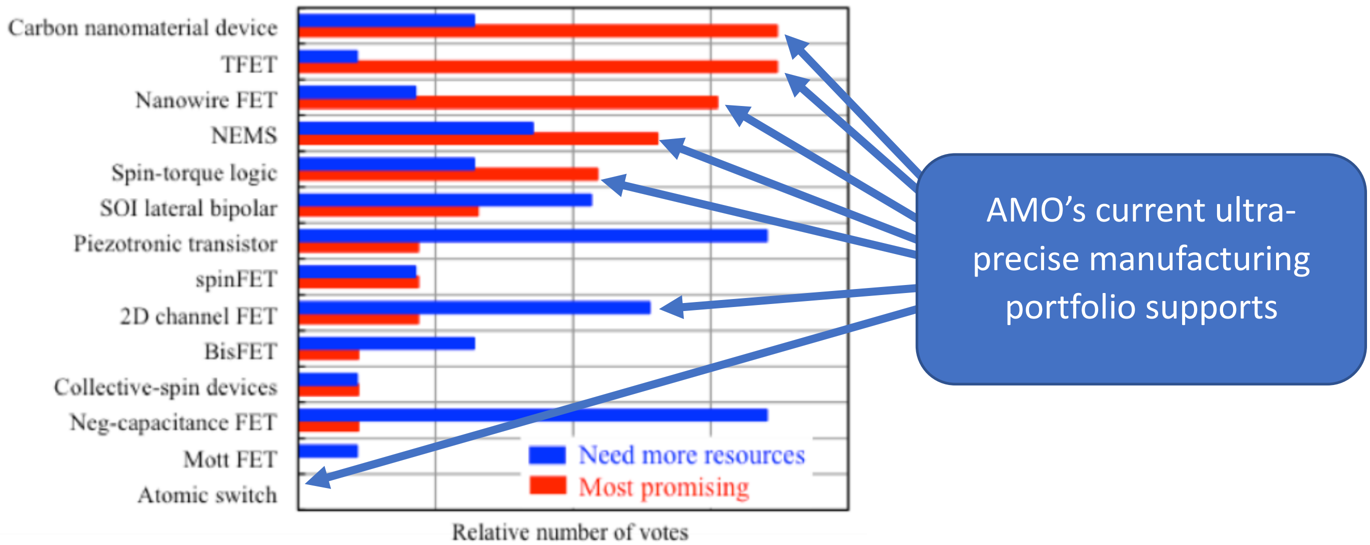

Figure 3. The IRDS list of most promising Beyond-Moore logic devices, with designation to AMO funded device research efforts.

comprehensive review of such devices is well beyond the scope of this document. Alternative-state variables for this broad class can include collective or single spins, magnetic domains, qubits, and even material domains (e.g., ferromagnetic).

Devices in the second category do not involve ferroelectric FETs, nanoelectromechanical (NEMS) switches, topological FETs, transistors based on collective electron phenomena such as Mott effect or exciton condensation (BiSFET), or any other form of spin or magnetism. Devices in this class rely on alternative state variables such as excitons, plasmons, and photons.

All three types of logic technologies (charge-based; non-charge, spin-magnetic; non-charge, non-spin magnetic) have to overcome challenges before they can be integrated with or replace conventional CMOS. According to the 2020 IRDS, these challenges include:

- Full interface control and a bandgap (e.g., TFETs, graphene)
- Synthesis (e.g., CNTs) with tight distribution of bandgap and mobility
- Low defect density (e.g., complex metal oxides)
- Low-resistance ohmic contacts (e.g., high-mobility transition metal dichalcogenides)
- Characterization of spin, magnetic, and electrical properties and correlation to nanostructure (e.g., spintronics)
- Large bandgaps much greater than κT at room temperature
  - Inability to modulate bandgaps efficiently with an electric field (e.g., topological materials)
- Key properties achieved at room temperature (e.g., exciton condensation for BiSFET heterostructures)

From literature searches focusing on the most explored concepts, AMO has identified the five logic devices with the highest energy efficiency, where comparative data are available. These technologies are described below.

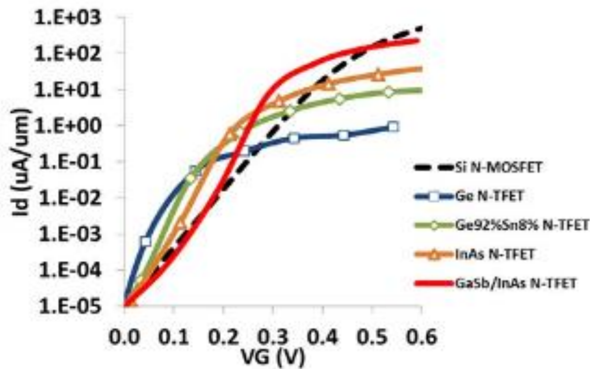

Figure 4. Comparison of transistor drain current per unit width versus gate-to-source voltage for n-channel Si MOSFET and TFETs. All TFETs exceed the 60 mV/decade upper limit slope of MOSFET. Source: Young, IEEE JEDS

1. Tunnel Field-Effect Transistors (TFET): Transistors based on quantum tunneling rather than thermionic emission were first proposed more than 50 years ago, but it wasn't until 2010 that experimentalists showed that ultra-low-power band-to-band quantum tunneling can operate at 1/10 the power of leading-edge conventional transistors (MOSFET). Since then, TFETs have been consistently ranked as the most energy-efficient of all logic devices (with switching energy as low as $2x10^{-18}$ Joules, or 2 attojoules). TFET's low subthreshold swing (SS) of less than 60 mV/decade at room temperature enables lower system power. In the past five years, different types of TFETs have proliferated at the bench scale. Their requirement for atomic precision, due to quantum tunneling, is exponentially dependent on the tunnel barrier thickness, is now preventing their scale-up. As shown in Figure 4, TFET's current is generally too low at higher voltages to serve as a drop-in replacement for conventional CMOS circuitry. With strain engineering and integration with other semiconducting materials, current can be enhanced. Recently, TFETs have been fabricated using 2D crystal technology based on the monolayer transition-metal dichalcogenides (MX_2) and ultra-thin topological insulators such as Bi_2Se_3. However, in practice, it is not clear whether there is a scalable technology that will enable utilization with known materials. Fabrication requirements (e.g., high temperature) for atomic precision prevent ready integration of TFET into CMOS, but manufacturing research (described in the next section) is under way to overcome these challenges.

2. **Carbon Nanomaterials:** Carbon allotropes have precise crystal structure at the nanoscale. These include carbon nanotubes and graphene, demonstrating that 1D materials (CNTs) and 2D materials (graphene) can have varying electronic properties, including metallic and semiconducting behavior. CNTs and graphene have different manufacturing challenges because of their differences in dimensionality. CNTs were first discovered and explored in the early 1990s by several scientists (precluding their receipt of a Nobel prize, which is awarded to no more than three scientists for one discovery)[6]. CNT's switching energy can be as low as 100 attojoules, two orders of magnitude lower than that of conventional cutting-edge transistors. But growing defect-free aligned CNTs require atomic-level control (see Nanowire FET, below). Graphene was found decades later by Geim and Novoselov, who isolated the first graphene monolayer in 2004.[7] They went on to win the Nobel prize in 2011, but other 2D materials (see 2D Channel FET, below) are becoming competitive with graphene for low-power performance.

[6] Iijima, Sumio (1991), "Helical microtubules of graphitic carbon", Nature, 354 (6348): 56–58, https://doi.org/10.1038/354056a0.
[7] Geim, A. K.; Novoselov, K. S. (2007). "The rise of graphene". Nature Materials. 6 (3): 183–191. https://doi.org/10.1038/nmat1849.

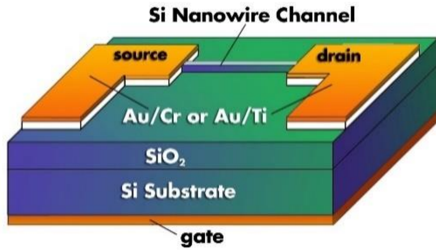

Figure 5. Schematic of nanowire FET. Source: NIST

3. **Nanowire FET:** Self-assembling CNTs—like other nanowire FETs—replace the conventional planar MOSFET channel with a 1D nanowire. One of two approaches is used to fabricate the nanowires: top-down lithography and etch, or bottom-up crystal growth. At small diameters, nanowires exhibit 1D ballistic transport and match well with gate-all-around structures. Nanowire growth uniformity and yield are the primary obstacles to commercialization.

4. **2D Channel FET:** Graphene—often considered separately from other 2D materials—was the first 2D channel FET. Non-carbon 2D materials, such as transition metal dichalcogenides (Figure 6), are proving to be more promising candidates than graphene for low-energy switching for future devices, as non-carbon materials provide improved electrostatic control and carrier mobility (in some materials).[8,9] Additionally, graphene's lack of bandgap limits its utility in digital applications. The planar surface of 2D FET allows for ease of integration. However, these relatively new materials still need to be optimized for widespread device fabrication. Control of atomic layers is essential, and advances in selective atomic layer deposition (ALD) and atomic layer etching (ALE) (sometimes known as area-selective deposition [ASD]) are needed to accelerate commercialization.

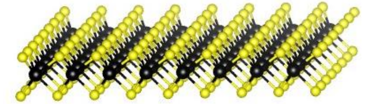

Figure 6. Transition metal dichalcogenide

5. **Spin-Based Logic:** The energy efficiency potential of conventional spin-transfer torque (STT) devices is limited because the technology has already reached the quantum limit in minimizing the energy required to flip a spin. This energy, $\hbar/2$, is comparatively high by modern standards. Magnetoelectric spin–orbit (MESO) devices combine magnetization and polarization in one switch and have the potential to achieve attojoule-class logic gates for computing. These devices exhibit collective switching, strong thresholding behavior, and non-volatility.[10] However, the inclusion of a wide array of novel materials and layering schemes in MESO devices will present significant manufacturing challenges.

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[8] H. Lu and A. Seabaugh, "Tunnel Field-Effect Transistors: State-of-the-Art," *IEEE Journal of the Electron Devices Society* 2(4) (2014): 44–49, https://doi.org/10.1109/jeds.2014.2326622.

[9] M. Hartmann, S. Hermann, P. F. Marsh, C. Rutherglen, D. Wang, L. Ding, L.-M. Peng, M. Claus, and M. Schroter, "CNTFET Technology for RF Applications: Review and Future Perspective," *IEEE Journal of Microwaves* 1(1) (2021): 275–287, https://doi.org/10.1109/jmw.2020.3033781.

[10] S. Manipatruni, D. E. Nikonov, and I. A. Young, "Beyond CMOS computing with spin and polarization," *Nature Physics* 14(4) (2018): 338–343, https://doi.org/10.1038/s41567-018-0101-4.

New architectures: As noted in the recent SRC decadal plan and elsewhere, computing architectures beyond von Neumann architecture will be needed to minimize energy use for rapidly emerging applications such as artificial intelligence (AI)- and machine learning (ML)-related computational functions. A full discussion of these architectures (neuromorphic, quantum, etc.) is beyond the scope of this workshop, and it is unclear whether such architectures could have significant hardware deployment by 2030. However, even the energy consumption of traditional architectures can be dramatically lowered by integrating more components of the device into a system-on-chip (SoC) architecture (the new Apple M1 chip is one example) or by using massive parallelism in integrating traditional devices. Consider Cerebras' recent development of huge Si "chips." By placing 400,000 CPUs on a single piece of silicon, this technology avoids off-chip communication, allows each core to have its own local memory, and connects all cores on-chip, leading to 3000x more capacity and 10,000x greater bandwidth.[11] While increased energy efficiency was not the goal, Cerebras has opened a portal to improved efficiency with conventional devices. Note that this approach also has created some new ultra-precision manufacturing challenges in inspection, metrology, and testing.

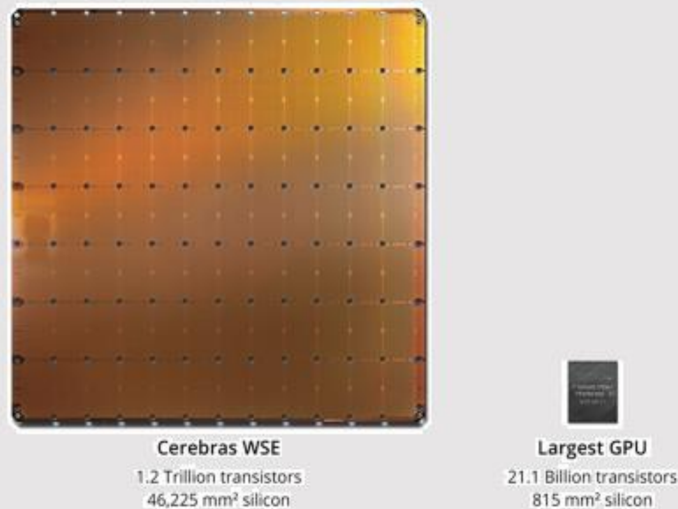

Figure 7. Comparison of Cerebras Wafer Scale Engine (WSE) to industry's largest GPU.

4.2 Memories for Potential Ultra Energy Efficiency

As with logic devices, novel channel materials or device physics can be leveraged for ultra-energy-efficient memory devices. AMO's ultra-precision manufacturing R&D portfolio supports four of the top nine memory devices identified in the IRDS.

[11] Cerebras Systems, *Cerebras Wafer Scale Engine: An Introduction*, white paper, 2019, https://www.cerebras.net/wp-content/uploads/2019/08/Cerebras-Wafer-Scale-Engine-Whitepaper.pdf.

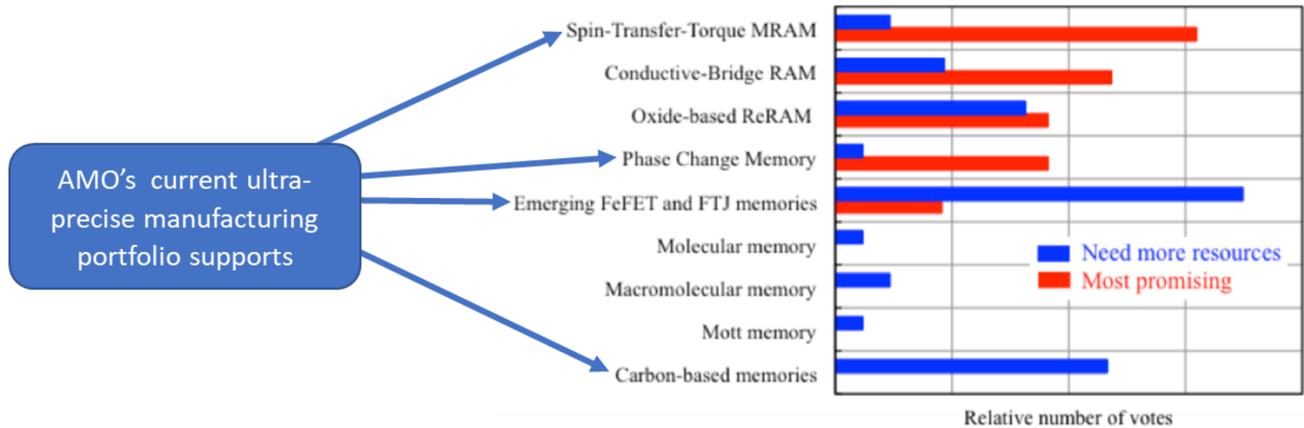

Figure 8: The IRDS list of the most promising beyond-Moore memory devices, with designation to AMO-funded device research efforts.

As with logic devices, there are three types of emerging memory devices: devices that rely on electric charge; non-charge-based devices that rely on spin and magnetism; and devices those that use state variables other than electric charge, spin, or magnetism. An example of the first type—emerging memory devices that rely on traditional thermionic emission—is carbon-based memories, using carbon nanotubes, graphene, or insulating carbon.

Of the second type (those that rely on spin and magnetism as the state variable), spin-transfer torque (STT) devices are the most mature and have recently entered production stage. Spin-orbit torque (SOT) is in a much earlier stage of research. This technology has shown great promise as an alternative to STT devices, thanks to sub-nanosecond switching speeds, but SOT suffers from higher write energy.

The third, and largest, type of emerging memory devices include those that rely on redox ions (oxide-based ReRAM); changes in crystal structure (phase-change memory [PCM]); electrochemical migration of ionic species (conductive-bridge, molecular memory); changes in polarization states (ferroelectric FET); collective electron phenomena (Mott memory); and incorporation of polymer structures (macromolecular memory).

According to the IRDS, long-term challenges for emerging memory devices include 1) Curie temperatures >400 K and 2) high remnant magnetization to >400 K (e.g., multiferroic and ferromagnetic semiconductor); 3) control of oxygen vacancy formation at metal interfaces and interactions of electrodes with oxygen and vacancies (e.g., complex oxides); 4) memory element synthesis (e.g., oxide-based ReRAM); and 5) needs for long-term reliability of the switching mechanism and improvements in switching speed, 6) cyclic endurance, and 7) uniformity of the switching bias voltage and resistance, both for the on-state and the off-state (e.g., conductive bridge RAM, PCM, molecular memory, and macromolecular memory).

From literature searches focusing on the most explored concepts, FeFET, FeRAM, and PCM represent the most energy-efficient non-traditional memory devices, where comparative data are available. The primary difference between FeFET and FeRAM is the device configuration. FeFET is a single-transistor device (1T) and incorporates the ferroelectric material in the gate stack of the transistor. FeRAM also uses a transistor but incorporates a ferroelectric storage capacitor in the plate line (1T1C). FeFET, the most energy-efficient memory device, requires less than 1 femtojoule (10^{-15}J) per bit, while FeRAM and PCM require 50fJ/bit and 3pJ/bit, respectively. For comparison, traditional MRAM, RRAM and NAND Flash memories require 2pJ/bit, 50pJ/bit, and 1nJ/bit, respectively.

Note that the STT is *not* first on our list for energy efficiency, despite its being the IRDS's most promising memory device. In addition, the STT and FeRAM have already been commercialized, so our focus will be on

other devices on the IRDS ranking that have not yet been commercialized but that could be commercialized by 2030, ranked according to their energy efficiency promise.

Summarized below are memory devices identified to have the highest energy efficiency, where comparative data are available. It should be noted that the categories of devices listed below are not mutually exclusive.

1. **Ferroelectric FET (FeFET):** FeFET incorporates a ferroelectric oxide between the channel and gate electrode. The permanent polarization of the ferroelectric material enables its memory capabilities. While ferroelectric devices show higher energy use than non-STT spintronic devices, the former feature higher speed. The 2011 discovery of advanced CMOS-compatible HfO_2-based ferroelectric devices[12] will enable a wide range of devices from versatile, embedded non-volatile memory elements to compute elements made from HfO_2 thin films. As IoT devices become more ubiquitous, FeFETs are likely to be used for non-traditional, in-memory (e.g., neuromorphic) computing data-flow architectures to enable small, energy-efficient systems needed for edge computing. A majority of FeFET's low energy use is due to the close physical proximity of memory and logic devices, avoiding energy-intensive data movement. Current challenges include improved interface control of the gate stack and polarization hysteresis.

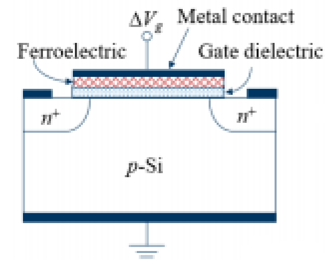

Figure 9. Schematic of FeFET. Source: Ng, solid-state communications

2. **Resistive Memories:** One of the most promising classes of emerging memory devices is resistance-based memories. These devices rely on resistance-based read-operation of a passive memory device and are characterized by high-speed read/write operation (10 ns), ultra-scalability below 10 nm, and compatibility with state-of-the-art CMOS processes. Resistive memory elements include oxide RRAM, floating gate resistors, valence change memory, electrochemical memory, phase-change memory, general spintronic and higher-resistance spin–orbit torque resistors, implemented as magnetic tunnel junctions (MTJs), and ferroelectric resistors (FTJ).

    a. **Phase-Change Memory:** PCM utilizes changes in conductance caused by change in a material's crystal structure (crystalline to amorphous). PCM's have zero leakage, because of the inability of current to flow in the amorphous state, thereby showing promise as an ultra-energy-efficient memory device. Integration of non-standard materials into current CMOS process flows will be a key challenge in commercialization efforts. Materials that can be switched by non-thermal phase changes are also being investigated.

3. **Spintronic:** To date, there are five types of spintronic memory: in-plane and perpendicular STT switches with perpendicular magnetic anisotropy, SOT switches, domain-wall (DW) motion devices, and magnetoelectric (ME) switched devices. Non-STT spintronic memories (especially those based on ME switching) show lower energy of operation than ferroelectric devices, which are also higher-speed. Similar to spin torque logic devices, STT memories use spin as the computational state variable and can induce flipping of the active elements in MRAM. STT MRAM devices exhibit near-zero leakage and better scalability than traditional MRAM, offering promise as ultra-energy-efficient devices. STT MRAM has entered commercial production under the name Everspin at major foundries across the world.

[12] A. I. Khan, A. Keshavarzi, and S. Datta, "The future of ferroelectric field-effect transistor technology," *Nature Electronics* 3(10) (2020): 588–597, https://doi.org/10.1038/s41928-020-00492-7.

Researchers at Stanford and SLAC National Accelerator Laboratory are developing non-volatile, ferroelectric hafnia-zirconia (HZO) alloys for FeFETs through high-throughput, ML-guided manufacturing process optimization. Thousands of in situ diffraction measurements, using synchrotron x-rays, are taken during the highly non-equilibrium flash annealing process to evaluate HZO crystal structures. This information, along with downstream device measurements, is then fed into a ML model to best inform HZO process parameters for an optimized film.

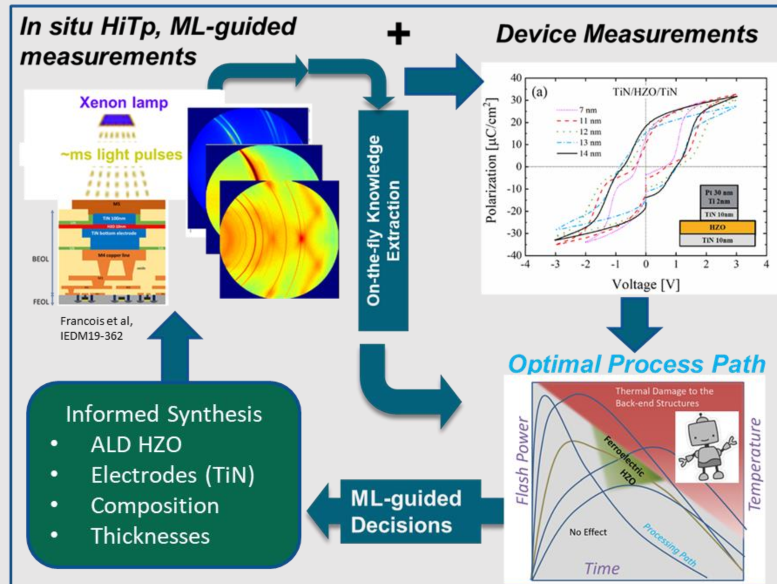

Figure 10. Block flow diagram of ML-guided process optimization of the HZO flash annealing process.

4.3 Radio Frequency for Potential Ultra Energy Efficiency

RF devices and circuits are widely deployed in communication systems. Discussed below are four materials that can reduce RF communication device energy consumption.

1. **Carbon Nanotubes:** CNTs' 1D geometry affords inherent linearity, which provides for a high dynamic range of CNT-based devices, making them ideal for electromagnetically noisy environments. High carrier mobility, high saturation velocity, and ballistic transport allow for extremely low power supply for CNT circuits.[13]

2. **Graphene:** Because they lack a bandgap, graphene-based devices may be better suited for analog applications. Graphene's extremely high carrier mobility, carrier modulation, and higher thermal conductivity make such devices an appealing, energy-efficient alternative to current technology. Cut-off frequencies up to 1.4 GHz have been demonstrated, making graphene-based devices and circuits particularly useful in RF communications technology.[14]

[13] Lian-Mao Peng et al., "Carbon Nanotube Electronics: Recent Advances," *Materials Today* 17(9) (2014): 433–442, doi:10.1016/j.mattod.2014.07.008.
[14] H. Wang, A. Hsu, K. K. Kim, J. Kong, and T. Palacios, "Graphene electronics for RF applications," 2011 IEEE MTT-S International Microwave Symposium, 2011, https://doi.org/10.1109/mwsym.2011.5972917.

3. **Gallium Arsenide (GaAs):** GaAs has been the flagship material for microwave devices since the 1970s, thanks to its high resistivity. High saturation velocity, carrier mobility, and larger bandgap make GaAs more energy-efficient than silicon-based RF components. Its mature product lines at large fabrication facilities still make it the go-to material for large-scale monolithic microwave integrated circuit (MMIC) production.[15]

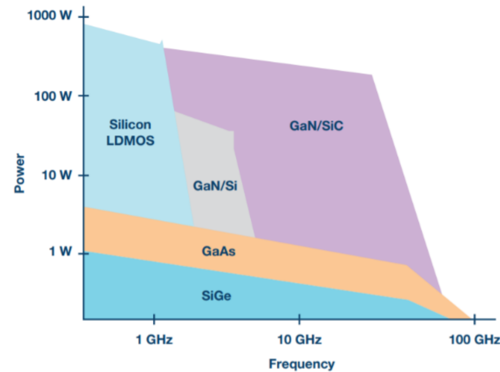

Figure 11. GaN is able to operate at significantly higher power at similar frequencies compared with traditional GaAs and SiGe technology.[15]

4. **Gallium Nitride (GaN):** Gallium nitride is an attractive alternative to standard GaAs MMICs because of its higher output power at microwave frequencies and higher operating temperatures and voltages. Faster switching speeds, lower on-resistance, and higher thermal conductivity make GaN-based RF devices more energy-efficient than both GaAs and silicon. Defect-free growth of GaN on non-native substrates is a pressing challenge.

5 Ultra-Precise Manufacturing for Semiconductors

AMO's hypothesis that increasing precision and control yields greater energy efficiency is certainly supported by decades of progress in semiconductor manufacturing. Reduction in energy consumption, faster operation, and more densely packed dies have led to increases in performance while decreasing device size. As semiconductor manufacturing technology has become more advanced, UPM has similarly developed, as seen in Figure 2. The predicament for semiconductor manufacturing is that down-scaling cannot continue past the atomic scale. As noted in the devices section, at the smallest scales, atomic precision will be required in material growth, deposition, and etching to enable high-performance devices; even a single defect can greatly reduce performance.

However, the need for ultra-precision also presents an opportunity for UPM to take advantage of the quantized nature of matter to control the precision of what is being fabricated. Manufacturing and metrology techniques that rely on and control quantum mechanical phenomena such as tunneling, magnetism, and spin will be particularly useful in this domain.

During the workshop, the second day will be divided into two focus areas: manufacturing processes and manufacturing tools. These are highly overlapping categories; however, from the perspective of how the technology will be deployed, there are distinct differences between a technology that is ready to be commercialized as a tool (especially as an R&D tool) and one that is ready to be deployed widely as a manufacturing process. In many cases, the difference between the tool and the process is the technology or manufacturing readiness level (TRL or MRL). Depending on their needs, researchers may want to adopt a new technology well before it is mature enough for manufacturing R&D (scaling up or scaling out, higher throughput and speed, higher precision). Conversely, budget-conscious researchers might stick with an older technology if they don't have a need for improved performance.

AMO's Atomically Precise Manufacturing (APM) program has contributed to ultra-precision advances that can be applied to semiconductor R&D—both for manufacturing R&D and for tool users. Hence, the workshop—and this document—has been organized into these two categories.

[15] Keith Benson, "GaN Breaks Barriers – RF Power Amplifiers Go Wide and High," *Analog Dialogue* 51(9) (2017).

The box below illustrates hydrogen depassivation lithography (HDL) research sponsored by AMO's APM program. The University of Texas at Dallas (UT Dallas) and Zyvex Labs (project partners) recently demonstrated an advance in scanning tunneling microscope (STM) control that enables an STM both to place dopants and to image them after they are buried in silicon using the same probe (Figure 12), avoiding the need for ex situ imaging with atomic force microscope-based techniques. Zyvex Labs used this in situ metrology capability in a manufacturing process R&D project for making analog bipolar junction transistors (BJTs) to allow alignment of donor dopant electrodes to acceptor dopant electrodes with atomic precision. This method will also benefit a separate but related Zyvex Labs semiconductor metrology (Tool) project (Figure 21) on scanning probe-based analysis of activated dopants for 2D devices. In addition to the BJT and metrology applications, this APM breakthrough could be used by Sandia National Laboratories in AMO-sponsored device R&D, as the labs develop a vertical APM TFET using atomically precise, selective n and p doping through HDL, as this method allows alignment of surface structures to buried features.

Hydrogen de-passivation lithography (HDL) has demonstrated the ability to use a scanning tunneling microscope (STM) to place dopant atoms in silicon for research in quantum devices and other nanoelectronics. However, HDL does not escape Tennant's Law,[16] and as a high-resolution[17] serial write technique, its throughput restricts its current implementation to research into new devices. Furthermore, HDL is currently limited to a single mask material and a few substrates (to date, silicon, germanium, and diamond have been identified as substrates). However, these limitations are being actively addressed. The throughput is, in principle, scalable in a manner that conventional e-beam lithography is not, such as via arrays of micro-electromechanical systems (MEMS)-based STM scanners and distributed local control, which can reach massively parallel levels (millions of tips on a 300 mm wafer).[18] Even so, while useful for high-value premium applications such as quantum computing, HDL will not be directly useful for consumer electronics. Further development of this technique to other masks (Cl), substrates (III-V semiconductors, 2D materials), and pattern transfer techniques (selective epitaxy, ALD, ALE, nano-imprint lithography) would greatly extend HDL's applicability.

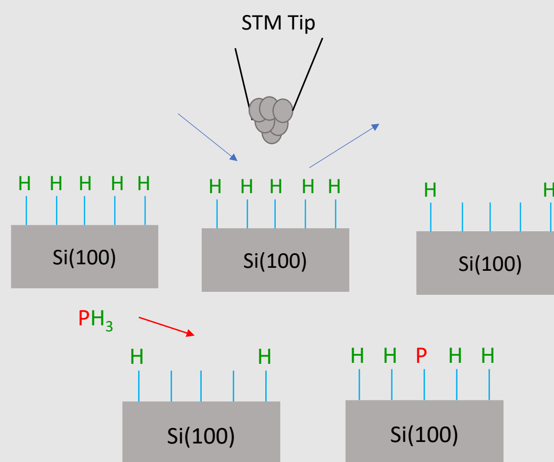

Figure 12. General flow diagram of HDL with selective phosphorous doping.

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[16] D. M. Tennant, "Progress and issues in e-beam and other top-down nanolithography," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films* 31(5) (2013), 050813, https://doi.org/10.1116/1.4813761.

[17] J. Randall et al., "Next generation of extreme-resolution electron beam lithography," *Journal of Vacuum Science & Technology B* 37(6) (2019), 061605, https://doi.org/10.1116/1.5119392.

[18] J. Randall et al., "Highly parallel scanning tunneling microscope-based hydrogen depassivation lithography," *Journal of Vacuum Science & Technology B* 36 (2018): 6–10, https://doi.org/10.1116/1.5047939.

5.1 Ultra-Precise Manufacturing Processes (Lithography, Assembly)

Current UPM processes are undergoing intensive manufacturing R&D to increase accuracy, throughput, and reliability. Near-atomic UPM techniques such as ALD are currently deployed in semiconductor manufacturing environments for high-κ dielectrics and peripheral applications such as environmental coatings. Listed below are several UPM techniques currently used in semiconductor R&D that we were able to identify. This list is not exhaustive, and a major function of the workshop is to gather input on other UPM methods necessary to enable ultra-energy-efficient devices.

Some guiding questions to consider before the workshop include the following:

- Which ultra-precise manufacturing processes are likely to make the greatest impact on chip-level device energy efficiency in the next 10 years?
- What are the primary obstacles/challenges in integrating UPM processes into current semiconductor fabrication lines?
- What are the primary advantages of deploying ultra-precise manufacturing (UPM) processes over traditional processing techniques for the fabrication of ultra-energy-efficient devices?
- Is CMOS compatibility the most important consideration in developing new manufacturing processes for the near term (commercial by 2030)?

The manufacturing process can be roughly divided into the two steps: the process of creating the pattern, usually by a lithography technique, followed by pattern transfer into a desired material by assembly, typically by deposition or etching. Atomic precision in both pattern creation and pattern transfer are required to enable ultra-energy-efficient devices. Both for R&D and quality control, ultra-precision characterization and metrology tools are needed throughout this process. Note that while the Ultra-Precise Manufacturing section is divided into Manufacturing Processes and Characterization/Metrology tools, some techniques can be used for both patterning and metrology.

5.1.1 Lithography

1. **Focused Ion/Electron Beam:** Ion or electron beams at high energies can be used to physically cut surfaces with atomic-scale precision; different ions will have different resolutions. These beams can be used for machining tiny features and structures into desired substrates with precision at the level of a few nanometers.

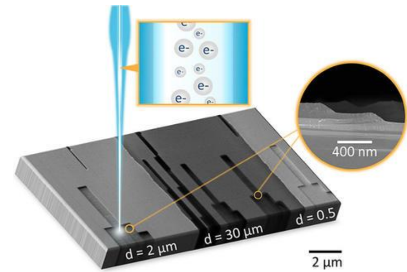

Figure 13. E-beam lithography. Source: NIST

2. **Hydrogen De-passivation Lithography (HDL):** HDL is accomplished with STM instrumentation and removes H atoms that passivate semiconductor surfaces to create chemically reactive patterns with atomic resolution. Crucially, the imaging and lithography modes are performed with the same probe, which allows a unique capability of closed loop lithography, taking advantage of the surface atomic lattice as a global fiducial grid reducing the metrology task to counting atoms. Thus, HDL uses the quantized nature of matter to control the size of the features that it makes.

3. **Nanoimprint lithography:** Nanoimprint lithography, being essentially a molding process, has much higher precision than competing semiconductor lithography, including EUV (see below), although nanoimprint lithography does not quite have atomic resolution. This technique is already being used for semiconductor memory devices. More accurate templates could be used to produce high-efficiency

electronics, possibly including quantum computing devices. HDL has been used to create nanoimprint templates with single-nanometer resolution with much greater accuracy than is possible with any other template-writing technique.

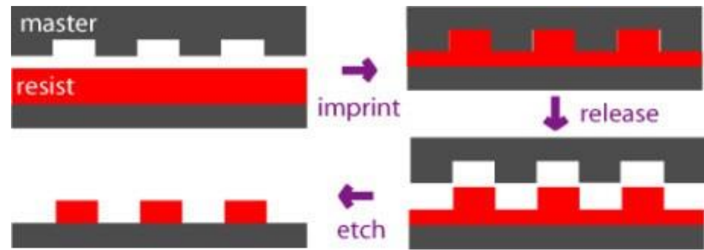

Figure 14. General flow diagram of nanoimprint lithography. Source: NIST

4. **Extreme Ultraviolet (EUV) Lithography:** EUV lithography uses a wavelength of light of roughly 13.5 nm. These tools are capable of creating dimensions several nanometers in size but are largely hindered by stochastic phenomena and feature roughness due to shot noise. Samsung and TSMC have already begun integrating these tools into their production lines. However, as device nodes become smaller, the usefulness of photon-based lithography systems must be considered because of the exorbitant cost of new tools, resolution limited by light diffraction, and available photoresist materials capable of such small dimensions.[19]

5.1.2 Ultra-Precise Assembly Techniques

1. **Single-Atom Manipulation with STM:** The pioneer of STM atom manipulation, Don Eigler from IBM, used an STM tip to position Xe atoms on a Ni surface at 4K, producing, apart from his company logo, quantum corrals that exhibited electron density standing waves,[20,21] Other notable examples include the work of Sander Otte, who positioned Cl vacancies on Cl/Cu (100) into ASCII codes to spell out the opening sentences of Feynman's "Plenty of room at the bottom" speech.[22] This directed assembly technique is capable of atomic-level precision, but the throughput is even worse than HDL.

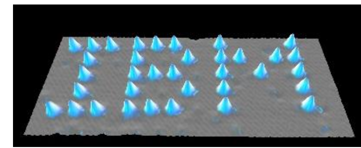

Figure 15. IBM logo spelled from 35 Xe atoms. Source: IBM.

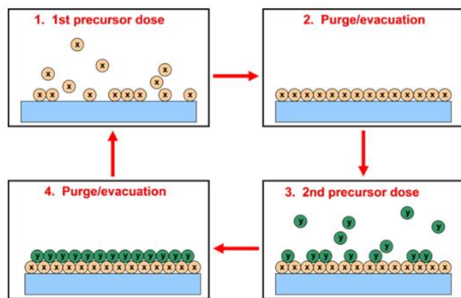

Figure 16. General flow diagram of ALD. Source: Kurt J. Lesker

2. **Atomic Layer Deposition (ALD):** ALD is a self-assembly-driven UPM technique. Precursor gases are sequentially pulsed into the reaction chamber to form a film, one layer thick. The precursor gas does not adsorb to itself, creating a self-limiting reaction that has the potential for defect-free, near-atomic resolution. Furthermore, as a chemical deposition technique, ALD (and ALE) can be made selective to a lithography pattern, thus transferring ultra-precise patterns with very high fidelity.[23] ALD is

[19] N. Mojarad, J. Gobrecht, and Y. Ekinci, "Beyond EUV lithography: a comparative study of efficient photoresists' performance," *Scientific Reports* 5(1) (2015), https://doi.org/10.1038/srep09235.
[20] D. M. Eigler and E. K. Schweizer, "Positioning Single Atoms with a Scanning Tunnelling Microscope," *Nature* 344 (1990): 524–526.
[21] M. F. Crommie, C. P. Lutz, and D. M. Eigler, "Confinement of Electrons to Quantum Corrals on a Metal Surface," *Science* 262 (5131) (1993) 218–220, doi: 10.1126/science.262.5131.218.
[22] F. E. Kalff, M. P. Rebergen, E. Fahrenfort, J. Girovsky, R. Toskovic, J. L. Lado, J. Fernández-Rossier, and A. F. Otte, "A Kilobyte Rewritable Atomic Memory," *Nature Nanotechnology* 11 (2016): 926–929.
[23] J. Ballard et al., "Pattern Transfer of Hydrogen Depassivation Lithography Patterns into Silicon with Atomically Traceable Placement and Size Control," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* 32 (2014), 041804.

starting to be deployed in high-throughput fabs for high-κ dielectrics.

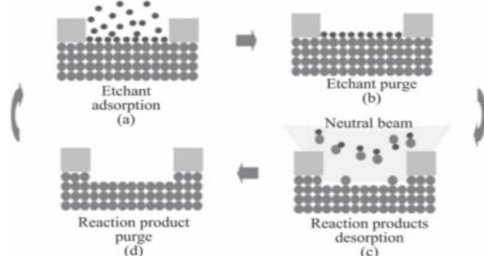

Figure 17. General flow diagram of ALD. Source: Engelmann et al.[24]

3. **Atomic Layer Etching (ALE):** ALE uses the same principles as ALD but instead etches a desired surface by removing a single crystallographic layer. ALE is primarily confined to etching of oxides but has been demonstrated for nitrides and some metals.[25] Processes to etch single layers of Si have also been demonstrated.

4. **Diblock Co-Polymer:** Block co-polymers are composed of discrete blocks of chemically distinct monomer units. When mixed with immiscible block co-polymers, they tend to self-assemble with nano-meter scale precision. Its versatility, tunability, dimensionality, and feature size make it attractive as a UPM technique.[26]

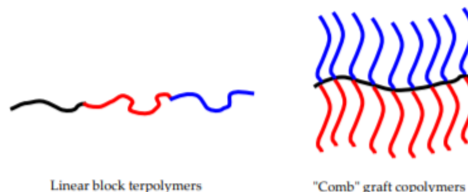

Figure 18. Examples of block co-polymers. Source: Feng, Polymers

5.2 Ultra-Precise Tools for Characterization and Metrology

Atomic-scale patterning and assembly techniques will require measurement and characterization techniques with similar resolution for understanding and exploiting atomic-scale phenomena. Ultra-precise metrology will be critical in deploying ultra-energy-efficient devices and validating UPM techniques by gaining a more precise view of the underlying atomic structure upon which the devices and UPM techniques depend.

Some guiding questions to consider before the workshop include the following:

- What are the most pressing challenges in UED manufacturing that can be addressed through advances in metrology?
- What metrology advances are needed to support manufacturing of 3D ultra-efficient devices?
- What challenges exist in integrating new metrology techniques into production lines for in-operando characterization?
- What other promising metrology techniques for UPM are not discussed?

[24] S. U. Engelmann, R. L. Bruce, M. Nakamura, D. Metzler, S. G. Walton, and E. A. Joseph, "Challenges of Tailoring Surface Chemistry and Plasma/Surface Interactions to Advance Atomic Layer Etching," *ECS Journal of Solid-State Science and Technology* 4 (2015), N5054.
[25] Fengzhou Fang et al., "Towards Atomic and Close-to-Atomic Scale Manufacturing," *International Journal of Extreme Manufacturing* 1(1) (2019): 012001. https://doi.org/10.1088/2631-7990/ab0dfc.
[26] Hongbo Feng et al., "Block Copolymers: Synthesis, Self-Assembly, and Applications," *Polymers* 9(12) (2017): 494, https://doi.org/10.3390/polym9100494.

1. **Scanning Electron Microscopy (SEM)**: One of the most versatile and oft-used metrology techniques, scanning electron microscopes image the surface of a sample by using a focused electron beam and collecting secondary and backscattered electrons. This technique has been shown to provide sub-nanometer resolution. In particular, critical dimension SEM (CD-SEM) has been a cornerstone in IC manufacturing by enabling repeatable, non-destructive, and high-speed imaging and metrology through advancements in low electron landing energies, high-efficiency electron detectors, and fast and accurate sample stages. New developments in SEM include sparse and optimized beam-scanning schemes to image only regions of interest; deep learning algorithms for denoising SEM images to enable unprecedented speed and imaging performance; and single-column, multi-beam, and multi-detector SEMs for fast data acquisition. Challenges include limiting error sources such as drift, vibration, beam damage, charging, and contamination; optimizing low-energy operation; and minimizing electron energy variation.[27]

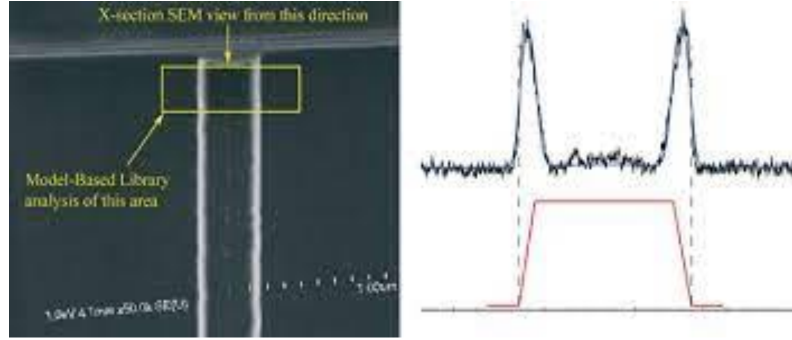

Figure 19. CD-SEM. Source: NIST

2. **Scanning Probe Microscopy (SPM):** SPM is a class of microscopy that relies on an atomic probe to scan the surface, measuring changes in physical forces. The two most common SPM techniques are atomic force microscopy and scanning tunneling microscopy.

   a. **Atomic Force Microscopy (AFM):** AFM is a type of SPM that uses a cantilever with a tip, one atom thick, to observe the surface nondestructively and also to physically manipulate atoms on the surface, or the surface itself, into desired positions or conformations with single-nanometer precision.

   b. **Scanning Tunneling Microscopy (STM):** STM is a type of SPM that uses a tip, one atom thick, to image surfaces with atomic resolution. The same probe can also, under different scanning conditions, be used to physically manipulate atoms on the surface, including removing atoms from the surface to create chemically reactive patterns or desired arrangements of atoms on the surface.

   c. **Kelvin Force Microscopy:** Imaging or relocating buried dopant devices outside of UHV (ultraviolet/visible) systems requires a minimally invasive scanning probe technique. Frequency-modulation Kelvin probe force microscopy (FM-KPFM) allows for the imaging of the surface using a surface potential map, interleaved with a peak-force mode topography scan. The primary advantage of this method is that there is negligible surface oxidation damage because the technique provides the ability to control maximum applied contact force.

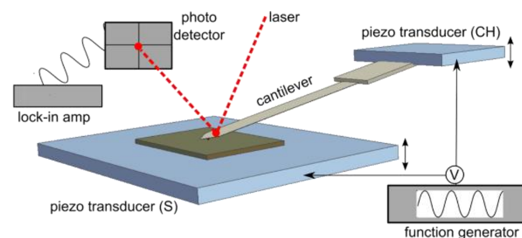

Figure 20. AFM Source: NIST

[27] N. G. Orji, M. Badaroglu, B. M. Barnes, C. Beitia, B. D. Bunday, U. Celano, R. J. Kline, M. Neisser, Y. Obeng, and A. E. Vladar, "Metrology for the next generation of semiconductor devices," *Nature Electronics* 1(10) (2018): 532–547, https://doi.org/10.1038/s41928-018-0150-9.

Researchers at Zyvex Labs and the UT Dallas Center for Atomically Precise Fabrications of Solid-State Quantum Devices are collaborating to develop new STM-based spectroscopy techniques to locate and measure buried-dopant structures. By making modifications to the STM feedback control loop, the researchers have been able to acquire dI/dV images of buried structures at significantly higher resolutions than conventional spectroscopy methods.[27] More recently, the research team demonstrated an ultra-high-speed method for acquiring I-V measurements of a surface while imaging at regular STM speed. Conventional STS requires hours to produce similar measurements. State-of-the-art single dopant atom imaging requires cryogenic temperatures. Zyvex Labs and UT Dallas are developing methods to leverage contrast between the number of buried dopants to provide quantitative measures in these areas.

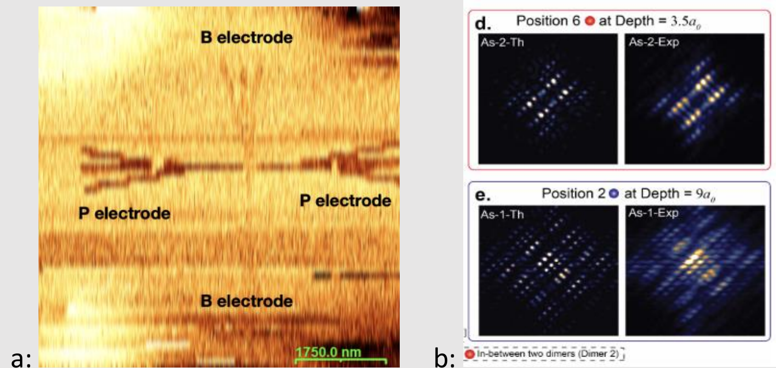

Figure 21. a. dI/dV STM image showing aligned HDL-patterned P and B electrodes; b. low-temperature STM image and DFT simulations of a single buried dopant atom.

3. **Micro-electro-mechanical System (MEMS) Actuators for Massively Parallel Scanning Probe Arrays:** Scanning probe techniques suffer from low throughput because of their serial nature. Increasing overall throughput can be achieved through parallel arrays of scanning probes; however, standard piezoelectric actuators are too bulky to make such arrays feasible. Instead, by using a MEMS architecture for the actuators, such arrays become feasible. The technology path and infrastructure to produce massively (millions) parallel arrays of MEMS scanning probes is well established. Such arrays would meet the demands of throughput and accuracy of in-line inspection and provide a tool for atomic resolution metrology.

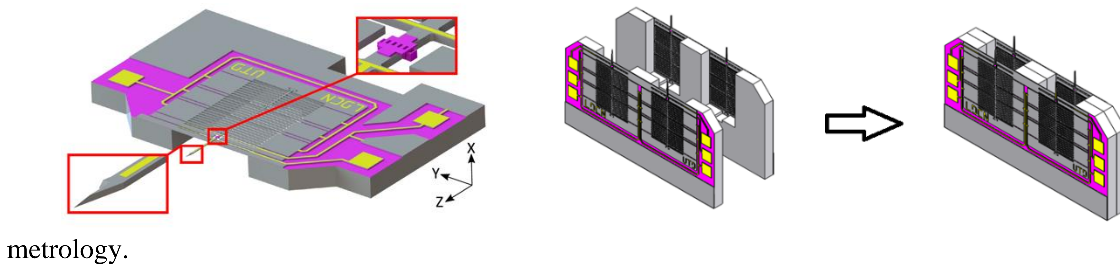

Figure 22. MEMS STM (left) can be scaled up to enable parallel operation of a large array of tips.[28]

[28] A. Alipour, et al. MEMS nanopositioner with integrated tip for scanning tunneling microscopy. *IEEE Journal of Microelectromechanical Systems*, 2021, doi: 10.1109/JMEMS.2021.3052180.

4. **Transmission Electron Microscopy (TEM):** TEM uses electrons transmitted through an ultrathin specimen to form an image. Coupling superior spatial resolution with elemental analysis, TEM is particularly useful in characterizing semiconductor device interfaces and structures, crystal structures, film thicknesses, and sub-nanometer features with resolution down to 0.05 nm. Scanning transmission electron microscopy (STEM) has also been used to detect and then reposition impurity atoms in thin Si specimens and graphene.[29] Recent developments include coupling automated FIB with STEM to extract site-specific ultra-thin samples for 3D measurements and TEM ptychography to image beam-sensitive, low-contrast materials (e.g., CNT, graphene, MoS_2).[30] The primary limitation is that TEM is a destructive technique, requiring ultra-thin, cross-sectional samples.

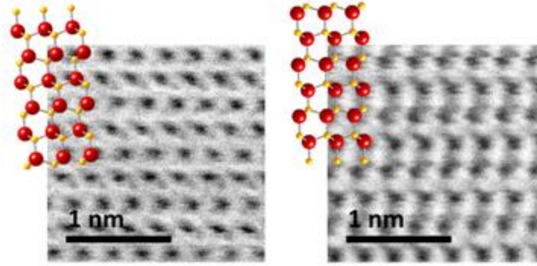

Figure 23. TEM Scan. Source: NIST

5. **X-Ray Diffraction:** X-ray diffraction is used to measure the crystallographic structure of materials and is particularly useful as a metrology tool in semiconductor manufacturing to study the composition and thickness (nanometer scale) of compound semiconductors and thin films.

6. **Small-Angle X-Ray Scattering (SAXS)**: SAXS measures small deviations in radiation from its incident direction caused by interactions with inhomogeneities in matter. SAXS has resolution down to single-nanometer scale and can determine the shape of nanostructures.[31,32] Like X-ray diffraction, SAXS data are in reciprocal space, making structures easier to resolve at smaller lengths scales, and will be especially useful for characterization of advanced node (sub-10 nm) devices. Recently, critical dimension SAXS (CD-SAXS) has seen increasing use as a non-destructive characterization technique for nanostructures, directed self-assembly, and multiple patterning structures. However, because of its particularly long characterization time, SAXS is rarely deployed in the lab, and reducing characterization time is an active area of research.[33]

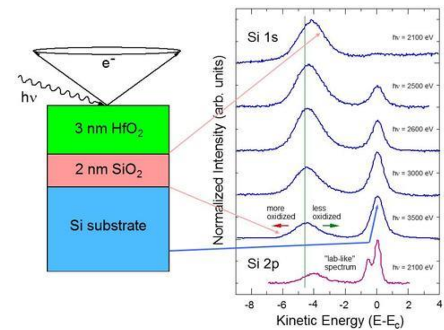

Figure 24. X-Ray Diffraction. Source: NIST

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[29] O. Dyck et al., "Building Structures Atom by Atom via Electron Beam Manipulation," *Small* 14 (2018): 1–9.
[30] N. G. Orji, M. Badaroglu, B. M. Barnes, C. Beitia, B. D. Bunday, U. Celano, R. J. Kline, M. Neisser, Y. Obeng, and A. E. Vladar, "Metrology for the next generation of semiconductor devices," *Nature Electronics* 1(10) (2018): 532–547, https://doi.org/10.1038/s41928-018-0150-9.
[31] B. R. Pauw, "Everything SAXS: small-angle scattering pattern collection and correction," *Journal of Physics: Condensed Matter* 25(38) (2013), 383201, https://doi.org/10.1088/0953-8984/25/38/383201.
[32] N. G. Orji et al. "Metrology for the next generation of semiconductor devices."
[33] Ibid.

7. **Scatterometry:** Scatterometry, a specialized variant of ellipsometry, is a non-imaging, model-based optical metrology technique capable of capturing deep-subwavelength size variations through polarization and intensity changes in scattered light. This technique is particularly useful in measuring overlay effects, geometric critical dimensions, and optical constants of arrayed structures. However, model fitting to determine desired parameters is reliant on measurement sensitivity and parameter correlation, often leading to inherent ambiguities in measurements. Further, parametric correlations, the number of approximations required, and difficulty determining acceptable uncertainty are cited as the primary challenges of this technique. Despite these challenges, scatterometry-based overlay measurements have experienced increased popularity in industry as a result of the technique's precision and process compatibility.[34]

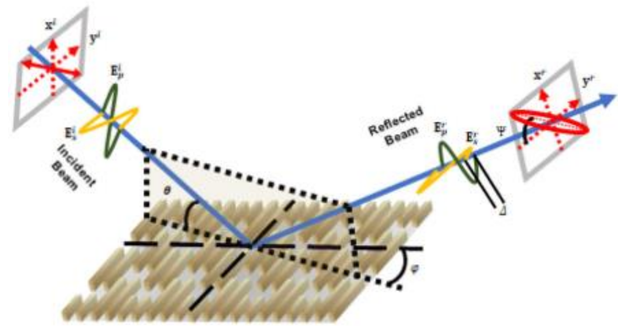

Figure 25. Light scattering off of a 3D fin structure Source: Orji, Nature Electronics (2018).

8. **High-Speed Atomic Precision Positioning:** Scanning probe-based lithography, imaging, and spectroscopy require positioning a probe in three-dimensional space with atomic or subatomic precision.[35] Vertical positioning with subatomic precision is achieved in STM with a feedback control system. However, lateral positioning is performed in open loop. It is possible to fabricate MEMS positioners with integrated sensors and actuators that can achieve subatomic precision under feedback control, thus increasing accuracy of scanning probe-based tools.[36] Furthermore, it is possible to design feedback control loops[37] and non-raster scan patterns[38] that significantly increase the speed of scanning probe devices, paving the way to scanning probe-based lithography, imaging, and spectroscopy at unprecedented speeds. DOE AMO is currently supporting the development of MEMS-based scanning probes that can be used for lithography and metrology. Atomic resolution imaging at much higher scanning speeds than is possible with piezoelectric actuators has already been demonstrated.

Figure 26. A silicon-on-insulator (SOI)-MEMS on-chip STM (left) and image of an H-passivated Si surface acquired with this device (right).

[34] N. G. Orji, M. Badaroglu, B. M. Barnes, C. Beitia, B. D. Bunday, U. Celano, R. J. Kline, M. Neisser, Y. Obeng, and A. E. Vladar, "Metrology for the next generation of semiconductor devices," *Nature Electronics* 1(10) (2018): 532–547, https://doi.org/10.1038/s41928-018-0150-9.

[35] S. Devasia, E. Eleftheriou, S. O. Reza Moheimani, et al., "A Survey of Control Issues in Nanopositioning," *IEEE Transactions on Control Systems Technology* 15 (5) (2007): 802–823.

[36] A. Sebastian et al., "Achieving sub-nanometer precision in a MEMS storage device during self-servo write process," *IEEE Transactions on Nanotechnology* 7 (5) (2008): 586–595.

[37] M. G. Ruppert et al., "On-Chip Dynamic Mode Atomic Force Microscopy: A Silicon-on-Insulator MEMS Approach," *IEEE Journal of Microelectromechanical Systems* 26 (1) (2017): 215–225.

[38] N. Nikooienejad et al., "Rosette-scan video-rate atomic force microscopy: Trajectory patterning and control design," *Review of Scientific Instruments* 90 (2019), 073702.

9. **Hybrid Metrology:** Hybrid, or combined, metrology leverages the capabilities of multiple tools to characterize a wider set of parameters than is possible using a single instrument. Further, statistical hybrid metrology techniques have been developed to reduce uncertainties for all parameters. Some examples of hybrid metrology include AFM and SEM, AFM and TEM, and CD-SAXS and SEM. Traceability to a reference becomes increasingly important when comparing results from different instruments in a hybrid framework. For example, measurement divergence between different instruments must be considered carefully to elucidate whether they are due to fundamental differences in measurement physics or whether the error sources were not fully accounted for and the measurements not traceable. At nanoscale dimensions, traceability, standardized parameter definitions, and sample registration methods are paramount for providing consistent and comprehensible measurements.[39]

10. **ML and AI for Automated Metrology and Pattern Error Correction:** A consequence of scaling to large arrays of scanning probes will be that human operators will no longer be able to operate these tools; automation of the lithography and metrology processes will become necessary. ML-based image recognition will enable alignment to surface atomic structures or previously written patterns and perform error correction of the pattern where possible.[40]

[39] N. G. Orji et al. "Metrology for the next generation of semiconductor devices."

[40] Maxim Ziatdinov et al., *Robust multi-scale multi-feature deep learning for atomic and defect identification in Scanning Tunneling Microscopy on H-Si (100) 2x1 surface*, The Center for Nanophase Materials Sciences, Oak Ridge National Laboratory, and Zyvex Labs LLC, February 2020, https://arxiv.org/ftp/arxiv/papers/2002/2002.04716.pdf.

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