Power Electronics Reliability

2010 Update Conference – DOE ESS Program

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NNSA National Nuclear Security Administration

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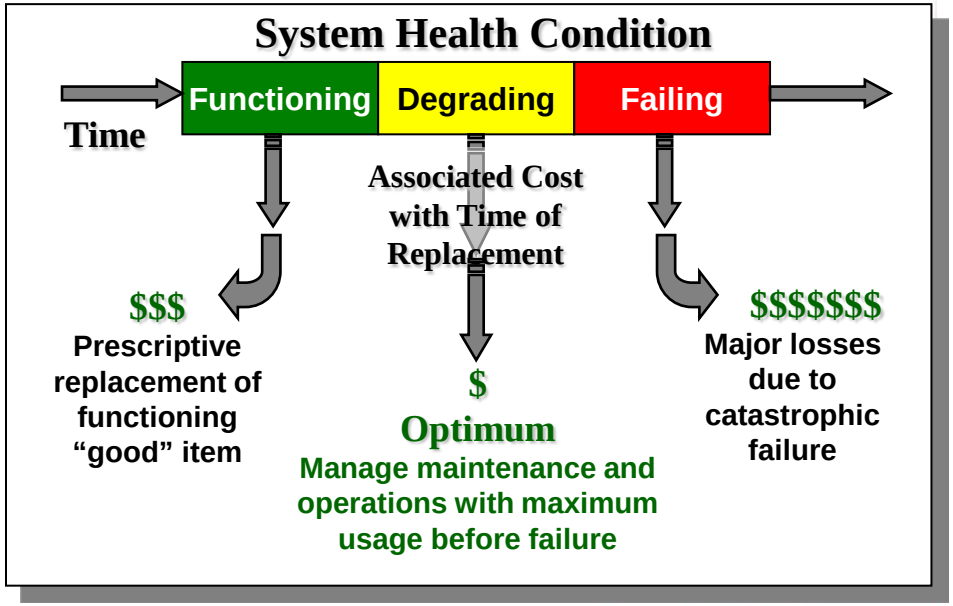
Project Goals

- **Use experiments and modeling to investigate and characterize stress-related failure modes of post-silicon power electronic (PE) devices such as silicon carbide (SiC) and gallium nitride (GaN) switches.**
- **Seek opportunities for condition monitoring (CM) and prognostics and health management (PHM) to further enhance the reliability of power electronics devices and equipment.**
  - **CM: detect anomalies and diagnose problems that require maintenance**
  - **PHM: track damage growth, predict time to failure, and manage subsequent maintenance and operations in such a way to optimize overall system utility against cost**



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Project Accomplishments

- Developed relationships with several industrial and academic partners involved in post-silicon device work
- Obtained a number of samples of SiC devices for stress testing
- Modified experimental test set-ups to accommodate new devices and provide new stress conditions
- Performed stress testing on several devices to induce representative degradation signatures
  - Dielectric breakdown and flatband/threshold voltage shifts in SiC MOS capacitors
  - Bias temperature stress induced increase in SiC MOSFET on-state resistance
  - I-V curve shift in Schottky diode
- Demonstrated corresponding concepts for CM and PHM

Materials and Devices/Tests

Material	Formula	Band Gap
Silicon	Si	1.11 V
Silicon Carbide	SiC	3.25 V*
Gallium Nitride	GaN	3.4 V*
*Depending on polytype		

- **SiC vs. Si**
  - **Higher breakdown field**
  - **Allows making lower on-state resistance devices**
  - **Higher temperature operation**
  - **Allows faster switching**
  - **More efficient grid equipment**
  - **Smaller footprint, higher density**

- **Stress Tests**
  - **SiC MOS capacitors**
  - **SiC MOSFETs**
  - **SiC Schottky Diodes**
- **I-V Tests**
  - **SiC JFETs**
  - **SiC Thyristors**
- **Future Tests**
  - **GaN HEMTs**
  - **Others (TBD)**

Stress Tests

Stresses

- **Voltage**
- **Current**
- **Elevated Temperature**
- **Bias Temperature Stress (BTS)**
- **Other Combinations**

Effects

- **TDDB (Time-Dependent Dielectric Breakdown)**
- **HCI (Hot Carrier Injection on smaller devices)**
- **NBTI (Negative-Bias Temperature Instability)**
- **Flatband/threshold shift (charge injection from BTS)**
- **Snapback**
- **Reverse Bias Breakdown**
- **Others (device dependent)**

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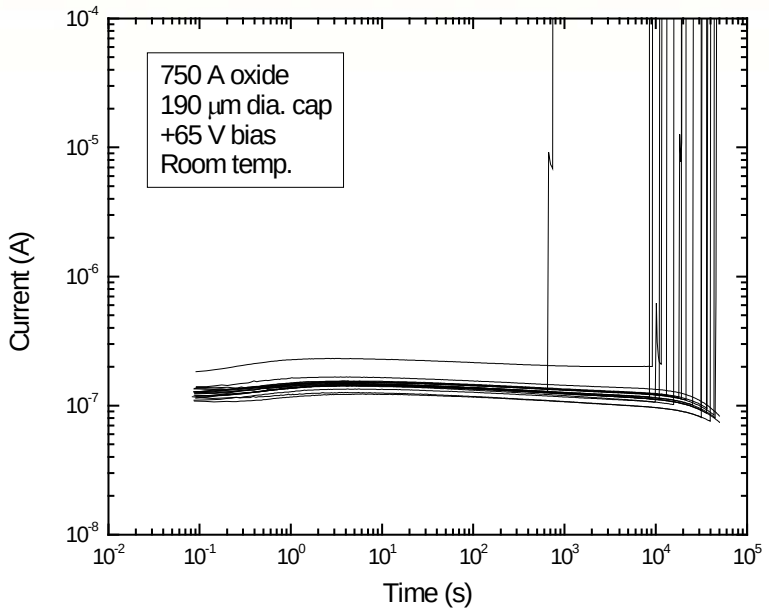
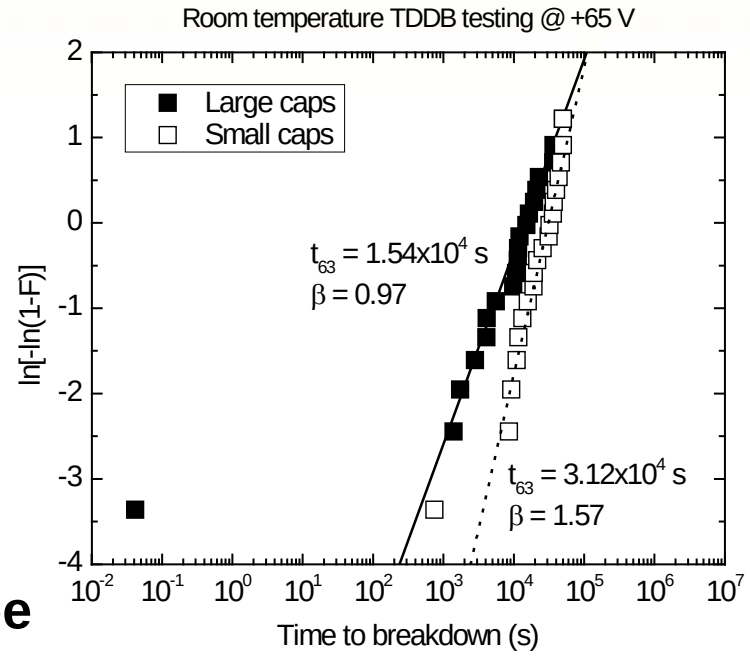
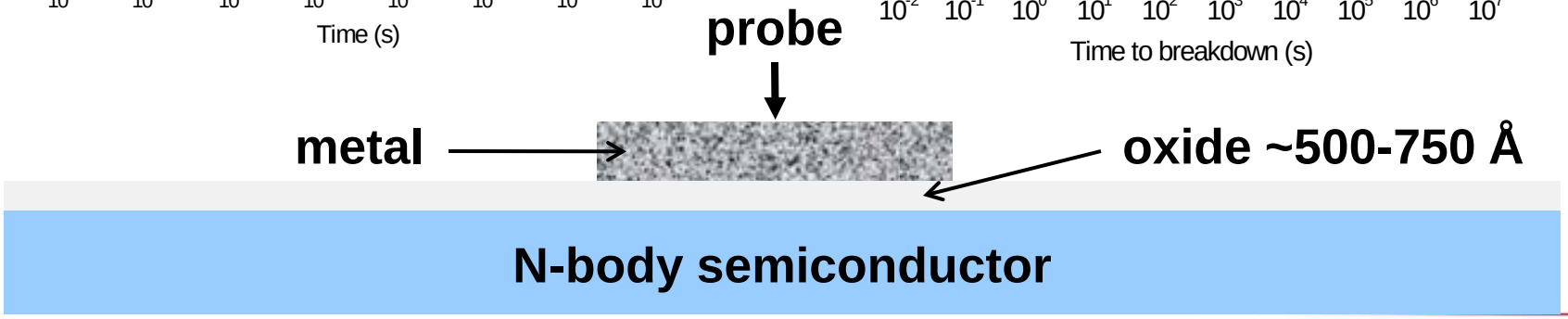
SiC MOS capacitors (TDDB)

Current vs. Time



Weibull Fit





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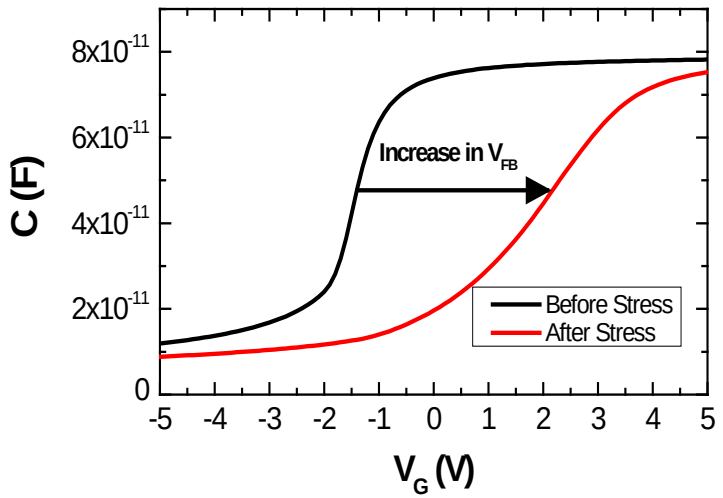
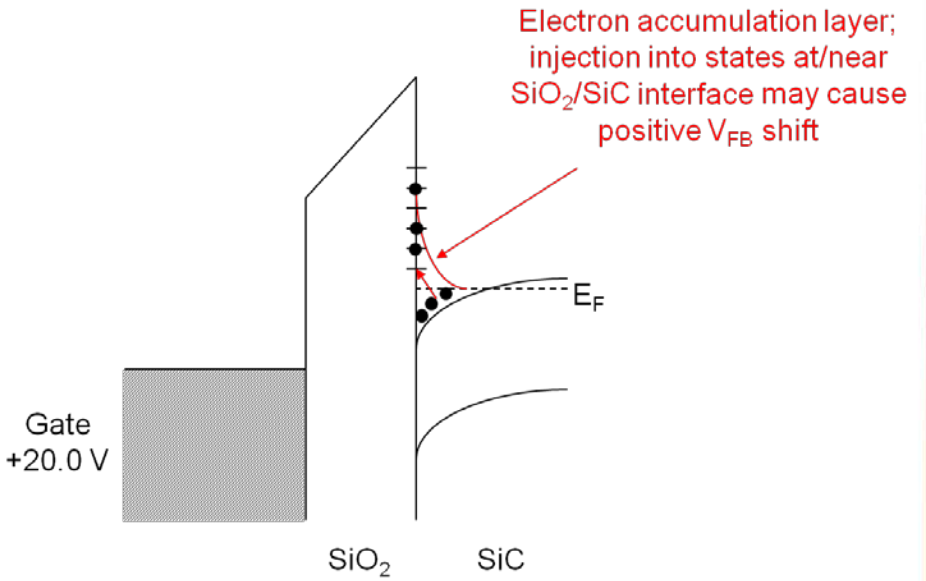
SiC MOS Capacitors (BTS tests)

Capacitance-voltage (C-V) curves before and after temperature stress



Negative charge injection into traps at/near the oxide semiconductor interface



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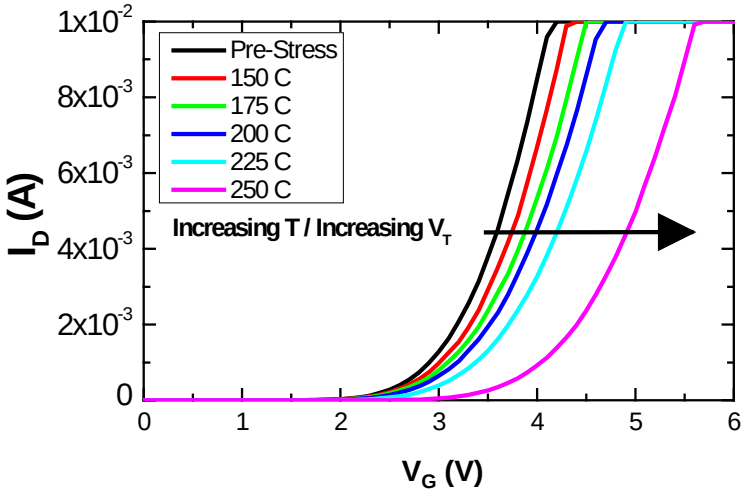
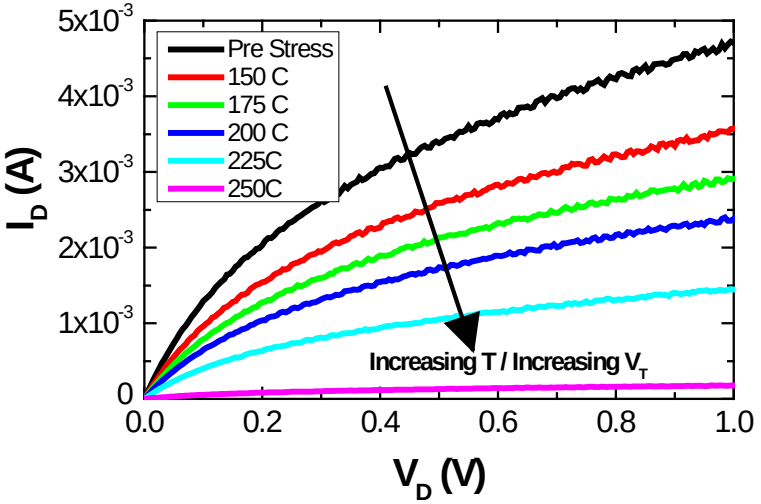
SiC MOSFET (BTS tests)

Drain Current vs. Gate Voltage (V_D = 1 V)



Drain Current vs. Drain Voltage (V_G = 3.5 V)



Bias temperature stress induces higher on-state resistance.

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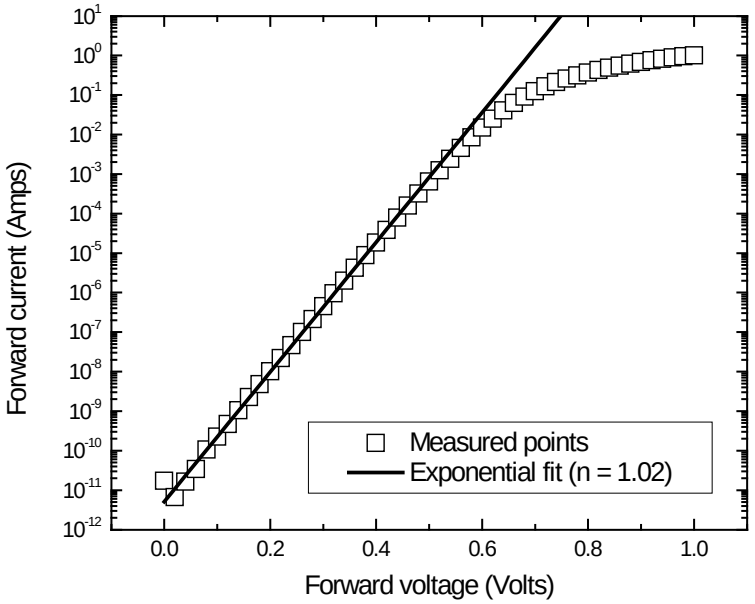
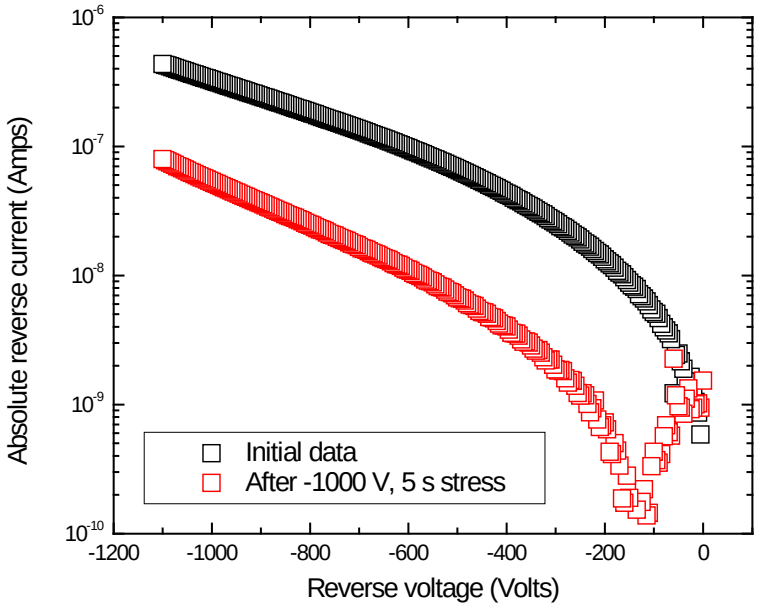
SiC Schottky Diodes

Forward I-V Curve



Effect of Voltage Stress on Reverse I-V Curve



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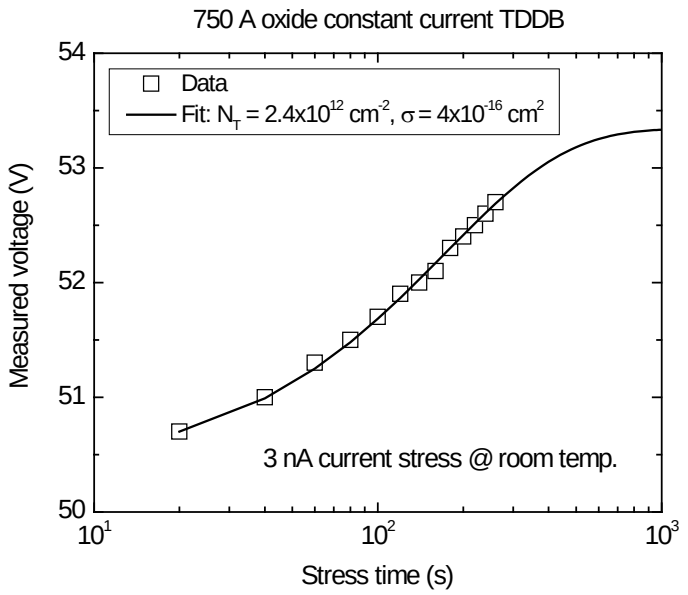
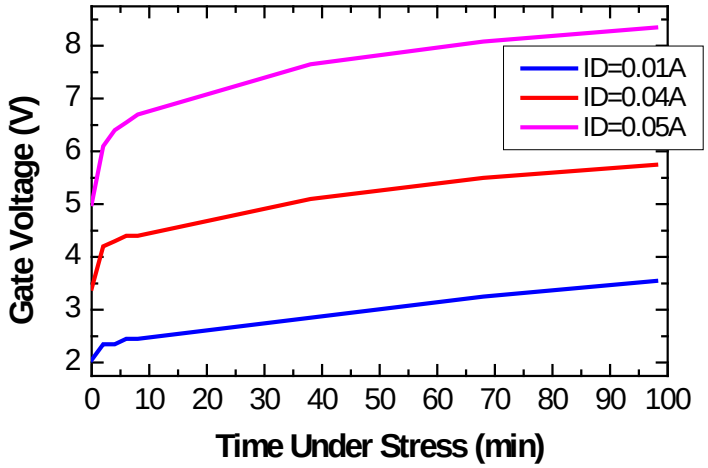
CM/PHM Concepts

Charge Accumulation in SiC MOS Capacitor



Voltage Threshold Shifts in SiC MOSFET



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Conclusions

- **Benefits of CM/PHM**
  - **Operate power conversion systems in ways that will preclude predicted failures**
  - **Reduce unscheduled downtime and thereby reduce costs**
  - **Pioneering reliability in SiC and GaN**
- **Future Work**
  - **Higher stresses**
  - **Test simple sensors vs. laboratory instruments**
  - **Once failure progression is understood, could design devices that degrade gracefully to facilitate PHM**
  - **Emerging field: publications in basic physics**

Questions?