Nuclear Energy

Office Of Nuclear Energy Sensors and Instrumentation Annual Review Meeting

Radiation Hardened Electronics Destined for Severe Nuclear Reactor Environments

Keith E. Holbert and Lawrence Clark
Arizona State University
NEET-2; Award DE-NE0000679

October 28-29, 2015

U.S. DEPARTMENT OF
ENERGY
Nuclear Energy

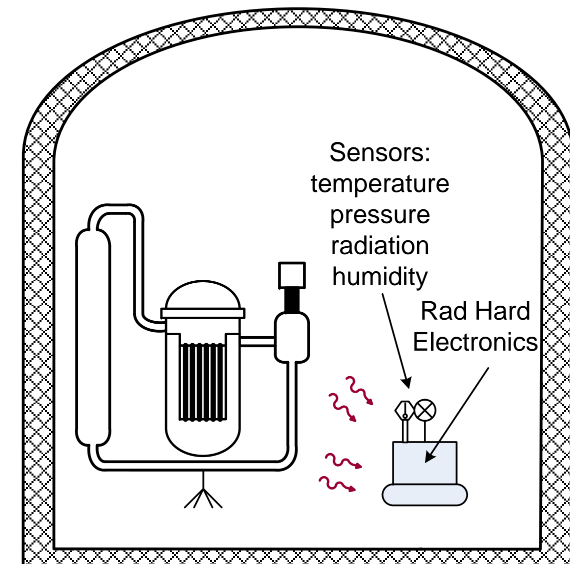
Project Overview

Goal, and Objectives

- This project seeks to increase the radiation resilience of sensitive electronics such that a robot could be employed for in-containment post-accident monitoring and sensing purposes
- This two-year project is developing both board and application-specific integrated circuit (ASIC) level radiation hard by design (RHBD) techniques for circuits destined for severe nuclear environments, specifically those that are vital to robotic circuits

Participants

- Principal Investigators:
  Keith Holbert and Larry Clark
- Graduate students:
  Yitao Chen, Anudeep Gogulamudi
- Undergraduate students:
  James Adams, Blake Anderson, Chad Farnsworth



Project Schedule

Two-year project began in mid-December 2013, and is presently at the end of month 10 of the second year

Tasks 1 and 3 are parallel to Tasks 2 and 4

- Task 1: Total ionizing dose (TID) and elevated-temperature in-situ testing of microcontroller electronics with embedded flash memory (Dec. 2013 – Dec. 2014)
- Task 3: Board-level demonstration (January – October 2015)
- Task 2: ASIC (application-specific integrated circuit) design and fabrication (July 2013 – March 2015)
- Task 4: ASIC characterization and radiation testing of microprocessor and non-volatile memory (April – December 2015)

Nuclear Energy

Accomplishments Task 1: Radiation Testing

- The total ionizing dose (TID) experiments were carried out in a Co-60 self-shielded irradiator that permits feed through of ribbon cables thereby facilitating in-situ measurements during irradiation
- Custom test and diagnostics codes were written to exercise the flash and microcontroller in order to assess the realistic performance of the devices when deployed in a radiation environment
- Although testing of the flash demonstrated operability to doses of a few hundred kilorad, the commercial off-the-shelf (COTS) 16-bit and 32-bit microcontrollers exhibited less radiation resilience than expected or desired (<100 krad)

Accomplishments
Task 1: Radiation Testing

- Radiation testing and analysis showed that marginal memory sectors can fail to erase much earlier than other sectors (each block below has 16 sectors and is 256 rows tall by 128 words wide with 16-bit words)
- The top and bottom sectors fail much sooner

□ 0x0000 ■ 0xFFFF
1→0 0→1

97.8 krad 98.8 krad 117.8 krad 118.8 krad 240 krad

U.S. DEPARTMENT OF
ENERGY

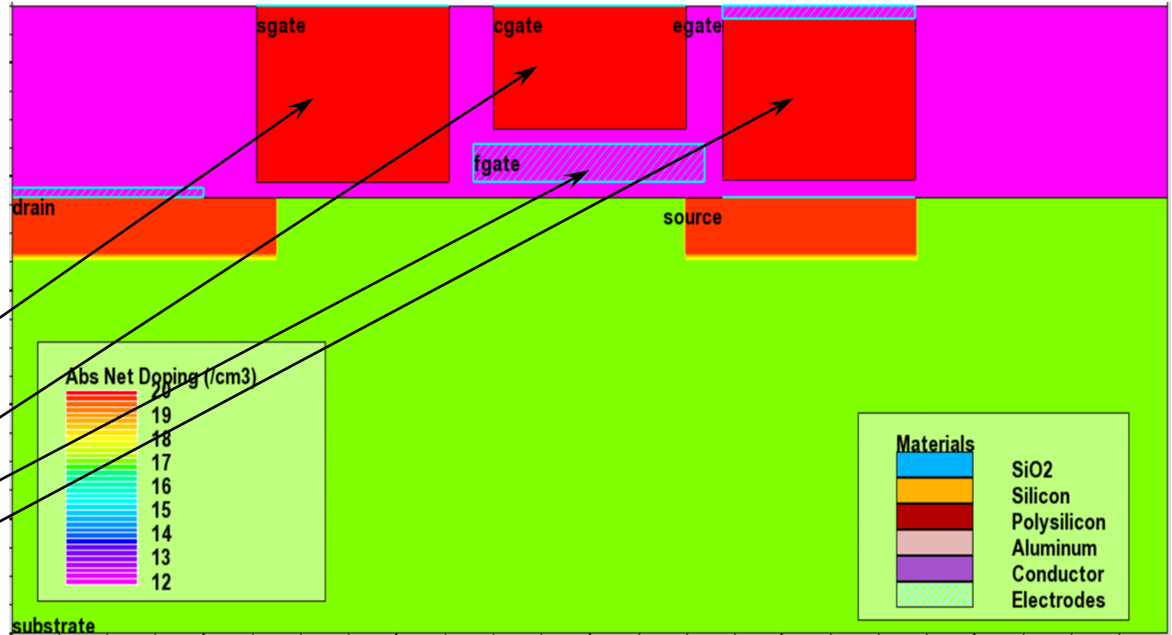
Nuclear Energy

Accomplishments Task 3: Demo Board

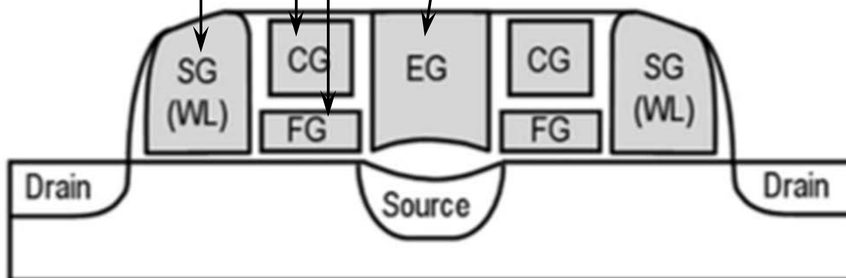
- Using the Silvaco TCAD (Technology Computer Aided Design) software tool Atlas to simulate the electrical behavior of the SST Generation III SuperFlash to better describe the radiation response of the devices
- These characterization efforts are undertaken to extend device lifetime by better understanding the eFlash limits
- The developed device model is incorporated into a circuit level simulation in order to explore mitigation strategies for the demonstration board
- The measured radiation response and some non-irradiation based electrical characterization measurements were used to ascertain device parameters for input into both the device and the circuit level simulation models

Accomplishments
Task 3: Demo Board

Third Generation SST SuperFlash Structure in Silvaco TCAD Atlas is shown right and the physical device below



- Select gate (SG)
- Coupling gate (CG)
- Floating gate (FG)
- Erase gate (EG)
- Drain (Bit line)



Three different operations must be modeled and simulated

3rd Generation

	WL (SG)	BL (Drain)	Source	EG	CG
Erase	0V	0V	0V	11V	0V
Program	1V	~2µA	4.5V	4.5V	10.5V
Read	Vcc	0.6V	0V	0V	Vcc

U.S. DEPARTMENT OF **ENERGY**

Nuclear Energy

Accomplishments
Task 3: Demo Board

ATLAS
Drain Current vs. fgate bias

Fig. 2. I_{cell} vs. FG potential (Curve A), and I_{cell} vs. erase voltage (Curve B, cumulative erase, 10 ms, 0.25 V step). Ir_1 is the cell read current in deeply erased state.

Source: Tkachev, IEEE IIRW, 2011

The TCAD device model dimensions (e.g., oxide thickness, and gate sizes) and simulation behavior are compared to published data (bottom inset)

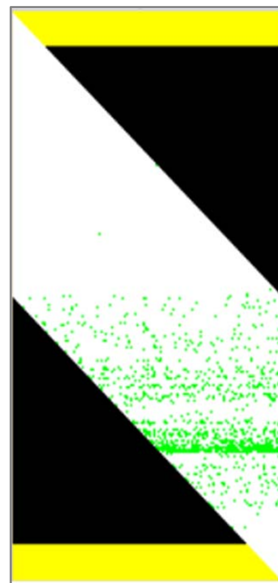
U.S. DEPARTMENT OF ENERGY

Nuclear Energy

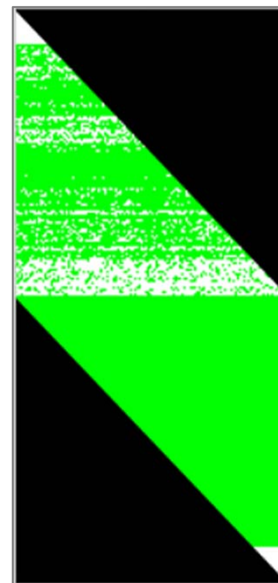
Accomplishments Task 3: Demo Board

- Additional radiation testing is carried out to determine operating mode(s) that increase lifetime of the devices in radiation field
- Below are results shown from programming diagonal regions to all zeros or all ones (left) and checkerboard (right) patterns
- Green and yellow denote failures in the words
- Testing of read-only versus erase and program usage models are performed

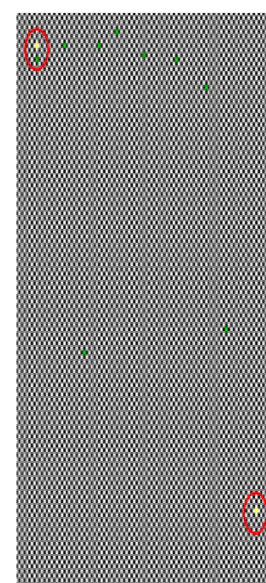
0x0000	0xFFFF
1→0	0→1



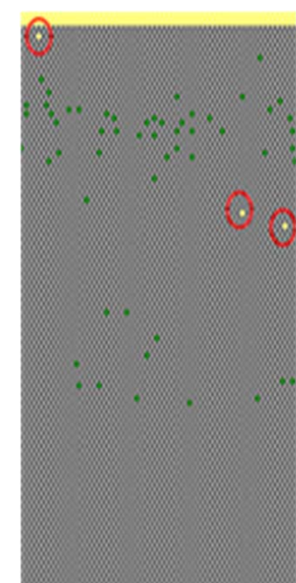
(a) 234 krad



(b) 246 krad



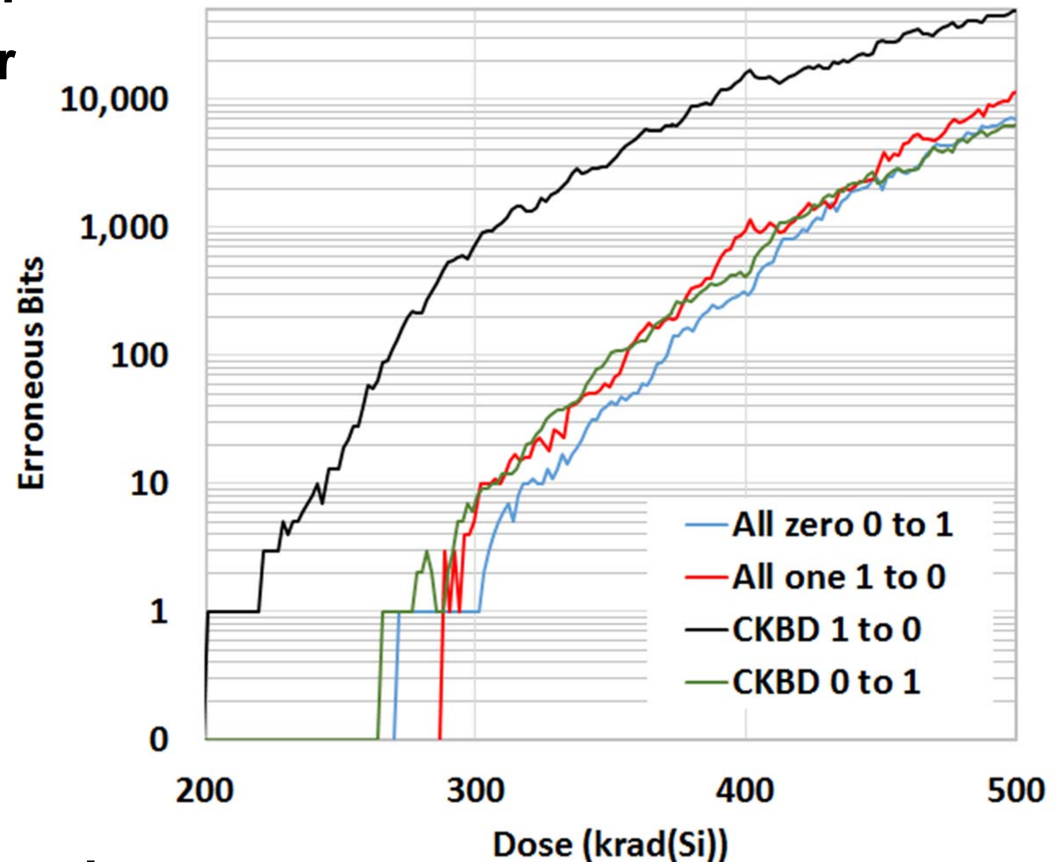
(c) 213 krad



(d) 214 krad

Accomplishments Task 3: Demo Board

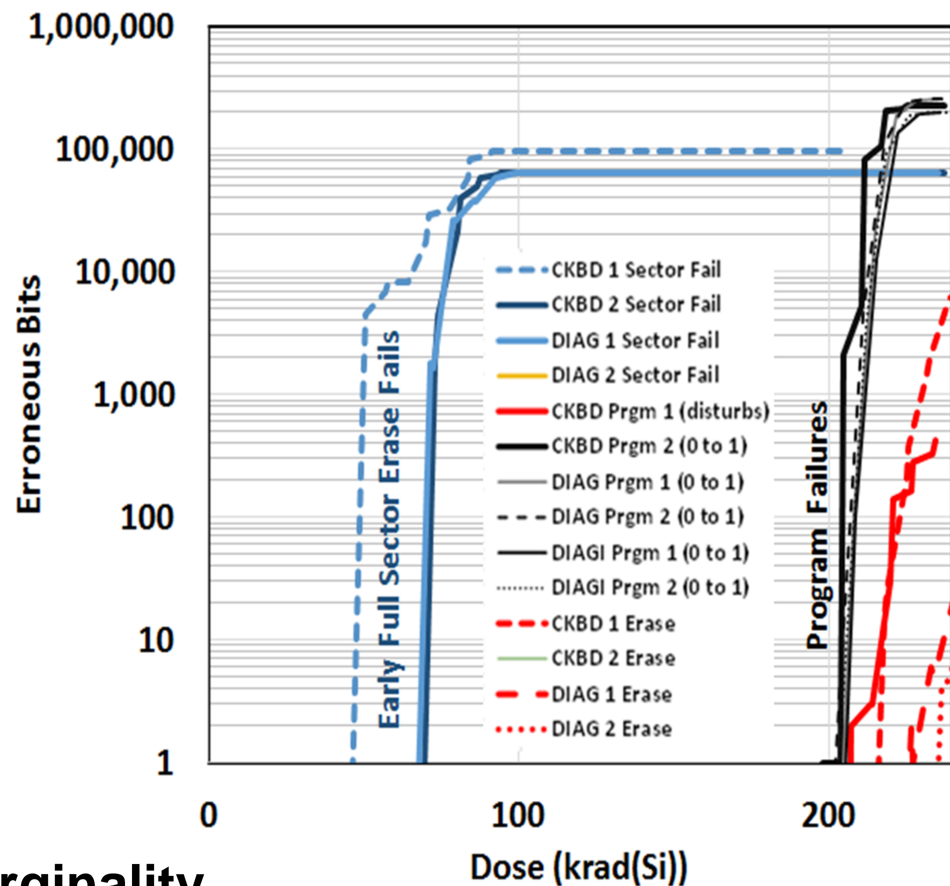
- Read only mode operation
- Earliest failures first occur at 201 krad for checker-board (CKBD) and were 1 to 0 failures
- CKBD 0 to 1 failures first occurred at 265 krad in this experiment
- Some devices were better as they were tested at lower activity factor
- All zero or all one block responses were similar
- Reads do not require high voltage which is supplied by an onboard charge pump



U.S. DEPARTMENT OF
ENERGY
Nuclear Energy

Accomplishments
Task 3: Demo Board

- Erase and program failure response of multiple 512 kilobit flash blocks at high (20x) activity factor
- When erase and program operations are performed, the radiation-induced failures occur at earlier doses, likely due to charge pump degradation
- The blue curves are those sectors which exhibit early failure, perhaps due to high voltage distribution marginality in the supporting circuitry



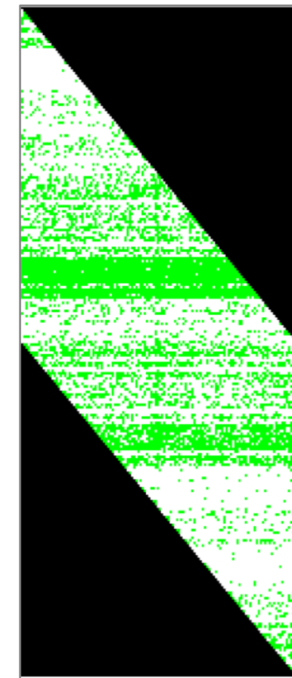
U.S. DEPARTMENT OF ENERGY

Nuclear Energy

Accomplishments Task 3: Demo Board

- To test whether the degradation of the charge pump is the source of the failure, the supply voltage V_{DD} was raised after irradiation to determine the post-TID response
- Comparison of nominal, i.e., V_{DD} = 3.3 V (left) and raised, i.e., V_{DD} = 4 V (right) operation after 263 krad
- At nominal V_{DD}, nearly every bit has failed to program (green); the upper and lower triangles are all 0's (white) since those sectors have failed to erase
- When the voltage is raised, the number of words with bits that failed to program is greatly reduced
- Raising the voltage eliminated all erase and two-thirds of the program fails post-irradiation

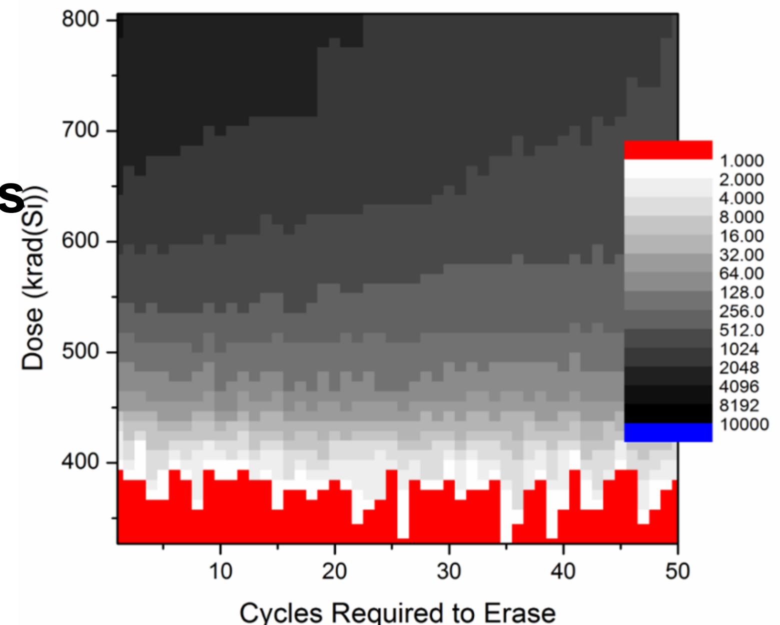
Nominal V_{DD}



Raised V_{DD}

Accomplishments Task 3: Demo Board

- Example electrical characterization
- Erase operations were interrupted to determine the relative oxide thickness
- We characterized 512k cells by the number of cycles required to erase with V_{DD} at low voltage
- At very high dose levels, i.e., above 500 krad(Si), there is a tendency for greater number of bit failures in cells that erase faster, which presumably have a thinner inter-poly tunnel oxide
- It was electrical characterization such as this which led accidentally to the discovery of a method [patent applied] for generating random numbers



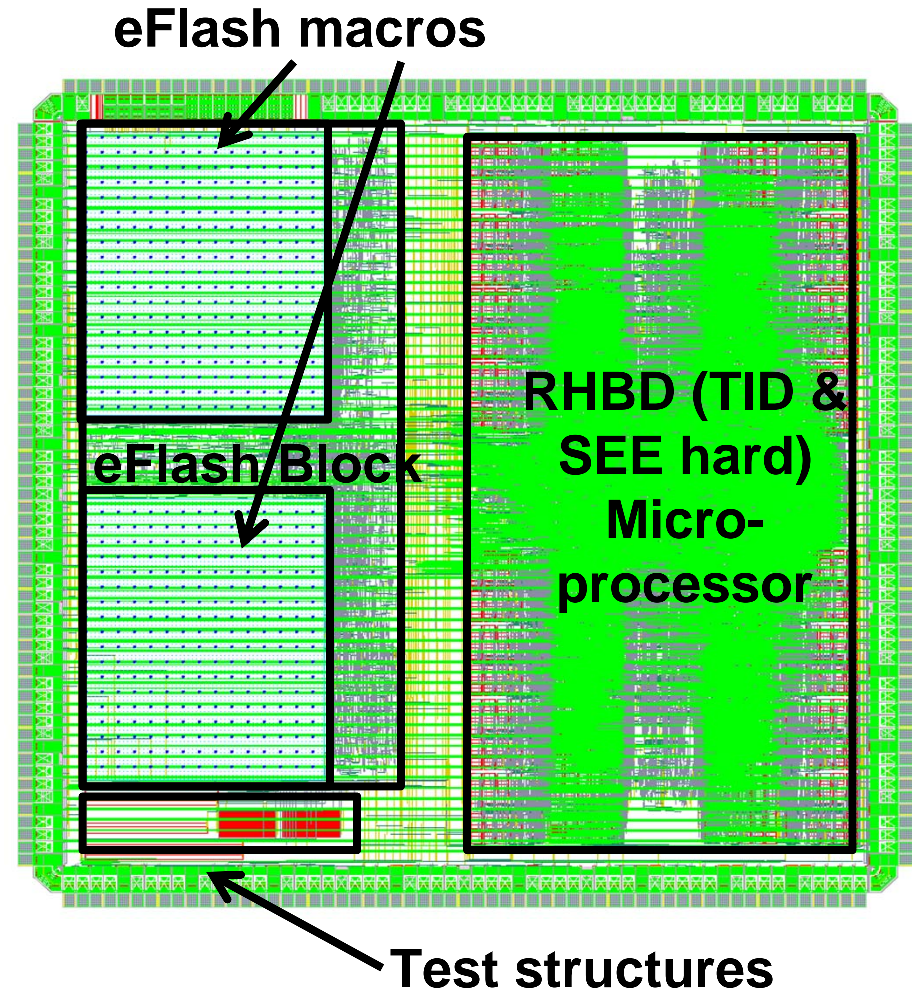
Contours showing the correlation of erase speed (proportional to tunnel oxide thickness) vs. 1 to 0 failure rate when in the read-only mode during irradiation. Red indicates no failures.

U.S. DEPARTMENT OF ENERGY

Nuclear Energy

Accomplishments
Task 2: ASIC Design & Fab.

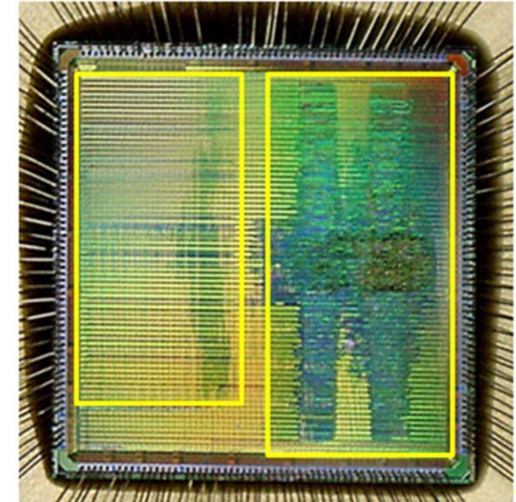
- **90-nm Test Die details 4x4 mm**
- **eFlash test chip macro details**
  - Two SST SuperFlash flash memory blocks; 3.28 M-bits per macro; 32-bit interface; 512 bytes/sector
  - 100k minimum sector endurance (erase/program cycles)
  - Rated to 100 years retention time
- **Taiwan Semiconductor Manufacturing Co.**
  - Low power process
- **This effort was co-sponsored by Space Micro**
  - Microchip Technology Inc. supported the tape-out



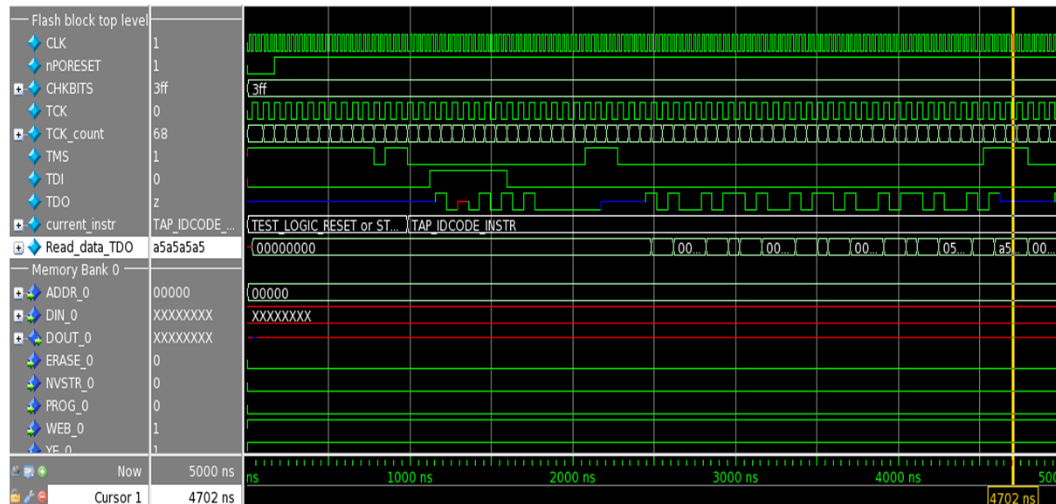
U.S. DEPARTMENT OF
ENERGY
Nuclear Energy

Accomplishments
Task 4: ASIC Packaging

- **The application-specific integrated circuit (ASIC) devices were packaged into test chips**
- **Processor is apparent at the right hand side; left is the embedded flash block**
- **Custom software was written to access the ASIC chips using JTAG constructs**



Die photomicrograph

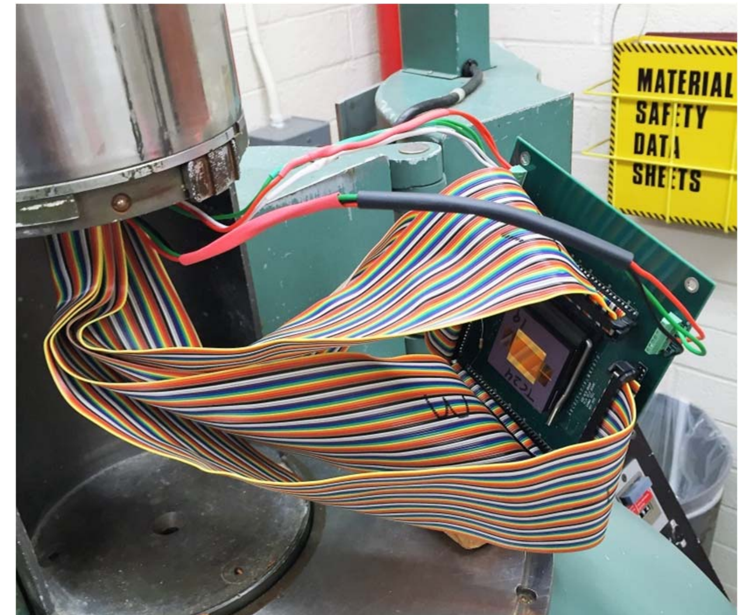


Interface to ASIC chip for programming and testing

Packaged ASIC and custom mounted

Accomplishments
Task 4: ASIC Rad Testing

- Radiation testing of the ASIC has begun
- The first experiment focused on the embedded flash as the ribbon cabling required to pass through the irradiator cable feedthrough port is limited
- Irradiated in tandem, the Hermes microprocessor was unpowered during the above experiment. After a dose of 2.5 Mrad, the processor was found to be fully functional. Dedicated micro-processor testing upcoming.
- This radiation hardness by design was expected, and one of the reasons that we have emphasized the eFlash studies in this project



Accomplishments

Public Dissemination

- Provided article for February 2015 Advanced Sensors and Instrumentation (ASI) newsletter
- Presentation of a paper entitled, “Rad hardening commercial-off-the-shelf microcontrollers destined for I&C applications in severe nuclear environments,” at the American Nuclear Society *Nuclear Plant Instrumentation, Control & Human-Machine Interface Technologies* (NPIC&HMIT) conference in Charlotte in February 2015
- Presentation at the IEEE *Nuclear and Space Radiation Effects Conference* (NSREC) in Boston in July 2015
- Acceptance of a journal paper entitled, “Evaluation of 1.5-T cell flash memory total ionizing dose response,” for publication in the *IEEE Transactions on Nuclear Science* (to appear Dec. 2015)
- Filing of a provisional U.S. patent in Sept. 2015 for “Secure True Random Number Generation Using 1.5-T Transistor Flash Memory” (application number 62/232,736)

Technology Impact

- The methods being developed in this work will facilitate the long-term viability of radiation-hard electronics and robotic systems, thereby avoiding obsolescence issues
- We are determining (physics based) specific failure mechanisms for eFlash arrays (prior work has been behavior based)
- We have correlated the mechanisms between temperature and radiation effects (both of which involve leakage)
- Determining limits to the technology and understanding the exact mechanisms allows better determination of the value of different system level mitigation approaches
- This technology not only has applicability to severe accident conditions but also to facilities throughout the nuclear fuel cycle in which radiation tolerance is required

Conclusions

- Ionizing radiation is intrinsic to the entire nuclear energy fuel cycle. The pervasive use of electronic systems demands devices that can withstand significant radiation exposure. The nuclear power industry needs to be able to benefit from the advancements in the semiconductor industry which have led to low-cost ubiquitous devices.
- This project is contributing to the deployment of state-of-the-art electronics that can improve the reliability, sustain the safety, and extend the life of current reactors. These results are also applicable to next generation reactors.
- The full station blackout experience at Fukushima shows the necessity for emergency sensing capabilities in a radiation-enhanced environment. This project serves to develop radiation-hard-by-design (RHBD) electronics.