Advanced Power Electronics and Electric Motors Program

2013

VEHICLE TECHNOLOGIES OFFICE

FY 2013

Annual Progress Report
for the Advanced Power Electronics
and Electric Motors Program

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Submitted to:

Energy Efficiency and Renewable Energy
Vehicle Technologies Office

December 2013

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ACRONYMS AND ABBREVIATIONS

3D	three dimensional
ac	alternating current
ACB	active current balancing
AEV	all electric vehicle
AGD	active gate driver
Al	aluminum
Alnico	(Al-Ni-Co-Fe; family of iron alloys)
ANL	Argonne National Laboratory
APEEM	Advanced Power Electronics and Electric Motors (program, DOE)
APEEM	Advanced Power Electronics and Electric Machinery (subprogram, ORNL)
AWG	American wire gauge
bemf	back electromotive force
BREM	Beyond Rare Earth Magnets
CAN	controller area network
CBC	current balancing controller
CDS	Combined Driving Schedule
CFD	computational fluid dynamics
CGD	conventional gate driver
CMOS	complementary metal-oxide semiconductor
CMR	common mode rejection
CT	current transducer
Cu	copper
CVD	chemical vapor deposition
DBC	direct bond copper
dc	direct current
DCR	dc resistance
DCT	differential current transformer
DOE	US Department of Energy
DSP	digital signal processing/processor
Dy	dysprosium
eGaN	enhancement mode gallium nitride
EM	electric machine
EMC	epoxy molding compound
EMI	electromagnetic interference
emf	electromotive force
EPA	Environmental Protection Agency
EPC	Efficient Power Conversion

ESR	equivalent series resistance
EV	electric vehicle
FEA	finite element analysis
FET	field effect transistor
FUL	fault under load
GaN	gallium nitride
GIR	gate impedance regulation
GPM	gallons per minute
GVC	gate voltage control
HEMT	high electron mobility transfer
HEV	hybrid electric vehicle
HIL	hardware in loop
HSF	hard switching fault
HSG	hybrid starter-generator
HV	high voltage
HWFET	Highway Fuel Economy Test
IC	integrated circuit
IGBT	insulated gate bipolar transistor
IM	induction motor/machine
IPM	interior permanent magnet
IR	insulation resistance
IR	International Rectifier
JBS	junction barrier Schottky
JFE	JFE Steel Corporation
JFET	junction field-effect transistor
K	thermal conductivity
K	degrees Kelvin
LA92	Los Angles 92 drive cycle
M/G	motor/generator
MIFP	multiple isolated flux path
MOSFET	metal oxide semiconductor field-effect transistor
Nd	neodymium
NREL	National Renewable Energy Laboratory (DOE)
OBC	onboard charger
OD	outer diameter
OEM	original equipment manufacturer
ORNL	Oak Ridge National Laboratory
PCB	printed circuit board
PCU	power converter unit

PD	power density (peak)
PE	power electronics
PEV	plug-in electric vehicle
PF	power factor
PFC	power factor correction
PM	permanent magnet
PSAT	Powertrain Systems Analysis Toolkit
PSIM	Powersim (circuit simulation software)
PWM	pulse width modulated/modulation
PwrSoC	power supply on chip
R&D	research and development
RC	resistor-capacitor
RL	inductor-resistor
RE	rare earth
RESS	regenerative energy storage system
rms	root mean square
SBD	Schottky barrier diode
SCC	switched capacitor converter
Si	silicon
SiC	silicon carbide
SJT	super junction transistor
SOA	state of the art
SOC	state of charge
SOI	silicon-on-insulator
SP	specific power
SPM	surface permanent magnet
SRM	switched reluctance motor
SSCB	solid state circuit breaker
TC	thermal conductivity
TDS	traction drive system
THD	total harmonic distortion
UC	ultracapacitor
U.S. DRIVE	Driving Research and Innovation for Vehicle efficiency and Energy sustainability (cooperative research effort between DOE and industry partners)
UDDS	Urban Dynamometer Driving Schedule
Vac	volts of alternating current
Vce	voltage across collector and emitter
Vdc	volts of direct current (operating voltage)
VGD	variable gate delay

VSATT	Vehicle Systems Analysis Technical Team
VSI	voltage source inverter
VTO	Vehicle Technologies Office (DOE)
WBG	wide bandgap
ZS	zero sequence

I. INTRODUCTION

I.0 Introduction

The U.S. Department of Energy (DOE) announced in May 2011 a new cooperative research effort comprising DOE, the U.S. Council for Automotive Research (composed of automakers Ford Motor Company, General Motors Company, and Chrysler Group), Tesla Motors, and representatives of the electric utility and petroleum industries. Known as U.S. DRIVE (Driving Research and Innovation for Vehicle efficiency and Energy sustainability), it represents DOE's commitment to developing public–private partnerships to fund high-risk–high-reward research into advanced automotive technologies. The new partnership replaces and builds upon the partnership known as FreedomCAR (derived from "Freedom" and "Cooperative Automotive Research") that ran from 2002 through 2010 and the Partnership for a New Generation of Vehicles initiative that ran from 1993 through 2001.

The Advanced Power Electronics and Electric Motors (APEEM) technology area within the DOE Vehicle Technologies Office (VTO) provides support and guidance for many cutting-edge automotive technologies now under development. Research is focused on developing revolutionary new power electronics (PE), electric motor, and traction drive system (TDS) technologies that will leapfrog current on-the-road technologies, leading to lower cost and better efficiency in transforming battery energy to useful work. The research and development (R&D) is also aimed at achieving a greater understanding of and improvements in the way the various new components of tomorrow's automobiles will function as a unified system to improve fuel efficiency through research in more efficient TDSs.

In supporting the development of advanced vehicle propulsion systems, the APEEM subprogram fosters the development of technologies that will significantly improve efficiency, costs, and fuel economy.

The APEEM subprogram supports the efforts of the U.S. DRIVE partnership through a three-phase approach intended to

- Identify overall propulsion- and vehicle-related needs by analyzing programmatic goals and reviewing industry recommendations and requirements, and then develop, and deliver the appropriate technical targets for systems, subsystems, and component R&D activities.

- Develop, test, and validate individual subsystems and components, including electric motors and PE.

- Estimate how well the components and subsystems work together in a vehicle environment or as a complete propulsion system and whether the efficiency and performance targets at the vehicle level have been achieved.

The research performed under this subprogram addresses the technical and cost barriers that currently inhibit the introduction of advanced propulsion technologies into hybrid electric vehicles (HEVs), plug-in HEVs (PEVs), all-electric vehicles (AEVs), and fuel-cell-powered automobiles that meet the goals set by U.S. DRIVE.

A key element in making these advanced vehicles practical is providing an affordable electric TDS. This will require attaining weight, volume, efficiency, and cost targets for the PE and electric motor subsystems of the TDS. Areas of development include

- Novel traction motor designs that result in increased power density and lower cost

- Inverter technologies that incorporate advanced semiconductor devices to achieve higher efficiency while accommodating higher-temperature environments and delivering higher reliability

- Converter concepts that leverage higher-switching-frequency semiconductors, nanocomposite magnetics, higher-temperature capacitors, and novel packaging techniques that integrate more functionality into reduced size, weight, and cost applications

- New onboard battery charging electronics that build from advances in converter architectures for decreased cost and size

- More compact and higher performing thermal controls achieved through novel thermal materials and innovative packaging technologies

- Integrated motor-inverter TDS architectures that optimize technical strengths of the underlying PE and electric machine subsystems.

DOE's continuing R&D into advanced vehicle technologies supports the administration's goal to produce a five-passenger affordable AEV with a payback of less than five years and sufficient range and fast charging capability to enable average Americans everywhere to meet their daily transportation needs more conveniently and at lower cost by the year 2022.

I.1. The *EV Everywhere* Grand Challenge

Background

In March 2012, President Obama announced the *EV Everywhere* Grand Challenge—to produce plug-in electric vehicles (PEVs) as affordable and convenient for the American family as gasoline-powered vehicles by 2022. Realizing the promise of PEVs is one of the grand challenges of this era. Today, our transportation system is still dependent on internal combustion engines and oil. In fact, 93% of our transportation fuel is derived from petroleum and much of this is imported. PEVs can decouple personal mobility from oil, cut pollution and help build a 21st Century American automotive industry that will lead the world.

America is the world's leading market for electric vehicles and is producing some of the most advanced PEVs available today. Consumer excitement and interest in PEVs is growing—in 2012, PEV sales in the U.S. tripled, with more than 50,000 cars sold, and a plug-in electric vehicle (the Chevrolet Volt) beat all other vehicle models in Consumer Reports' owner satisfaction survey for the second time. In 2013, PEV sales are on pace to nearly double prior year sales, with nearly 100,000 annual sales of PEVs projected.

PEVs have won critical acclaim with awards such as 2011 World Car of the Year (Nissan Leaf), 2013 Motor Trend Car of the Year (Tesla Model S) and 2012 Green Car Vision Award Winner (Ford C-MAX Energi). To maintain this leadership, strong growth in the U.S. PEV sector will need to continue.

The Department of Energy (DOE) developed an *EV Everywhere* "Blueprint" document that provides an outline for technical and deployment goals for PEVs over the next five years

[http://www1.eere.energy.gov/vehiclesandfuels/electric_vehicles/pdfs/eveverywhere_blueprint.pdf].

DOE will pursue these targets in cooperation with a host of public and private partners. The technical targets for the DOE PEV program fall into four areas: battery R&D; electric drive system R&D; vehicle lightweighting; and advanced climate control technologies. Some specific goals include:

- Cutting battery costs from their current $500/kWh to $125/kWh
- Reducing the cost of electric drive systems from $30/kW to $8/kW
- Eliminating almost 30% of vehicle weight through lightweighting.

These numbers represent difficult to reach "stretch goals" established in consultation with stakeholders across the industry—including the *EV Everywhere* workshops held during the summer and fall of 2012. When these goals are met, the levelized cost of an all-electric vehicle with a 280-mile range will be comparable to that of an ICE vehicle of similar size.

Even before these ambitious goals are met, the levelized cost of most plug-in hybrid electric vehicles—and of all-electric vehicles with shorter ranges (such as 100 miles)—will be comparable to the levelized cost of ICE vehicles of similar size. Meeting these targets will help to reduce the purchase price for plug-in electric vehicles

The *EV Everywhere* Blueprint document also describes the deployment programs related to charging infrastructure and consumer education. Efforts to promote home, workplace, and public charging can also help speed PEV deployment.

EV Everywhere Technical Targets

DOE defined *EV Everywhere* technology targets using an analytical framework that evaluated the performance of component technologies as well as vehicle cost and performance. We synthesized data about future vehicle potential by using expert projections of component technology to create virtual vehicles of the future via computer modeling and simulation. The range of vehicle costs and efficiencies made possible a comparison of the degree to which the portfolio of these technologies must progress, in both performance and cost terms, to yield PEVs that are cost-competitive, as measured by the initial vehicle purchase price and the fuel expenditure accrued over a 5-year ownership period. Ultimately, an analysis of this balance yielded technical targets at the technology progress frontier: *EV Everywhere* targets are consistent with what experts see as very aggressive but still possible within the *EV Everywhere* timeframe.

The complete set of *EV Everywhere* technical targets are presented in the Blueprint document. The specific technical targets that pertain to electric drive systems are as follows:

Electric Drive System 2022 Targets

		Current Status	Target
System Cost	$/kW	30	8
Specific Power	kW/kg	1.1	1.4
Power Density	kW/L	2.6	4.0
Peak Efficiency	%	90	94

Vehicle Charging 2022 Targets

		Current Status	Target
Charger Cost	$/kW	150	35

2013 Highlights

1. Inverter Meets DOE 2015 Goals

Developed, tested, and demonstrated an inverter (55 kW peak) that meets the DOE 2015 cost, weight, and volume targets when manufactured in quantities of 100,000 units/year, and operates in a higher temperature environment.

Delphi Automotive Systems, LLC (Delphi)

Delphi's High Temperature Inverter with integrated controller achieved DOE Advanced Power Electronics and Electric Motors (APEEM) 2015 R&D targets. Support tasks from industry partners and national laboratories included: power semiconductor development and characterization, capacitor development and testing, power device packaging, system modeling, thermal and heat exchanger experiments, interface material characterization, and inverter system testing.

Technology innovations developed during this project (low-loss world-class semiconductors and packaging, thermal stack-up and materials, and inverter level packaging concepts) have been incorporated in an inverter planned for production in mid-2015 (Figure I-1).

Figure I-1:Delphi prototype production inverter incorporating DOE inverter innovations.

Delphi's solution is also scalable across the range of 55 kW to 120 kW peak through the use of different die sizes and thermal materials. The Delphi/DOE inverter demonstrated its capability to operate with a standard 105°C coolant system in a 140°C ambient environment to eliminate the separate cooling loop typically required for today's inverters.

A primary enabler for the inverter's higher temperature capability was a dc-link capacitor developed by General Electric (GE), using polyetherimide (PEI) film as the dielectric. The newly developed PEI film has a permittivity that is 50% better than the polypropylene (PP) film used in today's dc-link capacitors and is also capable of 200°C operation vs. PP's 85°C. Additionally, a roadmap was created to show a path to a smaller, lighter, lower cost PEI capacitor (Figure I-2). Delphi also teamed with Argonne National Laboratory to develop a Lead Lanthanum Zirconium Titanate (PLZT) ceramic capacitor. The resulting sol-gel version of this capacitor exhibited benign failure, a very high permittivity, ε_r >64 (~30X greater than today's baseline PP capacitor) and relatively high breakdown voltage, >140 V/μm. The team identified low cost solutions for producing a high-temperature capable PLZT

capacitor-90% smaller than today's baseline PP dc-link capacitor.
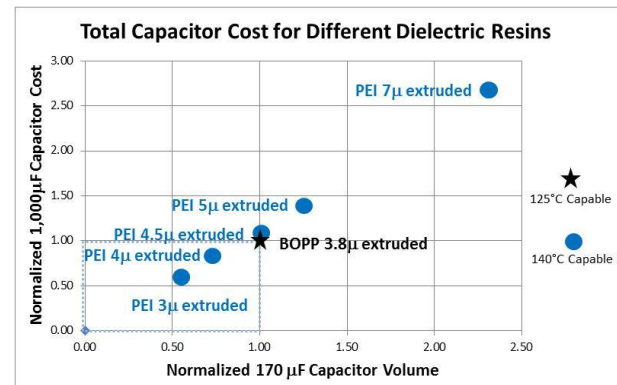
Figure I-2: Roadmap to a lower cost, smaller dc-link capacitor with high temperature capability.

Key to the project's success was Delphi's development of a silicon (Si) dual-side cooled power device package which involved collaboration with the National Renewable Energy Laboratory on thermal modeling and characterization. Delphi also worked with Dow Corning to develop a wide bandgap (WBG) power semiconductor platform and determined that cost parity with Si occurs when WBG current density reaches twice that of Si. Simulations from Oak Ridge National Laboratory showed that WBG (vs. Si) devices can significantly reduce losses.

2. Integrated Heat Exchanger for Power Electronics

An advanced integrated heat exchanger was developed with thermal performance improvements leading to smaller, lighter, and lower-cost power electronics.

National Renewable Energy Laboratory (NREL)

NREL developed and patented a novel heat exchanger integrated with the power semiconductor package for cooling the power electronics module. As shown in Figure I-3, the power silicon, thermal management and housing account for almost half of the inverter cost. As compared to a high-performance commercial baseline (Lexus LS 600h inverter), the developed heat exchanger prototype (Figure I-4b) doubles the heat rejection capability per silicon area. The result is increased power per silicon area, resulting in reduced cost per inverter power. The improved power capability enables inverter system cost reductions of 8%.

Synthesis Partners LLC., July 2011
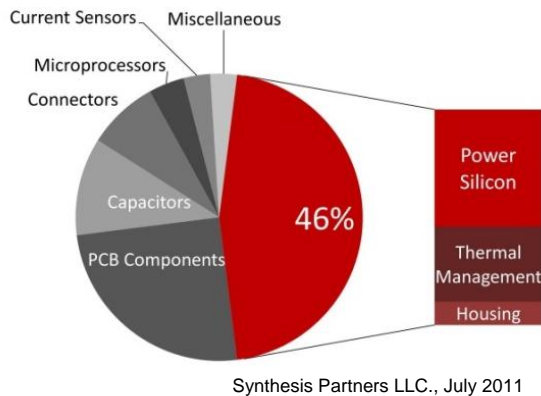
Figure I-3: Inverter cost drivers (Synthesis Partners LLC).

(a)

(b)
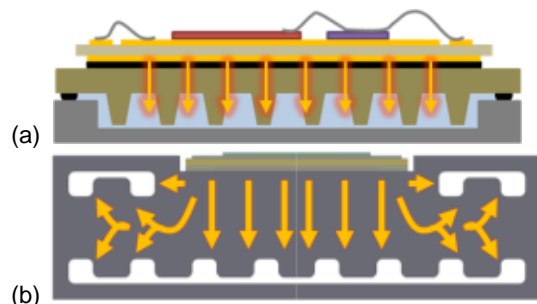
Figure I-4: (a) Conventional 1-D cooling; (b) Prototype heat exchanger showing multiple heat transfer paths.

The concept optimizes the passive and active heat transfer paths to increase the die heat rejection capability. Unlike conventional cooling approaches dominated by one-dimensional (1-D) heat transfer (Figure I-4a), the new design incorporates multiple heat transfer paths to enhance cooling (Figure I-4b), while enabling less aggressive and lower-cost cooling technologies. An extruded aluminum design was built in close collaboration with industry partner (Sapa Extrusions North America) and tested using water-ethylene glycol (WEG) coolant. The open channels (Figure I-4b) reduced the number

of internal voids resulting in a 25% tooling cost reduction. As compared to castings, which are typically used, extrusions have lower initial tooling cost. By enabling use of alloys with 36% higher thermal conductivity, extrusions also yield better thermal performance than castings. The design approach enables use of less effective coolants (air, transmission fluid) which would allow integrating the power electronics cooling with other vehicle systems, thereby eliminating a separate WEG coolant loop.

Future work will involve implementation of this concept in a power module/inverter in collaboration with industry partners. The concept will also enable future wide-bandgap packaging configurations. Improving power capability and reducing automotive power electronics costs will significantly contribute to making electric-drive vehicles more affordable.

3. Improved DC Bus Capacitors Using Glass Dielectrics

DC Bus capacitors are currently made from polypropylene which is fundamentally limited in high temperature performance. Commercial flat panel display glass is a large-scale material that has the potential to replace polypropylene for high temperature and high ripple current DC bus capacitors.

Pennsylvania State University

Current DC capacitors, made from polypropylene, do not have the high temperature performance required for use in future electric drive vehicle systems. However, glass is a high-temperature, high dielectric constant material and can be incorporated into a capacitor. Thin glass sheet production has grown substantially with strong demand from the flat panel display industry, and a large investment in the development of new glass fabrication methods. Glass manufacturers have been able to develop a continuous sheet casting process that creates significant lengths of thin flexible sheet. This enabled Penn State to prototype glass capacitors assembled in a similar manner to current polymer film capacitors, demonstrating that flat panel display glass is a viable material for high temperature DC bus capacitors used in electric drive vehicles.

High Temperature Capacitor Reliability Testing: Flat panel display glass has shown stable capacitance and low loss values up to temperatures of 140C and is a promising material for DC bus capacitors (Figure I-5); however, the long-term material reliability is unproven. A series of electrical tests has demonstrated that the materials can withstand high voltage and temperature operation conditions for the life of the vehicle. Figure I-6 shows the characterization of life through a test chamber at 400ºC and overall life prediction relative to the 13,000 hour DOE target using this data.
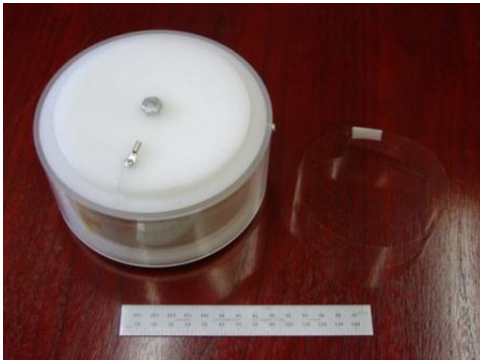
Figure I-5: Coiled glass capacitor fabricated and tested at Penn State using NEG 50 μm thick glass ribbon.
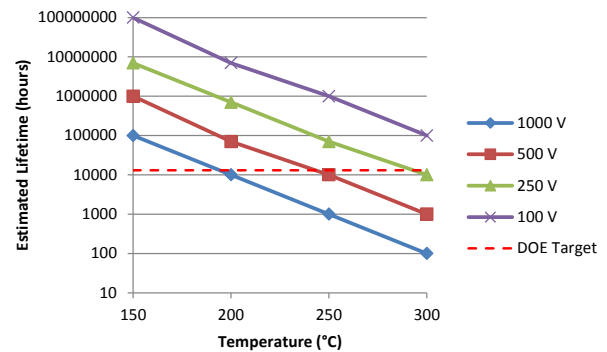
Figure I-6: Reliability testing at high temperature is used to predict performance for DC Bus capacitors in electric drive vehicles.

High Temperature Capacitor Performance Testing: Further testing of glass capacitors under high frequencies and at high temperatures has also yielded positive results. At 150°C and 10 kHz frequency, losses were measured an order of magnitude below DOE targets for DC bus capacitors, and remained low across a representative temperature and frequency range. Since typical polypropylene capacitors are limited to 125°C operation, these glass capacitors could also be used alongside wide bandgap semiconductors. This prototype capacitor fabrication and positive test results confirm the validity of flat panel display glass as a potential substitute for polypropylene in electric drive vehicle systems. The combination of new glass manufacturing methods and materials for the display industry has led to the promise for new applications such as in electric-drive vehicles.

4. 10 kW WBG Device-Based Inverter

Emerging WBG semiconductors offer opportunities for system level cost reduction, higher power density, temperature, and frequency operation as well as efficiency and reliability improvements.

Oak Ridge National Laboratory

Power electronics systems on hybrids, plug-in hybrids and all-electric vehicles impose harsh environmental requirements on electrical componentry. High operational temperatures necessitate costly thermal management systems to avoid device failures. Increasing cost pressures are demanding minimization of hardware which in turn benefits the vehicle's efficiency through weight reduction.

Emerging wide bandgap (WBG) devices are poised to offer significant improvements in power electronics. Their ability to operate with enhanced efficiency over higher temperatures and operational frequencies reduce cooling requirements as well as minimize passive component requirements providing opportunities for revolutionary strides in electronics. The characteristics of silicon carbide (SiC) and gallium nitride (GaN) are enablers for smaller, more efficient, and robust power electronics in a multitude of clean energy applications.

Third party analysis of WBG devices from multiple vendors contributed to ORNL's objective to develop a 10 kW, all-SiC inverter using commercially available 1,200 v, 100 A, SiC MOSFET modules (Figure I-7). The layout of the inverter is shown in Figure I-8.

Figure I-7: Commercial 1,200 V, 100 A, SiC module.
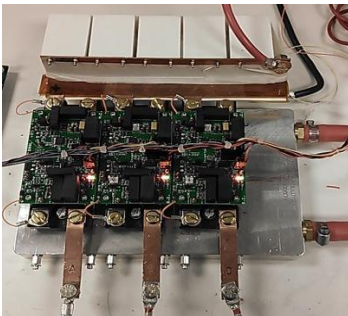
Figure I-8: 10-kW SiC inverter prototype.

The total inverter volume is (226mmx224mmx73mm) 3.6 L. Commercially available gate drivers from Rohm were used in the inverter. The gate driver is equipped with galvanic isolation up to 3,000 vrms and features integrated over current protection, undervoltage lockout, and temperature feedback. The modules are mounted on to a commercial heat sink with thermal grease as the heat transfer medium from the lower side of the power modules. This prototype model will be packaged as shown in Figure I-9 so that controls and

capacitors are packaged closely to the heat sink. The capacitors used in this design are smaller individual capacitors (not brick type) in series to ensure better cooling and reduced costs.
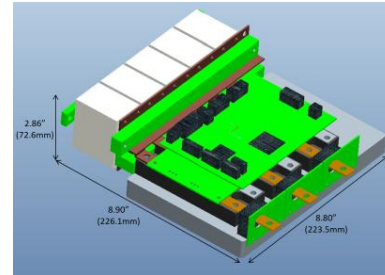
Figure I-9. Layout of ORNL 10 kW SiC inverter package.

The efficiency versus output-power plot at 325 V dc, 4 kHz switching, and 60° C coolant with a 1.5 gpm flow rate is shown in Figure I-10. Figure I-11 shows that the inverter efficiency does not change much as the switching frequency increases. The overall inverter efficiency is ~98% for different operating conditions. These inverter test results will also be used as a benchmark for the development of the next generation inverter that will be built using an ORNL-developed WBG package. The results indicate that if the inverter is scaled to 30 kW it will meet the 2020 inverter targets and that WBG technology will aid in the achievement of U.S. DRIVE targets for volume, efficiency, power density and system costs.
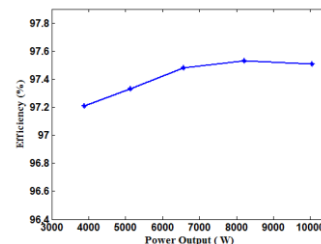
Figure I-10: Inverter efficiency vs output power.
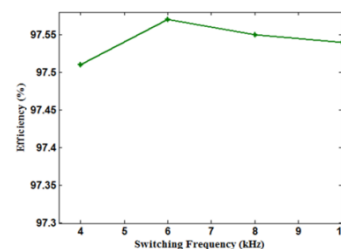
Figure I-11: Inverter efficiency vs switching frequency.

5. Thermoplastics Show Excellent Reliability for Power Electronics Packaging

Thermomechanical reliability characterization for power electronics substrate-to-base plate bonded interface materials (BIMs) showed that high-thermal performance thermoplastic BIMs have the potential for meeting the 15-year automotive life requirements.

National Renewable Energy Laboratory (NREL)

In automotive power electronics packaging, there is an industry trend towards high thermal performance bonded interfaces at the die and substrate attach layers. However, the reliability of emerging interface materials has not been proven for substrate-to-base plate (see Figure I-12) attachments. NREL, in collaboration with industry partners Btechcorp and Semikron, completed a thermomechanical reliability characterization and analysis for BIMs based on thermoplastic/polyamide adhesive with embedded near-vertical aligned carbon fibers, sintered silver, and solder as a baseline. This rigorous characterization showed that thermoplastics have superior reliability than solder and sintered silver for substrate-to-base plate attachment for power electronics in electric-drive vehicle applications (less than 175°C junction temperature). Thermoplastics-based BIMs also provide efficient pathways for heat removal in the package.
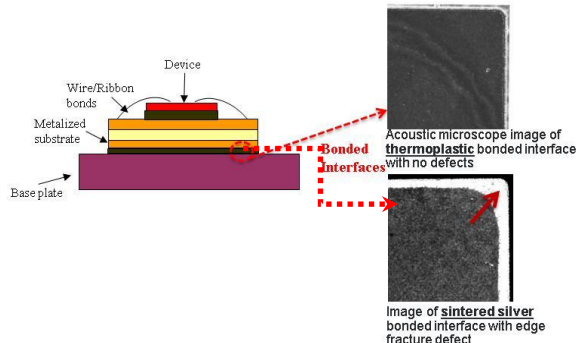
Figure I-12: Cross-section of package (left); Condition of bonded interfaces after 2,000 cycles (right).

Substrate-to-base plate bonded samples (50 mm X 50 mm footprint) were cycled between -40°C and 150°C. The ramp rate was 5°C/min with dwell times of 10 minutes at the maximum and minimum temperatures. Any degradation in the bonded sample was checked via acoustic microscopy every 100 cycles. Figure I-12 shows the microscopy images of the bonded interface after 2,000 cycles. The BIM thermomechanical modeling has shown highest strain energy density per cycle at the perimeter, which is the reason for perimeter defect initiation and propagation. Btech thermoplastic samples underwent 2,500 temperature cycles, and no defects were observed. Figure I-13 also illustrates that sintered silver is more reliable than solder. Sintered silver is on cost parity with solder, while Btechcorp is continuing work to further reduce the cost of thermoplastics to bring them on par with solder/sintered silver.
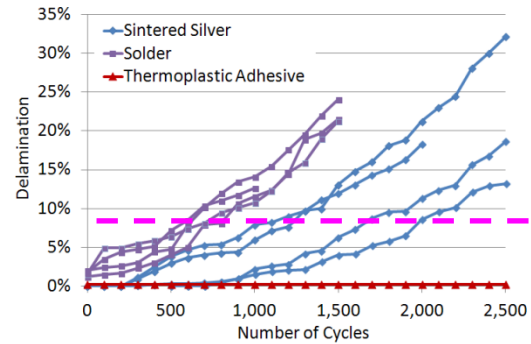
Figure I-13: Delamination percentage of initial bonded area for the tested materials. The dashed line shows a common definition of package failure (~20% delamination).

In collaboration with partners, future work with sintered silver material will focus on minimizing defects by optimizing processing conditions. The work will support future power electronics designs using wide-bandgap devices for higher temperature operation (>200°C). Improved reliability of automotive power electronics will contribute to cost reduction and wider market penetration of electric-drive vehicles.

6. Transmission Oil Jets for Motor Thermal Management

Rigorous characterization of thermal performance of transmission oil jets provided useful information for motor designers

National Renewable Energy Laboratory

NREL completed initial heat transfer experiments to characterize the thermal performance of automatic transmission fluid (ATF) jets impinging of target surfaces representing motor end windings. The tests were performed with Mercon LV ATF, and over multiple fluid temperatures, jet velocities, and targets surfaces representative of wire bundles in electric machines.

Figure I-14a and Figure I-14b show images of the ATF jet impingement with and without the fluid deflection or splashing caused by the wire bundle surface features. The fluid deflection is associated with the fluid being deflected off the surface by the samples' round, protruding features. Evidence of this splashing effect is indicated by a plateau in the heat transfer coefficient curves at higher jet velocities as seen in Figure I-14c. Because the fluid splatter was more prevalent at higher temperatures, we speculate that the lower ATF viscosities at higher temperatures are more conducive to this splattering effect. This effect reduced the fluid available for heat removal and thus reduced heat transfer coefficients. This phenomenon was more pronounced with the samples that had the larger surface features.

Cooling of electric motors with ATF is a common and practical method of cooling motors housed within a vehicle's transmission or transaxle. There is currently minimal public information regarding the jet impingement performance of ATF. The experimental ATF heat transfer coefficient results provided in this report are a useful resource for engineers designing ATF-based motor cooling systems. Moreover, results from this study may also be applicable to potential ATF cooling strategies for automotive power electronics components to support situations where the power electronics are integrated with the electric motor. Industry partners have expressed strong interests in the results of this work which confirms the relevance of this research.

Photo Credit: Jana Jeffers, NREL

a

Photo Credit: Jana Jeffers, NREL
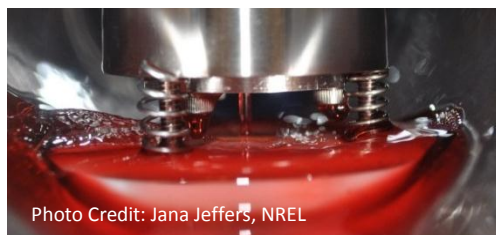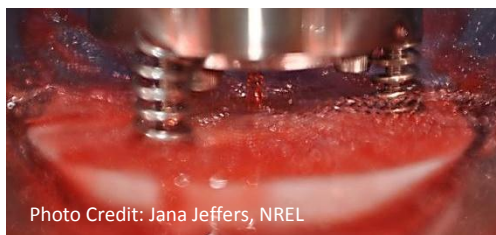
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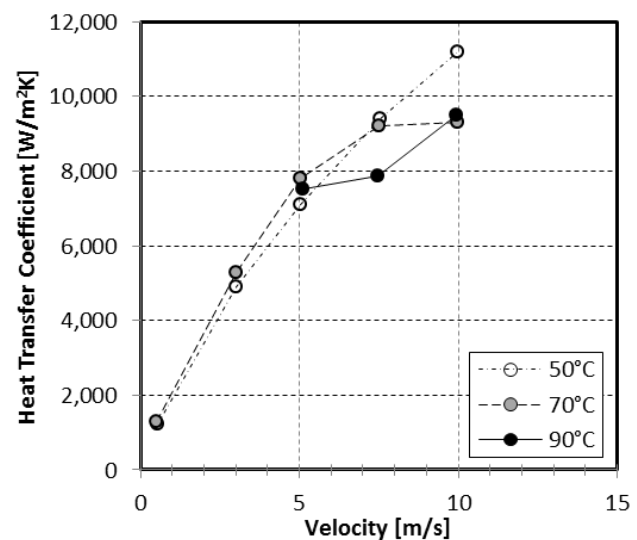
c

Figure I-14. a) ATF flowing over target surface without splashing effects. b) ATF deflecting off target surface at higher temperatures and flow rates. c) Heat transfer coefficients of 18 American Wire Gauge (AWG) sample for all inlet temperatures.

7. Passive Two-Phase Cooling System for Automotive Power Electronics

Passive two-phase cooling shows potential for improving thermal performance by over 50% over conventional cooling approaches

National Renewable Energy Laboratory

NREL has designed a proof-of-concept, inverter-scale passive two-phase cooling system for automotive power electronics. A simple schematic of the system is provided in Figure I-15a. The two-phase approach provides high heat transfer rates while the passive nature of the cooling system makes it a highly efficient mode of cooling. Experiments have demonstrated that the system can dissipate automotive heat loads (3.5 kW) under steady-state operation with small refrigerant requirements (< 330 grams) and low parasitic losses (38 watt condenser fan) (Figure I-15b). Analysis indicates that the cooling system can reduce the power electronics thermal resistance by as much as 50% as compared with the high-performance, dual side cooled, commercial baseline (Lexus LS 600h inverter).

The two-phase based cooling system was designed to minimize system cost via the use of lightweight and cost effective materials (i.e., aluminum construction) and fabrication techniques. The system incorporates features to increase the evaporator area and thus improve performance and decrease the size of the cooling system. The cooling concept utilizes a simple implementation of two-phase cooling to improve system efficiency and increase reliability (i.e., no pump or compressor). The indirect cooling approach of the system should improve the reliability of the system by eliminating contact between the electronic devices and the refrigerant.

Future work will involve implementing boiling enhancement coatings to further increase the thermal performance and experimentally measuring the thermal performance of the system while cooling an automotive power module (Delphi discrete power switch). Tests will also be conducted to evaluate the effects of inclination on system performance.
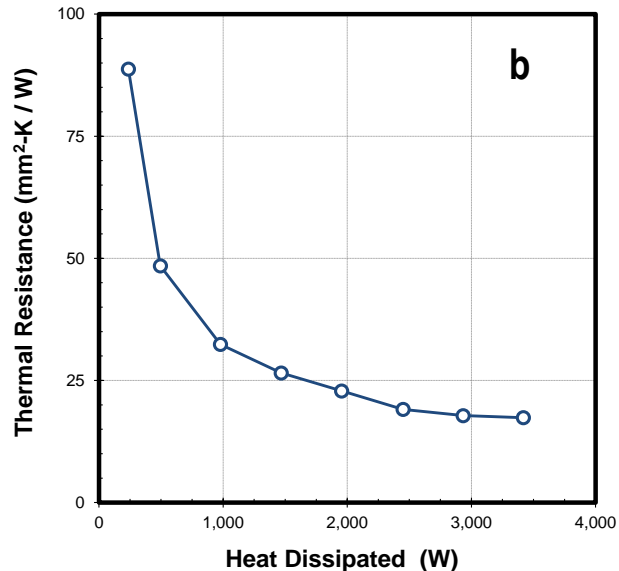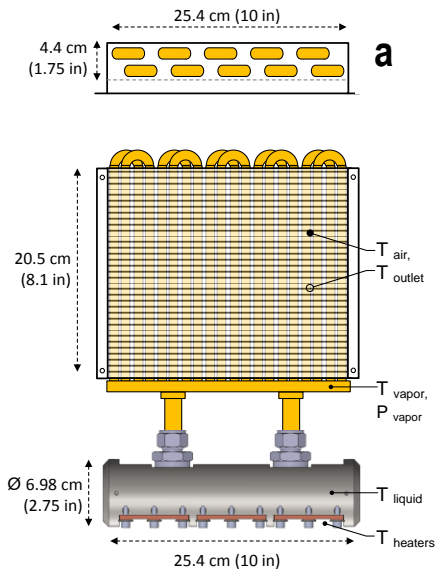
Figure I-15. a) Schematic of the proof-of-concept, passive two-phase cooling system. b) Thermal performance of the evaporator demonstrating the system can dissipate 3.5 kW of heat under steady state conditions with small refrigerant requirements (< 330 grams) and low parasitic losses (38 watt condenser fan).

8. Development of Low Loss Motor Lamination Steel

Static and dynamic testing of commercial high silicon steel validates excellent low loss characteristics. Novel, potentially much lower cost, processing technique developed at ORNL will facilitate efficiency improvement.

Oak Ridge National Laboratory

Electric traction drive systems (ETDS) contribute 16% of overall losses in all electric vehicles (AEV) over a Urban Dynamometer Driving Schedule (UDDS) drive cycle. The majority of these losses are accumulated in the traction motor. For example, the 2012 Nissan LEAF ETDS has a line averaged efficiency of 92.5%, the combined result of 95.2% traction motor and 97.2% inverter efficiency. ETDS efficiency improvements are therefore focused on motor materials that have potential to significantly reduce core losses.

Table I-1. Benchmarked AEV metrics vs. DOE Advanced Power Electronics and Electric Motor Program 2020 technical targets (line averaged efficiency).

Metric (units)	Motor	Inverter	ETDS	TDS 2020
SC ($/kW)	11.7	13.65	25.4	8
SP (kW/kg)	1.43	4.94	1.1	1.4
PD (kW/liter)	4.21	5.14	2.3	4
Efficiency (%)	95.2	97.2	92.5	94
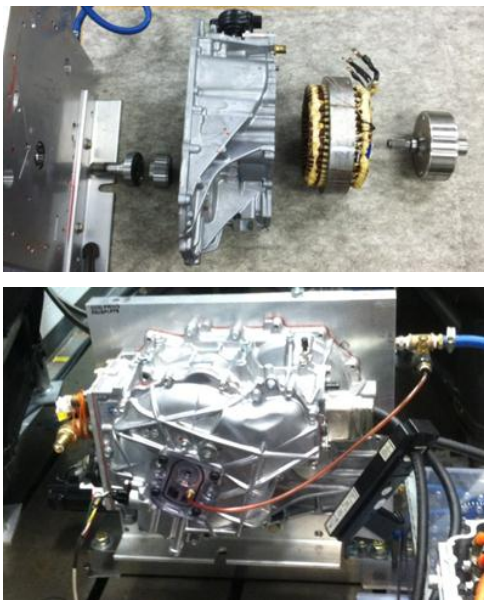
Figure I-16. Top: Exploded view of prototype of 6.5% silicon steel stator in spin test assembly. Bottom: Fully assembled spin test apparatus with rare earth magnet rotor and water/ethylene glycol cooling.

Test results based on comparison to production lamination core, grade 29M19C5 steel, and JFE 10JNEX900 confirm the benefits of high silicon steel (JFE Supercore ™ a 6.5% silicon iron material).
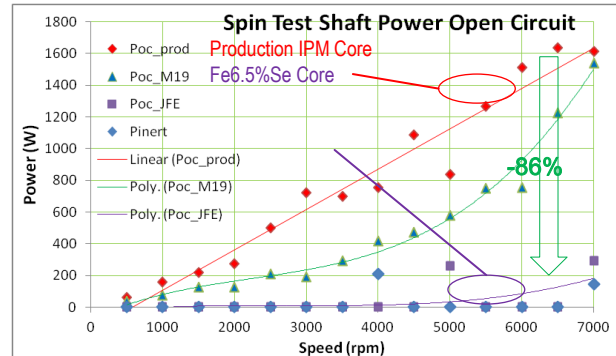
Figure I-17. Comparison of core only losses for the various materials at full rotor flux vs. speed.

Commercial, 6.5% silicon steel, processed by chemical vapor deposition (CVD), has low loss but is very expensive. ORNL has pursued an alternative process based on strain softening during warm deformation (first reported by Chinese) that effectively destroys lattice ordering (B2 phase) leading to restoration of ductility and subsequent ease of cold formability. This process leads to low cost Fe-6.5%Si steel sheet for motor laminations with the same or better magnetic properties compared to the CVD processed steel. Scaling up and commercialization of the process is important to industry and motor manufacturing because of the major beneficial impact. More development is needed, specifically, in the optimization of boron content and the thermo-mechanical process parameters. ORNL is exploring super-imposed ultrasonic vibration during deformation to eliminate as the means to eliminate the need for warm rolling.
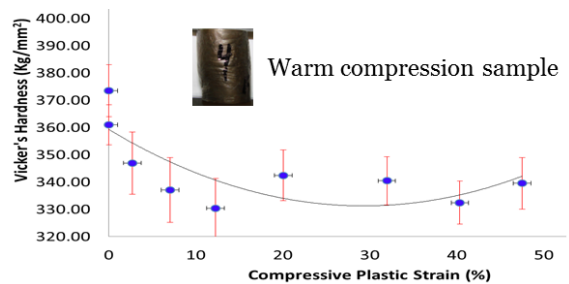
Figure I-18. Work softening at ORNL of Fe6wt%Si-500ppm-B during warm compression at 400°C.

Planned Activities

Electric drive system R&D is needed to accelerate the development of advanced power electronics and electric motors to enable a large market penetration of PEVs. Developing advanced power electronic, electric motor, and traction drive system technologies that will leapfrog current on-the-road technologies, with a system-level emphasis to improve fuel efficiency and reduce cost, are key to meeting the *EV Everywhere* Grand Challenge. Achieving *EV Everywhere* targets will require cutting-edge R&D in several areas including permanent magnet materials, non-rare earth magnets, advanced capacitors, thermal and electrical packaging, wide bandgap (WBG) semiconductors, and motor laminations. The R&D strategy to achieve the *EV Everywhere* cost and performance targets in this technology area includes:

- ELECTRIC MOTORS: Develop new low-cost and highly efficient motor designs, alternative magnetic materials with reduced rare earth content, and improved motor manufacturing methods. Long-term emphasis on non-rare earth motor architectures will reduce motor costs and mitigate rare earth market uncertainties for the original equipment manufacturers and their suppliers.
- POWER ELECTRONICS: Develop affordable WBG devices, high-temperature capacitors, advanced packaging, high voltage operation, and new circuit topologies. Designs using WBGs will increase as manufacturing processes enable improved device yield and performance. In addition, this research includes advancements in thermal management such as low cost heat transfer technologies, thermal stress and reliability, and thermal systems integration.
- TRACTION DRIVE SYSTEM: Integrate power electronic and motor technologies along with traction drive control

strategies, innovative integrated system designs, and thermal management.
- ON-BOARD CHARGERS: Reduce the cost for on-board chargers, followed by overcoming packaging and thermal limitations.

In 2013, U.S. DRIVE updated its Electrical and Electronics Technical Team Roadmap. This Roadmap can be found at http://www1.eere.energy.gov/vehiclesandfuels/pdfs/program/eett_roadmap_june2013.pdf.

In support of the *EV Everywhere* Grand Challenge, DOE released a Funding Opportunity Announcement (FOA) in March 2013, soliciting proposals in the areas of energy storage, electric drive systems, lightweight materials, and auxiliary load reductions. DOE announced the selection of 38 awards from the FOA in September 2013. These projects, which were initiated in September 2013, will be described in more detail in next year's annual report.

Four projects focus on power electronics for PEVs. These projects represent a DOE investment of $8 million. Compared to silicon-based technologies, WBG semiconductors–such as silicon carbide and gallium nitride–can operate at higher temperatures, have greater durability and reliability, and can lower the cost and improve performance of plug-in electric vehicle inverters. Separately, new approaches to enable high-temperature operation and cost reduction for capacitors in these inverters will also help to reduce the cost of vehicle power electronics. These projects will contribute to reducing the cost of a plug-in electric vehicle inverter by more than 30 percent.

I.2.   Small Business Innovative Research Grants

Steven Boyd (Technology Manager)
Vehicle Technologies Office

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Start Date: October 1, 2012
Projected End Date: September 20, 2013

Objectives

- Use the resources available through the Small Business Innovation Research (SBIR) and Small Business Technology Transfer (STTR) programs to conduct research and development of technologies that can benefit the Advanced Power Electronics and Electric Motors (APEEM) effort within the Vehicle Technologies Program.
- Achieve the four SBIR objectives: (1) to stimulate technological innovation; (2) to increase private sector commercialization of innovations; (3) to use small business to meet federal research and development needs; and (4) to foster and encourage participation by minority and disadvantaged persons in technological innovation.

Accomplishments

- Text Initiated three Phase I awards and one Phase II award.

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Introduction

The Small Business Innovation Research (SBIR) program was created in 1982 through the Small Business Innovation Development Act. Eleven federal departments participate in the SBIR program and five departments participate in the STTR program, awarding a total of $2 billion to small high-tech businesses. Small Business Innovation Research (SBIR) and Small Business Technology Transfer (STTR) are U.S. Government programs in which federal agencies with large research and development (R&D) budgets set aside a small fraction of their funding for competitions among small businesses only. Small businesses that win awards in these programs keep the rights to any technology developed and are encouraged to commercialize the technology.

A 1982 study found that small businesses had 2.5 times as many innovations per employee as large businesses, while large businesses were nearly three times as likely to receive government assistance. As a result, the SBIR Program was established to provide funding to stimulate technological innovation in small businesses to meet federal agency research and development needs. After more than a decade, the STTR program was launched. The major difference is that STTR projects must involve substantial (at least 30%) cooperative research collaboration between the small business and a non-profit research institution.

Approach

Each year, DOE issues a solicitation inviting small businesses to apply for SBIR/STTR Phase I grants. It contains technical topics in such research areas as energy production (Fossil, Nuclear, Renewable, and Fusion Energy), Energy Use (in buildings, vehicles, and industry), fundamental energy sciences (materials, life, environmental, and computational sciences, and nuclear and high energy physics), Environmental Management, and Nuclear Nonproliferation. Grant applications submitted by small businesses MUST respond to a specific topic and subtopic during an open solicitation.

SBIR and STTR have three distinct phases. Phase I explores the feasibility of innovative concepts with typical awards up to $150,000 for 9 months. Only Phase I award winners may compete for Phase II, the principal R&D effort, with awards up to $1,000,000 over a two-year period. There is also a Phase III, in which non-Federal capital is used by the small business to pursue commercial applications of the R&D. Also under Phase III, Federal agencies may award non-SBIR/STTR-funded, follow-on grants or contracts for products or processes that meet the mission needs of those agencies, or for further R&D.

Results

Phase I Topics for 2013

Below is the text for the Advanced Power Electronics and Electric Machines topic from the 2013 SBIR Phase I Release 2 topics. The full topic release can be found at http://www.science.energy.gov/~/media/sbir/pdf/solicitations/FY13PIR2Topics11912Ver3.pdf

Power electronic inverters and converters are essential for electric drive vehicle operation, and currently add significant cost to these vehicles, therefore limiting their commercialization potential. Improvements in their performance can lead to cost reduction or better utilization of their capabilities in vehicles, as outlined in the U.S. DRIVE partnership Electrical and Electronics Technical Team Roadmap at www.eere.energy.gov/vehiclesandfuels/pdfs/program/eett_roadmap_12-7-10.pdf.

Applicants are sought to develop subcomponent-level improvements to power electronic inverters or converters which would support commercialization of micro, mild, and full HEVs, PHEVs, and EVs. Specific improvements sought for this topic are:

1. Small, lightweight low loss magnetic materials for passive inductors
2. High temperature (250°C capable) thermal interface materials with low electrical resistivity
3. High temperature (250°C capable) on-chip high voltage gate drivers

The Phase I effort should involve the development and validation of the proposed technology or material with demonstrated performance under simulated operating conditions. In Phase II, the technology should be further advanced and demonstrated through the production of prototype devices.

Phase I Awards Made in 2013

Three Phase I awards were made in FY 2013 which resulted in the following projects:

Development of advanced soft magnetic nanocomposite materials with low loss

Dr. Hao Zhu

Spectrum Magnetics LLC

This SBIR Phase I proposal is aimed to develop advanced soft magnetic nanocomposite materials with low loss, high flux density, and capability to operate at high frequency ranges (100kHz-10MHz). With Spectrum Magnetics' proprietary technique, we will develop magnetic flake materials with thickness in the nanometer scale, which effectively reduces the eddy current loss and eliminates undesired demagnetization factor. Consolidation of laminated magnetic nano-entities leads to novel cores, which is a nano-scale version of conventional laminated soft FeSi (silicon steel) cores. Our process greatly simplifies the manufacture procedures and reduces the cost.

Small, lightweight low loss magnetic materials for passive inductors

Dr. Jacky Chen

Aegis Technology Inc.

In this Phase I study, Aegis Technology will develop an innovative class of advanced nanocomposites containing high moment CoFe nanoparticles, and demonstrate an innovative cost-effective approach to produce high permeability, large saturation, and induction, low-loss (hysteretic/eddy current) soft magnetic nanocomposite materials with high operating temperatures. The Phase I research will cover material design, processing development, characterization and prototyping, with an aim to identify the underlying technical issues that govern the fabrication and performance of this novel class of soft magnetic nanocomposites.

High Temperature (300°C) Silicon Carbide (SiC)-Based Integrated Gate Drivers for Wide Bandgap Power Devices

Mr. Brad Reese

Arkansas Power Electronics International, Inc.

APEI, Inc. will continue development of its patented high temperature gate driver technology, enabling the next generation of high-efficiency, high power density converters. At the conclusion of Phase I, APEI, Inc. will design, fabricate, and demonstrate a high temperature (300°C) gate driver utilizing discrete SiC circuitry while concurrently developing high temperature packaging techniques to enable reliable operation of the drivers over an extended period of time.

Phase II Awards Made in 2013

Under the SBIR/STTR process, companies with Phase I awards from FY 2012 are eligible to apply for a Phase II award in FY 2013.One Phase II award was made in FY 2013 that resulted in the following project:

Low-Cost Integrated Package and Heat Sink for High-Temperature Power Modules

Dr. James Connell

Advanced Thermal Technologies LLC

This The Phase I effort has established a novel, low-cost integrated package-heat sink technology for use in high-temperature power module packaging and thermal management. This integrated package-heat sink technology is enabled by a unique copper-ceramic-graphite-copper substrate technology and a highly effective compact heat transfer technology. The integrated assembly provides for electrical isolation of the semiconductor and electrical components, and minimizes the thermal resistance between the power semiconductor devices and the heat sink coolant. Further, the assembly provides for the minimization of the coefficient of thermal expansion (CTE) mismatch between the different material layers of the assembly in order to minimize thermal stresses resulting from cyclic power and temperature operation–key to achieving a reliable product with a long life. The Phase II effort is focused on the development and demonstration of products based upon the technology. The goal of the project is (1) the final design of the integrated package-heat sink assembly and (2) the establishment of the fabrication processes required to support its low-cost manufacture.cost.

II. RESEARCH AREAS

II.0 Systems, Modeling and Benchmarking

II.1. System Modeling, Efficiency Mapping, Identification of Research Gaps

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Susan A. Rogers, DOE Program Manager
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E-mail: Susan.Rogers@ee.doe.gov

Start Date: October 2013
Projected End Date: September 2014

Objectives

- Develop a baseline circuit simulation model—the 2012 Nissan LEAF traction drive.
- Find the high-energy-throughput points of a 2012 Nissan LEAF traction drive over the Combined Driving Schedule (CDS) which is formed by adding five driving schedules in series (UDDS+US06+HWFET+LA92+UDDS).

Technical Barriers

- Optimum operation of the TDS, not the component
- More detailed simulation of the TDS in a vehicle simulation
- Improved cost and efficiency

Technical Targets

- The TDS
- Cost: $8/kW (2020 target)
- Efficiency > 94% (2020 target)

Accomplishments

- Modeled a baseline Nissan LEAF inverter and motor
- Identified the highest-energy-throughput areas for the Urban Dynamometer Driving Schedule (UDDS) and CDS using the clustering and energy histogram methods

- Provided TDS operating targets to the PE and electric motors areas in the APEEM program
- Completed the TDS model in a circuit simulator

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Introduction

It is imperative that a comprehensive understanding be attained of all the interactions between driveline road load and regenerative energy storage system (RESS) power flows at the TDS level, as they influence the traction motor operating points and its attendant power inverter real and reactive power flows. For this reason, collaboration with Argonne National Laboratory is advised to avoid duplication and expedite the understanding of full system requirements. The objective of this task is to map out where the traction motor and power inverter must deliver optimum efficiency and how different material choices could benefit the full drive system. Examples are the application of new electrical steels in the electric machine, different conductor designs for the electric motor stator, thermal potting compounds, and the novel winding designs and overall geometry needed for higher-speed operation, if that is determined to be the route to pursue. In the PE inverter stage, modeling and simulation will benefit a deeper understanding of where the crossover in cost is between silicon (Si) and wide bandgap (WBG) semiconductor devices, including their matching gate drivers. The results of this system simulation are passed along to Subtasks 3.0 and 4.0 to guide their development roadmaps. For example, suppose results show a TDS can best accommodate WBG devices in the power inverter stage when their pulse width modulation (PWM) frequency is held in the conventional range of 10–20 kHz but voltage is increased to 1,000 Vdc. In that case, PE module development must proceed with a dielectric material suited to this voltage, and electric motor insulation systems and winding designs must also accommodate high voltages. Constraints on insulation systems, such as temperature endurance and high potential standardized test limits, must also be satisfied.

Approach

Circuit and system simulation software is used to model and simulate a baseline EV. The same simulation system is also used to model and simulate new PE and electric machines designed by APEEM and compare them with the baseline. In running the system simulation on the Autonomie software, the following tasks were completed:

- Define and develop at least five highest-energy-throughput zones in the TDS for further action
- Correlate operating efficiency at these five or more zones in the current baseline interior permanent magnet (IPM) TDS with a representative higher-efficiency TDS
- Cascade the requirements to the PE and electric machines sub-thrusts

Results

The project used two approaches to modeling: a top-down approach that includes vehicle-level and circuit-level simulation. Vehicle-level simulation is used to determine the high-energy-throughput points of a 2012 Nissan LEAF model, and the circuit-level approach looks at the operation of the TDS in finer time resolution for more detailed analysis and modeling.

Vehicle-level simulation

A CDS was defined to represent different driving schedules an EV would face, including city, highway, fast acceleration, and stop-and-start-driving. The CDS consists of the Environmental Protection Agency's (EPA) UDDS, the Supplemental FTP Driving Schedule (US06), Highway Fuel Economy Test Driving Schedule (HWFET), Unified Dynamometer Driving Schedule (LA92), and UDDS in sequence. These driving schedules are defined and are available at http://www.epa.gov.

UDDS occurs at the beginning and end of CDS. To observe the high-energy-throughput areas, the 2012 Nissan LEAF baseline vehicle was simulated over UDDS and the motor speed was plotted vs. time in Figure II-1. This plot is similar to the vehicle speed plot; since LEAF is an EV, the motor speed is expected to be a scaled version of the vehicle speed.
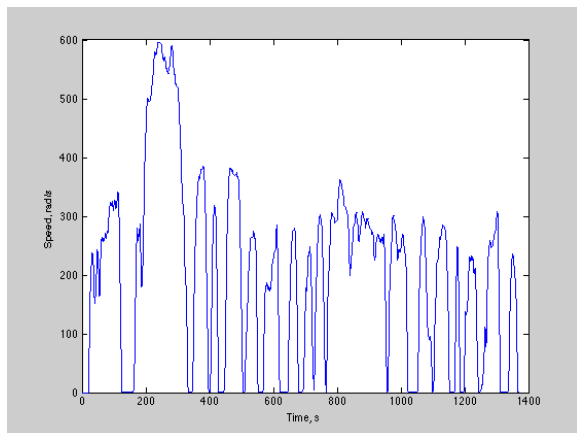
Figure II-1: The motor speed profile of the 2012 Nissan LEAF simulated over UDDS on Autonomie.

The high-energy-throughput areas of the traction motor can be obtained from the torque speed curve of the vehicle over the UDDS cycle (Figure II-2). As seen inFigure II-2, if the motoring only region (i.e., first quadrant) is considered, the motor is operated at high-torque, low-speed regions, as well as low-torque, medium- and high-speed regions.
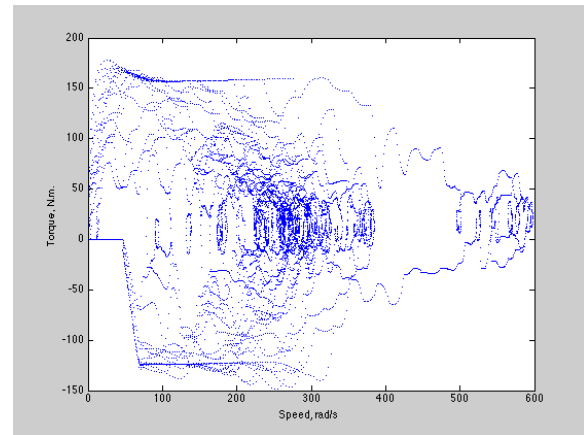
Figure II-2: The torque speed curve of the 2012 Nissan LEAF electric motor simulated over UDDS on Autonomie.

Two methods were used to determine the high-energy-throughput areas: energy histograms and clustering. For the energy histogram method, the torque and the speed values in the motoring region were divided into 40 bins each, forming 1,600 energy bins (40 torque bins $\times$ 40 speed bins = 1,600 energy bins). Figure II-3 shows the energy bins, where the colors signify the density of operating points in those areas (red=most crowded, blue=least crowded. The red points validate the observation for the high-energy-throughput areas from the torque–speed curve.
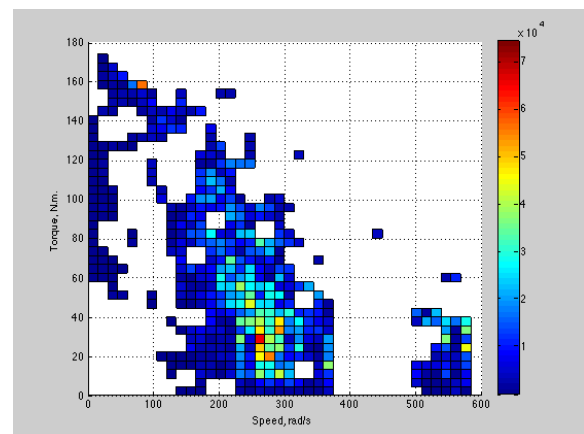
Figure II-3: The energy bins obtained from the torque–speed curve of the 2012 Nissan LEAF electric motor simulated over UDDS on Autonomie.

The clustering method uses the k-means clustering algorithm that forms a pre-specified number of clusters and their cluster centers by classifying each operating point according to its distance from the nearest cluster center. One by one, each operating point is assigned to a cluster in an iterative process. Figure II-4 shows the results of this clustering process for three clusters; Table II-1 lists the torque and speed values for the cluster centers. As can be seen, the centers of the green and blue clusters are close to the high-

energy regions observed using the energy histogram method; but the center of the red cluster is at a much lower torque value compared with the earlier case.
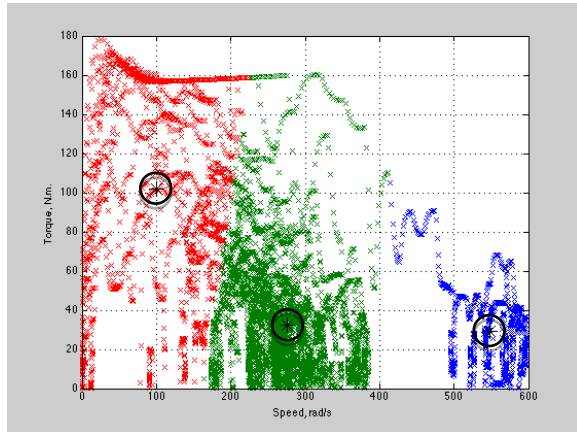
Figure II-4: The clusters obtained from the torque–speed curve of the 2012 Nissan LEAF electric motor simulated over UDDS on Autonomie.

Table II-1: Cluster centers

Cluster	Speed (rad/s)	Torque (N.m.)
Blue	548	29.3
Green	275.4	32.4
Red	100.3	102

Figure II-5 and Figure II-6 show the motor speed profile and the motor torque vs. speed plots of the 2012 Nissan LEAF simulated over CDS.
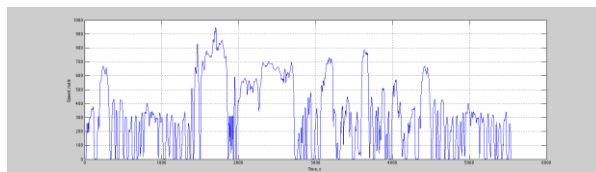
Figure II-5: The motor speed profile of the 2012 Nissan LEAF simulated over CDS on Autonomie.
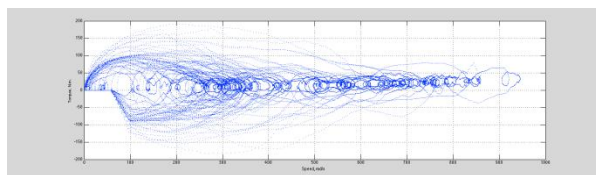
Figure II-6: The torque speed curve of the 2012 Nissan LEAF electric motor simulated over UDDS on Autonomie.

As seen in Figure II-6, there seem to be many areas of high energy throughput, some at the high-torque, low-speed regions but many along the speed axis, i.e. low-torque regions. To get a better understanding of these areas, the energy histogram and clustering methods were applied to the motoring region of the data in Figure II-6.

Figure II-7 shows there are some high-energy areas for low-torque, medium-speed regions, but no distinct clusters can be identified.

Figure II-8 shows the torque–speed curve with the clustering method applied for five clusters. The centers of the blue and green clusters are close to the high-energy points in Figure II-7. The other three cluster centers are not obvious from the figure. Table II-2 lists the torque and speed values for the cluster centers.
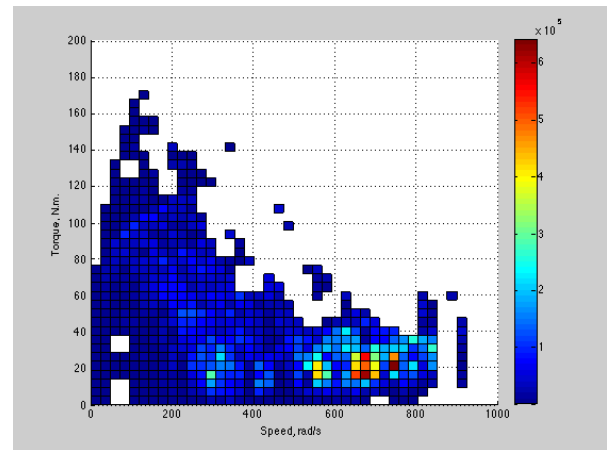
Figure II-7: The energy bins obtained from the torque–speed curve of the 2012 Nissan LEAF electric motor simulated over UDDS on Autonomie.
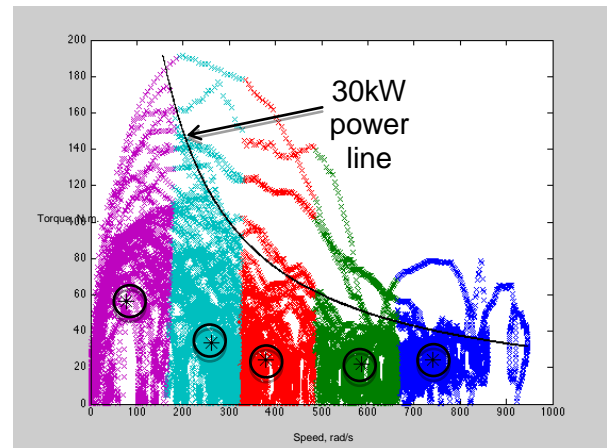
Figure II-8: The clusters obtained from the torque–speed curve of the 2012 Nissan LEAF electric motor simulated over CDS on Autonomie.

Table II-2: Cluster centers

Cluster	Speed (rad/s)	Torque (N.m.)
Blue	741.7	24.2
Green	586.5	21.8
Red	380.1	24
Cyan	262.2	33.7
Magenta	76.1	56.3

Since the high-energy areas are not obvious in Figure II-7, the figure is plotted in 3 dimensions (Figure II-9) to observe other possible peaks. This figure shows a concentration of high-energy-throughput peaks around the low-torque, high-speed and the low-speed, medium-torque regions, as expected. It is consistent with the results obtained from the clustering method.
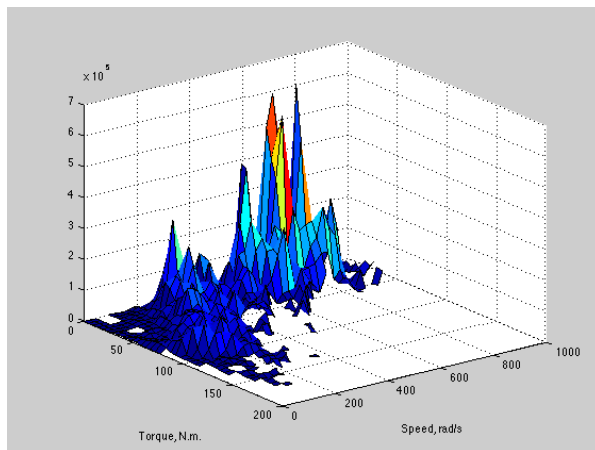
Figure II-9: The 3D plot of the energy bins in Figure 7.

Circuit-level simulation

Vehicle simulation is usually done at sampling times on the order of seconds or tenths of seconds. Those times would seem like an eternity for a power conversion simulation with device details, as the required sampling times for such conversions would be on the order of nanoseconds. A tradeoff on the level of detail is required. To evaluate the functionality and the performance of a power conversion circuit, sampling times on the order of microseconds would be sufficient. Vehicle-level simulation is conducted using Autonomie. It does not include circuit-level details, which would increase the Autonomie simulation time considerably. As a tradeoff, in this work, the PLECS software was selected for circuit-level simulation.

Figure II-10 shows the circuit model of an inverter in PLECS. Figure II-11 and Figure II-12 show the Nissan LEAF insulated gate bipolar transistor (IGBT) static characteristics and their implementation in PLECS; and Figure II-13 and Figure II-14, respectively, show the same for the diode.
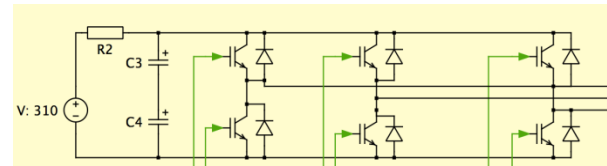
Figure II-10: The circuit-level model of the 2012 Nissan LEAF inverter in PLECS.
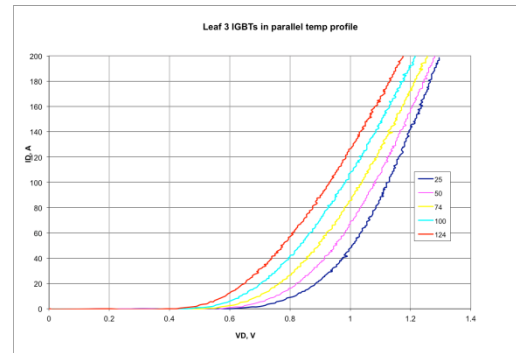
Figure II-11: 2012 Nissan LEAF IGBT static characteristics.
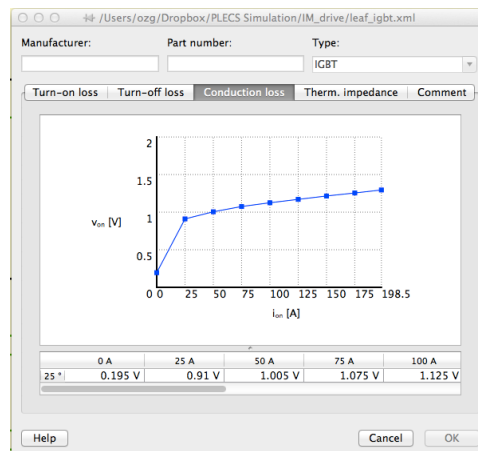
Figure II-12: The model implementation of the 2012 Nissan LEAF IGBT static characteristics.
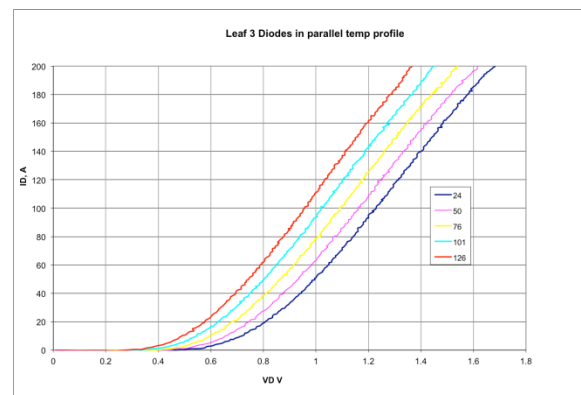
Figure II-13: 2012 Nissan LEAF diode static characteristics.
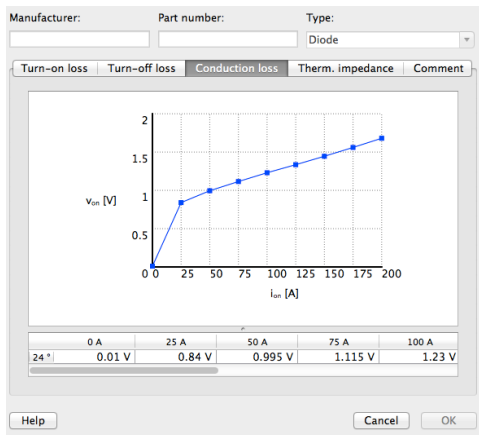
Figure II-14: The model implementation of the 2012 Nissan LEAF diode static characteristics.

In addition to the devices and the inverter, the traction drive motor was modeled in PLECS. Figure II-15 shows the 2012 Nissan LEAF traction motor model; Figure II-16 and Figure II-17 show the torque and speed responses, respectively, for a given command profile.
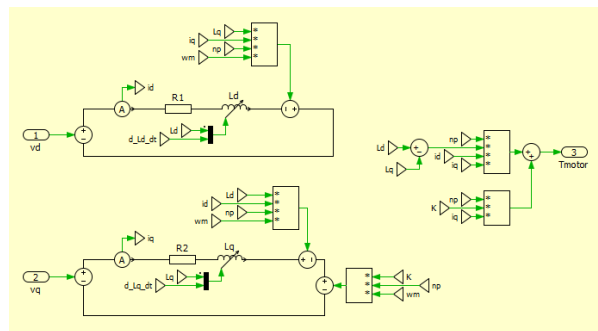
Figure II-15: The 2012 Nissan LEAF traction motor model implementation.
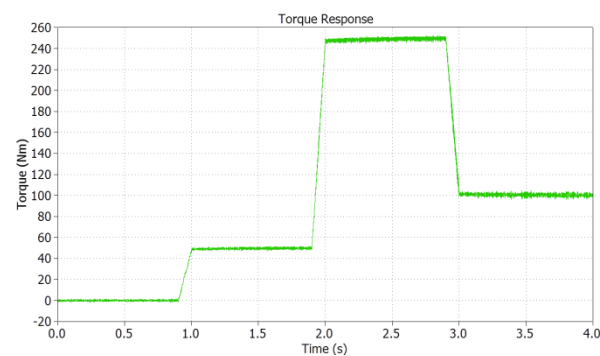
Figure II-16: The 2012 Nissan LEAF traction motor model simulation response to a torque command profile.
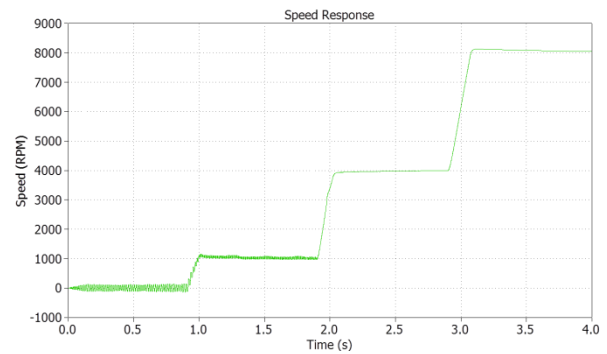
Figure II-17: The 2012 Nissan LEAF traction motor model simulation response to a speed command profile.

High-speed induction machine

The purpose of the circuit-level modeling is also to form a platform for simulating converters, inverters, and motors of varying power levels under the same operating conditions and validating their responses. A high-speed induction machine that was developed under another task was modeled and simulated using PLECS to validate its operation. The PLECS model of this high-speed induction machine is shown in Figure II-18, and the machine parameters calculated during the design process are shown in Figure II-19.
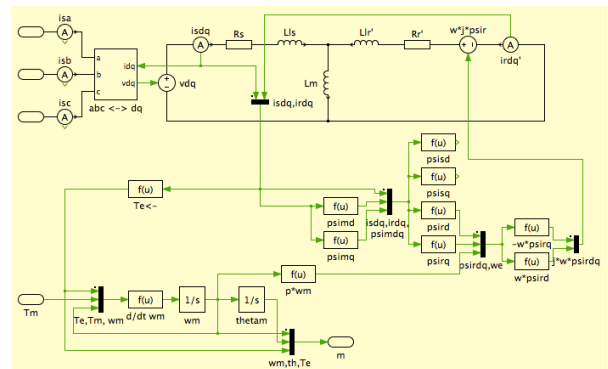
Figure II-18: Induction machine model from PLECS.
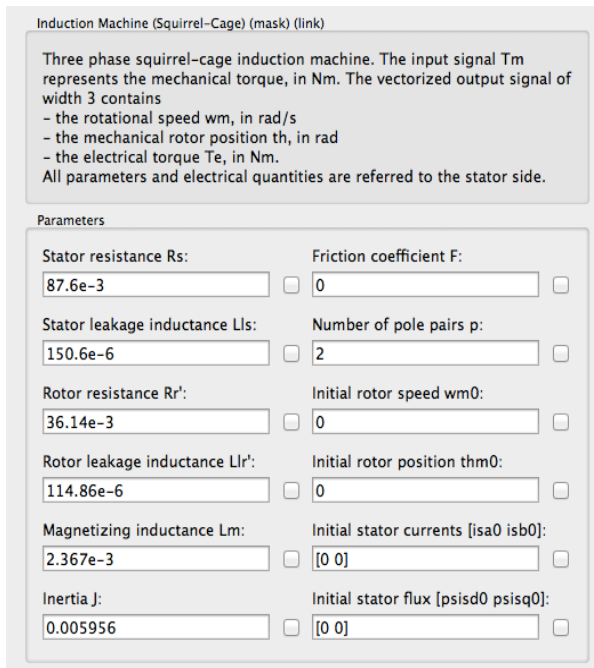
Figure II-19: The parameters calculated during the high-speed induction machine design process.

Figure II-20 shows the direct-on startup of the machine at no-load and its torque response to rated torque applied at 0.4 s. The torque oscillations observed during torque transitions occur because of the low-inertia design of the machine. Figure II-21 shows the speed response corresponding to the startup and step torque response shown in Figure II-20. Figure II-22 shows the torque vs. speed curve for this operation, and Figure II-23 shows the torque slip curve. As designed, at 200 Nm, the slip is at 6%.
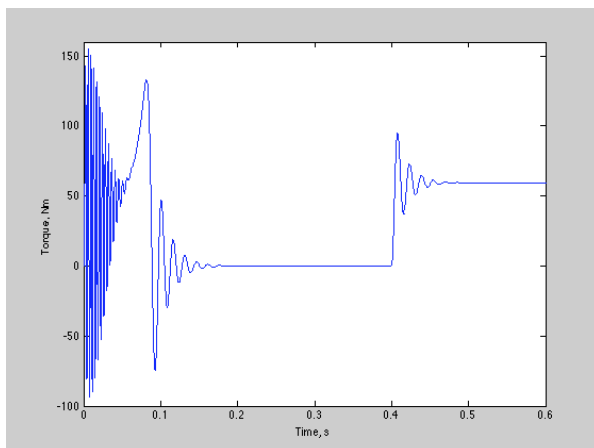
Figure II-20: Torque response of the high-speed induction machine during startup and after a step load torque.
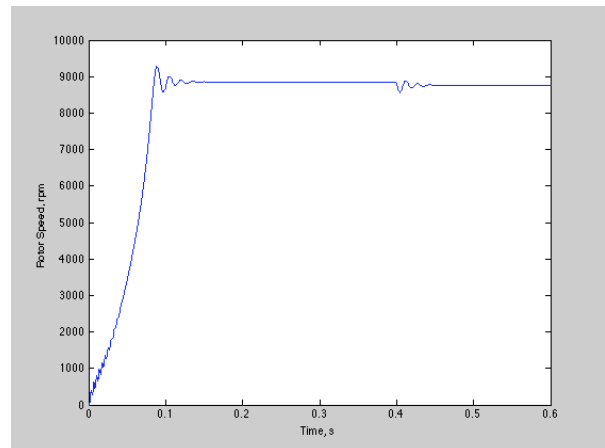
Figure II-21: Speed response of the high-speed induction machine during startup and after a step load torque.
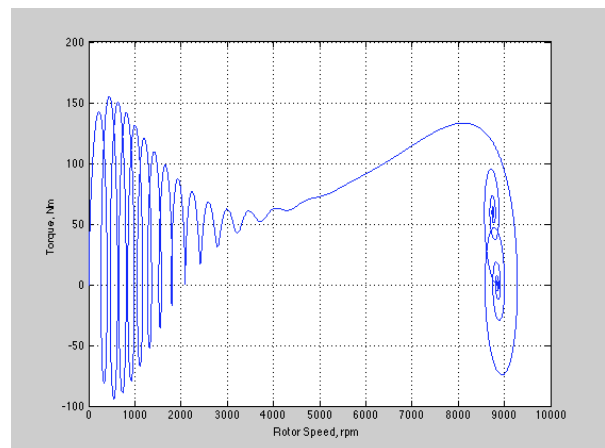
Figure II-22: Torque vs. speed curve of the high-speed induction machine during startup and after a step load torque.
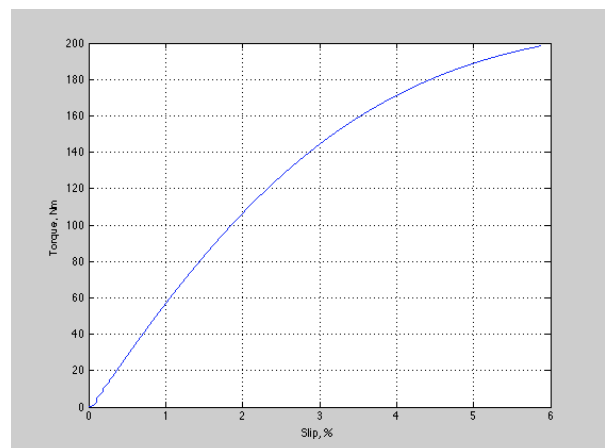
Figure II-23: Torque slip curve of the high-speed induction machine.

Conclusions and Future Directions

Typical electric motors and inverters are designed for rated power operation; however, they operate at very different operating points in EVs. The vehicle-level simulation results show the high-energy-throughput areas of a baseline EV, which should be used to design the TDSs. System simulations at the circuit and vehicle level can be used to show the operation of the components designed as a part of the program. Circuit-level simulations could be used as a software version of the dynamometers used in the lab to evaluate traction motors and inverters.

The system simulation work is proposed to be discontinued as an independent project during FY 2014. It will continue as a part of other projects.

FY 2013 Publications/Presentations

N/A

FY 2013 Patents

N/A

II.2. Inverter Development and System Controls

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Start Date: October 2012
Projected End Date: September 2015

Objectives

Overall

- Develop and design a WBG 55 kW inverter using the WBG device attributes. Reduce the size, weight, and cost of the inverter to meet DOE's 2020 inverter targets.

FY 2013

- Design, build, and test a 10 kW WBG-based prototype using commercially available WBG modules.

Technical Targets

- Maintain cognizance of state-of-the-art WBG power devices and acquire, test, and characterize novel devices.
- Develop loss models and circuit models using the test data and discern the inverter benefits.
- Develop and build a single-phase test bed based on conventional mid-point converter architecture to evaluate WBG module performance.
- Design a 10 kW inverter using commercially available WBG devices/modules to demonstrate the performance targets scaled to 30 kW operation.
- Enhance the 10 kW inverter design using the high-temperature packages and the gate drivers developed at ORNL to show the feasibility of achieving 2020 targets.

- Scale the low-power inverter design to demonstrate the performance at 30 kW continuous and 55 kW peak power operation while meeting the 2020 targets.

Accomplishments

- Acquired, tested, and characterized a gallium nitride (GaN) switch, a silicon carbide (SiC) super junction transistor (SJT), and an SiC junction barrier Schottky (JBS) diode.
- Completed design, build, and testing of an all-SiC 10 kW inverter using a state-of-the-art commercial all-SiC module.

✧   ✧   ✧   ✧   ✧

Introduction

Problems associated with PE for advanced vehicle applications include

- Cost, size, and weight of power converters and their cooling systems
- Need for increased efficiency and reliability

It should be no surprise that none of the EV traction drive systems on the market can meet cost and efficiency goals. Efficiency is attained by using lower-loss devices and materials that tend to be expensive, even as quantities increase. A case in point is motor lamination steel, for which lower-loss grades are manufactured using novel processes that add cost. Table II-3 summarizes the specific power and power density of the components in commercially available HEVs and EVs and their system-level metrics relative to DOE 2020 targets. Currently available commercial systems are subject to the following caveats:

- The LEAF motor has lower specific power since it is designed for continuous duty in an EV.
- The LEAF motor has 3 water–ethylene glycol coolant local loops in the stator housing, adding manufacturing complexity.
- All motors shown rely on IPMs containing rare earth (RE) materials that add cost.
- Induction motors (IMs) are less expensive, but are bigger, heavier, and less efficient
- All inverters shown are Si-based, the Prius at 250 A and the LEAF at 640 A.
- For comparison, the Tesla inverter is 800 A and contains more than three times as much Si as the Prius inverter.

Table II-3: Commercial traction drive system benchmark summary

Metric	Units	2020 target	2010 Prius	2011 LEAF	2011 Sonata
Peak power	(kW)	55	60	80	30
Inverter	SP (kW/kg)	14.1	16.7 (5.9*)	4.94	6.9
	PD (kW/liter)	13.4	11.1 (6.9)	5.14	7.3
Motor	SP (kW/kg)	1.6	1.6	1.43	1.1
	PD (kW/liter)	5.7	4.8	4.21	3.0
System	SP (kW/kg)	1.44	1.46 (1.25)	1.1	0.95
	PD (kW/liter)	4.0	3.35 (2.8)	2.3	2.13
System efficiency	(peak %)	>94%	~95	~94	93

- The goal of this research is to reduce the size and weight of power converters to meet the 2015 and 2020 inverter targets. The overall strategy for cost reduction is shown in Figure II-24. Cost reduction can be achieved by
- Reducing the number of components by integrating functionality
- Eliminating/reducing the existing liquid cooling loops
- cutting manufacturing costs by decreasing the part count and manufacturing steps
- Minimizing high-cost materials, like copper (Cu), through bus bar optimization current reduction
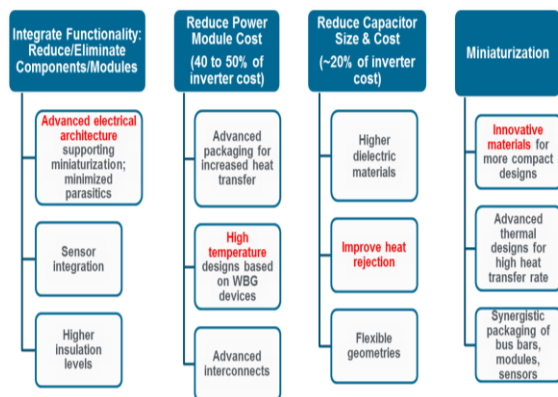
Figure II-24: Strategy to reduce power electronics cost.

Approach

There is an increasing need for higher-temperature operation of PE in automotive applications. The ability of components to operate reliably at elevated temperatures can deliver cost and weight savings by reducing heat sinks and eliminating secondary cooling loops. Additionally, devices capable of higher-frequency operation can reduce requirements for passive components, leading to further reductions in cost, weight, and volume. WBG devices, specifically SiC and GaN semiconductors, are emerging technologies that enable higher-temperature and higher-frequency operation as well as efficiency and reliability improvements. The development of WBG devices is promising

for helping achieve these goals and VTO targets. The WBG technology assessment performed under this project will help to determine when it is viable to introduce these devices to the market for automotive use. The independent assessment of such devices enables the automotive industry to monitor their progress and provides data readily when the need arises.

A pivotal point in the traction drive program is the PE stage showing single-phase electrical and thermal characterization and the point at which thermal management innovations are put into practice in a WBG-based module. The purpose of focusing on single-phase hardware characterization is that it affords development teams the opportunity to validate hardware at a much simpler stage than the full power inverter and to validate thermal performance.

Single-phase testing and characterization are performed at a bus voltage of up to 800 Vdc and are controlled to synthesize nominal electric machine phase current wave shape, amplitude, and base and switching frequency. The results will be used in subsequent electric motor tests.

Single-phase testing will be followed by multiphase testing under an electric motor equivalent R-L (inductor-resistor) loading. The overall objective of this project is to design and develop a high-voltage WBG 30 kW continuous-power, 55 kW peak-power inverter. WBG devices offer some distinct advantages over Si components. Their primary advantage is that they can operate at higher junction temperatures. This allows for hotter coolant and smaller heat sinks and can potentially help facilitate air-cooling without sacrificing performance.

Many of the typical components in a commercial inverter, e.g., capacitors and gate drivers, cannot withstand the desired operating temperatures of WBG devices. Thus the whole inverter must be considered in developing new high-temperature packages.

Design innovations in this project include the following.

- Layers of high-temperature thermal insulating material are used to separate low-temperature components from the high-temperature zone.
- The high-temperature operating capability of WBG devices enables air cooling, and newer fast-switching Si IGBTs are used for high-temperature liquid designs.
- The innovative heat sink design minimizes thermal resistance.
- There are new control and sensing techniques for system control and efficiency optimization.
- The design is optimized for the most frequently operated points.

These new concepts will increase the power density and decrease the volume and weight for EV traction drive inverters.

Results

1. Device Testing

The new WBG devices acquired this year are a 1200 V, 7 A SiC SJT; a 600 V, 5 A GaN field effect transistor (FET); and a 1200 V, 20 A normally-on junction field effect transistor (JFET). The devices were packaged differently, as shown in Figure II-25. On-state characteristics and switching energy losses of the devices were obtained over a wide temperature range. The test results for these devices will be presented in the following sections. All the devices obtained were experimental samples.

600 V, 5 A GaN FET

1200 V, 7 A SiC SJT   1200 V, 20 A SiC JFET

Figure II-25: WBG devices tested in FY 2013.

1.1. SiC 1200 V, 7 A high-temperature package SJT

The static characteristics of the 1200 V, 7 A SiC SJT were obtained over a temperature range of 25 to 200°C at Ig= 200 mA for all the tests. The SiC SJT was tested at higher temperatures because it was packaged in a high-temperature metal package. The forward characteristics are shown in Figure II-26. The switching characteristics were obtained over a temperature range of 25 to 200°C at 400 V dc up to 7 A. The energy losses of the device for different currents are shown in Figure II-27.

Static characteristics of a 1200 V, 20 A normally-on SiC JFET for different operating temperatures are shown in Figure II-28. The forward characteristics were obtained for a gate voltage of +0 V. The forward voltage drop of the device at 15 A increased from 0.7 V at 25°C to 2.2 V at 175°C.
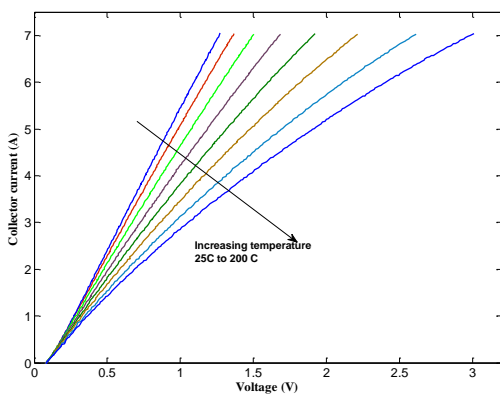
Figure II-26: The i-v curves of a 1200V, 7 A SiC SJT.
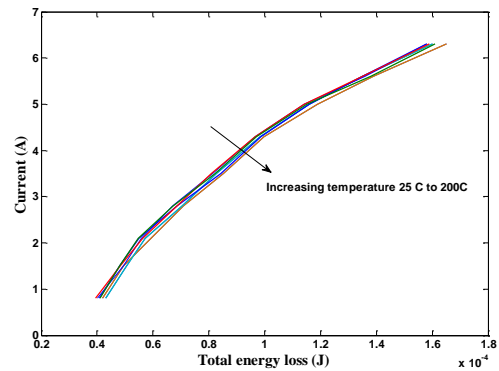
Figure II-27: Total switching energy losses of a 1200 V, 7 A SiC SJT at 400 V.
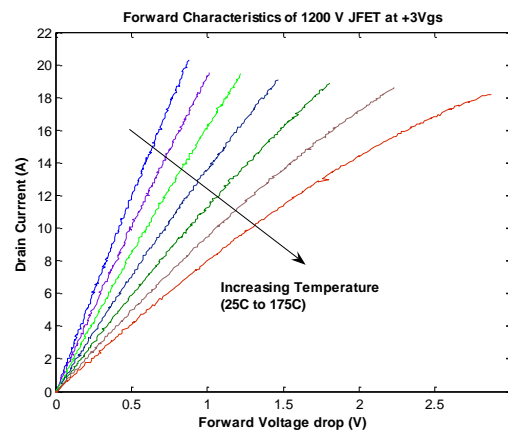
Figure II-28: The i-v curves of a 1200 V, 20 A SiC JFET.

The turn-on and turn-off energy losses of the JFET were obtained using a double pulse circuit with a load inductance of 360 µH; a 1200 V, 30 A SiC JBS diode was used as the clamping diode in the circuit. The gate driver used for this testing was a commercial gate driver board, SGDR600P1. The device requires constant current for the device to remain switched on, and this features demands more power from the gate driver. The data were obtained at 600 V dc for various currents at 25 and 175°C. The total energy losses increase with an increase in current; however, the losses do not change much with increasing temperature (Figure II-29).
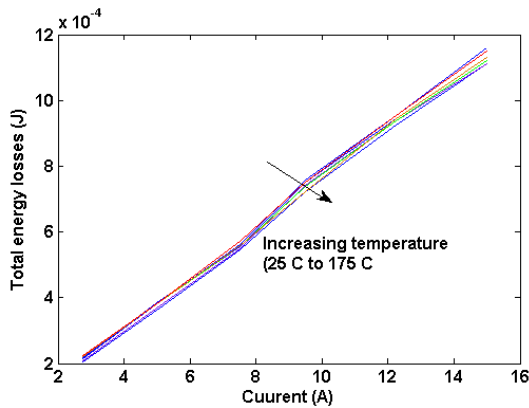
Figure II-29: Total switching energy losses of 1200 V, 20 A SiC JFET at 600 V.

1.2. 600 V, 5 A GaN FET

This normally-on FET is the first GaN-based device tested under the DOE VTO program. The static characteristics of a 600 V, 5 A GaN FET were obtained over a temperature range of 25 to 150°C at Vgs = +2 V (Figure II-30). The test setup for the dynamic characterization is shown in Figure II-31. A special test setup was designed to test the device with the pc board. An airflow system with an electrical isolation pad was used to heat the device to just under test, and the rest of the board components were at room temperature. The switching characteristics were obtained at 25 and 50°C at 300 V dc up to 2 A. The switching test waveforms are shown in Figure II-32. The energy losses of the device at a measured temperature of 48.4°C were turn-on losses 17.9 µJ, turn-off losses 7.2 µJ, for total energy losses of 25.1 µJ at 300 V, 2 A, ± 2 V Vgs.
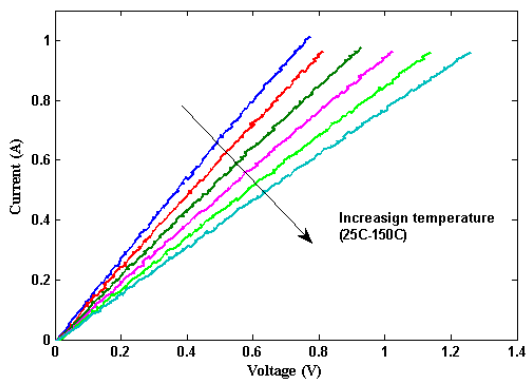
Figure II-30: The i-v curves of a 600 V, 5 A GaN FET.
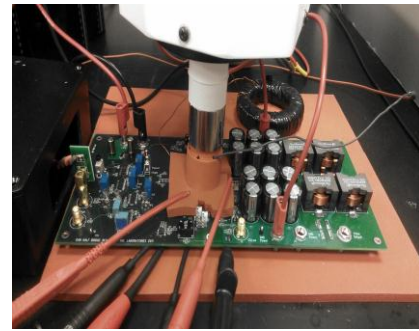
Figure II-31: Experimental setup for dynamic characterization of a 600 V, 5 A GaN FET.
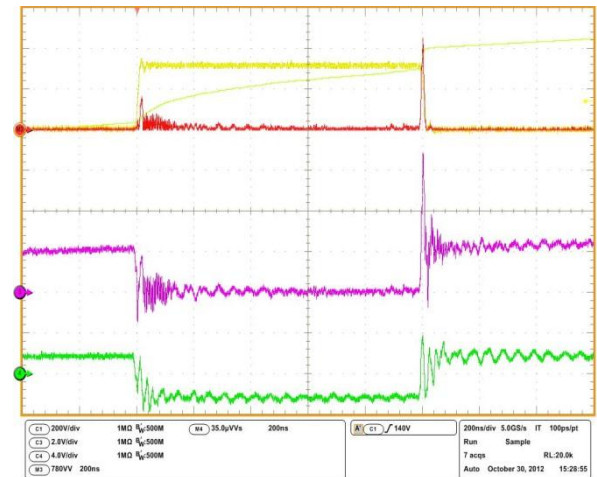
Figure II-32: Switching waveforms for a 600V, 5 A GaN FET at 300 V,2 A.

1.3. 2012 Nissan LEAF silicon module

In addition to the WBG devices, a 2012 Nissan LEAF Si power module was evaluated during FY 2013. The test setup is shown in Figure II-33. The Si module was tested over a temperature range of 25 to 150°C at 365 V and up to 200 A. The forward and switching characteristics are shown in Figure II-34 and Figure II-35. The data obtained were used in the LEAF system simulation model by the APEEM team at ORNL. In the future, these data will be used to compare WBG devices with Si devices.
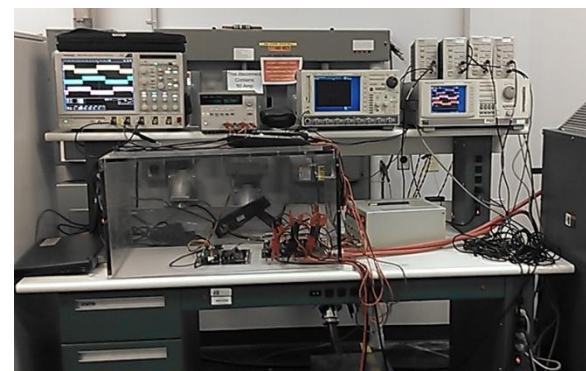
Figure II-33: Continuous test bench test setup.
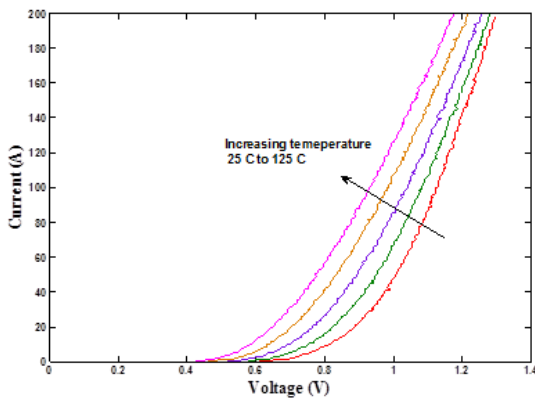
Figure II-34: The i-v curves of a 600 V, 600 A Si IGBT.
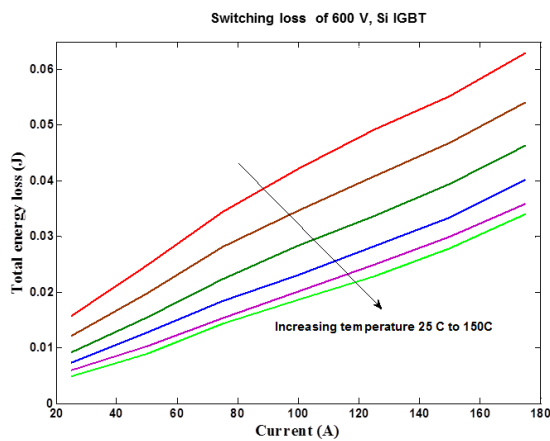
Figure II-35: Total switching energy losses of 600 V, 600 A Si IGBT.

2. Continuous test bench for evaluation on WBG devices

Figure II-36Figure 13 illustrates a conceptual single-phase test based on a conventional midpoint converter architecture. As mentioned earlier, the continuous test bed was set up to evaluate the performance of modules and gate drive electronics before they are used in power converters, to ensure reliable operation of the converter. For the 10 kW all-SiC inverter, the 1200 V, 100 A SiC modules and the new gate driver boards were evaluated for functionality. The setup is shown in Figure II-33. The single-phase converter was tested with a resistive load. The waveforms obtained from the test bed are shown in Figure II-37.

3. WBG Inverter Design and Development

3.1 Commercial module–based inverter design

The 10 kW all-SiC inverter was designed using a commercially available 1200 V, 100 A SiC metal oxide semiconductor FET (MOSFET)–based module. The module is shown in Figure II-38 and the layout of the inverter in Figure II-39. The total inverter volume is 3.6 L (226 × 224 × 73 mm). Commercially available gate drivers from Rohm were used. The gate driver has galvanic isolation up to 3000 Vrms and integrated overcurrent protection, undervoltage lockout, and temperature feedback. The performance of the

module was evaluated before the inverter was built. The cooling system for this prototype is a single-sided cooling commercially available heat sink. The modules were mounted on the heat sink, with thermal grease as the heat transfer medium from the lower side of the power modules. This prototype model will be packaged as shown in Figure II-39, with controls and capacitors packaged close to the heat sink. The capacitors used in this design are not a brick type but small individual capacitors in series to ensure better cooling and reduce costs.
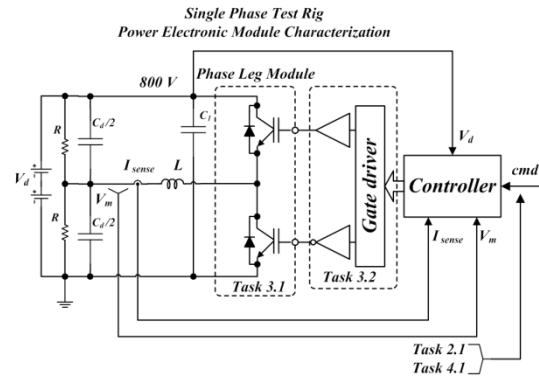
Figure II-36: Power electronic single-phase characterization.

Figure II-37: Single SiC H-bridge test waveforms obtained using the single-phase test bed. The tests were conducted at 250 V, 15 A continuous operation at 20 kHz.

Figure II-38: 1200 V, 100 A SiC MOSFET commercial module.
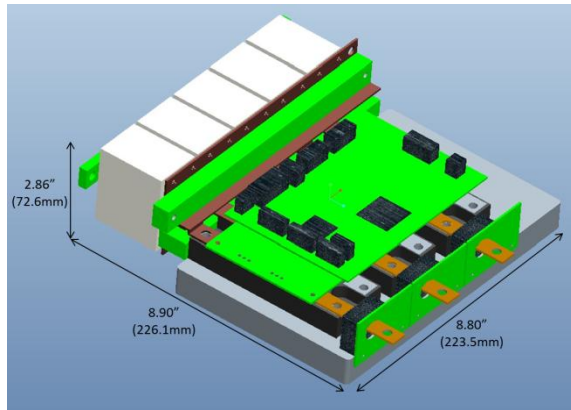
Figure II-39: The 10 kW SiC inverter layout.

3.1.1. Characterization of the SiC module

Figure II-40 shows forward characteristics of the (1200 V, 100 A) SiC MOSFET for operating temperatures from 25 to 150°C, in 25°C increments. SiC MOSFETs exhibit a linear relationship between voltage and current and have a positive temperature coefficient, which means their conduction losses will be higher at higher temperatures.
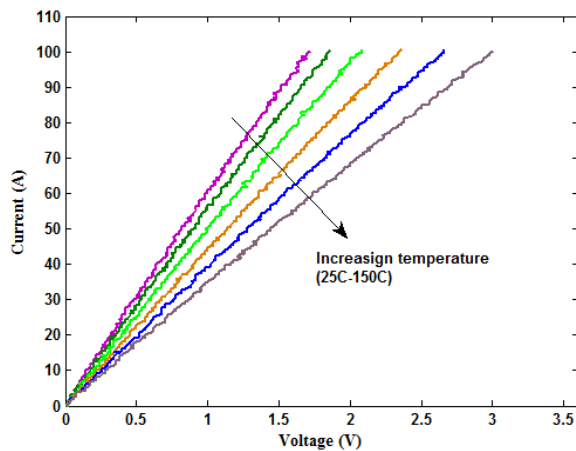
Figure II-40: Forward characteristics of 1200 V, 100 A SiC MOSFET module.

A standard commercial driver integrated circuit (IC) from Rohm was used in the drive circuit for both devices. The driver can provide a peak output current of 5 A with a maximum output resistance of 1 Ω. The maximum rise time is 45 ns for a capacitive load of 10 nF with VCC=24 V, according to the data sheet specifications. This feature enables the driver to supply a high dynamic gate current to the SiC MOSFET with a short rise-time. Switching measurements (double pulse tests) were performed to characterize the SiC MOSFET dynamically. The actual test setup is shown in Figure II-41. A load inductance of 120 µH was used for all the tests. The equipment used was a Tektronix DPO 7104 1GHz, a TEK differential probe P5205 100 MHz bandwidth, and a Pearson current probe to 2877 MHZ bandwidth. The total energy losses of the devices were obtained at 600 V and at different currents of up to 100 A (Figure II-42).
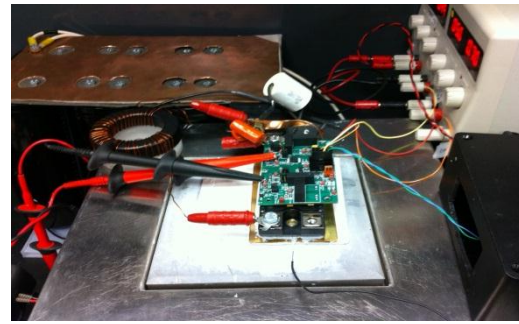
Figure II-41: Test setup for the SiC MOSFET module with a gate driver.
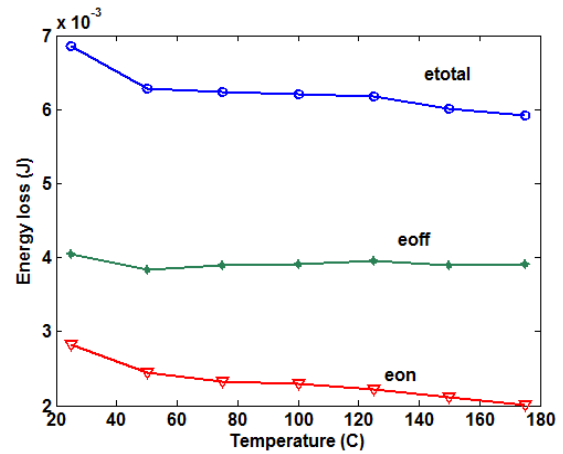
Figure II-42: Turn-on and turn-off waveform of 1200 V, 100 A SiC MOSFET module at 800 V.

3.2. ORNL module-based inverter design

To take advantage of the high-temperature operating capability of WBG devices, device packages that can withstand high temperatures are required. Various organizations are working toward high-temperature packaging for high-temperature devices. Several high-temperature packages have been reported in recent years that include discrete device packages to power modules. This project focuses on the development of high-power-density power modules, which will enable size and volume reductions at the system level by integrating low-temperature components with high-temperature active devices and reducing the amount of material used to build the heat exchangers in inverters. This prototype uses single-sided cooling for the power modules, which are mounted using spring pressure. Thermal grease serves as the heat transfer medium from the lower side of the direct-bond copper (DBC) boards. This model of the prototype will be packaged as shown in Figure II-43, with controls and capacitors closely packaged to the heat sink.
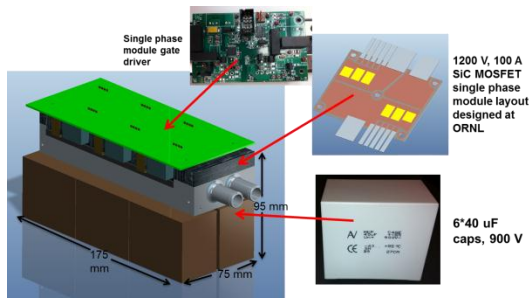
Figure II-43: Layout of the 10-kW SiC inverter.

3.2.1. Power module development

An SiC MOSFET-based phase-leg module designed and developed in the internal packaging facility at ORNL is shown in Figure II-44. Figure II-45 shows the layout of the die and interconnection pattern. The module includes four SiC MOSFETs and two SiC diodes, which form a totem pole or phase leg (half-bridge) configuration, a building block for an inverter. The package is designed to work at a temperature of at least 200°C ambient. The electrical interconnection is achieved by bonding aluminum (Al) wires on top of the dies and soldering dies on the Cu traces of DBC substrates, which offer electrical insulation with their ceramic slice inside. The layout of multiple SiC dies on the DBC substrate and their interconnections has been optimized to reduce parasitic electric parameters.

Figure II-44: ORNL high-temperature SiC phase-leg module.
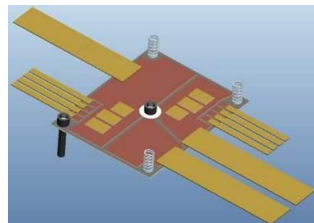
Figure II-45: Power module layout design.

3.2.2. Characterization of the SiC module

Figure II-46 shows forward characteristics of the (1200 V, 100 A) SiC MOSFET for different operating temperatures from 25 to 150°C in 25°C increments. SiC MOSFETs exhibit a linear relationship between the voltage and current and can be modeled as resistors.
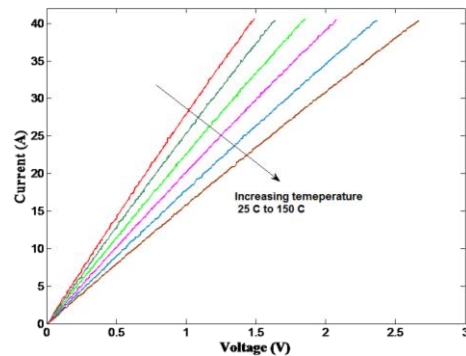
Figure II-46: Forward characteristics of 1200 V, 50 A SiC module.

A standard commercial driver IC from IXYS, IXDN509, was used in the drive circuit for both devices. The driver can provide a peak output current of 9 A with a maximum output resistance of 1 Ω. The output stage of the drive includes resistor R2 and capacitor C1 for transient current and parallel resistor R1 for static current. The device turn-on and turn-off times are controlled by selecting the values of capacitor C1, and the resistor dampens the oscillation caused by C1 and the parasitic inductance of the circuit. A negative gate voltage of −5 V was chosen for the SiC MOSFET. The resistor R1 in the range of 9–15 Ω for Vcc of 20 V, the capacitor C2 in the range of 10–100 nF, and the resistor R2 in the range of 1–7 Ω were tried to achieve a high dynamic gate current during switching. A schematic of the gate drive circuit topology is shown in Figure II-47.

Switching measurements (double pulse tests) were performed to characterize the SiC MOSFET dynamically. The actual test setup is shown in Figure II-48. A load inductance of 120 uH and a 1200 V, 30 A SiC JBS freewheeling diode were used for all the tests. The total energy losses of the devices were obtained at 800 and 600 V and at different currents up to 35 A (Figure II-49 and Figure II-50).
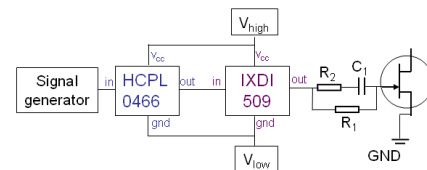
Figure II-47: Schematic of the drive circuit.
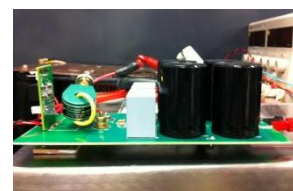
Figure II-48: Experimental test setup for dynamic characterization of the 1200 V, 100 A SiC module.
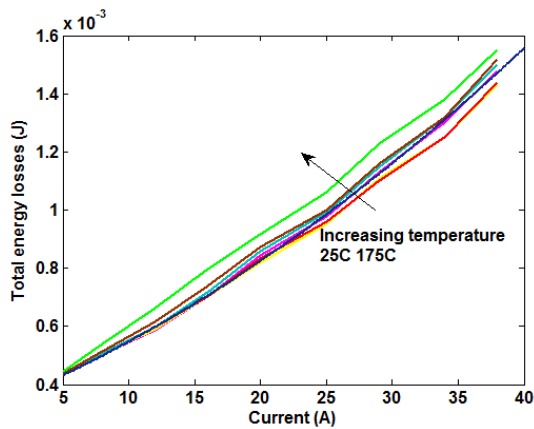
Figure II-49: Total energy losses of the SiC MOSFET at 600 V.
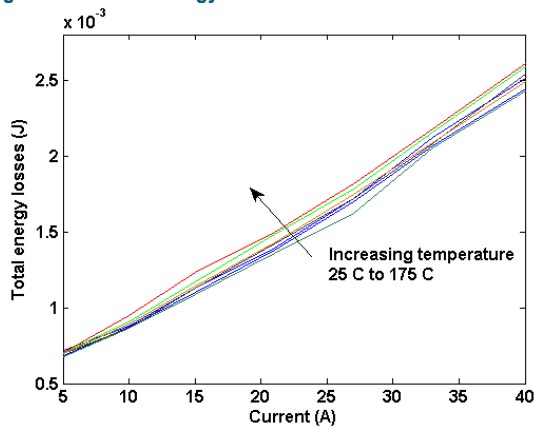
Figure II-50: Total energy losses of the SiC MOSFET at 800 V.

4. Inverter Assembly and Testing

The final inverter assembly inverter is shown in Figure II-51. For this test, the dc-link voltage was fixed at nominal operating voltage (325 V) to the maximum bus voltage (450 V). The load resistance was set to the minimum value, and the current was controlled by changing the modulation index. The coolant was set at 20°C at a flow rate of 1.5 gpm. The open-loop frequency of operation and the PWM frequency were fixed and the current command was varied for a particular dc-link voltage. The command current was increased in steps without exceeding the power rating of the inverter or of the load. The coolant temperature was changed to 60ºC and data were recorded for a wide range of current and switching frequencies. The experimental waveforms for 325 and 450 V operation are shown in Figure II-52.

Figure II-51: Final assembled inverter prototype.

(a)

(b)

(c)

Figure II-52: Experimental waveforms of 10 kW SiC inverter. (a) 450 V dc-link voltage (b) screen shot of 325 V dc-link operation (c) screen shot of 450 V dc-link operation.

The efficiency versus output-power plot for several operating conditions, comparing efficiencies at different voltages, is shown in Figure II-53. Inverter efficiencies are higher at the 450 V than at the 325 V operating condition, as expected. Figure II-54 shows that the inverter efficiency does not change much as the switching frequency increases. The overall inverter efficiency is ~98% for different operating conditions.
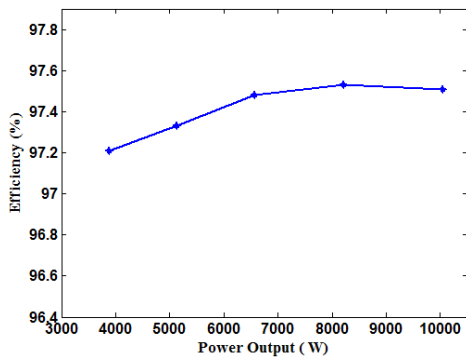
Figure II-53: Inverter efficiency vs. output power.
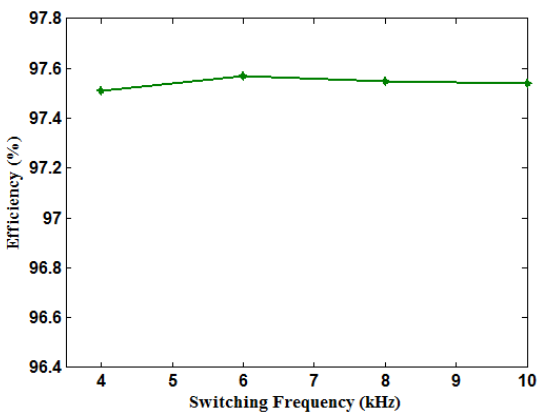
Figure II-54: Inverter efficiency vs. switching frequency.

5. Air-Cooled inverter

ORNL has worked with the National Renewable Energy Laboratory (NREL) to develop an air-cooled inverter to further optimize the thermal design. The air-cooled inverter developed in FY 2011 was redesigned using thermal simulations from NREL. The initial inverter size was reduced by 33% through fin design optimization (Figure II-55). Balance-of-plant analysis is currently being conducted to establish the feasibility of air cooling at the system level.
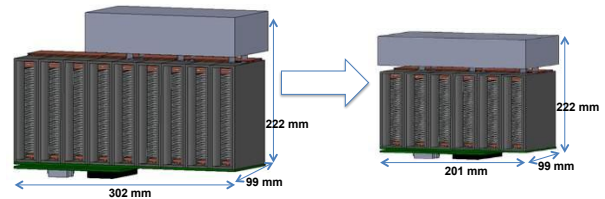
Figure II-55: Air-cooled inverter design layout.

Conclusion and Future Directions

WBG device evaluation will continue until the technology transitions to industry. The inverter test results obtained this year will be used as a benchmark for a next-generation inverter to be built using ORNL PEEM's WBG package. The results obtained show that if the inverter is scaled to 30 kW, it will meet the 2020 VTO targets. They also show that WBG technology will aid in achieving U.S. DRIVE targets for volume, efficiency, power density, and system costs.

II.3. Benchmarking Competitive Technologies

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Start Date: October 2012
Projected End Date: Ongoing

Objectives

- Benchmark HEV/EV components
  - Assess design, packaging, and fabrication innovations in subsystems and components
    - Determine techniques used to improve specific power and power density and reduce cost.
    - Perform compositional analysis of key components.
  - Examine performance and operational characteristics during comprehensive tests and evaluations
    - Obtain peak torque and power capability
    - Identify detailed information regarding time-dependent and condition-dependent operation
  - Compile information from evaluations and assessments
    - Identify new areas of interest
    - Compare results with other EV/HEV technologies and DOE targets.

Technical Barriers

- Integrating custom ORNL inverter-motor-controller with original equipment manufacturer (OEM) components
  - Optimizing controls for nonlinear motors throughout operation range
- Intercepting, decoding, and overtaking OEM controller area network (CAN) signals
- Adapting nonstandard motor shaft and assembly to dynamometer and test fixture

Technical Targets

- This project helps with program planning and the establishment and verification of all DOE 2020 targets.

Accomplishments

- Overall: Conducted thorough benchmark assessments and reported on many HEV/EV technologies, including the following:
  - 2004 Prius, 2006 Accord, 2007 Camry, 2008 Lexus LS 600h, 2010 Prius, 2011 Hyundai Sonata motor, 2012 Nissan LEAF, 2012 Hyundai Sonata hybrid starter-generator (HSG)
- FY 2013
  - Conducted comprehensive teardown assessment and testing/evaluation of the 2013 Nissan LEAF 6.6 kW onboard charger
  - Procured and disassembled 2013 Toyota Camry power converter unit (PCU) and determined device characteristics
  - Performed dynamometer testing of Remy induction motors (IMs; one with Al and one with Cu rotor bars)
  - Performed dynamometer testing of the 2012 Hyundai Sonata HSG

✧   ✧   ✧   ✧   ✧

Introduction

Benchmarking plays an important role in program planning efforts by defining the current state of the art for components and subsystems, defining performance and design metrics for DOE's competitive R&D efforts, and identifying technology gaps to provide guidance on future research focus areas. To establish practical targets, baseline technological status must be obtained from subsystems currently in the marketplace. Therefore, benchmarking cutting-edge technologies in competitive global markets establishes a solid technology baseline for the DOE APEEM program. It also assists in determining if performance goals established for the program are realistically achievable and if they present sufficient challenge to warrant a robust program.

Benchmarking activities also ensure that the DOE APEEM program will not duplicate technical innovations found in commercially available technologies. They provide technical insight, allowing the DOE program to move more rapidly by maintaining awareness of current trends and technical innovations in advancing on-the-road technologies. Findings and results from the benchmarking efforts are detailed in reports and presentations. These publications are frequently cited in technical conference papers and have received high recognition from industry, academia, and car enthusiasts.

Approach

Appropriate HEV and EV components are selected by DOE based on information from the Internet, technical publications, published specifications, and feedback from automotive manufacturers and suppliers. Several components were evaluated in FY 2013 and each is discussed in the following sections.

2013 Nissan LEAF 6.6 kW charger

With the recent advent of the first mass-produced fully-EV, the Nissan LEAF, it is important to note that the onboard charger (OBC) is a critical component that impacts overall efficiency and the cost to operate the vehicle. The charger requires several power stages and many components, so there are significant associated cost and design requirements. The Nissan LEAF inverter and motor were benchmarked by ORNL in FY 2012 and the results published. The 2012 LEAF includes a 3.3 kW OBC, and the 2013 LEAF upgraded to a 6.6 kW charger, both of which accept ac power in standard forms (i.e., 120 and 240 V). A separate "fast-charging" port is available that accepts dc power from a large off-board charger.

The focus of DOE's APEEM program is on components and subsystems; therefore, the entire vehicle was not procured and used during analyses of the LEAF's OBC. Various standards (namely SAE J1772) are in place to regulate charger functionality and impact on grid power quality (IEEE 519). Since harmonic analysis for total harmonic distortion (THD) and other metrics related to standards requires the entire system, ORNL focused on obtaining design, functionality, and operational characteristics at a detailed subsystem level. This includes destructive teardown and invasive investigations to determine the layout and connectivity of all items in the charger. ORNL evaluated the operation of converter stages by implementing custom-developed control algorithms, and plans are being developed to compare the custom controls and ensure that they closely mimic OEM controls on a fully operational vehicle.

2013 Toyota Camry power converter unit

The 2013 Toyota Camry was selected for Stage 1 benchmarking assessments, which include disassembly for design, functionality, and volumetric assessments as well as device characterization. Although this does not include testing on a dynamometer, valuable information in regard to advancing on-the-road technology can be gained without devoting the resources required for full dynamometer testing. This facilitates the capability to obtain benchmark information on the components while components from other vehicle models are prepared for evaluation with a dynamometer.

Remy induction motor testing

The most common type of electric motor used in EV/HEVs is the permanent magnet (PM) motor with neodymium-iron-boron magnets. Recent R&D efforts involve the development of electric motors that do not use RE materials, which have a history of high and uncertain costs. The IM is a possible alternative, but in general, detailed operational characteristics (such as efficiency maps) are not readily available for induction motors. Remy offered to provide ORNL with two pre-production IMs, one with Cu rotor bars and one with Al rotor bars. ORNL designed and fabricated the appropriate high-precision shaft and alignment/support fixture. Additionally, ORNL implemented an inverter drive system and developed motor control algorithms to optimize motor operation with respect to efficiency.

2012 Hyundai Sonata hybrid starter-generator

The Hyundai Sonata HSG was chosen because it is seen as a component that can facilitate the hybridization of existing vehicle product lines. The HSG is slightly larger than a conventional alternator, yet it replaces not only the alternator but also the starter for the combustion engine. It is belt-driven by the engine crankshaft pulley, and it is more efficient than a conventional alternator since it operates at the hybrid battery voltage (270 V) as opposed to the conventional alternator/battery system 12 V. The primary hybrid motor of the Hyundai Sonata is about the same size as the non-hybrid's automatic transmission torque converter, and it essentially replaces the torque converter. Therefore, this is a convenient approach to hybridizing an existing vehicle design without major modifications to the drivetrain components. The HSG was tested on a dynamometer in both motoring and regenerative mode. The primary drive motor was benchmarked in FY 2012 and the results were published.

Results

2013 Nissan LEAF 6.6 kW charger

Design and functionality assessments

The 2013 Nissan LEAF charger is shown on the upper left in Figure II-56. As received, the mass of the charger was about 16.3 kg, which includes the mass of the external off-white line filter and its support bracket weighing a total of 3.2 kg. The main charger assembly width and length are about 9.9 and 10.9 in., and the height varies from about 3 to 4.5 in., giving a volume of approximately 11.1 L. Using these metrics with a power rating of 6.6 kW, the specific power and power density are 0.4 kW/kg and 0.6 kW/L, respectively. These figures seem quite low, but it should be noted that the charger operates continuously at a power level of 6.6 kW, and isolation and power quality specifications required by standards ultimately require additional components.

The underside of the charger assembly is also shown in Figure II-56, where cast (then machined) Al channels for liquid cooling with a water ethylene-glycol mixture are visible. The internal compartment includes a control-communication circuit board, a driver and signal conditioning board, a black power module, large passive components for various charger stages, and many smaller devices and peripheral passive components. The control board includes a Renesas R5F71476FPV microcontroller, which is the type of microcontroller used for the Nissan LEAF motor controller.

The block diagram in Figure II-56 describes the various stages of the OBC and indicates where the associated devices are located in the power module. The corresponding circuit schematic is shown in Figure II-57 and Figure II-58.
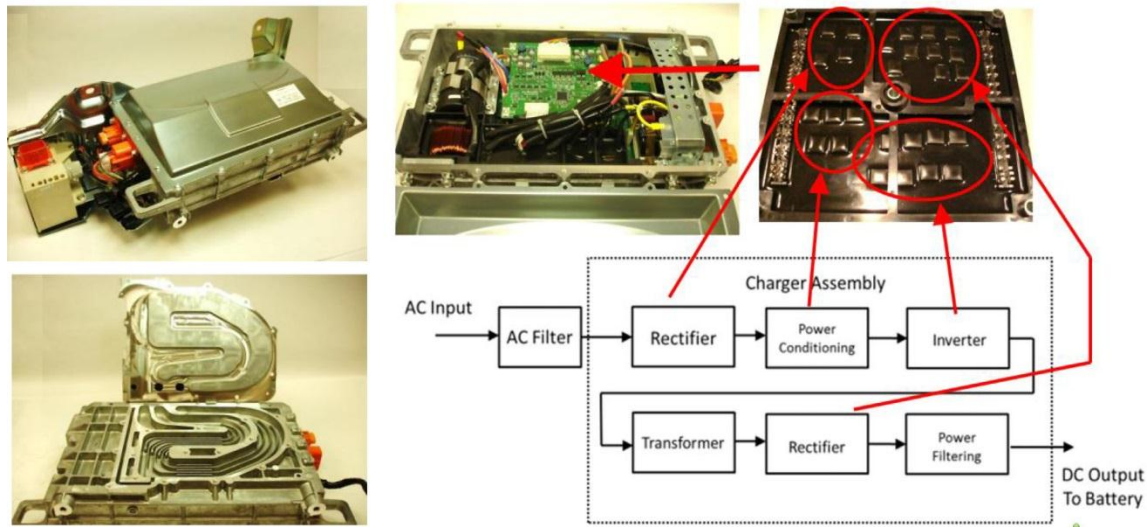
Figure II-56: Nissan LEAF charger ac input and boost-PFC.
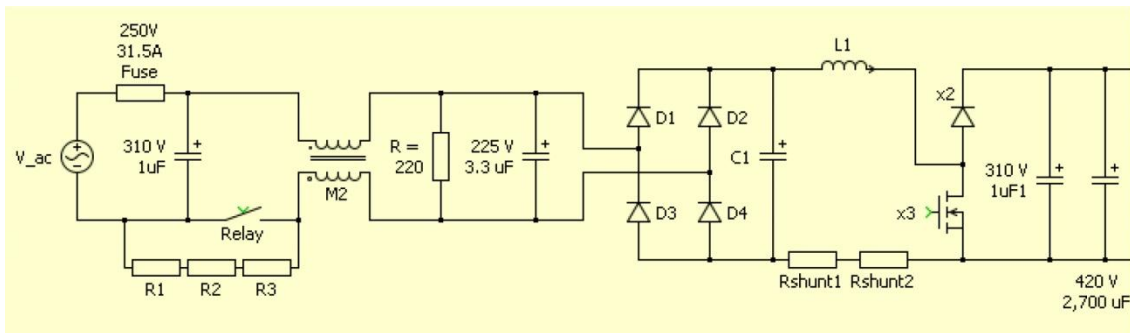
Figure II-57: Nissan LEAF charger ac input and boost-PFC.
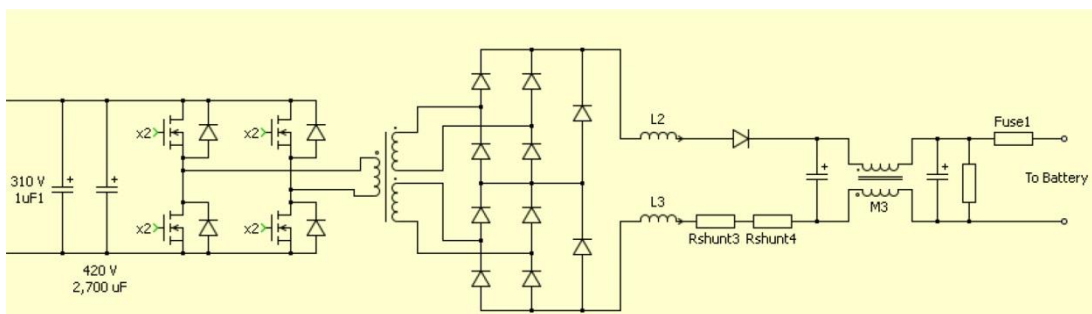
Figure II-58: Nissan LEAF charger isolation and rectification stage.

Note that the latter two figures are actually one schematic, but they are separated for image clarity. Also note there is only one 310 V, 1 µF and 420 V, 2,700 µF capacitor in the circuit, and it is duplicated in both figures as a reference item. After the external line filter, the ac input of the charger is fused and additional filtering (including common mode) is applied with relatively small passive components. A relay remains open until ac voltage has been applied for a certain amount of time to avoid high in-rush currents by charging system capacitors through three resistors. The first conversion stage of the charger is a conventional rectifier with four diodes. The next stage is a boosting power factor correction (PFC) stage, which includes three MOSFETs in parallel for chopping action, and two diodes in parallel to prevent reverse current and to allow energy to be stored in the inductor as the MOSFETs are active. The boosted voltage is regulated to between about 360 and 400 V, and a large 420 V, 2,700 µF electrolytic capacitor is located at the boosted output.

The final stages of the charger, shown in Figure II-58, include an H-bridge inverter with two MOSFETS for each switch and one small anti-parallel diode for each switch. The inverter drives the primary coil of the large isolation

transformer, which has two secondary windings. Output from the two secondary windings is fed to two full-bridge rectifiers, with outputs placed in series and balancing diodes in parallel with each rectifier. In total, ten diodes are located in the final rectification stage. The rectified output is fed through two large inductors, a diode (not located in the power module), a common mode filter, and small passive filters before passing through the output connector that connects to the battery.

The battery voltage varies with the state of charge; therefore, the output voltage of the charger must have a fairly wide range to maintain a constant charging power level and avoid overcharging conditions. It can be roughly estimated that the charger output voltage is in the range of 300–400 V for normal charging conditions.

Testing and characterization

Since the operation of the charger is largely dependent on battery characteristics and OEM controls, as the charger is operating with the battery pack, ORNL performed basic operational tests to verify assessments made during functionality studies. ORNL is working to establish a collaboration with other organizations that perform full-vehicle assessments to verify and analyze in situ operational characteristics. However, the invasive efforts required to obtain this information create a difficulty: there is some risk of compromising vehicle integrity/value, and most test vehicles are borrowed or will be used in company fleets. Nonetheless, system-level efficiencies are easier to obtain. Argonne National Laboratory performed full-vehicle testing and reports that the 3.3 kW 2012 LEAF charger and EV service equipment have a total efficiency of about 86.3%, which is the efficiency from the ac receptacle to the dc power input to the battery.

In carrying out basic operational tests, it was discovered that the driver circuitry for the H-bridge inverter is unconventional, as the MOSFETs are controlled with only the power isolation transformer and no additional control signal isolation (i.e., optocoupler) is used. This is possible largely because the H-bridge is controlled with phase-shift control and therefore variable pulse width is not used. Additionally, it appears that the dead-time is generated on the output of the secondary with passive components.

2013 Toyota Camry power converter unit

Design and functionality assessments

The 2013 Toyota Camry PCU is manufactured by Denso and has a total mass of 15.3 kg and a volume of about 12.3 L. The PCU, shown in Figure II-59, serves functions similar to those of many Toyota PCUs, including motor inverter, generator inverter, bi-directional boost converter, and dc-dc converter to convert the hybrid battery voltage to 12 V for auxiliary loads. Note that the first-generation Camry PCU does not include the 12 V dc-dc converter. The boost converter boosts the hybrid battery voltage of about 244 V up to a maximum of 650 V. Sections of the PCU are labeled on the right side of Figure II-59. The uppermost portion of the PCU contains the control and driver circuitry, which is shown in Figure II-60. The upper middle section contains the power modules, cooling infrastructure, and boost inductor; and the lower middle section houses the large capacitor module. The bottom section contains the 12 V dc-dc converter, and the output terminal is labeled accordingly.

Figure II-59: 2013 Toyota Camry power converter unit.
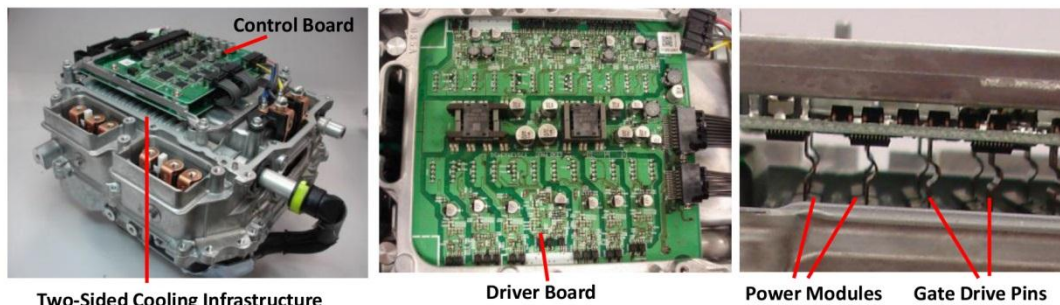
Figure II-60: 2013 Toyota Camry circuit boards.

The mass and volume of the 12 V dc-dc converter are roughly 3.1 kg and 1.45 L, and the boost converter, motor inverter, and generator inverter account for about 12.2 kg and 10.9 L. The PE devices for the boost converter and both inverters are located together; they were in separate locations in previous Camry designs. This transition has been made in most recent Toyota/Lexus PCUs.

There are a total of 12 phase legs, three dedicated to the 3-phase generator inverter, six (two in parallel for each phase) used for the inverter, and three in parallel for the boost converter. Therefore, the motor inverter mass and volume can be approximated to be about 6.1 kg and 5.5 L, respectively. Using the published motor power rating of 105 kW, the specific power of the motor inverter is 17.2 kW/kg and the power density is 19 kW/L.

The 105 kW power rating has not been verified during dynamometer testing. Also, a critical factor that yields improved power density and specific power is the high voltage enabled by the boost converter (and partially by regenerative power from the combustion engine via the generator). If the boost converter mass and volume are included with the motor inverter, the power density and specific power are 12.7 kW/L and 11.5 kW/kg, respectively. Even so, these metrics are the highest for any PCU benchmarked thus far, and the improved performance is largely due to the use of power modules that are cooled on both sides.

The 2013 Toyota Camry PCU closely resembles that of the 2008 Lexus LS 600h, which also uses power modules with two-sided cooling. Each module includes one IGBT and one diode with control and sensing pins protruding upward to the driver board (Figure II-60) and Cu collector and emitter bus bars extending downward to the phase output and the negative or positive dc bus (Figure II-61). Thin ceramic sheets are located between both sides of the module and the adjacent cooling infrastructure, with thermal paste on both sides of each insulator. A large metal arch support is used to apply substantial mechanical pressure to the entire stack-up of power modules to ensure sufficient heat transfer is achieved.

A clear advantage of using power modules with two-sided cooling is realized by comparing the number of Si devices with that in the previous generation. For each switch, the previous generation used three IGBTs/diodes in parallel, whereas the current generation uses only two IGBTs/diodes for the same power rating. In 2008, it was not clear whether Toyota was pursuing this type of design for mass-produced vehicles, as the 2008 LS 600h luxury sedan had relatively low production volume and a base sale price of $104,000. Although fewer devices are used in the current design, there are cost tradeoffs with the Cu bus bar infrastructure, costly ceramic insulators, and increased requirements to overcome mechanical stresses due to mismatching of coefficients of thermal expansion on both sides of the power devices.
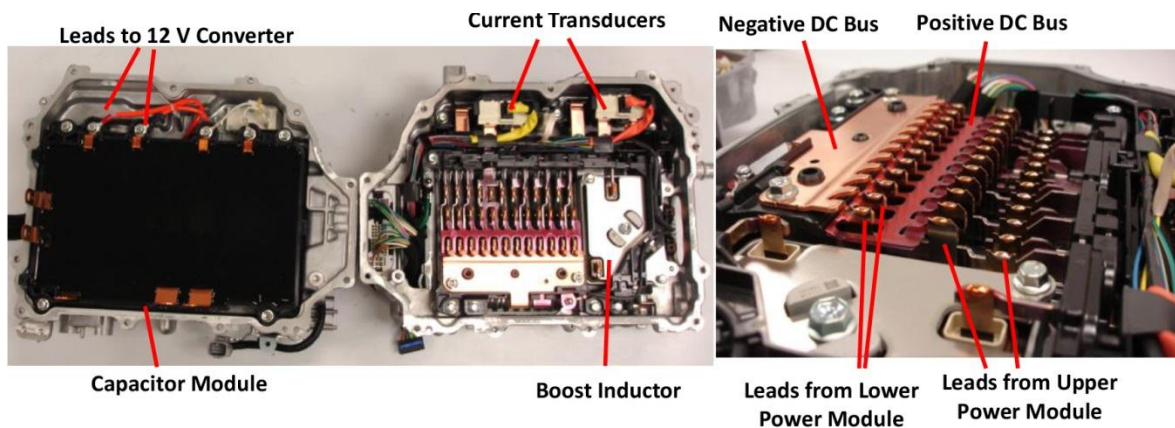
Figure II-61: 2013 Toyota Camry capacitor, dc bus, and power modules.

A 420 V, 320 μF boost capacitor (connected to the battery input) and 750 V, 1,600 μF dc link capacitor are both located in the same module. It is manufactured by Panasonic and it contains internal bus bars that connect the battery input to the dc link and boost inductor, a ~70 kohm bleed resistor, and the 12 V dc-dc converter. In addition to the two-sided cooling infrastructure, a cast Al heat exchanger cools the 12 V dc-dc converter, which mates to the bottom of the cooling surface. The capacitor mates to the top side of the heat exchanger, but there is no additional material (e.g., thermal paste) to facilitate thermal coupling between the case of the capacitor module and the heat exchanger.

Overall, compared with the 2008 LS 600h PCU, it is clear that the design and packaging of the 2013 Camry PCU has been improved with less wasted space, simpler bus bars, and

reduced driver and control circuit board complexity. It will be interesting to see if Toyota will use the two-sided cooling approach in other product lines.

Testing and characterization

Device characterization was performed on an IGBT from one of the 2013 Camry power modules. The current vs. voltage characteristic curve is provided in Figure II-62. At 200 A, the forward voltage drop of the IGBT is about 2 V. Therefore, the power loss at this operation point is about 400 W, and with two in parallel (for the motor inverter), the total conduction loss is 800 W at this operation point. The peak current required by the motor to produce peak torque is estimated at between 400 and 500 A. To derive inverter efficiency, switching losses and diode losses also need to be included, but for six-step operation at high speeds, switching

loss contributions drop significantly, and so it is possible to attain inverter efficiencies above 99%, considering the peak power of 105 kW.
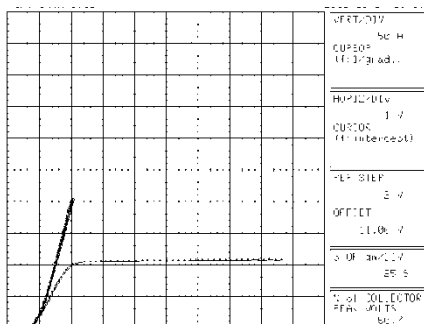
Figure II-62: 2013 Toyota Camry device characteristics.

Remy induction motor characteristics

Remy provided 3-phase IMs with 10 poles, a maximum dc voltage of 700 V (~480 V peak ac), and a maximum current of 300 A (rms). The motor is cooled with automatic transmission fluid and has a maximum speed of 10,600 rpm. As shown in Figure II-63, simulation results from Remy predicted that the motor will produce a peak torque of about 320 Nm, a peak power of 180 kW, and efficiencies above 90% for peak power operation points over much of the operational speed range.
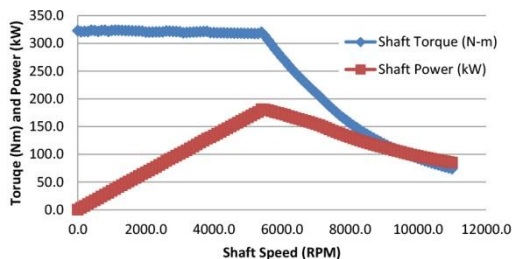
Figure II-63: Simulated performance of induction motor.

Design of a mechanical interface was required to adapt the IM to ORNL's test setup. As shown in Figure II-64, a custom high-precision face-mount adapter and spline adapter shaft were designed and fabricated by ORNL. Also shown in Figure II-64 is the IM on the dynamometer test system with the oil cooling system. Both peak torque and efficiency results have been verified, but operation at a peak power of 180 kW has not yet been verified. ORNL is working with Remy to ensure proper control conditions are being met; detailed performance and efficiency information will be reported thereafter.
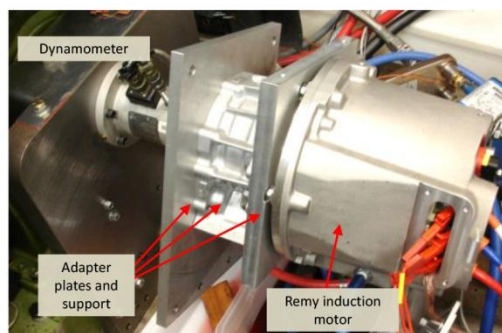
Figure II-64: Adapter, shaft, and Remy induction motor in dynamometer test cell.

2012 Hyundai Sonata hybrid starter-generator

Design and functionality assessments

Although the PCU of the Hyundai Sonata hybrid has been reported upon in the past, a brief overview will be given since the PCU also contains the controls and PE that drive the HSG. The PCU assembly is shown in Figure II-65, where the compartments are identified according to their functionality. Both the HSG and primary motor operate off the same dc link, which is connected to a battery with a nominal voltage of 270 V. A water ethylene-glycol mixture cools the PCU, which has a cast Al heat exchanger. The upper section contains the 270 to 12 V dc-dc converter, and the lower section contains the HSG and motor drive components with interconnects labeled accordingly.

HSG and motor control boards are shown on the left in Figure II-66, with details regarding integrated circuitry and other notable information indicated. As shown on the right in Figure II-66, the HSG and motor PE modules are the same size, although the published power ratings for the HSG and primary motor are 8.5 kW and 30 kW, respectively. Detailed information about the PE module is shown in Figure II-67. Inverters for both the HSG and motor use two IGBTs and two diodes in parallel for each switch of the 3-phase inverter, giving a total of 12 IGBTs and 12 diodes. The IGBTs and diodes in the HSG inverter are roughly 8.9 by 6.0 mm and 6.6 by 4.0 mm, respectively. These are notably smaller than the IGBT and diode dimensions of the motor inverter, which are 10.2 by 9.7 mm and 9.2 by 5.41 mm, respectively.

The HSG assembly, shown in Figure II-68, is slightly larger than a conventional alternator. It mounts to the side of the engine and is belt-driven, similar to a conventional alternator. Published specifications for the HSG indicate that it is capable of producing a peak torque of 43 Nm and peak power of 8.5 kW and operating at up to a maximum speed of 15,750 rpm. The HSG replaces the conventional starter (which is gear and sprocket driven); it starts the engine from a cold start and restarts during stop-and-go driving conditions. Additionally, the HSG operates as a generator when the battery has a low state of charge, allowing the engine to replenish the battery pack even when the vehicle is not in motion. The overall mass and volume of the HSG are about 12 kg and 3.1 L, respectively.

The stator and rotor of the HSG, shown in Figure II-69, have masses of 5.1 kg and 2.0 kg, respectively. The 3-phase machine is an IPM machine with 36 stator slots and six poles, as is evident by the magnets shown on the right in Figure II-69. Each rotor pole consists of two magnets along the axial direction of the rotor. This is a common practice, as eddy currents within the magnets are reduced by segmenting them along the axial direction, an effect similar to that of using laminated steel. A resolver, shown in Figure II-68, is used for absolute position sensing. It has 12 stator poles and 3 salient lobes on the rotor. A thermistor is installed in the stator windings to monitor motor operation temperature, and it is accessed via the same connector as the resolver.
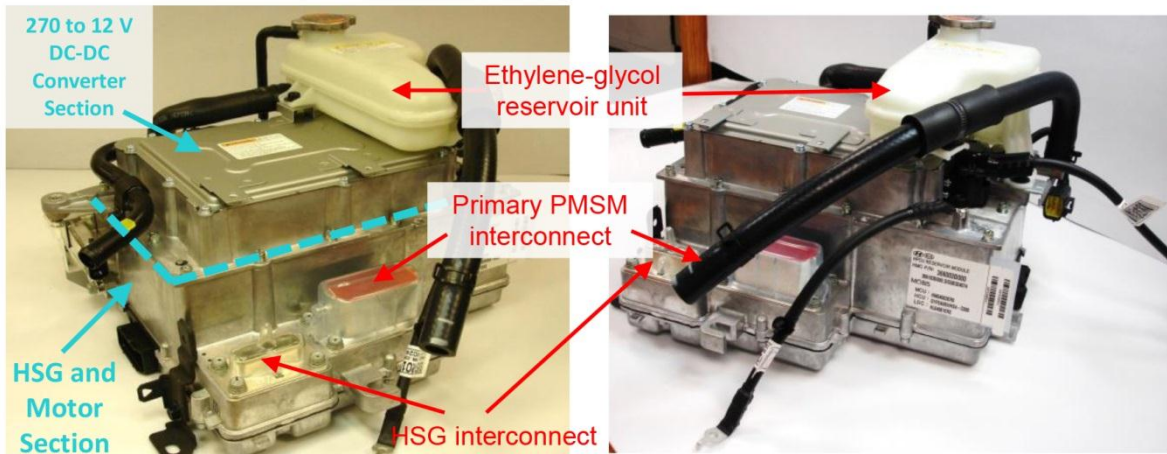
Figure II-65: 2012 Hyundai Sonata power converter unit.
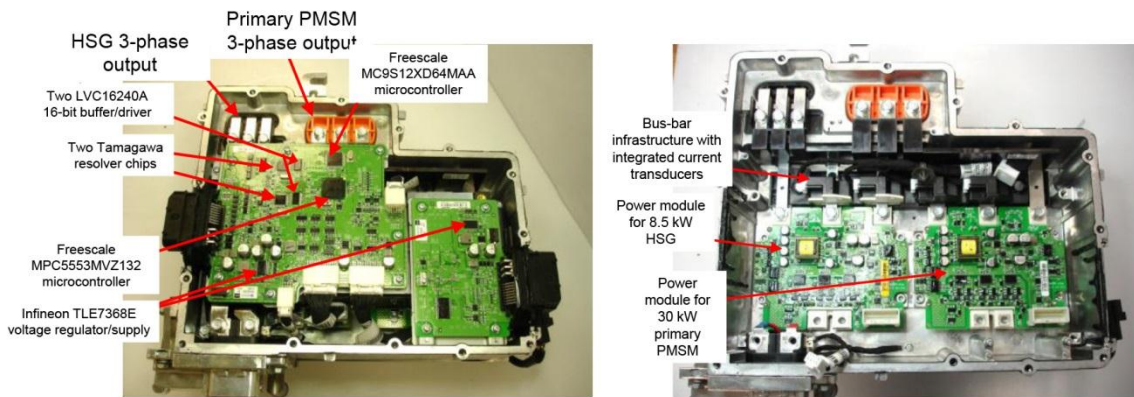
Figure II-66: 2012 Hyundai Sonata control boards (left) and power modules (right).
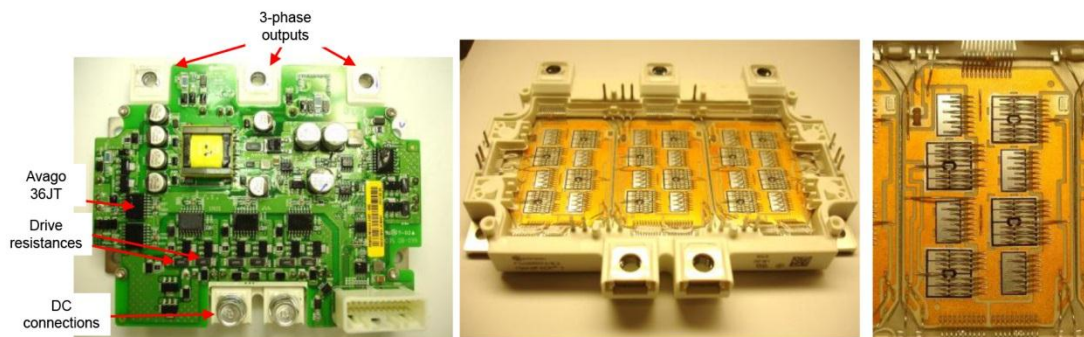
Figure II-67: 2012 Hyundai Sonata HSG power module.
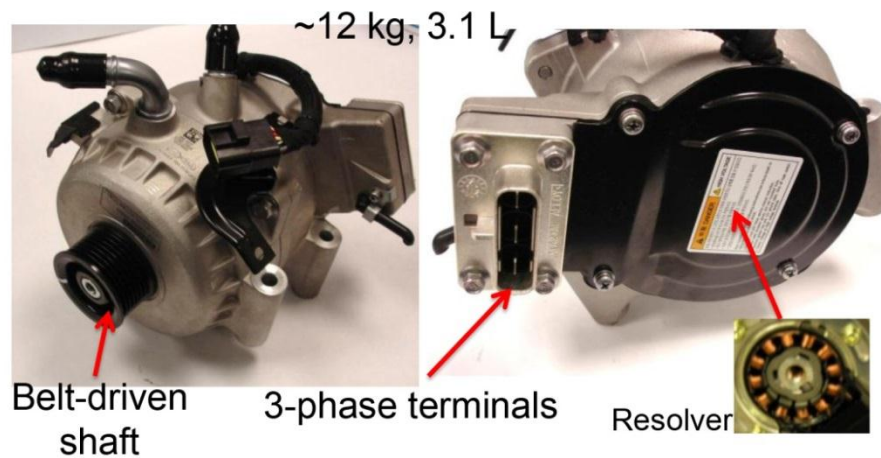
Figure II-68: 2012 Hyundai Sonata HSG assembly.
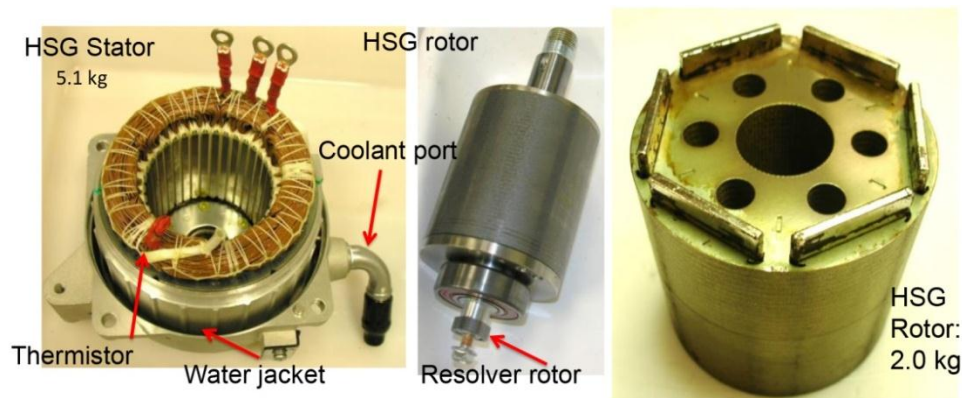
Figure II-69: 2012 Hyundai Sonata HSG components.

Testing and characterization

The HSG was tested using the OEM PCU but with custom motor software controls developed and implemented by ORNL. Both motoring and regenerative operate mode were analyzed while efficiency, various temperatures, dc voltage, dc current, ac voltages, ac currents, mechanical power, ac electrical power, dc electrical power, and many other metrics were recorded at each operation point. The efficiency map in Figure II-70 indicates the measured HSG efficiency as it operated in motoring motor. It can be seen that the peak efficiency is about 88% for high loading between 6,000 and 8,000 rpm. Note that belt losses are included in this efficiency map, and in general they contribute 1–2% of the loss at high power levels and about 3–6% of the loss at low and moderate load levels.

One major finding of the tests is that the HSG actually operated above 20 kW, although the published power level is only 8.5 kW. All efficiency maps have a light-grey trace superimposed for operation at 8.5 kW and a light-green trace superimposed for operation at 20 kW. These curves simply portray the torque required to produce the given power level (8.5 or 20 kW) at each speed. This gives a clear picture of the nature of operation above 8.5 kW and 20 kW. Note that the peak efficiency is only 84% if the HSG operates within the published 8.5 kW power rating.

An efficiency map for the HSG inverter during motoring mode is shown in Figure II-71. The peak HSG inverter motoring efficiency reaches above 98% even if operation is kept below 8.5 kW. The combined (inverter and motor) efficiency map for motoring operation is shown in Figure II-72. A peak combined efficiency of 87% is reached, and if operation is below 8.5 kW, the highest efficiency is 82%. The combined (inverter and motor) efficiency map for the HSG operating in regenerative mode is shown in Figure II-73. Note that although the torque is indicated as positive, it is actually in the opposite direction to that of the motoring plots; but regenerative torque is plotted in a similar manner to facilitate comparison. Combined system HSG efficiencies for regenerative mode are very similar to those of the motor mode, with a peak efficiency of 86% and only 82% if operating below 8.5 kW.

A plot of various temperatures and power versus time during continuous testing conditions is provided in Figure II-74. A power level of 8.5 kW at 5,000 rpm was maintained for about 30 min and the motor temperature stabilized at about 120°C. At 3,000 rpm, the motor temperature reached 160°C after 3 min of operation. Operation at 8.5 kW was maintained at 7,000, 9,000, and 11,000 rpm, and the motor temperatures stabilized at about 100°C for all three test conditions.
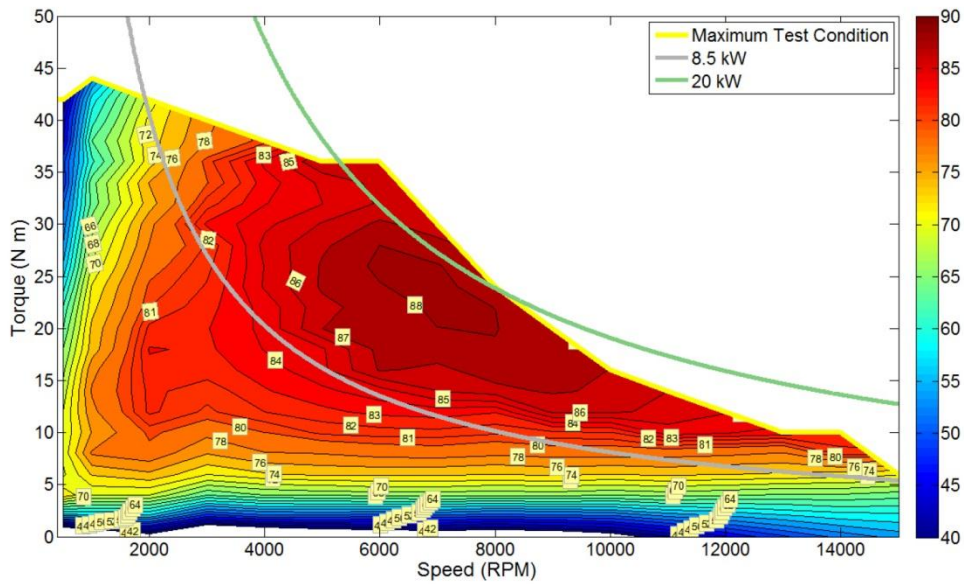
Figure II-70: 2012 Hyundai Sonata HSG motoring efficiency (motor only).
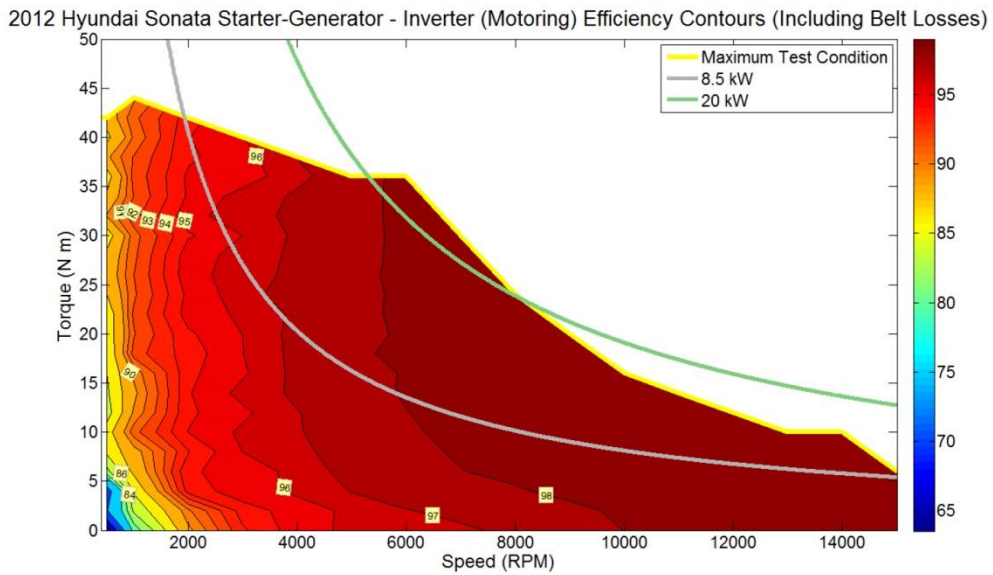
Figure II-71: 2012 Hyundai Sonata HSG motoring efficiency (inverter only).
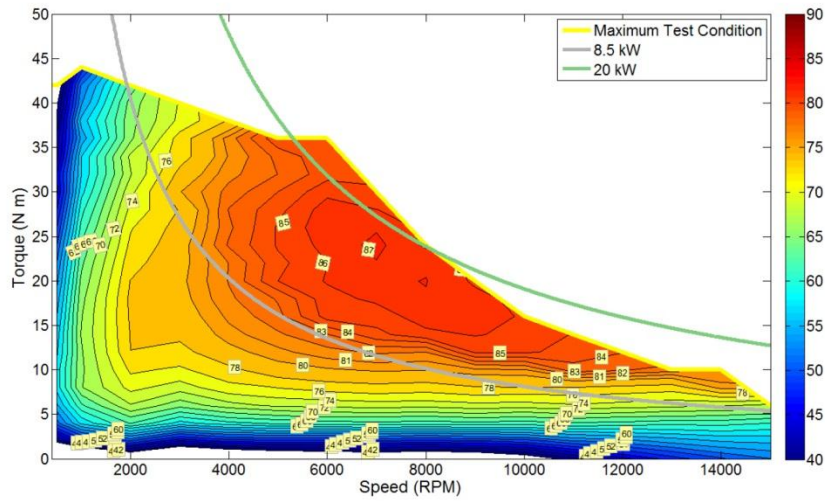
Figure II-72: 2012 Hyundai Sonata HSG motoring efficiency (motor and inverter combined).
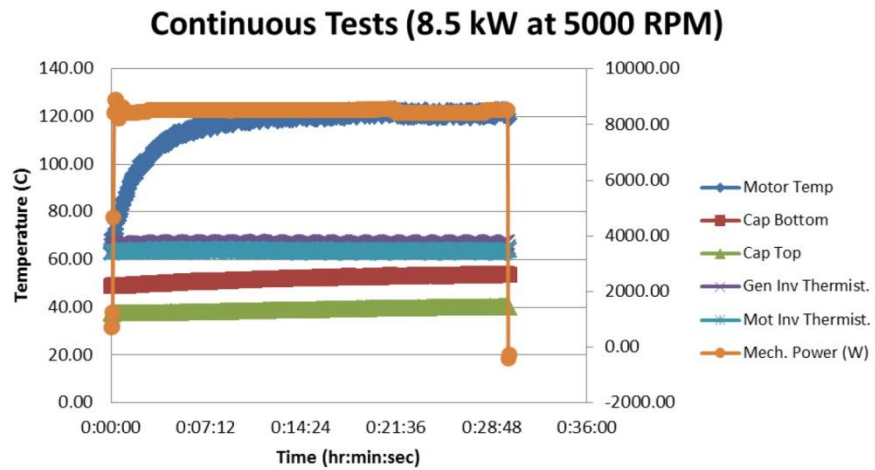
Figure II-73: 2012 Hyundai Sonata HSG generating efficiency (motor and inverter combined).
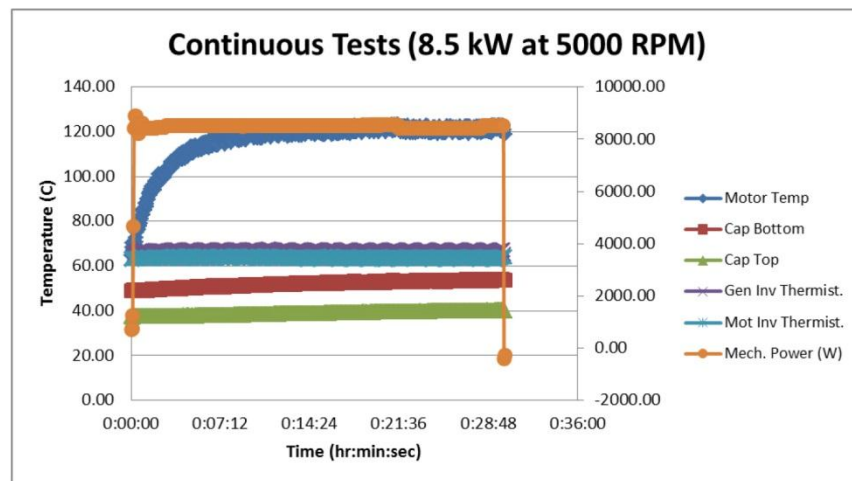
Figure II-74: 2012 Hyundai Sonata HSG generating efficiency (motor and inverter combined).

Conclusions and Future Directions

Valuable information continues to be gathered on various EV/HEV components. Details of the 2013 Nissan LEAF charger design were determined and presented. Overall, the charger design uses mostly conventional techniques, except that the isolation stage includes a transformer with two secondary windings and the outputs are rectified with two full bridge rectifiers placed in series with balancing diodes in parallel with each full bridge. Conformational testing affirmed the anticipated functionality of the charger.

Details of the 2013 Toyota Camry PCU design were obtained and presented. The design is quite similar to that of the 2008 Lexus LS 600h, as it uses discrete power modules with cooling applied to both sides. This facilitates a 33% reduction in the number of devices required for the motor inverter, as smaller devices can be used because cooling is greatly improved. Power devices contribute a significant portion of the cost of the PCU.

IMs from Remy were tested and peak torque and efficiency were confirmed. ORNL is interfacing with Remy to ensure proper operation was implemented before publishing the results.

Dynamotor testing of the 2012 Hyundai Sonata HSG revealed that the PM machine is capable of operating well beyond its published peak power of 8.5 kW, up to about 24 kW. Peak combined efficiencies reached about 86–87% regardless of whether the HSG was operating in motoring mode or regenerative mode. A visual comparison of the motoring and regenerative efficiency maps reveals the slightly higher-efficiency behavior of the motoring mode. Although efficiencies are lower than for most machines benchmarked thus far, the HSG is much more efficient than a conventional alternator, which can be 50% efficient or less. Overall, the design is well suited for hybridization of mild and medium HEVs.

A summary of power density and specific power for motors and inverters that have been benchmarked is provided in Table II-4.

FY 2013 Publications/Presentations

"Benchmarking EV and HEV power electronics and electric machines," presented at the IEEE Transportation Electrification Conference, June 2013.

Table II-4: Comparison of specific power and power density for various EVs/HEVs benchmarked by ORNL.

Component & Parameter	2020 DOE Targets	2012 Leaf (80 kW)	2012 Sonata HSG 23 (8.5 kW)	2011 Sonata (30 kW)	2010 Prius (60 kW)	2008 LS600h Lexus (110 kW)	2007 Camry (70 kW)	2013 Camry (105 kW)	2004 Prius (50 kW)
Motor									
Peak power density, kW/L	5.7	4.2	7.42 (2.7)	3.0	4.8	6.6	5.9		3.3
Peak specific power, kW/kg	1.6	1.4	1.9 (0.7)	1.1	1.6	2.5	1.7		1.1
Inverter									
Excludes generator inverter (parenthetical values exclude boost converter mass/volume for Toyota Vehicles)									
Peak power density, kW/L	13.4	5.7	5.6 (2.0)	7.3	5.9 (11.1)	10.6 (17.2)	7.4 (11.7)	12.7 (19.0)	4.5 (7.4)
Peak specific power, kW/kg	14.1	4.9	5.4 (2.0)	6.9	6.9 (16.7)	7.7 (14.9)	5.0 (9.3)	11.5 (17.2)	3.8 (6.2)

II.4. System Integration and HIL Validation

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Start Date: October 2012
Projected End Date: September 2013

Objectives

Overall Objectives:

Use ORNL's hardware-in-the-loop (HIL) system as a testing platform for development of next-generation TDSs.

- Validate converter, inverter, and motor performance using standard or custom drive cycles
- Provide feedback for DOE VTO APEEM program planning, target setting, and identification of R&D gaps
- Propose TDS refinements that address R&D gaps for the VTO APEEM program

FY 2013 Objectives

- Design and fabricate universal circuit boards needed for operation on the HIL system
  - Digital signal processor (DSP) control board
  - driver boards
- Work jointly with Vehicle Systems Integration (VSI) staff to define the needs of a high-performance dynamometer and other HIL components
- Perform subscale HIL testing with scaled motors

Technical Barriers

- Measurement of system and component efficiencies during transient conditions
- Limitations in refresh rates, continuous monitoring, and customizability of most commercially available power measurement systems

Technical Targets

- This project aids program planning and the establishment and verification of all DOE targets.

Accomplishments

- Completed design of universal control circuitry and board population
- Programmed and implemented DSP control board with driver circuitry needed in experimental test setup
- Built, programmed, and assembled power analysis equipment
- Developed and successfully operated subscale dynamometer system
- Designed, fabricated, and assembled custom IM with GlidCop and Al rotor bars for subscale testing
- Procured battery emulator and ordered dynamometer (by VSI team)

✧   ✧   ✧   ✧   ✧

Introduction

Development and utilization of an HIL drive cycle testing platform for components expands testing and validation capabilities for prototype and commercial components. The expansion of HIL testing capabilities is important for DOE VTO program planning with regard to program portfolio development (by identifying development thrust areas) and target setting (perhaps additional ones) with consideration of system-wide impacts and characteristics. Drive cycle validation ensures prototype development is conducted with respect to realistic on-the-road operation. This project intends to increase the cohesiveness between DOE's APEEM and Vehicle Systems programs.

The VSI team at ORNL is developing an HIL platform for component testing that emulates drive cycle conditions by using a dynamometer that generates the appropriate torque (throughout a drive cycle speed reference profile) for environmental conditions (e.g., grade, temperature) and a given vehicle profile (e.g., mass, rolling resistance, drag coefficient). A functional diagram of the system is shown in Figure II-75. Items researched within DOE's APEEM Program are located within the green dotted boundary, and they constitute the primary focus of this project.

The system will use a battery emulator so impacts of converter or motor designs upon battery operation can be assessed. For example, if the size of the main inverter capacitor (one of the largest inverter components) is reduced, the full effect is not realized unless dc current ripple is monitored. A significant increase in current ripple will reduce the operational life of the battery; therefore, current ripple should be carefully considered in evaluating prototype designs. System-wide characteristics can be observed in
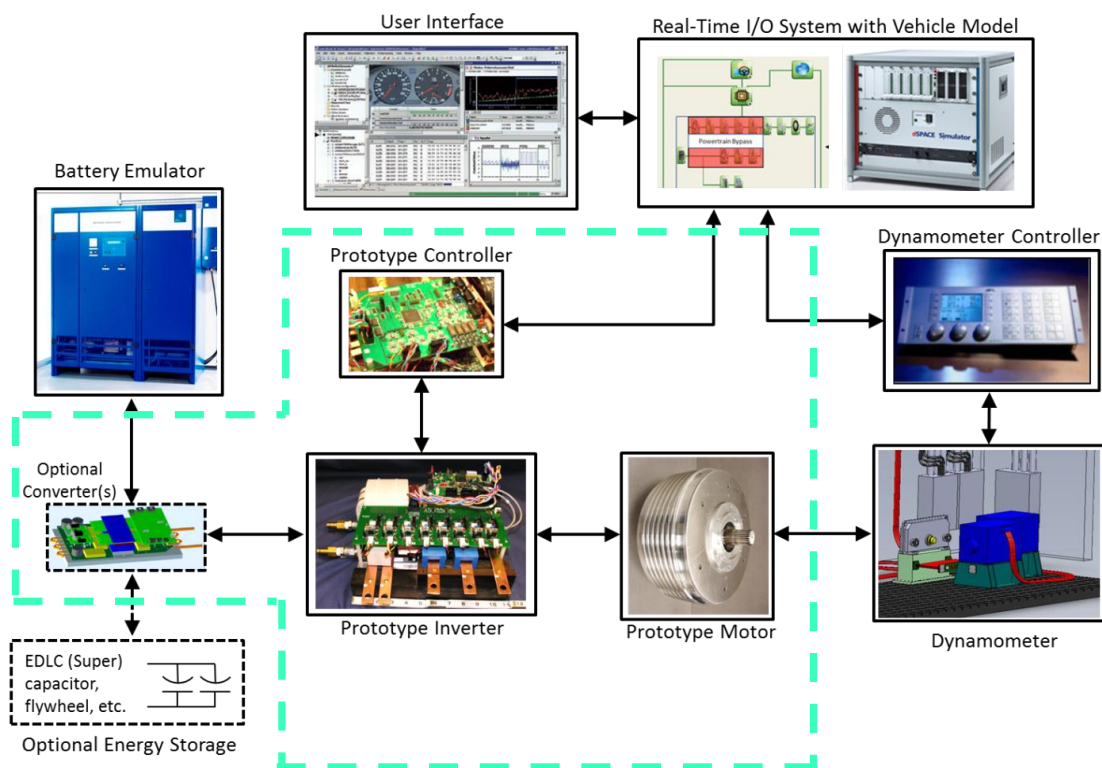
Figure II-75: HIL testing platform under development.

evaluating requirements and impacts of operating with high dc-link voltages, which would require higher battery voltage levels or a bi-directional dc-dc converter. Another area of interest may be driveline matching, in which the impacts of various transmission architectures upon converter, inverter, and motor operation can be assessed. In combination with the emulation of vehicle operation described above, the HIL system will have the capability to emulate an EV transmission-transaxle or even HEV power split operation. Ultimately, the HIL system provides the capability to emulate realistic operation so system characteristics of various design and hardware arrangements can be monitored while components operate throughout a drive cycle. The focus of this project is to prepare the controls, inverter, motor, and other components for operation on the HIL system and to develop a data acquisition system to capture and record high-accuracy measurements over the extent of a drive cycle.

Approach

To prepare for operation on the full-size HIL system that is under development by the VSI team, a subscale system representative of the dynamometer system was used to carry out preliminary testing of controls and measurement developments. Fractional horsepower motors were used to facilitate rapid assembly of the system and minimize safety concerns. Nonetheless, the basic functionality of controls and measurement is the same regardless of scale. The following

tasks were carried out to support and implement subscale HIL testing.

Design and fabricate circuit boards for dynamic testing

The HIL testing platform in the VSI laboratory is designed to test the entire EV (or HEV) drive system, which may include multiple converters and electric machines. Therefore, custom control and driver boards are needed to implement optimal control of these devices throughout the drive cycle. ORNL has previously developed optimized controls for individual components (e.g., motor/inverter and converter) of electric drive systems, but a new and more robust DSP and communication circuitry are needed for simultaneous operation of various components throughout challenging drive cycle profiles. Additionally, driver circuitry is required to operate the PE devices in various power conversion stages. A key part of the project is the development of these circuit boards for transient drive cycle operation.

Develop dynamic controls

ORNL has developed optimized motor controllers (for both commercial and prototype motors) for steady state operation to conduct operational efficiency mapping, determine peak performance, and analyze other operational metrics throughout the entire operation range. However, optimal operation during transient conditions for drive cycle testing presents a greater challenge, especially for erratic driving schedules.

Although detailed control algorithms will vary depending on the components used within each electric drive system,

development and implementation of customizable controls for the primary motor types is a vital step in performing HIL drive cycle testing.

Develop dynamic measurement system

Many parameters and quantities need to be measured to perform full characterization of the electric drive system during HIL testing. Most of the parameters are the same as those needed during steady state performance and operational characterization. As shown in Figure II-76, many physical quantities such as dc voltage(s) and current(s), ac voltages and currents, torque, speed, and temperature need to be measured throughout the entire drive cycle. Additionally, it is preferable to stream this data to a memory storage device so that transient operation of the system can be inspected and analyzed after the tests are completed.

It is very important to synchronize the measurement of electrical power (obtained from voltage and current) and mechanical power (obtained from torque and speed). For steady state measurements, a lack of close synchronization of the measurements is less crucial because mechanical and electrical power levels are relatively constant for these conditions. However, transient power conditions require that the measurements be highly synchronized. Otherwise, both motor and inverter efficiency calculations will be erroneous, as it would be uncertain whether the transient mechanical power and electrical power were measured at the same instant.

Some electric power analyzers include the capability to measure torque and speed from a torque transducer. This capability greatly facilitates the synchronization of power measurements, as opposed to using separate instruments to obtain electrical power and mechanical power. Some power analyzers are advertised as having subsecond data refresh

rates; but when appropriate time observation windows are used, the actual refresh rate is on the order of seconds. It is important to use an observation window that captures at least a few fundamental electrical cycles; otherwise, power calculations could be erroneous. For analysis of an electric drive during transient conditions, it is desirable to have subsecond refresh rates (e.g., 0.1 second). Otherwise, the value of having transient testing capabilities is diminished.

In addition to the issue of slowing refresh rates, it should be noted that these products provide only processed numerical data at these refresh rates, not actual waveform data. For example, ac rms current, ac rms voltage, and ac power can be obtained via Ethernet or serial communication at the published refresh rates; but the original waveforms are not available at the published refresh rates. Additionally, each observation window is not recorded consecutively in time; therefore, continuous waveform data are not available.

It was determined that there are no commercially available power analyzers that offer the capabilities desirable for comprehensive analysis of transient drive cycle behavior. Therefore, as a part of this project, ORNL developed a measurement system that is capable of measuring and recording data in a continuous manner.

Fabricate custom induction motors

A primary function of the HIL system is to evaluate prototype motors throughout transient drive cycle conditions. Since the IM is an alternative to RE PM motors, subscale IMs with Cu rotor bars and Al rotor bars were fabricated for comparison testing on the HIL system. Instead of using pure Cu, which has low mechanical integrity for high rotational speeds, an alumina-filled Cu termed "GlidCop" was used in rotor bar fabrication.
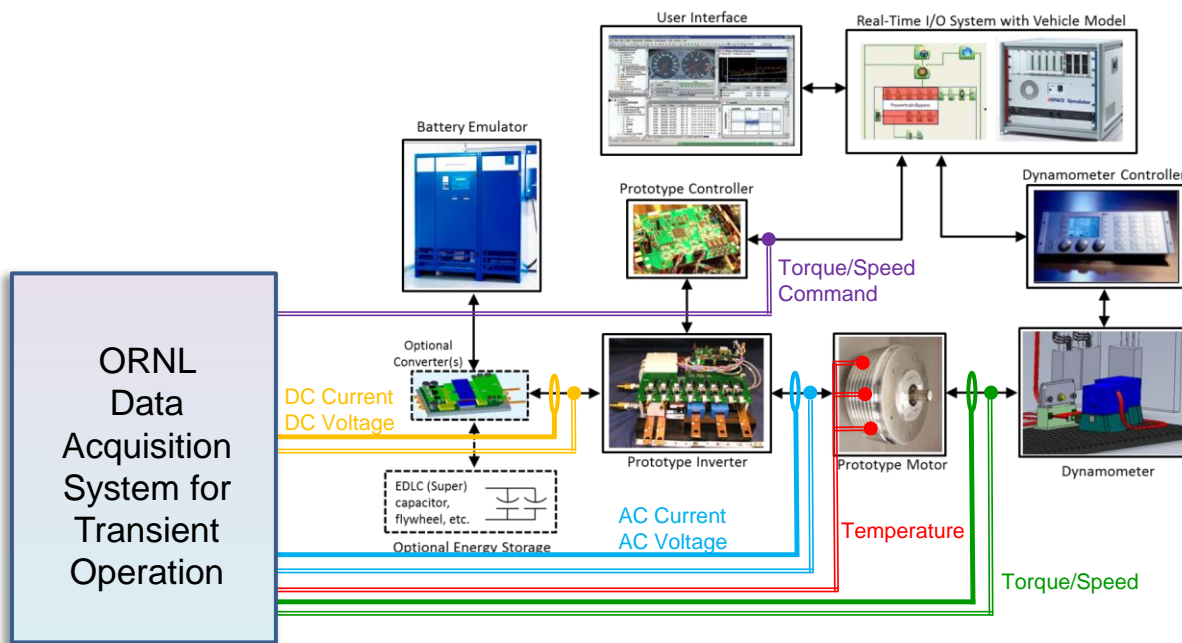
Figure II-76: Measurement and data acquisition system diagram.

Perform subscale HIL testing

Subscale testing was carried out to evaluate developments for robust dynamic electric machine controls and the advanced custom measurement system. A commercially available fractional horsepower dynamometer (Figure II-77), was identified and purchased. It offers considerable flexibility for testing various machine types, and the procurement avoids excessive design and fabrication time, which is beyond the focus of this project. The subscale dynamometer kit includes a torque transducer to monitor torque between the motor under test and the loading generator.

Results

Design and fabrication of circuit boards

Previous work on control circuitry by Gui-Jia Su, Lixin Tang, and Cliff White was leveraged to develop the universal

DSP board shown on the left in Figure II-78. The board has the capability to control at least two motors/inverters and two converters at once, with current and position feedback for motor operation, and voltage and current feedback for converter operation. The DSP board has the capability to communicate via various methods such as CAN, USB, and other serial communication formats. The performance of the universal DSP board and driver boards will be highlighted when subscale HIL test results are discussed.

Development of dynamic controls

Dynamic controls were developed to operate subscale motors with a dc load motor, which served as a dynamometer during subscale HIL testing. Control methods for various motor types were based on conventional control theory, but each required customization for robust operation. Controls for the IMs use observer feedback to improve the dynamic performance of the feedback control loop, which uses current and speed proportional-integral regulators. The performance of the controllers is highlighted when subscale HIL test results are discussed.
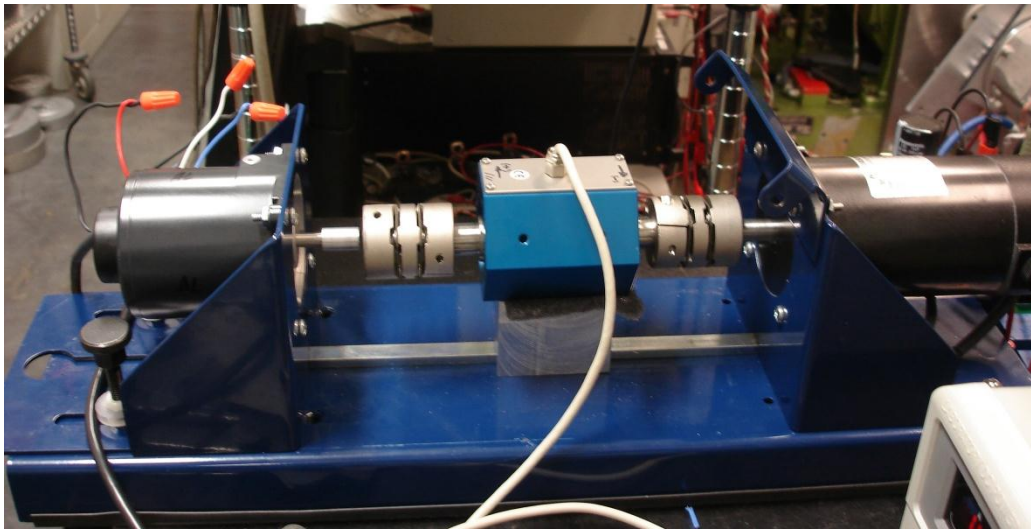
Figure II-77: Fractional horsepower dynamometer assembly.
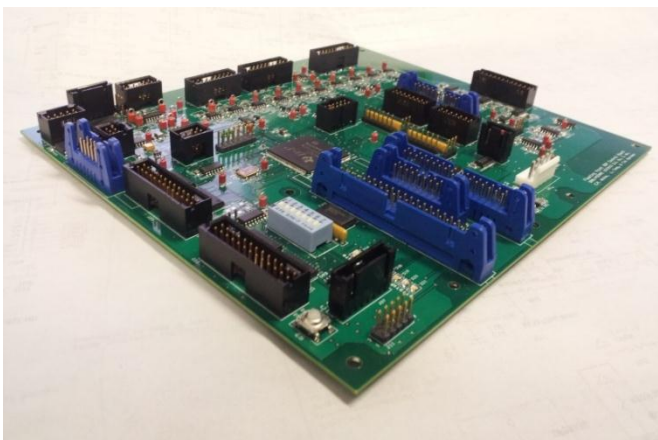
Figure II-78: Universal DSP control board (left) and driver board (right).

Development of dynamic measurement system

After a survey of various platform options upon which to base the development of a measurement system, it was decided that hardware from National Instruments (NI) offered the most flexibility and customizability. The system (Figure II-79, left side) has an optional high-accuracy (14 bit), high-speed (50 MS/s) analog-to-digital accessory card that is well suited for current and PWM voltage measurement. Note that although switching frequencies on the order of kHz are used, PWM voltages have very high-frequency transients. For example, the transients associated with the switch-on and switch-off times of high-current power devices can be on the order of microseconds (1 MHz). Therefore, to appropriately monitor inverter efficiency, it is desirable to capture data at a rate that is even higher than 1 MHz.

In addition to high speed and accuracy capabilities, the NI system offers the capability to continuously stream data to a built-in hard drive. The robustness of the system allowed ORNL staff to focus on programming NI software to develop cutting-edge measurement capabilities without devoting too many resources to hardware development and data management. The graphical display (right side of Figure II-79) is an example of display options for the drive cycle data output

by the custom software. Detailed results will be discussed in a later section.

Fabrication of custom induction motors

Copper and Al induction rotor bars were fabricated and assembled for comparison studies on the subscale HIL testing system. GlidCop is Cu that has ~15% alumina filler material to improve mechanical integrity without significantly reducing conductivity. These properties are attractive for IMs with high speed ratings, for which the mechanical properties of pure Cu can be a limitation. The fabricated GlidCop rotor bars and end rings, shown on the left in Figure II-80, had to be nickel plated before soldering, since the alumina makes normal bonding processes more difficult to perform. This is a primary drawback of alumina-filled Cu. Even more difficulty was encountered in the bonding of the fabricated Al pieces (shown on the right in Figure II-80). Aluminum quickly forms an oxidation layer that hinders many bonding processes and conductivity if the bond is not made properly. A collection of the IM pieces is shown in Figure II-81, where the stator, rotor shaft, bearings, empty rotor laminations, and two fabricated rotors are visible. The IM rotors are semi-closed slot with full slot skew for reduced ripple torque. A magnetic position encoder was attached to the shaft to facilitate speed feedback control.
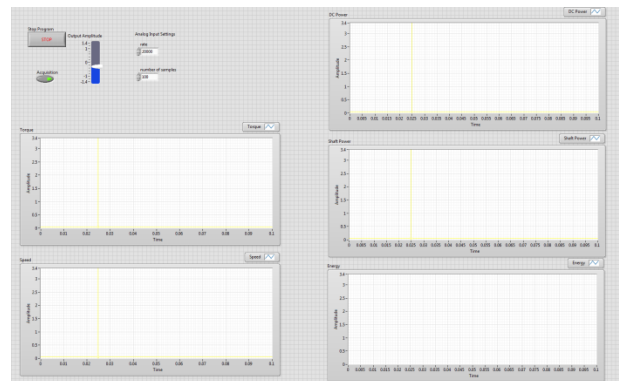
Figure II-79: Measurement system (left) and display (right).
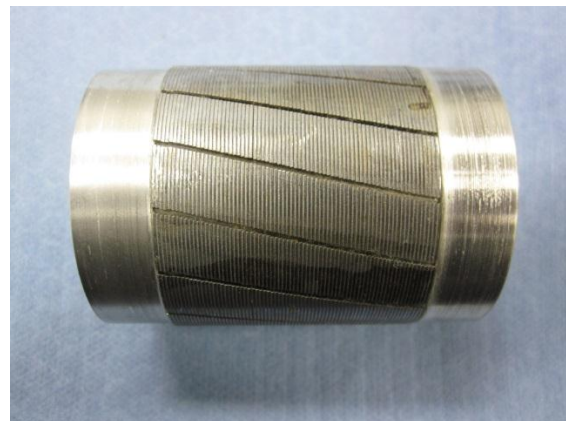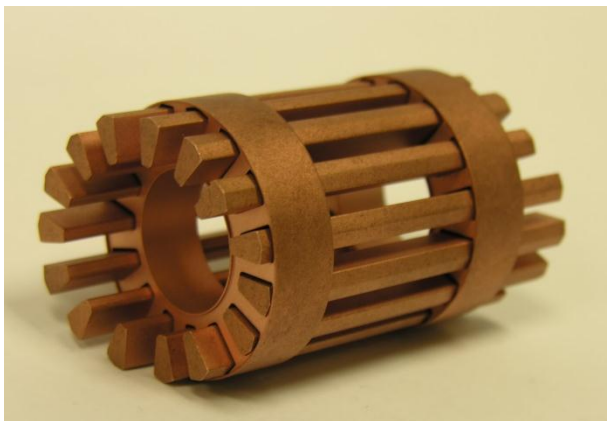
Figure II-80: Fabricated GlidCop rotor bars and end rings.
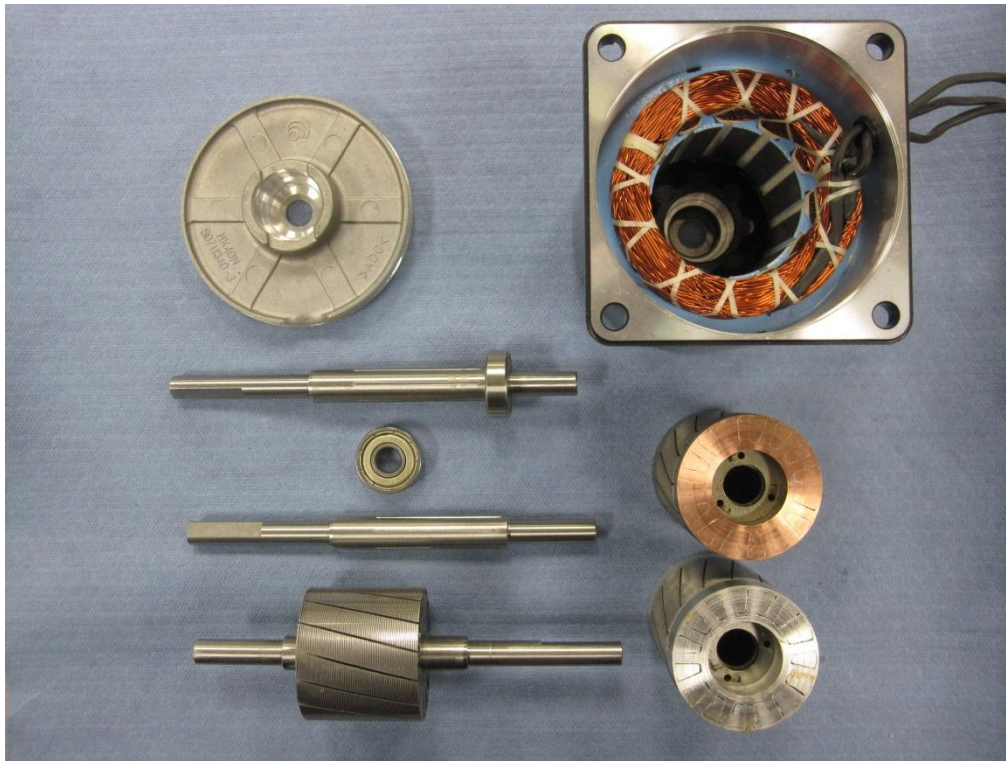
Figure II-81: Scaled induction motor components (copper and aluminum rotors).

Subscale HIL test results

The scaled IMs were first tested under steady state conditions for efficiency and performance mapping. The efficiency map for the GlidCop Cu IM is shown in Figure II-82. The torque and speed axes were scaled by 560 and 2.44, respectively, to match those of Nissan LEAF motor operation. The efficiency is much lower than that of full-size electric motors, partially because of the much lower operation voltage of 42 V and because the physical air gap does not scale proportionally with power rating. It was also discovered that the Al bar motor performance was significantly lower, probably as a result of a manufacturing defect. Nonetheless, the overall FY 2013 goal of the project was not to develop, test, and compare the characteristics of these motors, but rather to develop and implement dynamic controls and an advanced measurement system.

The subscale dynamometer test system was used to emulate electric drive operation with a vehicle similar in size to a Nissan LEAF. The torque required to propel the vehicle throughout the US06 drive cycle was scaled to match the small IM performance and used as a command for the load motor, and the drive cycle speed profile (Figure II-83) was scaled and used as a speed reference for the proportion-integral loop of the small IM. The IM torque and speed operation points throughout the US06 drive cycle were scaled and superimposed on top of the steady state operational efficiency map in Figure II-84.

The superimposed torque and speed points in Figure II-84 are clear indicators that the US06 drive cycle does not require the electric drive to operate near peak torque or peak power conditions. However, it is important to note that some of the most heavily frequented areas of operation correspond with low motor efficiencies, and this is true for both subscale IM efficiencies and the full-size LEAF motor efficiencies. The scaled dc-link energy produced and regenerated by the scaled IM throughout the US06 drive cycle is shown in Figure II-85. The red trace represents the energy produced during motoring operation, and the green trace represents the energy recovered through regenerative braking. The blue trace represents the total energy, in which the regenerative energy reduces the overall required energy from the battery pack.

It is clear that the low efficiency of the scaled prototype motor yields very little benefit from regenerative braking. Simulations were conducted using the Nissan LEAF motor and inverter efficiency maps that were obtained with the Benchmarking project. The motoring, regenerative, and total energy using the LEAF components in the US06 drive cycle are shown in Figure II-86. It can be seen that the total energy at the end of the drive cycle is about 0.75 kWh versus a value of 7.6 kWh for scaled IM operation. Note that battery efficiency and transmission (gear and bearing) losses are not included in the basic vehicle model.
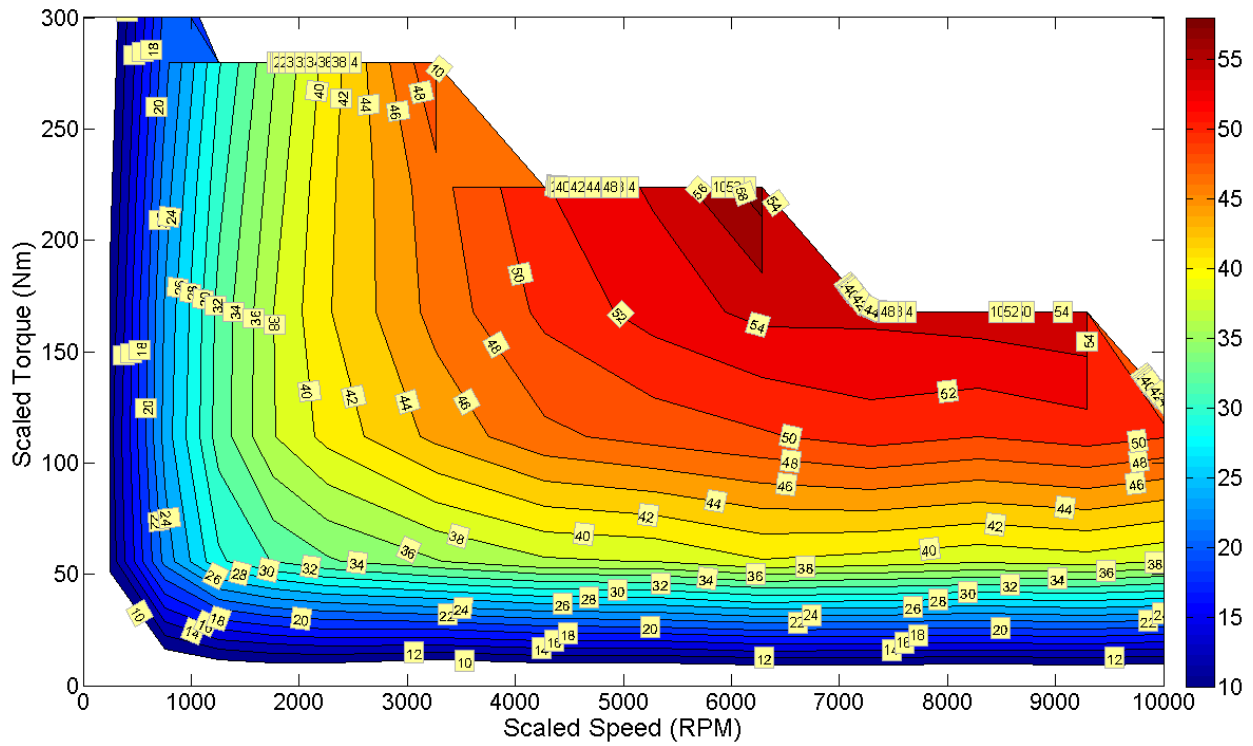
Figure II-82: Scaled copper induction motor efficiency map.
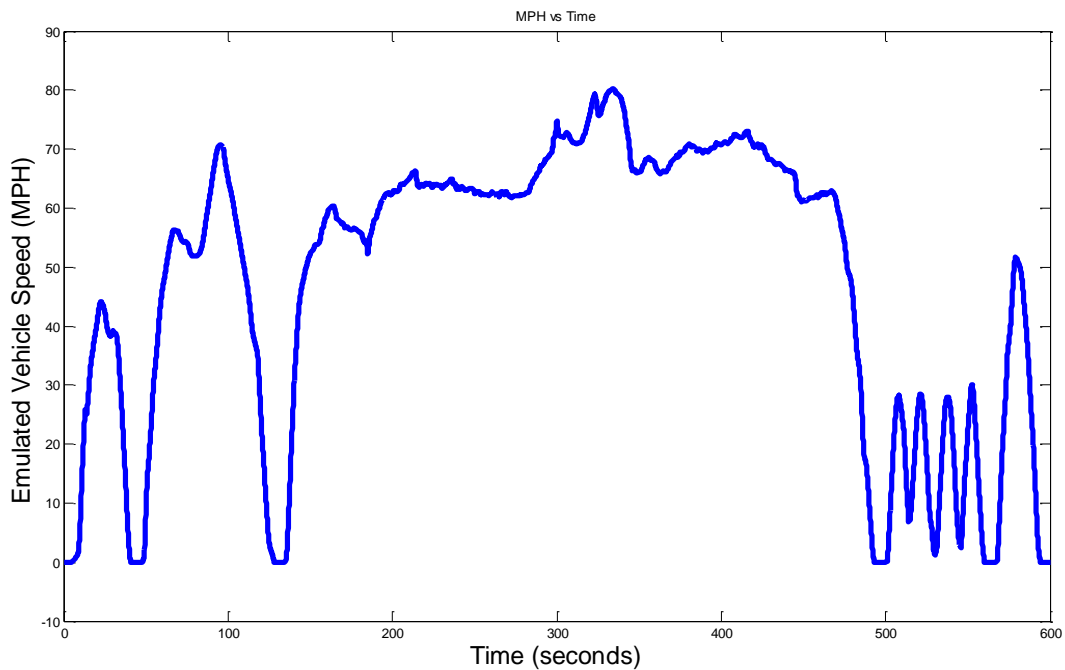
Figure II-83: US06 drive cycle speed reference.
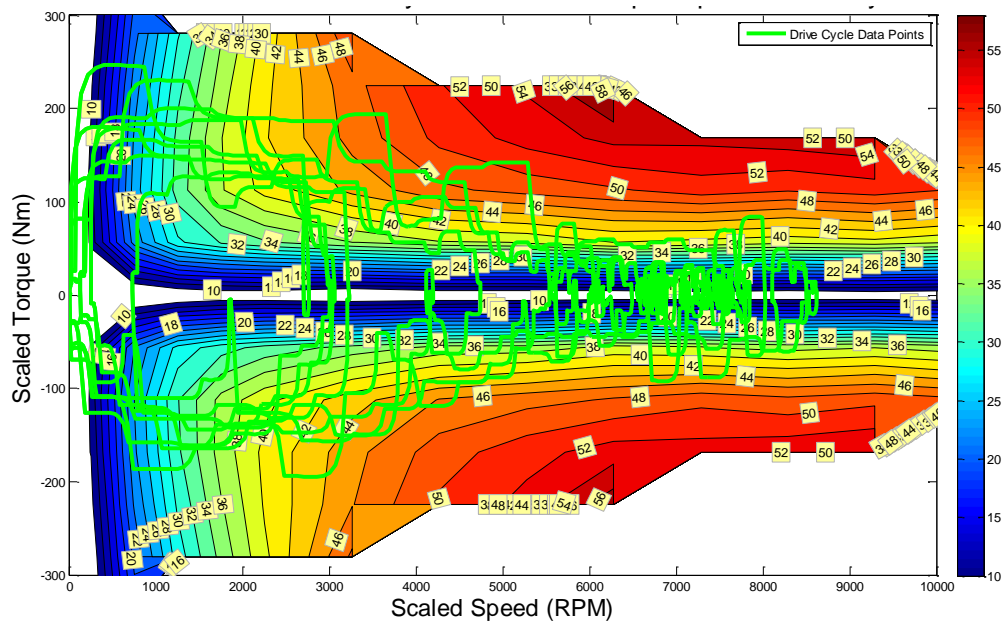
Figure II-84: Overlay of US06 drive cycle operation points on scaled induction motor efficiency map.
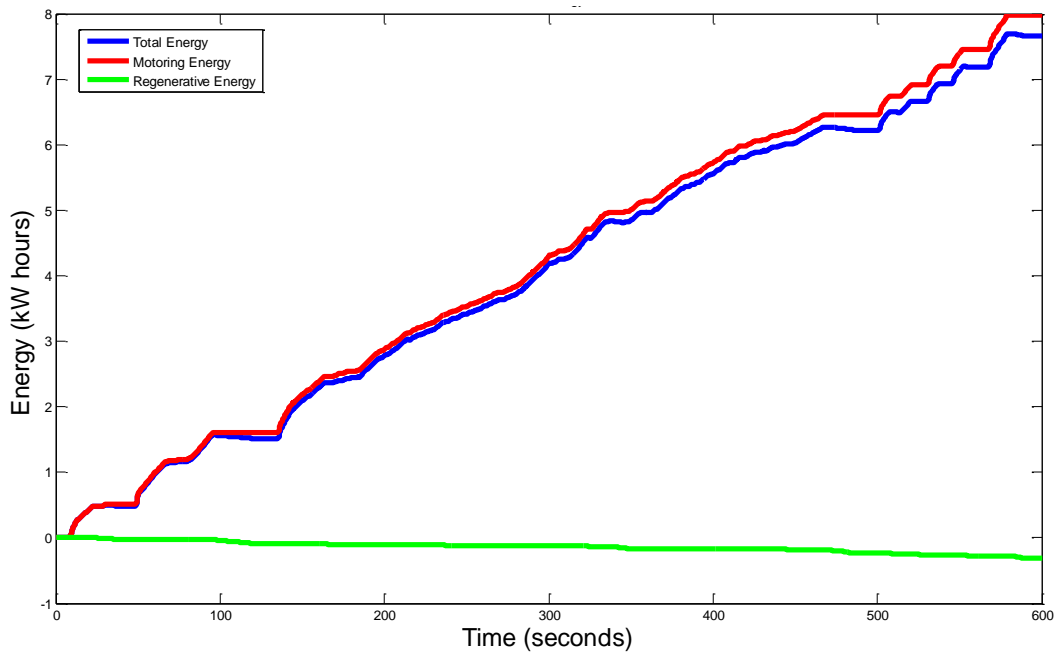
Figure II-85: Scaled HIL energy produced and regenerated throughout drive cycle with induction motor.
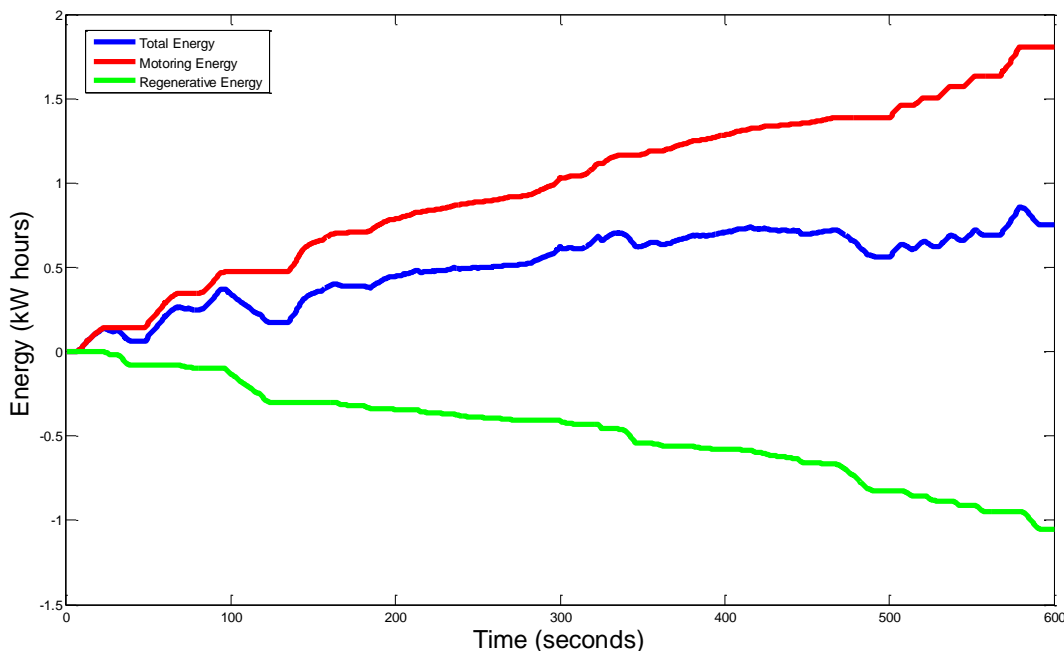
Figure II-86: Simulated energy produced and regenerated throughout drive cycle with LEAF components and efficiencies.

For the vehicle to follow the drive cycle speed profile, the required torque and speed at the drive wheels is the same for both cases. However, since the efficiency characteristics of the scaled IM are inferior, much more energy is required from the battery for motoring operation for the same road conditions. Similarly, the inferior efficiencies also prevent the battery from recovering as much energy from regenerative braking. Using the total energy consumed throughout the drive cycle, the scaled IM drive system achieves only about 1.05 miles per kWh, whereas the simulated LEAF energy consumption leads to about 10.7 miles per kWh (includes aero load). According to DOE's fuel economy website, the LEAF is reported to achieve 3.4 miles per kWh during common driving conditions. In addition to transmission losses and battery efficiency, other aspects to consider are ancillary loads such as heating and air conditioning, lights, power steering, various pumps, and running lights. However, for the case of HIL comparison studies of electric drivetrain components, these considerations are not necessary.

Conclusions and Future Directions

The overall FY 2013 goal of this project was not to develop, test, and compare characteristics of prototype motors, but rather to develop and implement dynamic controls, an advanced measurement system, and various analysis methods for future operation on the full-size HIL system. The performance of the dynamic controller was robust, and it facilitated the capability of the subscale IM to follow the drive cycle speed profile, maintaining the emulated vehicle speed within 0.2 MPH of the reference. For propelling a LEAF-sized vehicle through the

US06 drive cycle, the drastic difference between the scaled energy consumption curves of the subscale prototype IM and the simulated energy consumption of the Nissan LEAF drivetrain components highlights the importance of the energy efficiency of these components.

Various types of drive cycle profiles should be carried out for a true assessment of real-world drivetrain performance and characteristics. Enhancements of the custom measurement system can easily be implemented to address specific interests, such as spectrum analysis of various signals or current ripple analysis. The exemplar approach and analysis methods used to compare these technologies offers a framework for testing future prototypes and commercial components to analyze performance, efficiency, and other characteristics under realistic operation conditions. Ultimately, these results and analysis methods provide informative feedback with regard to focus areas for future R&D on converters, inverters, and electric motors.

FY 2013 Publications/Presentations

1. "System integration and HIL validation," presented at DOE Vehicle Technologies Program Advanced Power Electronics and Electric Motors R&D FY 2013 Kickoff Meeting, November 2013.

2. "System integration and validation," presented at 2013 U.S. DOE Hydrogen and Fuel Cells Program and Vehicle Technologies Program Annual Merit Review and Peer Evaluation Meeting, May 2013.

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Objectives

The objective is to provide the theoretical foundation, measurement methods, data, and simulation models necessary to optimize power modules' electrical, thermal, and reliability performance for Advanced Plug-in Hybrid Electric Vehicle Power Conditioning Systems and Motor Drives.

Approach

- Develop dynamic electro-thermal Saber models, perform parameter extractions, and demonstrate validity of models for:
  - Silicon IGBTs and PiN Diodes
  - Silicon MOSFETs and CoolMOSFETs
  - SiC Junction Barrier Schottky (JBS) Diodes
  - Advanced Wide Bandgap power devices including SiC Power MOSFET
- Develop thermal network component models and validate models using transient thermal imaging (TTI) and high speed temperature sensitive parameter (TSP) measurement.
- Develop thermal-mechanical degradation models and extract model parameters using accelerated stress and monitoring:
  - Stress types include thermal cycling, thermal shock, power cycling
  - Degradation monitoring includes TTI, TSP, X-Ray, C-SAM, etc.

Major Accomplishments

- In previous year (FY12), this project developed and validated models and simulation tools needed for FY13 and FY14 simulations including:

  - Dynamic electro-thermal semiconductor device models for Silicon IGBTs, Silicon PiN Diodes, Silicon MOSFETs, Silicon CoolMOSFETs and SiC Junction Barrier Schottky (JBS) Diodes
  - Thermal network component package models for the Delphi Viper double-sided cooling power module and Virginia Tech soft switching power module.
- Additional model development in FY13-FY14 include:
  - Develop electro-thermal models for advanced wide-bandgap semiconductor devices including SiC MOSFETs, SiC JFETs and GaN diodes.
  - Thermal network component models for air a liquid heatinks

FY13 Accomplishments included:

- Developed cross-coupling TSP measurement capability and used to validate thermal coupling model within VTech module thermal model.
- Included liquid- and air-cooling thermal network component models in electro-thermal simulations of vehicle inverters.
- Used electro-thermal-mechanical simulations to evaluate thermal stresses in Delphi Viper double-sided cooling power module for nominal and fault operating conditions. This included extending the IGBT model to represent fault current and near intrinsic temperature conditions for the full voltage blocking range.
- Developed thermal-network-component models for representative cooling systems with NREL
- Used simulations to evaluate thermal stresses at module interfaces for Virginia Tech soft switching power module.
- Performed package stress and monitoring for a wide range of conditions of thermal cycling, thermal shock, and power cycling degradation for two different DBC stack technologies to characterize mechanical reliability properties of representative Virginia Tech modules. The parameterized module reliability characterization results are intended to be used to determine parameters for physics-of-failure models.
- A method for including physics-of-failure models into electro-thermal simulations was developed to enable simulation of the module degradation that would occur during vehicle driving cycle conditions. This is intended to enable evaluation of the impact of advanced technologies on module live and the impact of module degradation on near end-of-life performance.

Future Direction

FY14 Milestones:

- Investigate the suitability of using NREL bonded interface reliability characterization to determine parameters for physics-of-failure models.
- Perform electro-thermal simulations to evaluate the impact of advanced wide bandgap semiconductor device technology and advanced power module package technology in vehicle propulsion and bi-directional vehicle charger storage/inverter applications.

Other Potential Future Milestones:

- Utilize the advanced technology electro-thermal network simulation tools developed by this project to support industry transition of the technologies into products.
- Transfer models developed by the project into Saber component libraries for transfer to industry vehicle simulation programs.
- Develop electro-magnetic package/system interconnect models.
- Perform EMI simulations using electro-magnetic package/system interconnect models, electro-thermal semiconductor models and thermal-network-component models.
- Determine grid storage/inverter applications for bi-directional vehicle chargers and develop circuit

simulation scripts for chargers operating in these conditions.

Technical Discussion

The goal of this work is to characterize and model advanced power semiconductor devices and power module package technologies being developed and considered for Advanced Plug-in Hybrid Electric Vehicle Power Conditioning Systems and Motor Drives. The characterization includes full electrical and thermal performance, as well as stress and monitoring experiments necessary to characterize module and component failure and wear-out mechanisms. The component failure and wear-out results are validated with physical measurements of interface wear-out performed at NREL.

Dynamic electro-thermal models have been developed to represent the semiconductor device and power module characterization results, and have been implemented in the Saber simulator to aid in optimizing the advanced modules and packages being developed by DOE EERE Vehicle Technology Program's Advanced Power Electronics and Electric Motors projects, e.g., the Soft Switching Power Module being developed by Virginia Tech, the High Current Density Double Sided Cooling IGBT Package being developed by Delphi, and advanced cooling technologies being developed and evaluated by NREL. The failure and wear-out data are represented by empirical expressions and included in the Saber models to enable calculation of component lifetimes and impact of degraded performance resulting from vehicle fault condition and driving cycle stress.

Figure II-87 depicts the overall goal of the electro-thermal-mechanical simulation for Advanced Plug-in Hybrid Electric Vehicle Power Conditioning Systems and Motor Drives. It shows the models and parameter determination including thermal component, electrical component, and mechanical reliability. It also shows the simulation applications including electrical, electro-thermal, and reliability.
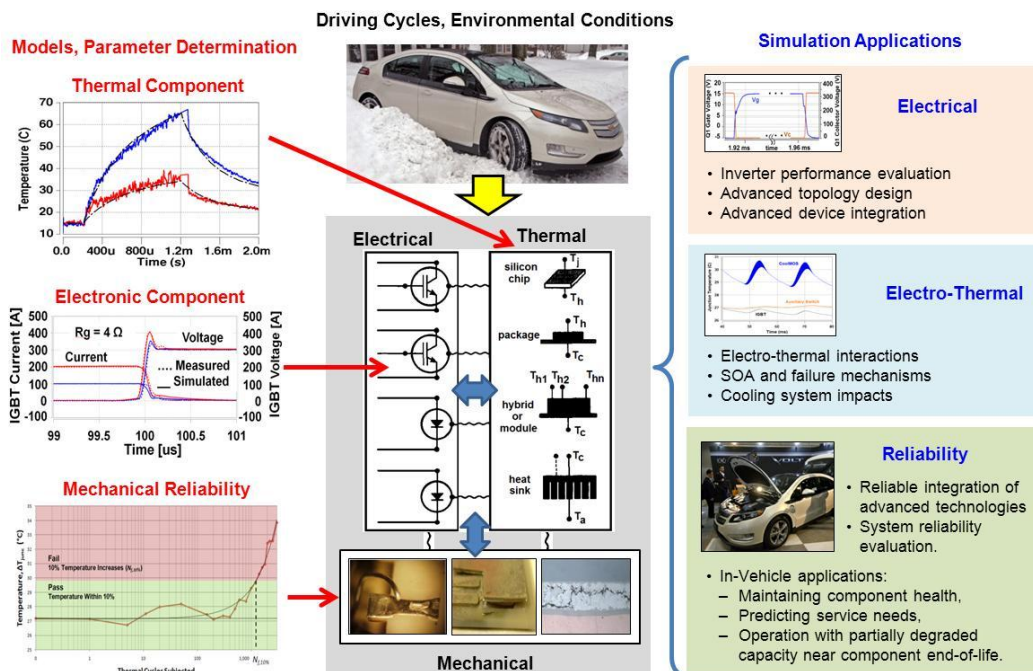
Figure II-87: Goal of the electro-thermal-mechanical simulation.

Figure II-88 shows a timeline and interaction of recent project accomplishments through FY2013 along with future direction for FY 2014 (future direction in red font).
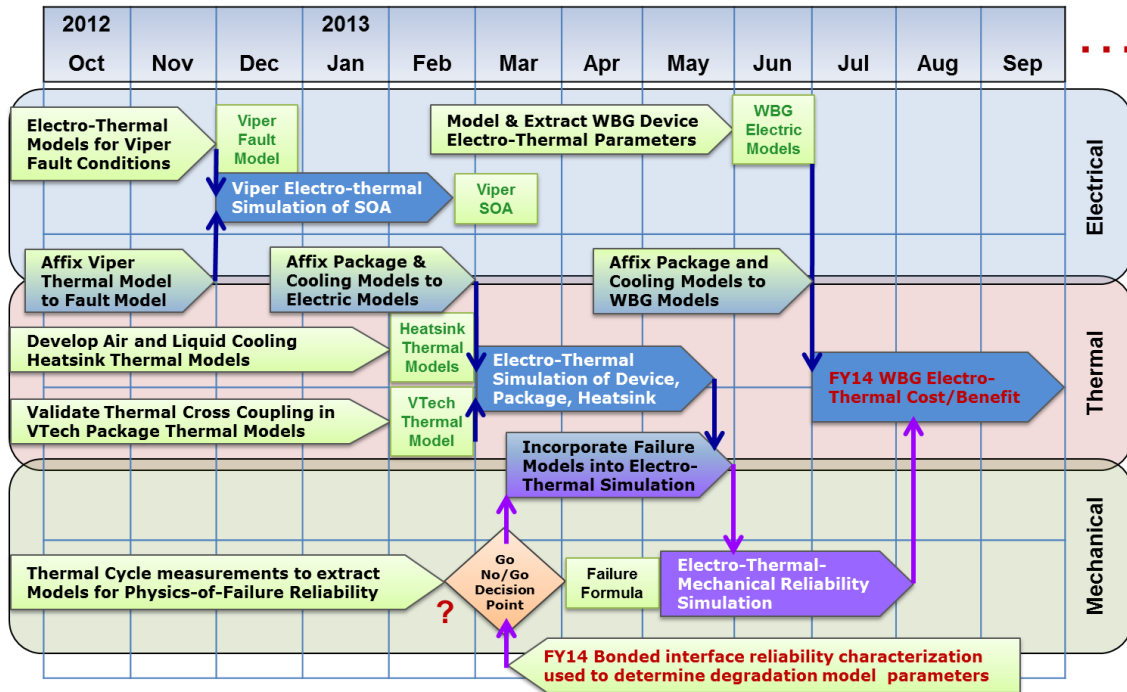
Figure II-88: Timeline for 2013-2014 project milestones.

Results:

A. Results for Delphi High Current Density Double-Sided Cooling Module:

Figure II-89 shows a doubled-sided temperature-controlled test-fixture heatsink that was developed for the Viper module. This heatsink uses a spring-loaded piston to apply a controlled four kg compressional pressure to the Viper module. This heatsink actually has three thermocouples, although only the two that are in close proximity to the top and bottom of the module are represented in the figure. A third is located in the bulk of the heatsink.
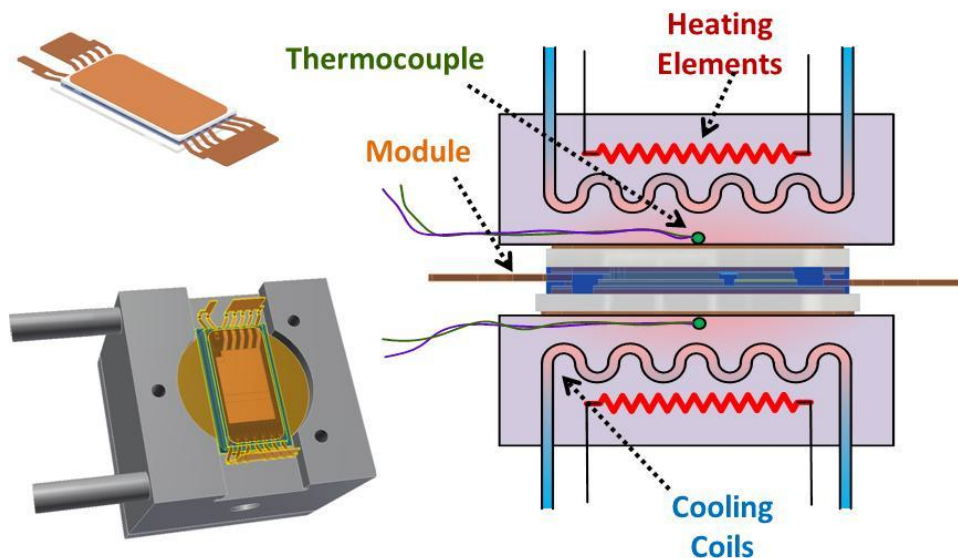
Figure II-89: Delphi Viper module with test-fixture heatsink.

Figure II-90 shows the electro-thermal model for the high current density Delphi-Viper double-sided cooling IGBT module. The electrical component models predict electrical performance (a function of temperature) and device power losses. The power losses output from the electrical model are input to the thermal models which predict the instantaneous temperature distribution in the thermal network and feeds the junction temperatures back into the device electrical models.
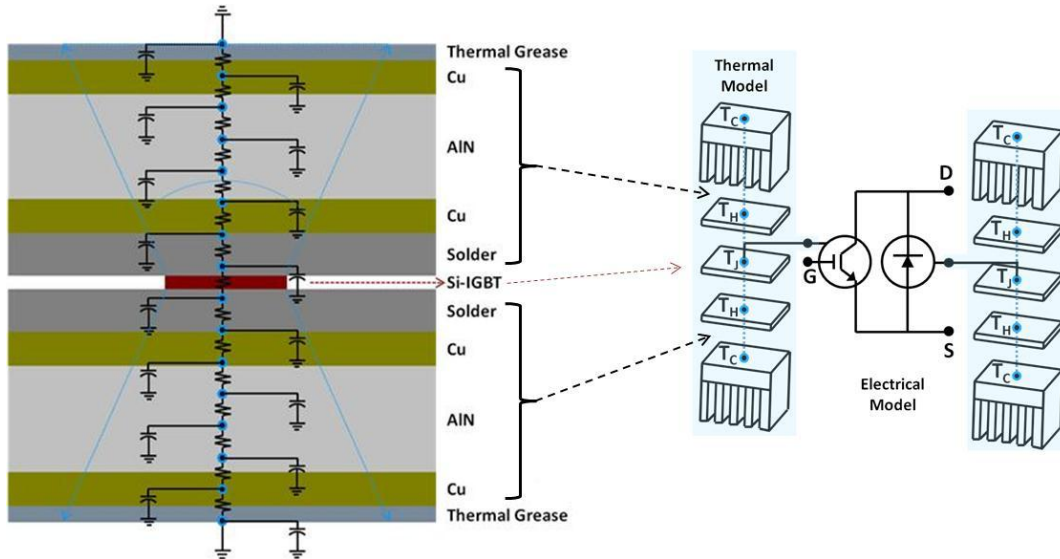
Figure II-90: Electro-thermal model for double-sided cooling Viper module.

Figure II-91 demonstrates electrical model validation for the Delphi Viper high current density IGBT module (more details on the validations are given in the previous year reports). The top graph shows a validation result of output characteristics for the IGBT at 25°C. The output characteristics validations were performed at various collector-emitter voltages (V_{CE}), collector currents (I_C), gate voltages (V_G), and temperatures (T). The bottom graph shows a validation result of current dependence of inductive-load turn-off switching at a clamp voltage of 300 V at 25°C. The switching validations were performed for different circuit parameters including collector-emitter voltage (V_{CE}), collector current (I_C), gate voltage (V_G), gate resistor (R_G), temperature (T), and clamp voltage (V_{Clamp}). Similarly, validations were also performed for the Viper Silicon PiN diodes. These validated modes are used to perform electro-thermal-mechanical simulations to evaluate electrical failure mechanisms and thermal stresses in Viper module for nominal and fault operating conditions as discussed below.
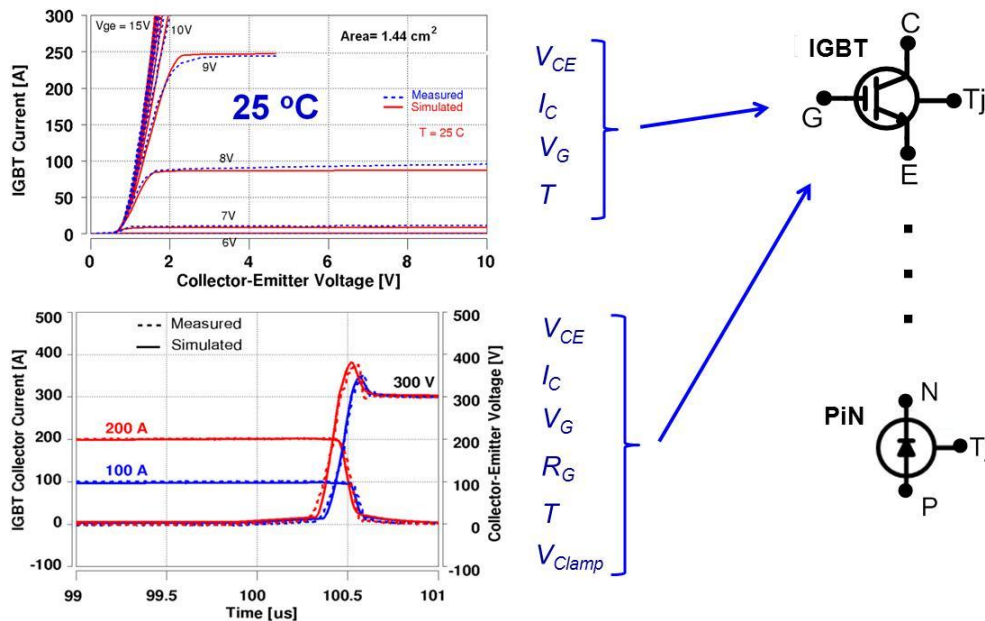
Figure II-91: Validation of Delphi Viper electro-thermal semiconductor models.

Figure II-92 demonstrates short circuit simulations and describes the resulting adiabatic chip heating for this condition. The left graph shows the collector-emitter voltage (V_{CE}), collector current (I_C), junction temperature (T_j), and total dissipated heat (Q_{Total}). The right graph shows how the heat is distributed in each node within the chip during the fault condition. During the short duration fault condition, the heat does not diffuse significantly beyond the chip junction depletion region (shown by E(t) at two voltages) and results primarily in local adiabatic chip heating.
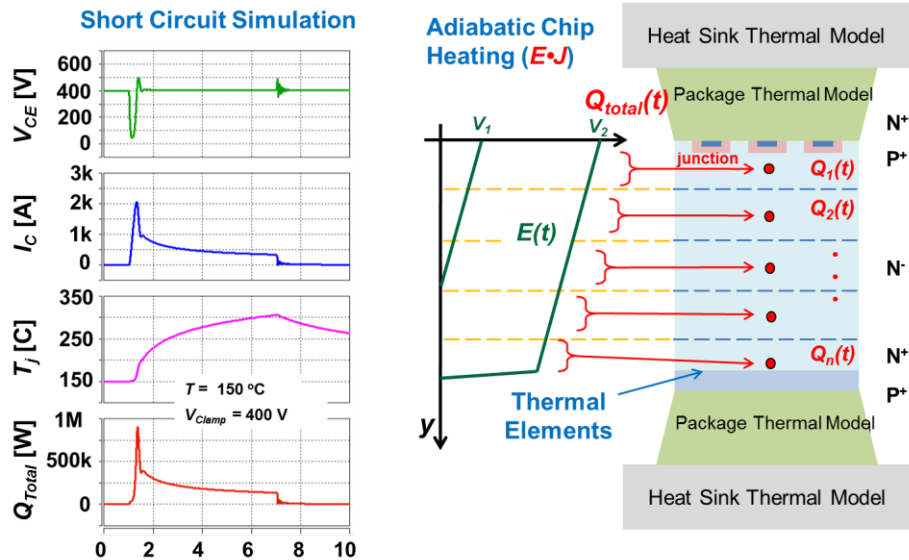
Figure II-92: Electro-thermal simulation of adiabatic heating for short circuit conditions.

Figure II-93 compares measured and electro-thermal simulations for various Viper short circuit conditions. It shows the measured (dashed) and simulated (solid) IGBT voltage, IGBT current, and IGBT junction temperature (T_j) for a gate pulse width of 10 µs, gate resistor of 2.2 Ω, temperature of 150°C, and for different gate voltage pulse amplitudes (i.e., 9 V, 11, V, 13 V, and 15 V). Other conditions compared (not shown in this report) include several gate pulse widths (3 µs, 5 µs, 7 µs, 10 µs), two different gate resistors (2.2 Ω and 5.6 Ω), different temperatures (25°C, 75°C, 125°C, 150°C), different clamp voltages (100 V, 150 V, 200 V, 250 V, 300 V), and different gate voltage pulse amplitudes (9 V, 10 V, 11 V, 12 V, 13 V, 14 V, 15 V). The comparison between model and electrical measurements for low voltage, low current, and short times are used to validate the electrical and thermal models for the device, package, and test circuit. The comparisons are then used to extend the Viper IGBT model to high-current with simultaneous high-voltage conditions using a short pulse to reduce heating during the pulse. Fianally, longer gate pulse widths extend the model validations to self-heating temperatures that are too high to be applied externally (near intrinsic temperatures).
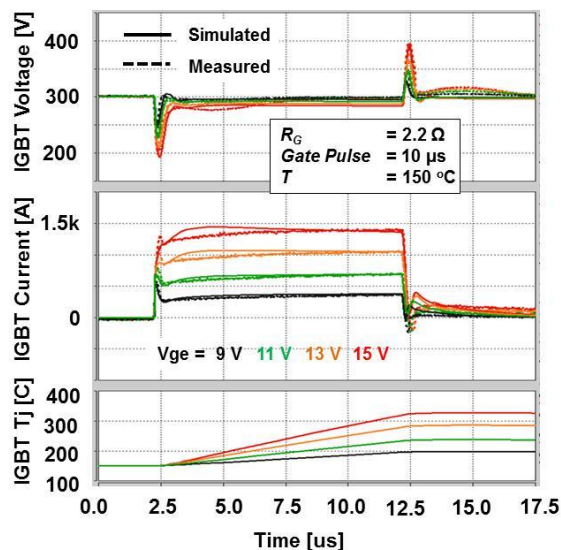
Figure II-93: Viper module short circuit fault operating conditions.

For longer times than the short circuit pulse widths shown above, the heat generated during the fault conditions or other operations conditions diffuses from the die into the package and heatsink. To validate the thermal model for the Viper package, a well-controlled and well characterized temperature controlled test fixture is needed. Figure II-94 shows the Viper module thermal test fixture of Figure II-89 (top picture) and the Viper module 262 W steady state ANSYS simulation for double-cooled test fixture (bottom picture).
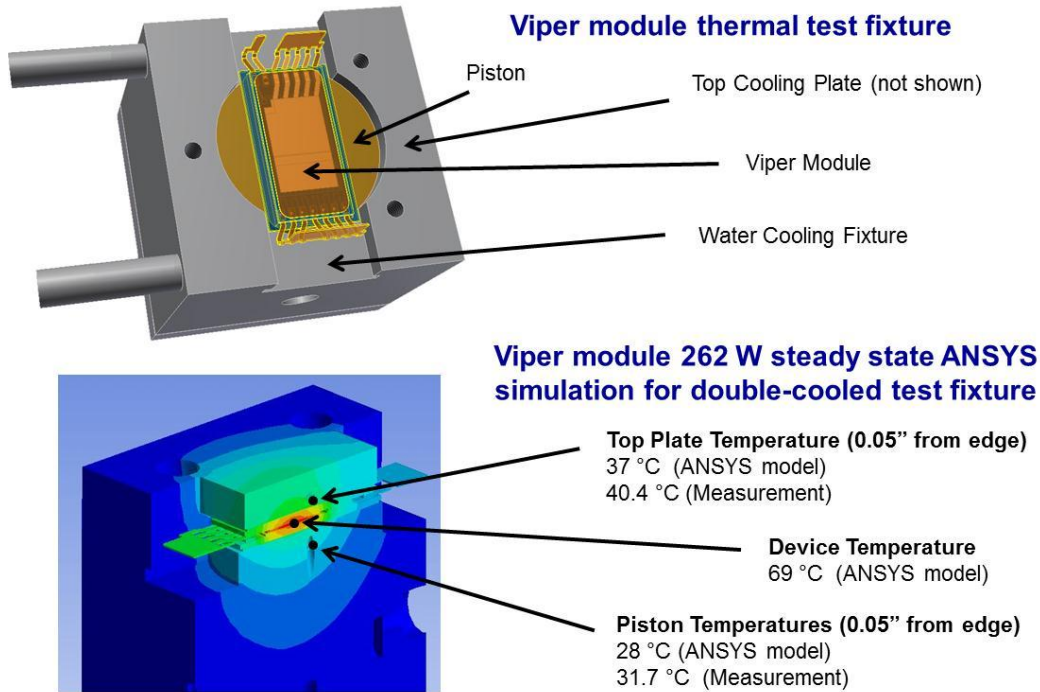
Figure II-94: Validation of viper module thermal test fixture in steady state.

Figure II-95 on the left shows the comparison of simulated (dashed) and measured (solid) junction temperature (using TSP) for short duration (5 ms) high power (600 W, 800 W, and 1000 W) pulses. Figure II-95 on the right shows the comparison of simulated (black) and measured (red) junction temperature (using TSP), plate, and piston temperatures (thermocouples) as shown in Figure II-94 for a low power (200 W) long duration (30 s) pulse.
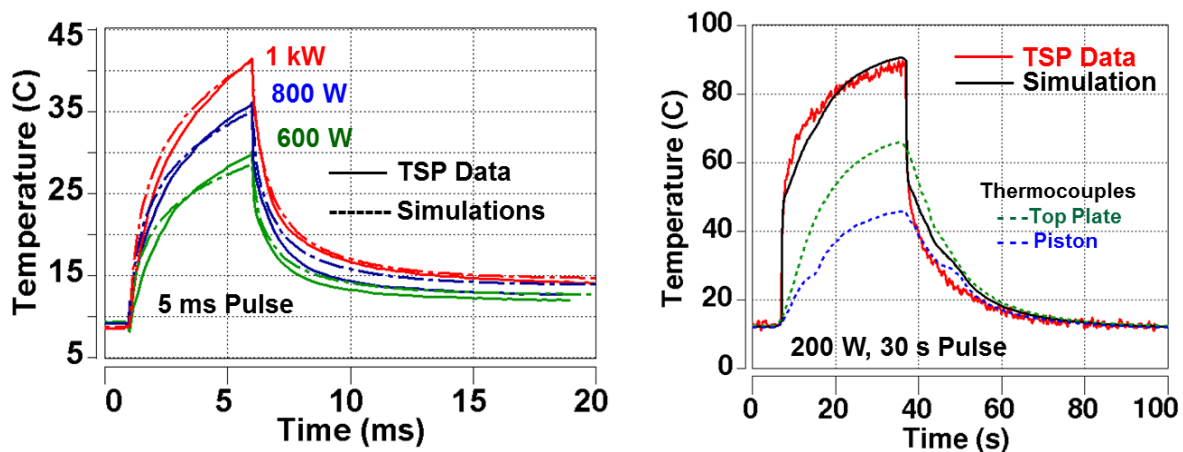
Comparison of simulated and measured Junction Temperature (TSP) for short duration, high power pulses.

Comparison of simulated and measured Junction Temperature (TSP), and Plate and Piston Temperatures (thermocouples) for a low power, long duration pulse.

Figure II-95: Validation of thermal network component model for Viper module package.

Figure II-96 shows simulation of the liquid-cooling thermal network component model for a double-side cooling Delphi-Viper module at the power level of 500 W and a pulse of 540 ms. The left graph shows the junction temperatures for the chip nodes, direct-bonded-copper (DBC) nodes, and heat sink nodes. The heatsink model is parameterized in terms of chip area and location; the heatsink base thickness, material density, heat capacity, and thermal conductivity; fluid flow speed; and fin area, number of fins, and fin channel length so that various cooling configurations can be simulated by altering these parameters.
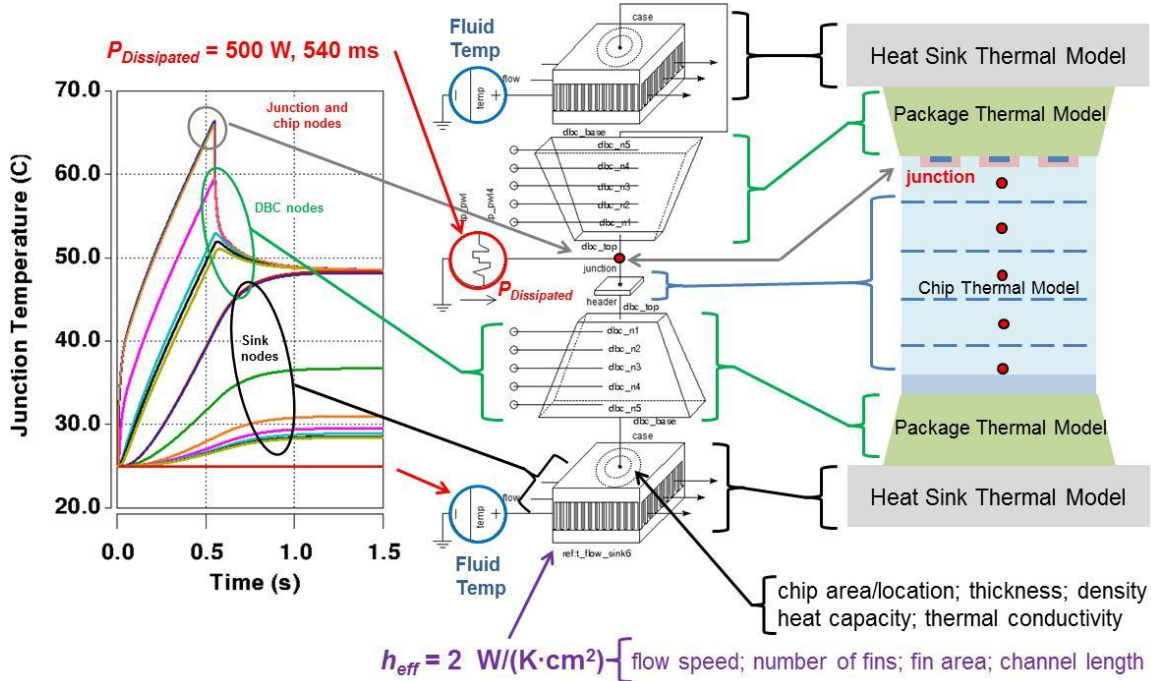
Figure II-96: Demonstration of liquid-cooled viper module thermal simulation.

B. Results for Virginia Tech Soft Switching Module:

Figure II-97 shows the circuit diagram (top) and its module components (bottom) for the Virginia Tech soft switching module that is designed for very high efficiency and low thermal impedance to enable operation with higher temperature coolant.
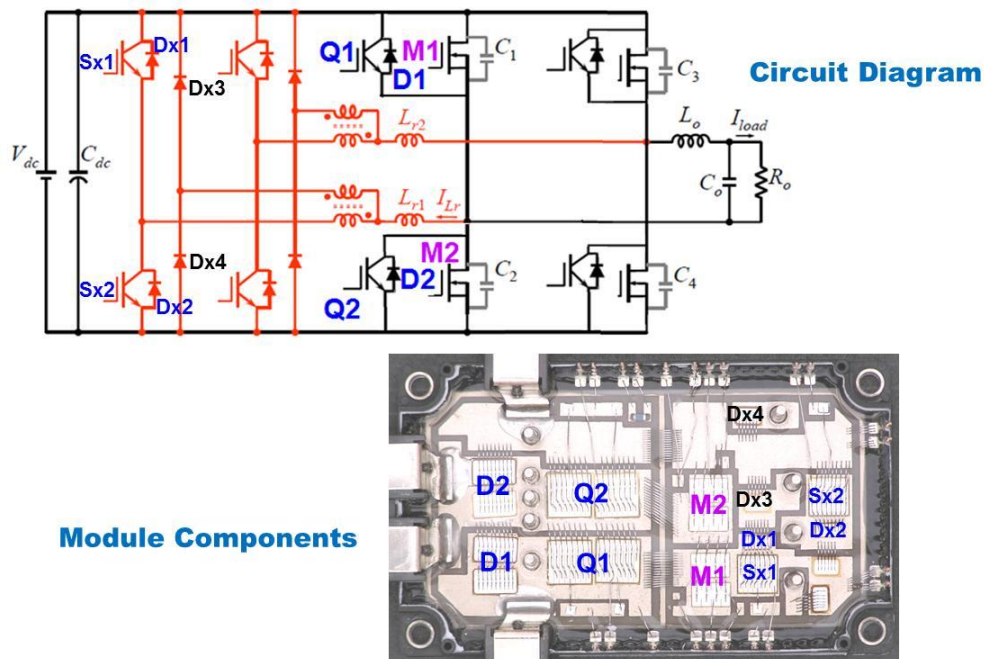
Figure II-97: Application of Virginia Tech soft switching module.

Figure II-98 depicts the approach used by the thermal network component model for the Virginia Tech soft switching module. The model is parameterized in terms of the die dimensions, die location within the module, and the materials thermal properties so that different layout and material configurations can be compared by altering these thermal model parameters. The model calculates the thermal resistance and capacitance of the internal thermal nodes based upon these parameters and the symmetry conditions of the nodes. The thickness of the thermal elements increases logarithmically with distance from the heat sources so that the model represents the wide range of thermal time constants with a minimum number of thermal elements. The thermal coupling resistances are particularly important for this Virginia Tech soft switching module model due to the large number of electro-thermal devices within the module.
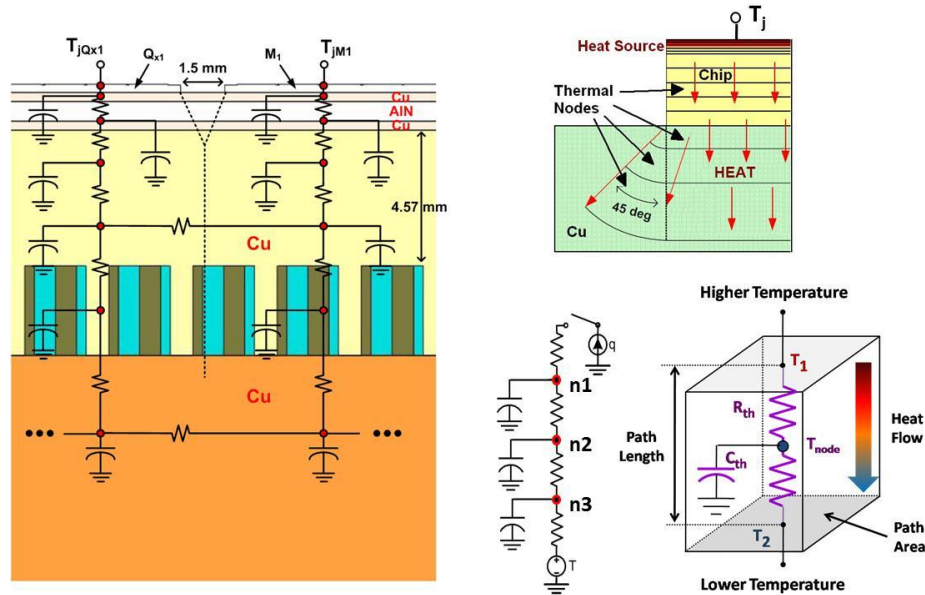
Figure II-98: Thermal network component modeling.

Figure II-99 summarizes the electro-thermal semiconductor model validation for the devices within the soft switching power module developed by the Virginia Tech program. The top graph shows the current dependence of inductive-load turn-off switching for the 600 V Silicon CoolMOS device at a clamp voltage of 300 V and gate resistor of 22 Ω at 25°C. The bottom graph shows the validation of current dependence of inductive-load turn-off switching for 600 V Silicon IGBT at a clamp voltage of 300 V, a gate resistor of 4 Ω, and a temperature of 25°C. The switching validations for both the CoolMOS and IGBT devices were performed at different circuit parameters (not shown) including different collector-emitter voltages (V_{CE}), collector currents (I_C), gate voltages (V_{GG}), gate resistors (R_G), temperatures (T), and clamp voltages (V_{Clamp}). The diode model is similarly validated for A wide range of circuit conditions. Representative validation results are shown in the following figures.
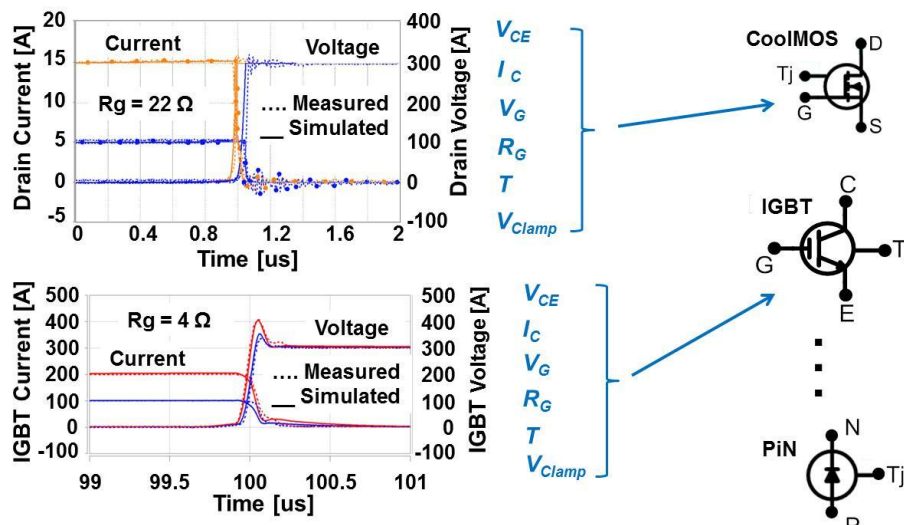
Figure II-99: Switching characteristic model validation for Virginia Tech module electro-thermal semiconductor models.

Figure II-100 shows the output characteristics mode validations results for the 600 V, 300 A Si IGBT and a 650 V, 60 A Si CoolMOS within the soft switching power module developed by the Virginia Tech at a) 25°C and b) 125°C.

600 V, 300 A Si IGBT

650 V, 60 A Si CoolMOS

Comparison of measured (dashed) simulated (solid) output characteristics at a) 25 °C and b) 125 °C for a 600 V, 300 A Si IGBT.

Comparison of measured (dashed) simulated (solid) output characteristics at a) 25 °C and b) 125 °C for a 650 V, 60 A Si CoolMOS.
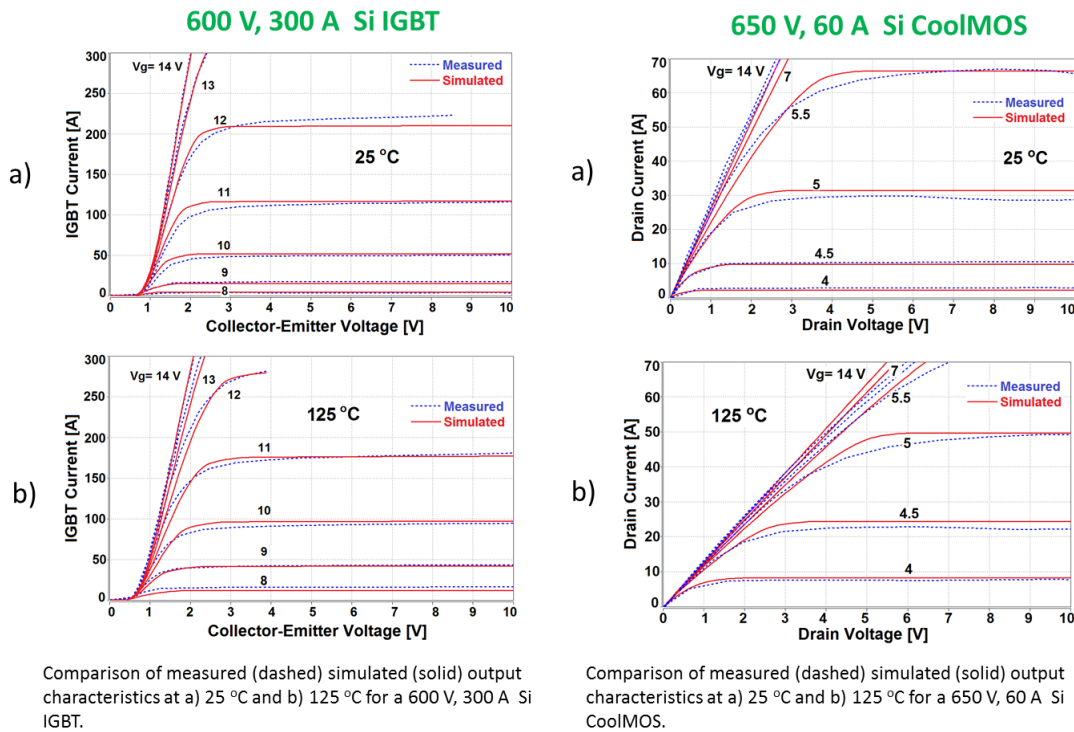
Figure II-100: Output characteristic model validation for Virginia Tech module electro-thermal semiconductor models.

Figure II-101 shows the measured (dashed) and simulated (solid) capacitance model validation results for a 650 V, 60 A CoolMOS within the soft switching power module developed by the Virginia Tech.

C_{GD} – Gate Sweep

C_{GD} - Drain Sweep

C_{DS} - Drain Sweep

C_{GS} - Gate Sweep
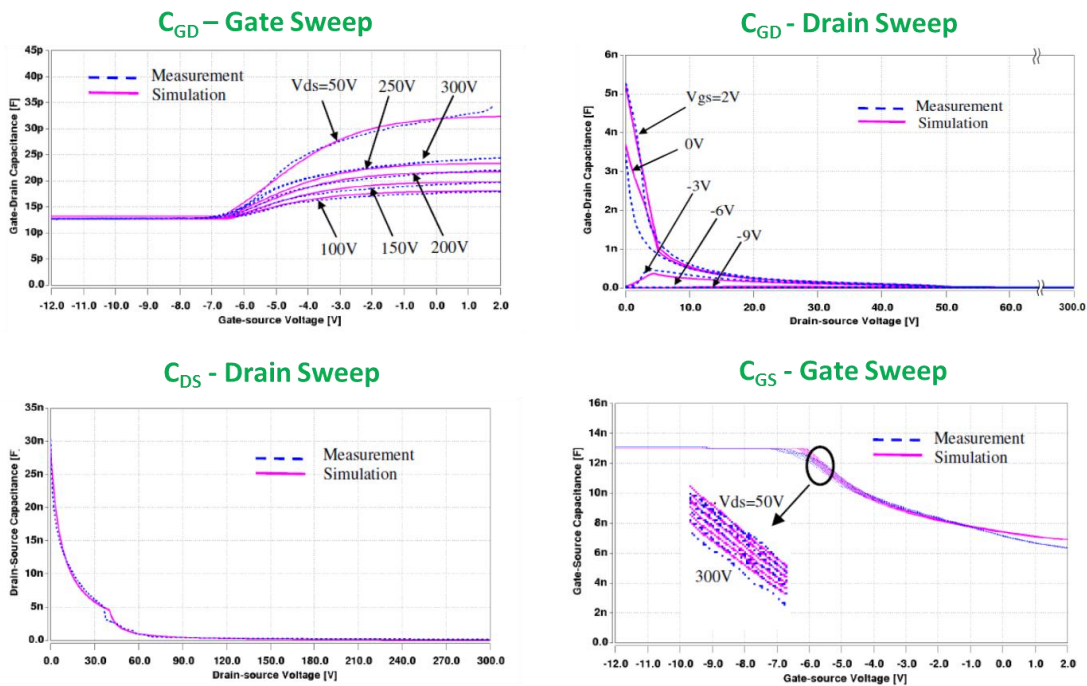
Figure II-101: Capacitance characteristics model validation for 650 V, 60 A CoolMOS within Virginia Tech module.

Figure II-102 (left) illustrates the Si CoolMOS model validation results for a drain current of 15 A, a drain voltage of 300 V (bottom) and three different gate resistances *Rg* (22 Ω, 50 Ω, and 75 Ω) at 25°C. Figure II-102 (right) shows the Si CoolMOS model validation results for inductive switching turn-off waveforms at 5 A and 15 A, and the drain clamp voltage of 300 V at 25°C for *Rg* = 22 Ω.
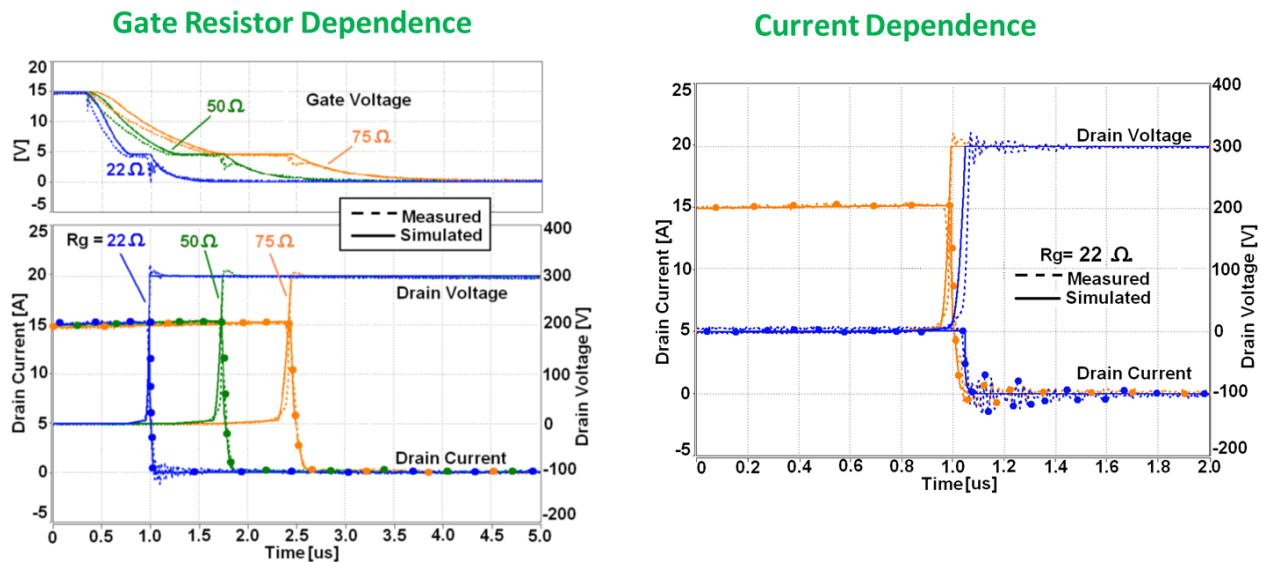
Figure II-102: Inductive load turn-off validation for a 650 V, 60 A Si CoolMOS.

Several options and issues have been addressed for the anti-parallel diode within the soft switching power module developed by the Virginia Tech with the support of the validated electro-thermal modeling. Figure II-103 shows the forward characteristics model validation results for a 600 V, 200 A Si PiN diode (top-left graph), a 650 V, 60 A Si CoolMOS-body diode (bottom-left graph), a 600 V, 6 A SiC JBS diode (top-right graph), and a comparisons of those three diodes.
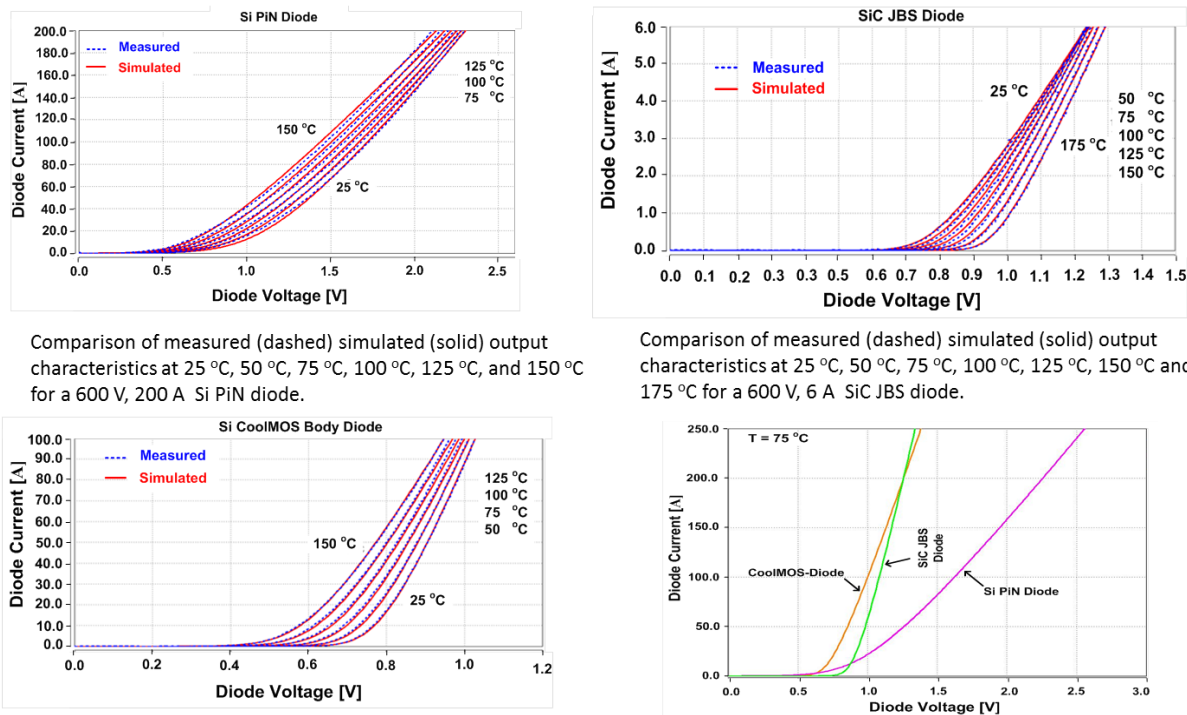
Comparison of measured (dashed) simulated (solid) output characteristics at 25 °C, 50 °C, 75 °C, 100 °C, 125 °C, and 150 °C for a 600 V, 200 A Si PiN diode.

Comparison of measured (dashed) simulated (solid) output characteristics at 25 °C, 50 °C, 75 °C, 100 °C, 125 °C, 150 °C and 175 °C for a 600 V, 6 A SiC JBS diode.

Comparison of measured (dashed) simulated (solid) output characteristics at 25 °C, 50 °C, 75 °C, 100 °C, 125 °C, 150 °C and 175 °C for the body diode of a 650 V, 60 A Si CoolMOS.

Comparison of forward characteristics for 650 V, 60 A Si CoolMOS anti-parallel diode; 600 V, 200 A SiC JBS diode; and 600 V, 200 A Si PiN diode at 75 °C.

Figure II-103: Si PiN, SiC JBS, and Si CoolMOS-body diodes.

The thermal network component model for the Virginia Tech soft switching module are validated using ANSYS simulations and high speed TSP measurements. Figure II-104 shows the multidimensional steady-state (SS) temperature distribution of the Virginia Tech module using ANSYS. The 3-D simulated data was used to calculate thermal resistances and power losses required as inputs for the network thermal component model developed in SABER.

Module Section	Legend in the Circuit Diagram	Total Avg Power Loss/Chip (W)
Main Switch	Q1, Q2	116.0
	M1, M2	36.0
	D1, D2	58.0
Auxilary Switch	Qx1, Qx2	18.0
Re-Setting Schottky Diode	Dx1, Dx2	0.5
	Dx3, Dx4	6.5
Noise Kick Diode	Dx5, Dx6	0.5

Average power losses were simulated.

Steady State Conditions @ 25 °C
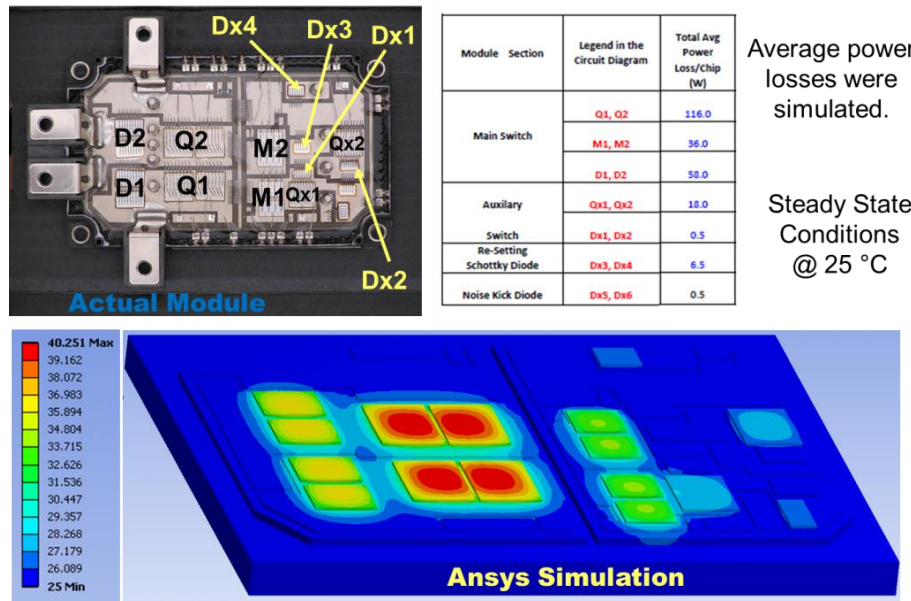
Figure II-104: 3-D ANSYS Simulation of Virginia Tech Module.

Figure II-105 shows the TSP measurement system configuration including cross-coupling of heat dissipated in the IGBT that increases the temperature of the adjacent MOSFET. During TSP calibration, the heat source is the hotplate temperature. During dynamic TSP measurement for a device, the heat source is the internal heat generated within the device during the heating phase. For the new enhanced cross-coupling TSP measurement, the temperature rise in the monitored device comes from the heat generated by an adjacent device. Both devices are individually calibrated for TSP using the temperature controlled hotplate, but during the transient measurement the power pulse is applied only to the device that serves as the heat source.

For the method to work, the **IGBT** has to dissipate a given **power** while the **MOSFET** remains off, and their gates must be measured independently.

$$TSP_{IGBT} = V_{CH1} - V_{CH2}$$

$$TSP_{MOS} = V_{CH3} - V_{CH4}$$

The devices were chosen for having physical proximity, different power dissipation ratings, and being thermally coupled through the same conductive layer on top of the DBC
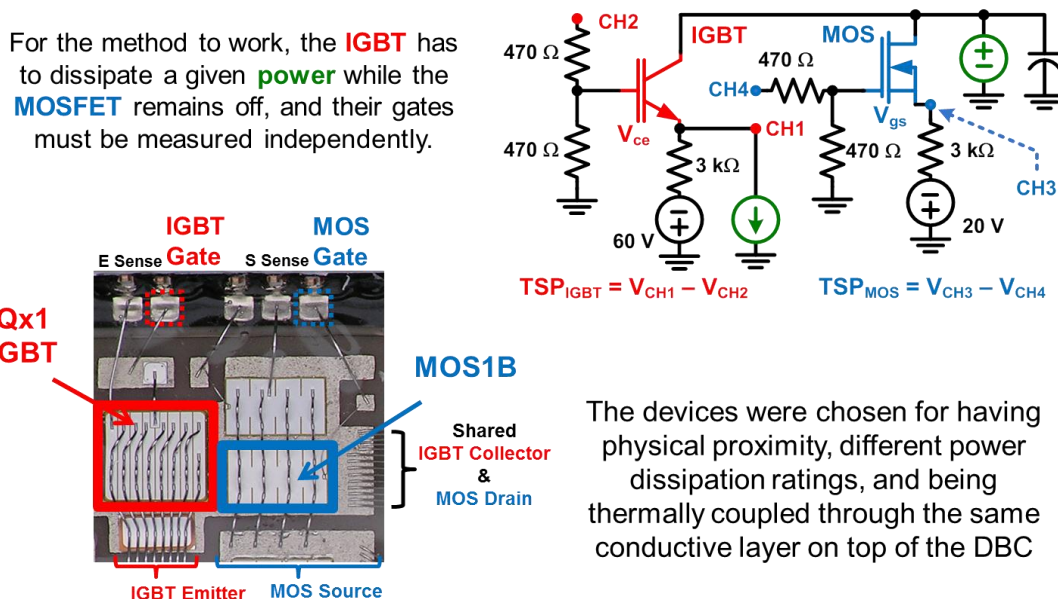
Figure II-105: Cross-coupling TSP measurement.

Figure II-106 shows the measured MOSFET junction temperatures that results from thermal cross-coupling of the adjacent IGBT shown in Figure II-105. To monitor how the temperature changed in the MOSFET junction due to heating from the IGBT, a 100 W-peak power pulse was applied to the IGBT with different duty cycles. Since the power was applied in the IGBT, its junction temperature curves show the typical self-heating profiles of dynamic TSP measurements when the pulse if turned on and off. However, there is a thermal delay for the heat dissipated in the IGBT to diffuse through the thermal stack before it reaches the MOSFET junction.

The IGBT was powered with a train of pulses at different duty cycles to generate enough average heat to be sensed in the MOS vicinity.

This IGBT measurements were used to validate the thermal transient behavior for the thermal stack model, and the MOS measurements were used to validate the thermal coupling model between adjacent power devices.
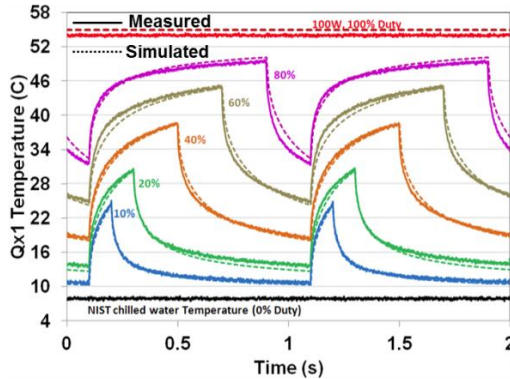
Preliminary electro-thermal coupling model results for the MOS measurements show a close correspondence in their behavior.
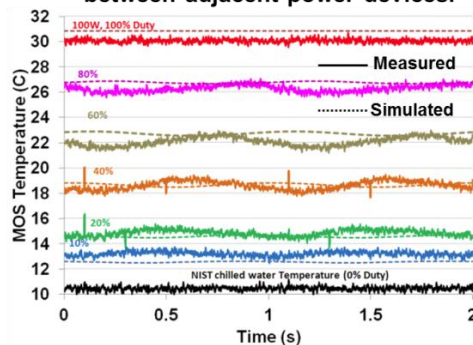
Figure II-106: TSP measurements of the Virginia Tech soft switching module used to validate thermal cross-coupling between the IGBT and MOSFET within the thermal network component model.

Figure II-107 shows the cross-coupling TSP measurements that were performed for three different peak power pulses: 50 W, 80 W and 100 W. The duty cycle of each power pulse was varied from 0% duty to 100% duty in steps of 5%. Measurements were acquired in a similar way as shown in Figure II-105 and Figure II-106, and then the average IGBT junction temperature for each duty cycle waveform was plotted against the respective average MOSFET junction cross-coupling temperature. The devices were allowed to reach a thermal steady state before acquiring the measurements. The cross-coupling curves show a linear behavior that comes from the thermal resistance path of the thermal stack below the devices.
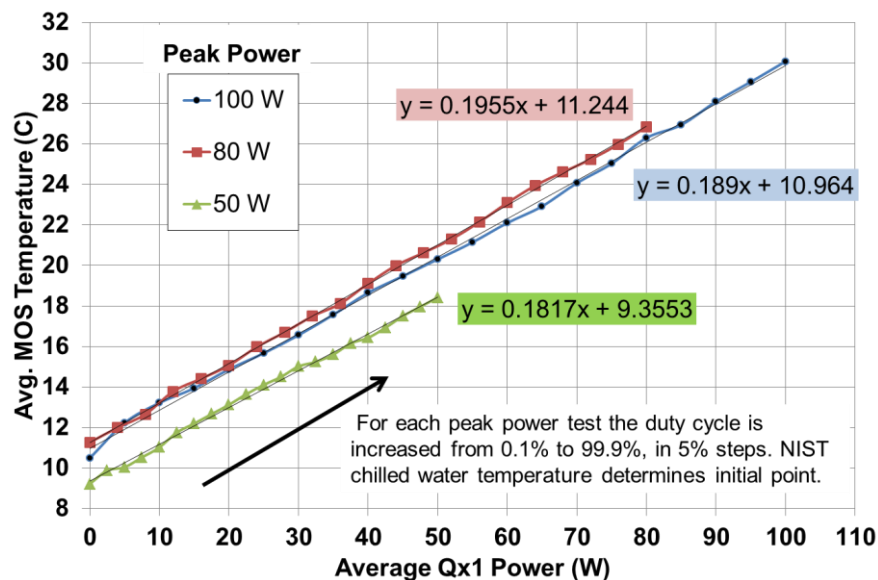
Figure II-107: TSP measurements of thermal coupling from powered IGBT to MOSFET.

Figure II-108 shows the Virginia Tech soft switching inverter circuit and full electro-thermal simulation temperature waveforms for the junction and header of the main and auxiliary switches.
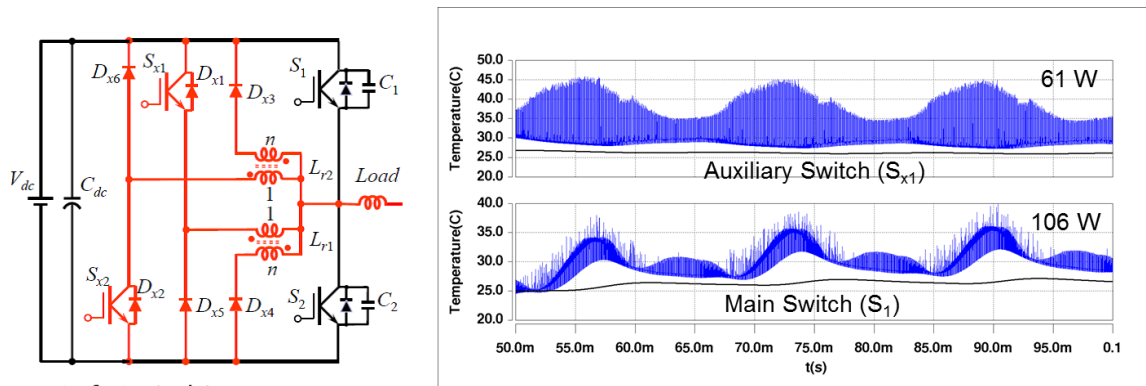
Soft Switching Inverter Topology

Electro-thermal simulation of junction temperature for switches undergoing half-sine wave power cycle.

Junction temperature (**blue lines**)
Bottom of the chip temperature (**black lines**)

Figure II-108: Soft switching inverter circuit and electro-thermal simulation of temperature waveforms.

Figure II-109 shows soft switching inverter electrical waveforms simulated using both a generic IGBT model (left graph) and the physics-based IGBT model (right graph) indicating that the actual voltage-current soft switching crossover timing predicted by the physics based model is delayed from the predictions of the generic model used to design the circuit. Accurate timing simulation is important for optimizing the zero-voltage soft switching crossover unless an automatic soft switching crossover circuit is used.
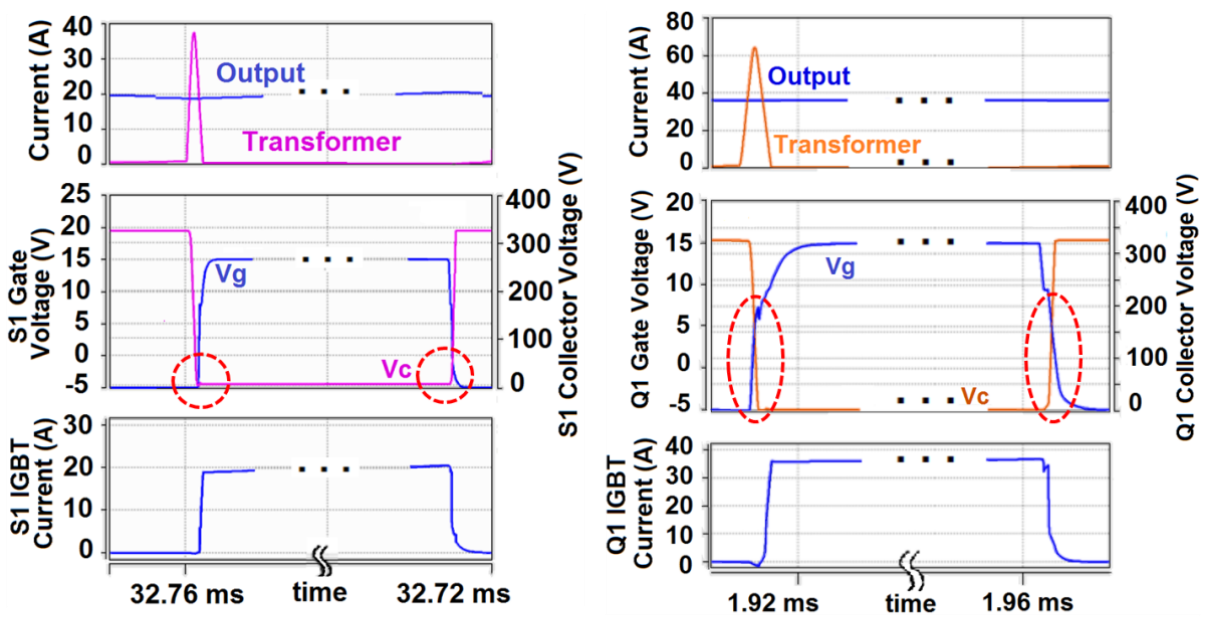
Simulations with generic IGBT model originally used to optimize timing for Zero-voltage switching.

Simulations with physics-based IGBT model indicate that timing is delayed from ideal model prediction.

Figure II-109: 5 kW electro-thermal simulation optimization of soft switching crossover.

Figure II-110 shows the full electro-thermal simulation of junction temperature for switches (CoolMOS, Auxiliary switch, and IGBT) during the half-sine wave power cycle at a 5 kW low power condition. For the low power condition the majority of the conduction and heating is in the CoolMOS device.
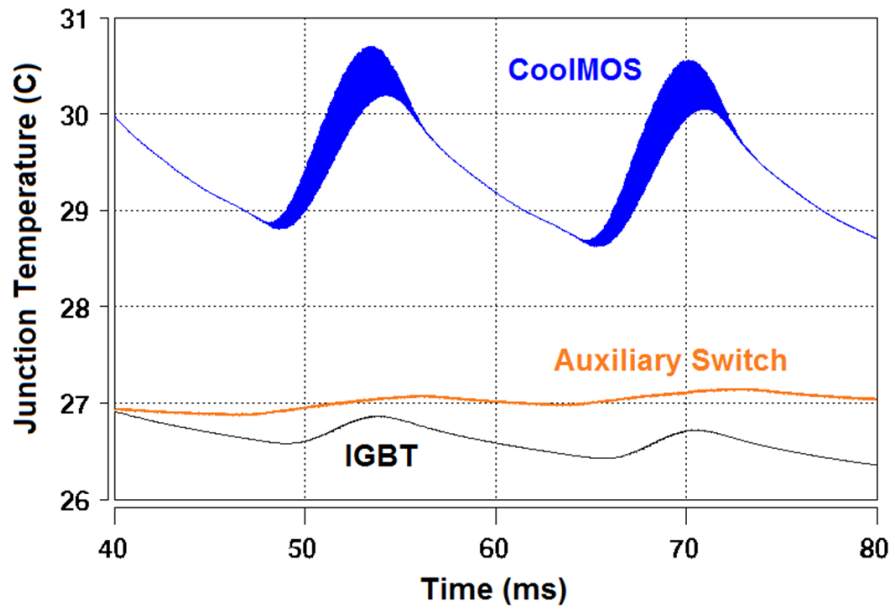
Electro-thermal simulation of junction temperature for switches undergoing half-sine wave power cycle.

Figure II-110: 5 kW electro-thermal simulation operating temperatures of devices.

Figure II-111 and Figure II-112 are full electro-thermal simulation results for the Virginia Tech soft switching inverter at the higher power 20 kW conditions. Figure II-111 shows the inverter sine wave output and the module main switch current and voltage details.
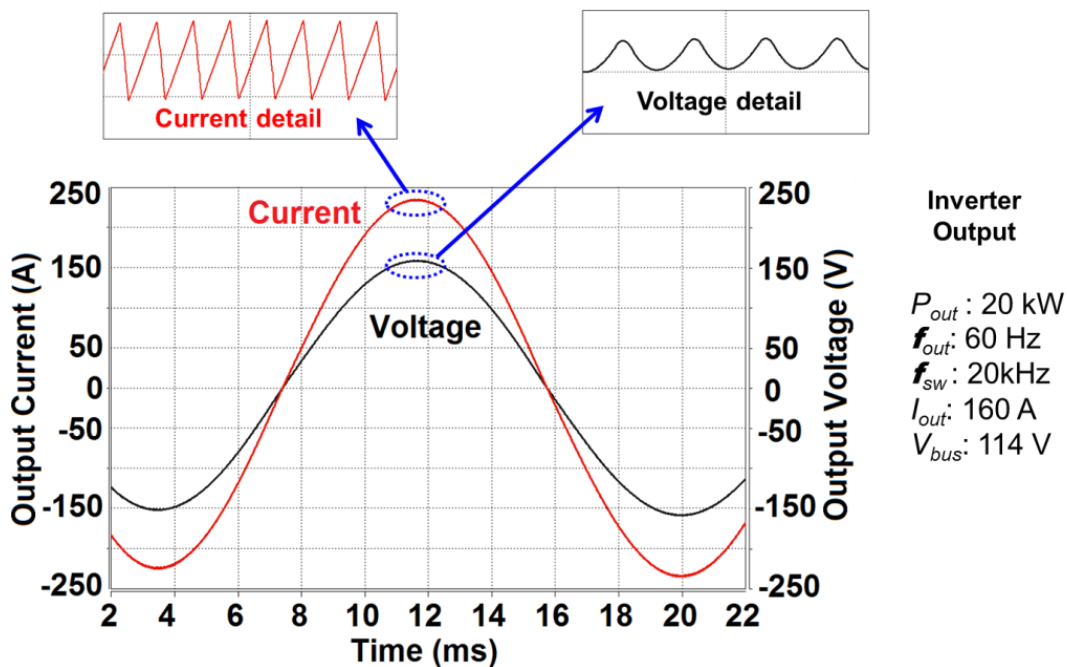
Figure II-111: Inverter output voltage and current from full electro-thermal simulation.

Figure II-112 (bottom-right graph) shows the device voltage and current within a 20 kHz switching cycle under soft switching conditions. The transformer current allows enough energy to discharge the main device (Q1) voltage to zero prior to main device conduction, enabling the zero-voltage switching condition. A dynamic dead time control is implemented which adjusts the turn on delays to allow for the soft switching condition over the entire load range. Figure II-112 (top-right graph) also shows how the main switch paralleled IGBT (Q1) and CoolMOS (M1) share current during a switching cycle. Depending on the load current, either Q1 or M1 will dominate the current conduction. This optimizes inverter efficiency by allowing MOSFET conduction at lower current levels and IGBT conduction at higher currents. Figure II-112 (upper-left graph) indicates the phase of the inverter output where each device dominates current conduction.

A variable timing scheme that uses a voltage sensing circuit to detect the zero voltage crossing condition is used to determine the main switch turn-on time. The transformer current allows enough energy to discharge the main device (Q1) voltage to zero prior to main device conduction, enabling the zero-voltage switching condition.
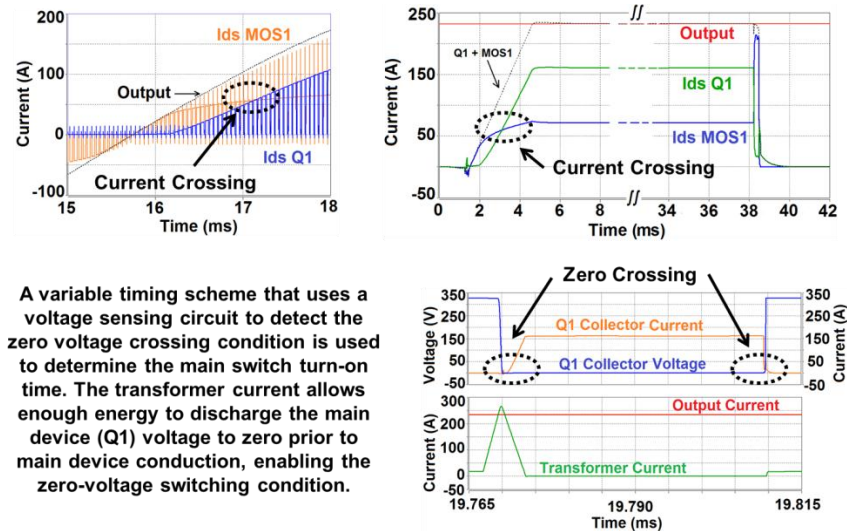
Figure II-112: Current sharing behavior of main device Q1 and M1 within a switching cycle (top-right graph) and device voltage and current showing soft-switching behavior of a full electro-thermal simulation and optimization of soft switching crossover (bottom-right graph).

Figure II-113 shows an example analysis of possible trade-offs for different semiconductor component selections in the Virginia Tech module. This demonstrates the analysis of current sharing of paralleled switches (Si IGBT and Si CoolMOS) and sharing of paralleled diodes (Si PiN, Si CoolMOS-body diode, and SiC JBS diode) at 25°C and 125°C. The left two graphs indicate that the hybrid switch (i.e., Si IGBT in parallel with Si CoolMOS) has lower on-state voltage drop at all current levels compared to discrete Si IGBT or discrete CoolMOS at different temperatures. The right two graphs indicate that for the devices used in this example, the SiC JBS diode has the lowest forward voltage drop at currents exceeding 250 A at 25°C and that the Si CoolMOS-body diode has the lowest forward voltage drop at currents below that. This crossover occurs at approximately 180 A for a temperature of 125°C. Careful consideration of the current sharing between diodes and resulting reverse recovery current versus temperature is necessary in this hybrid paralleled die module to minimize losses and optimize die size of the most costly components.

Analysis of current sharing of paralleled Switches (Si IGBT and CoolMOS)

Analysis of current sharing of paralleled Diodes (Si PiN, CoolMOS-body Diode, SiC JBS Diode)
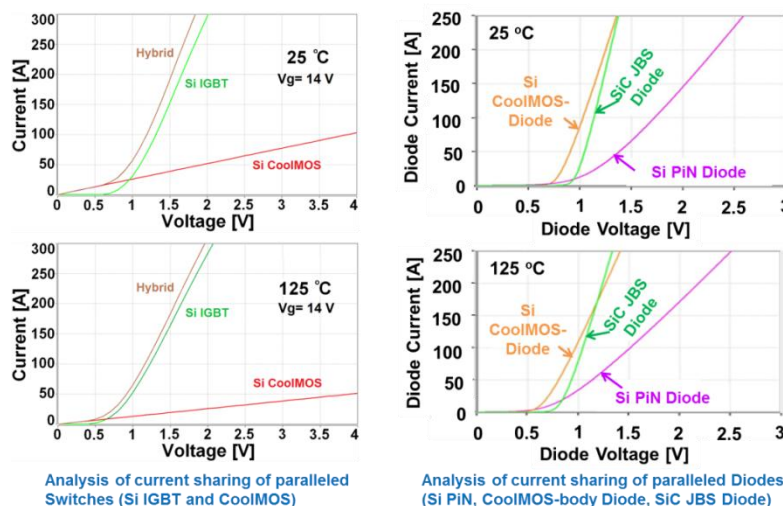
Figure II-113: Analysis of paralleled Si IGBT, CoolMOS, and diodes.

C. Results for Mechanical Reliability Model Development:

Figure II-114 depicts the methods for measuring damage to the die attach that occurs during thermal cycling experiments. The upper left graph of Figure II-114 show simulated junction temperature waveforms for a 10 ms heating pulse and for different values of die attach integrity quantified as the fraction of the die that is conducting heat to the header. As indicated, the junction temperature begins to reflect the change in thermal impedance after the heat has diffused beyond the die attach interface. The top right hand figure defines the increase in peak junction temperature at the end of the pulse (ΔT_j) which is used a measure of the degree of die attach damage. Since ΔT_j can be measured with the NIST high speed TSP system, it provides a means to nondestructively monitor the degradation during cycling experiments. The lower left graph of Figure II-114 shows a CSAM image indicating the die attach damage that was correlated with the damage monitored by TSP measurements of ΔT_j.
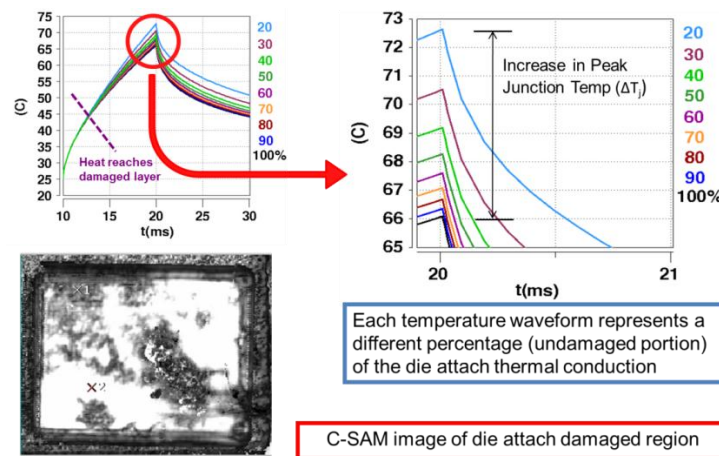
Figure II-114: Delamination results in decreased solder conduction and increased peak Tjunc.

Figure II-115 depicts the method of determining parameters for mechanical degradation models and for using the models in electro-thermal-mechanical simulations to predict degradation for application conditions. The process first involves the determination of set of thermal cycling degradation parameters and the value ranges that will provide information necessary to determine parameters for the physics-of-failure models. In this experiment, the thermal cycling parameters chosen are mean average temperature (T_{av}), temperature swing (ΔT), and dwell time at the min and max temperatures (t_{dw}). These parameters were chosen because they best fit physics-of-failure models being considered. Numerous modules (representative of the Virginia Tech soft-switching module) are them thermally cycled for all necessary parameter value combinations while being thermally monitored to detect and characterize buried thermal interface damage. Physics-of-failure models are then developed utilizing the collected degradation data sets. The physics-of-failure models will be used to perform full electro-thermal-mechanical simulations that predict the component life and degraded operation impact for vehicle driving cycle and fault conditions.
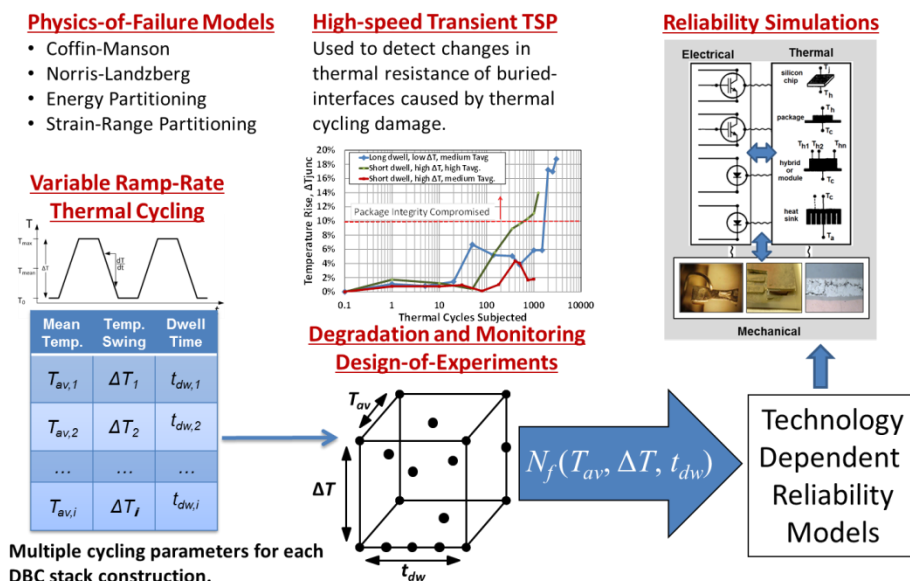
Figure II-115: Package reliability prediction method.

Figure II-116 show the different test parameters for 24 samples where colored letters show the conditions for samples that have been tested so far. In the left figure, the axis in red indicates the thermal cycling magnitude (ΔT) that the sample is to be subjected to, the axis in blue indicates the average temperature (T$_{avg}$) that the device is going to reach during test, and the axis in black indicates the dwell time that the device is going to stay at maximum and minimum temperature. Most of the tested so far have have been located in the upper portion of the cube to expedite extreme conditions.

Device ID	Cube Location	ΔT (°C)	T$_{avg}$ (°C)	t$_{dwell}$ (min)
I	Corner	120	100	15
A	Side	120	110	15
J	Corner	175	120	15
K	Corner	120	100	5
F	Side	175	110	5
H	Side	160	120	5
B	Corner	175	120	5
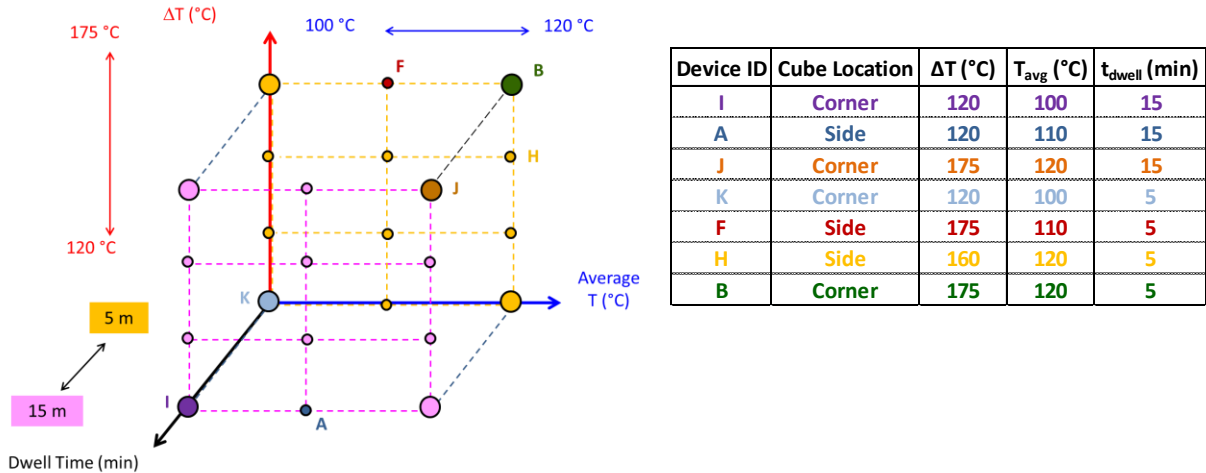
Figure II-116: Test Parameters for module thermal cycling experiments.

For the devices tested so far, Figure II-117 shows the ΔTj values measured with TSP as described above versus the number of cycles. Most of these samples tested so far were subjected to the extreme thermal stress conditions (high ΔT and T$_{avg}$) and show significant junction temperature rise at around 1000 thermal cycles. On the other hand, samples tested so far with mild cycling conditions (Device I and Device K) do not yet show significant junction temperatures rise after 1000 thermal cycles. However, further testing is needed to confirm these results and to determine degradation model parameters.
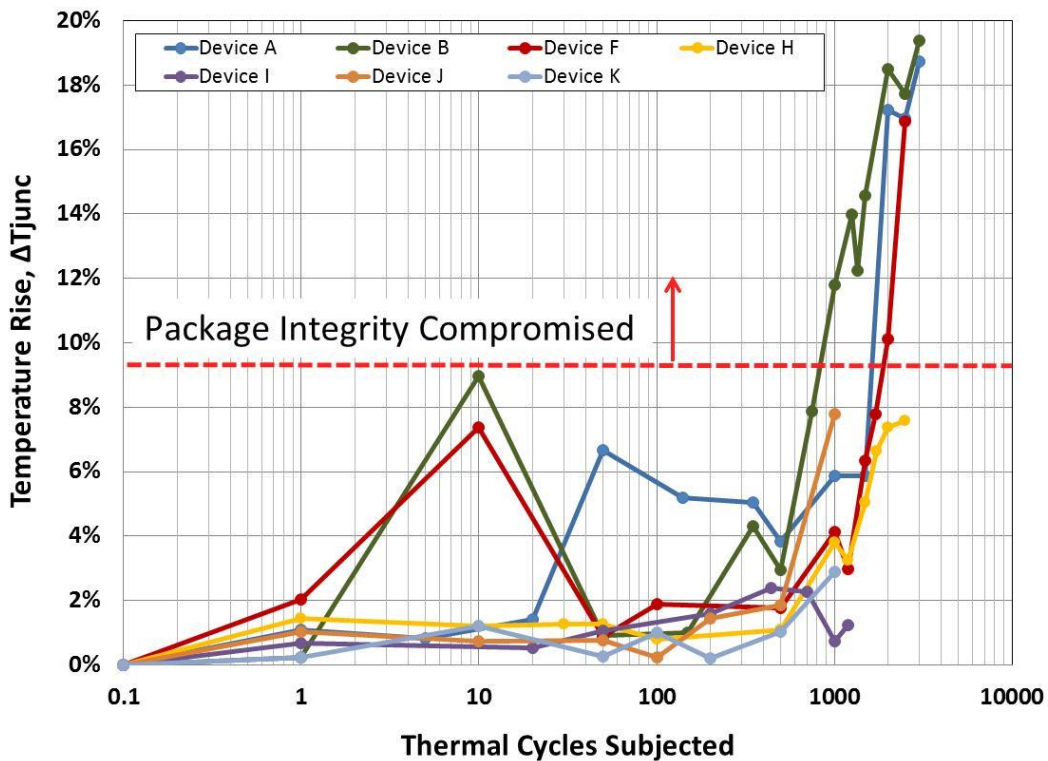
Figure II-117: Preliminary degradation results for different thermal cycling conditions.

Conclusion

This report summarizes the progress during 2013 towards FY13 and FY14 milestones using results of FY13 and prior work. The project includes the characterization and modeling of advanced power semiconductor devices and power module package technologies that are being developed and considered for advanced plug-in hybrid electric vehicle power conditioning systems and motor drives. The characterization includes full electrical and thermal performance, as well as stress and monitoring experiments necessary to characterize module and component failure and wear-out mechanisms. The validation results and simulation analysis are expected to provide confidence in the direction and progress of the Advanced Power Electronics and Electric Motors program, as well as to provide tools and methods for industry to more rapidly adopt the new technologies. This project utilizes the advanced characterization methods and equipment and models and extraction tools developed under several previous programs including previous Advanced Power Electronics and Electric Motors programs (previous reports show additional characterization and model validation results as well as test method and equipment development).

Publications

1. Reichl, J.; Ortiz-Rodríguez, J.M.; Hernandez,M.; Hefner, A.; Lai, J.; "High Speed Thermal Coupling Measurements for Multichip Electro-Thermal Model Validation," *Control and Modeling for Power Electronics (COMPEL), 2013 IEEE 14th Workshop on*, 23-26 June 2013, S.L.C., Utah

2. B. J. Grummel, H. A. Mustain, Z. J. Shen, and A. R. Hefner, "Reliability Characterization of Au–In Transient Liquid Phase Bonding through Electrical Resistivity Measurement," IEEE Trans. Compon., Packag., Manufact. Technol., submitted for publication Apr. 2012, accepted Dec. 2012

3. B. J. Grummel, H. A. Mustain, Z. J. Shen, and A. R. Hefner, "Thermo-Mechanical Characterization of Au–In Transient Liquid Phase Bonding," IEEE Trans. Compon.,

Packag., Manufact. Technol., submitted for publication Feb. 2012, accepted Dec. 2012.

4. B. J. Grummel, H. A. Mustain, Z. J. Shen, and A. R. Hefner, "Comparison of Au-In Transient Liquid Phase Bonding Designs for SiC Power Semiconductor Device Packaging," in Proc. Int. Conf. and Exhibition High Temperature Electronics Network (HiTEN), Oxford, United Kingdom, 2011.

5. B. J. Grummel, H. A. Mustain, Z. J. Shen, and A. R. Hefner, "Reliability study of Au-In transient liquid phase bonding for SiC power semiconductor packaging," in Proc. 23rd Int. Symp. Power Semiconductor Devices & IC's (ISPSD), San Diego, CA, 2011, pp. 260–263.

6. Hernández-Mora, M.; Ortiz-Rodriguez, J.M.; Grummel, B.; Hefner, A.R.; Berning, D.; Hood, C.; McCluskey, P.; , "Computer-controlled thermal cycling tool to aid in SiC module package characterization," Control and Modeling for Power Electronics (COMPEL), 2010 IEEE 12th Workshop on , vol., no., pp.1-6, 28-30 June 2010

7. McCluskey, F.P., and Hefner, A., Presentation at the Interagency Power Group Joint Mechanical and Electrical Engineering Workshop, Golden, CO. May 2010.

8. Hefner, A., Keynote Presentation at the IMAPS International Conference and Exhibition on High Temperature Electronics (HiTEC 2010) Albuquerque, NM. May 2010.

9. McCluskey, F.P., "Electrothermal-mechanical Modeling of Power Electronics Modules," Electronic Packaging Symposium, Niskayuna, NY. Sept. 2010.

10. McCluskey, F.P., "Vehicle Inverter Power Module Electrothermal-mechanical Simulation and Reliability," IEEE/CPMT 2010 Workshop on Accelerated Stress Testing and Reliability (ASTR), Denver, CO. October 2010.

11. McCluskey, F. P., and Hefner, A., "Electrothermal-mechanical Modeling of Power Electronic Modules," DOE Vehicle Technologies Program APEEM R&D Kickoff Meeting, Oak Ridge, TN. Nov. 2010.

II.6. Assessing the North American Supply Chain for Automotive Traction Drive Power Electronics

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Start Date: January 2013
Projected End Date: September 2013

Objectives

Synthesis Partners (Synthesis) was tasked by the Department of Energy (DOE) to undertake research to address the following specific questions regarding the North American (NA) supply chain of technologies for traction drive power electronics (PE) for plug-in, hybrid and electric vehicles:

1. How did the current PE production leaders succeed (in terms of volume) and what are their actions and strategies relevant to NA PE supply-network expansion activities?

2. What are the top constraints or bottlenecks that currently limit NA Tier 1-4 producers from achieving high volume power inverter manufacturing?

3. Can alternative scenarios and singular issues be leveraged to achieve a significant expansion in NA power inverter manufacturing volume?

✧   ✧   ✧   ✧   ✧

Introduction/Accomplishments

This research and analysis effort accessed thousands of secondary sources and hundreds of primary sources during an eight-month timeframe from January to August 2013. Table II-5 provides a detailed summary concerning the secondary sources searched, and Table II-6 provides statistics on the primary sources accessed during the course of this study period.

Synthesis employed a template of research questions to frame discussions with each of the primary sources, along with an introductory letter from Mr. Pat Davis, Director of

DOE's Vehicle Technologies Office (VTO). The introductory letter helped initiate contacts and explain the background and purpose of this research effort.

Table II-5: Secondary Source Research Statistics.

Research Statistics–Secondary Sources (All sources are English language unless otherwise specified)	
Market research reports reviewed	50+
Number reviewed (synopsis review)	30+
Number found to be relevant to topic	10+
Web sites reviewed	2,500+
Web pages reviewed in depth	5,000+
Companies identified and reviewed for relevance	1000
Companies reviewed in-depth (NA Power Electronics Supply Chain participants)	183
OEMs	20
Tier 1s	12
Tier 2–4s	151
Automotive R&D programs reviewed through secondary research	16
OEMs	9
BMW	
Daimler	
Ford	
GM	
Honda	
Hyundai	
Nissan	
Toyota	
VW	
Tier 1s	9
Calsonic-Kansei	
Continental	
Denso	
Hitachi	
Mitsubishi Electric	
Robert Bosch	
Toshiba	
Delphi	
Magna	

Research Statistics–Secondary Sources (All sources are English language unless otherwise specified)	
Japanese and Chinese language Web Sites Reviewed	200
Reviewed in depth	50
Key documents found	10
Journal Articles	
Number found	450+
Number reviewed	150+

The following table provides an overview of the scope of primary research conducted during the course of this study.

NOTE: Multiple contacts were frequently made with the same organization and more than one interview was often conducted with different personnel from the same organization.

Table II-6: Primary Source Research Statistics.

Research Statistics–Primary Sources (All sources are English language unless otherwise specified)	
Total contacts made	675+
E-mails	420+
Phone Calls	220+
In-Person Conference Contacts	35+
Distribution of in-depth interviews	
OEMs	23%
Tier 1s	40%
Tier 2-3s	23%
Others	14%
Automotive OEMs contacted	10+
Tier 1 suppliers contacted	25+
Tier 2-3 suppliers contacted	40+
Other companies and individuals contacted	50
University programs/researchers contacted	30
State-Federal government labs/agencies contacted	20

Synthesis discovered significant interest among sources in participating in technical discussions regarding the future of the NA automotive PE supply chain. There is also interest in providing input to DOE to support effective R&D and other investment decisions.

Synthesis fielded nearly 50 requests for information on or copies of the prior DOE-sponsored reports completed by Synthesis to date on behalf of the VTO. Primary source contacts and others have expressed interest in accessing the results and learning of DOE-VTO viewpoints and decisions

that may be partially based on these findings and other market research.

This research effort has found that the transplant OEMs (foreign companies that have located significant operations in NA) and Tier 1, 2 and 3 suppliers have clear interest in increased participation in this and other DOE-sponsored studies. These companies stated their interest in building information exchanges along the lines of the current research activity. Some transplant OEM executives made specific statements to Synthesis regarding their support of building out the NA supply chain.

Synthesis notes that the fact that a particular company did not participate was generally not for a lack of interest. In general, companies and sources stated that they did not have time, but stated their interest in continued engagement in the future.

Key Findings

Task #1: Lessons learned from the current leaders

- Synthesis assessed the paths taken to achieve global automotive traction drive PE leadership by Denso, Mitsubishi Electric and Continental.
  – Each company was investigated through a limited scope case study.
- Synthesis selected the three case study companies from among the global PE production leaders in the 2012 Top 10 inverter manufacturer list.
  – These companies consist of the two largest Japanese Tier 1s (Denso and Mitsubishi Electric) and the lead European Tier 1 (Continental). Synthesis ruled out Toyota because it produces its own inverters, and our tasking was to focus on Tier 1-4 supply chain dynamics rather than on internal OEM suppliers. DOE reviewed and approved of the selection criteria employed.
- Corporate analogies of each of these companies in terms of American companies are:
  – Denso: Delphi (nee Delco)
  – Mitsubishi Electric: General Electric
  – Continental: no current analogy, unless Goodyear were to buy Hitachi Automotive Systems America.
- The different approaches taken to supplier relations by these companies is striking, while the success of each is undeniable.
  – Whereas Denso and Mitsubishi Electric operate tightly integrated supply chains that institute common internal business standards and practices, Continental maintains a competitive Tier 2-4 supplier network with open opportunities for capable companies to participate. Continental does not rely on a vertical integration strategy (e.g., Toyota). Interestingly, Continental began as a tightly integrated firm, and then made the strategic decision to expand its supplier base beyond its initial relatively constrained supply chain, first to include European suppliers and later to encompass NA and Asian suppliers.

- The specific lessons learned relevant to NA PE suppliers, including the core ingredients to success that were found apply across each of the three companies, include:
  - Long-term, sustaining relationships with OEM(s)
  - Intent and capability to deliver global top-ranked quality, competitiveness and volume, and for a broad portfolio of automotive and beyond-automotive products
    - PE-only does not work
    - Automotive-only is not sufficient
  - Capability to invest hundreds of millions of dollars over decades
    - Patient capital linked to global growth strategy required
- Capability to build and sustain competitive facilities wherever the market demands and rapidly achieve proximity to fast-growing markets.
- Capability to produce consistent engineering reliability and product quality standards–communicated throughout a global supply chain–to achieve optimal supply chain value management.

Task #2: Top constraints or bottlenecks that currently limit NA automotive PE Tier 1-4 producers

- The issue of declining competitiveness of American automotive engineering and supplier networks is a key constraint affecting any potential growth of the American automotive supply chain. Market research data indicates that the loss of market share and competitiveness among American suppliers has accelerated as of 2012. In comparison to 2011, the 23 American automotive suppliers lost one rank on average in 2012.
- The market for automotive PE is more volatile and a fraction of the size of other PE markets such as industrial motors.
- Low profit margins
  - Profit margins of suppliers to mass market automotive OEMs are low and difficult to maintain
  - Anecdotal evidence indicates that profit margins in automotive PE are low relative to PE applications in other industries (e.g., oil and gas, industrial motors)
- Global competition
  - Global suppliers can meet–both through expanded investments in NA (an opportunity) and supply from abroad (a constraint)–current and expected demand for high-quality traction drive PE products
- Cost structure of the NA business operating environment
  - Labor and regulatory costs constrain new entrants and capital investment, particularly when non-NA sourcing arrangements do not hinder NA PE sales goals
- Lack of reliable information is a constraint on NA PE supply chain revenue growth. OEMs and suppliers repeatedly expressed a need for a comprehensive, up-to-date and accessible database on the NA PE supply chain to assist OEMs and suppliers to readily identify:

  - Suppliers of target items within a specific geographic area;
  - Brief descriptions of suppliers capabilities; and
  - Links to suppliers' websites or other data for more detailed information.
- Similar to the more familiar pyramid supply chain diagram (Figure II-118), the following supply chain diagram begins with the top point representing the OEMs, then widens out as the number of Tier 1, Tier 2 and Tier 3 suppliers are represented. However, around the Tier 3 level, at the widest part of the diagram, a gradual narrowing of the diagram begins to take place, representing the smaller number of suppliers at the Tier 4 and below levels. This narrowing continues until the diamond shape is completed again at a point at the base, representing the raw material suppliers. The narrow point at the bottom of the diamond could represent a critical weakness in automotive PE supply chain. This potential brittleness could constrain its future growth potential.
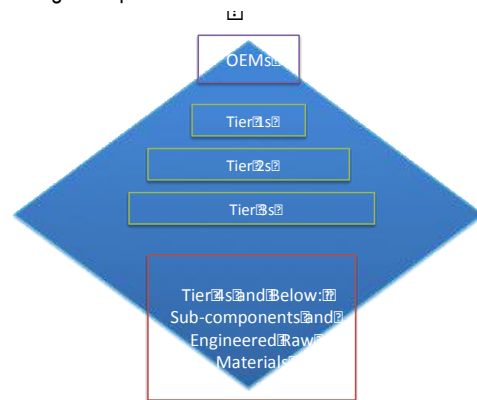
- While OEMs can seek to avoid supply disruptions by working with a range of Tier, 1, 2 or 3 companies, they appear to remain vulnerable to disruptions at the critical Tier 4 and below raw material layers.
- The brittleness finding does not indicate that there are no suppliers for materials essential to PE. Instead, this study has found that for many types of advanced materials and components needed for traction drive PE there may be suppliers that could offer products, but there are very few competing suppliers at the Tier 4 and below. This can cause disruptions in cases such as a period of strong market demand in which Tier 1s and 2s are seeking to expand production quickly. At such critical moments, brittleness in the supply chain works to constrain supplier volume and can extend the vicious cycle of low production volume, higher per unit costs, and the resulting low investment.
- There appear to be at least three factors contributing to the persistence of the present supply chain:
  - An insufficient understanding of both the nature of the problem and the level of the risk. The combination of these factors directly reduces the participants' motivation and capability to spur growth in the numbers and quality of Tier 4s and below.

- – Formidable barriers-to-entry exist for would-be new Tier 4s, as the incumbents are niche players, have deep connections to the Tier 2 and 3 automotive suppliers, and are extensively certified and warranted for automotive work.
  - – Profit margins in automotive supply are in general low relative to many other industries. There are significant alternative markets with higher volumes and/or higher profit margins, particularly for PE suppliers.
- Inconsistent levels of annual EV/HEV sales and long-term break-even points are likely causes of suppliers' reluctance to commit significant resources. This further contributes to the diamond-shaped supply chain.
  - – By contrast, a Tier 1 interview source noted that electrical machines consume 60-70% of global energy and demand for industrial sector electrical machines is growing 20% per year. This appears to indicate that market demand for industrial applications of PE will outstrip automotive growth rates in the near-, mid- and longer-terms.

Task #3: Scenarios and issues that could be leveraged to achieve a significant expansion in NA automotive traction drive power inverter manufacturing volume

- Primary and secondary research indicates that a significant expansion in NA power inverter manufacturing volume is unlikely in the foreseeable future due to:
  - – Current insufficient market demand to lead to shift a significant portion of the global supply chain to NA
  - – Globally competitive suppliers can satisfy current and expected demand for high quality products
  - – Profit margins in traction drive PE applications are low relative to PE applications in other markets (e.g., oil and gas, industrial motors)
  - – Industries other than automotive offer larger volumes for power inverter manufacturers
  - – The higher cost structure of the NA operating environment, including labor and regulatory costs
- The above factors contribute to capital and engineering talent flowing to non-automotive PE markets.
- Nonetheless, Synthesis finds evidence in favor of the likelihood of a limited expansion occurring within five years.
  - – Foreign-based OEMs are committed to expanding their NA-based production and their NA-supply chains. This represents an opportunity for Tier 1-4s in the NA PE supply chain that can meet the OEMs' requirements.
- Three distinct scenarios were produced by Synthesis to illustrate potential scenarios leading to a limited expansion in NA power inverter manufacturing volume
  - – <u>Scenario #1</u>: Increase NA Volume by Increasing Supply Chain Integration
    Supply chain integration involves a rationalization of the number of PE architectures, designs, and other aspects to increase supply chain efficiencies. Synthesis considers this scenario as the most likely to occur of the three outlined here. However, achieving this scenario will still be difficult.

- – <u>Scenario #2</u>: Increase NA Volume by Increased Investment, via a NA OEM-in-House Inverter Development
  This scenario acknowledges the competitive advantages that could accrue to an OEM should it pursue a Toyota-like strategy of in-sourcing inverter design and engineering. In order to implement such a strategy, significant investments would be required of the NA OEM. The viability of this strategy relies on the projected ROI. Synthesis assess that the likelihood of a NA OEM pursuing this strategy is low, but possible.
- – <u>Scenario #3</u>: Increase NA Volume by Increased Investment and Supply Chain Integration through Multiple OEM Collaboration
  Two or more OEMs may in-source the design and production of power inverter and collaborate to establish common integrated requirements for traction drive inverter components. In addition to the benefits outlined in scenarios 1 and 2, this scenario would result in more comprehensive understanding of technology gaps and the required investments and engineering skills. This scenario is judged to be very unlikely, as it incorporates the risks of the first two and further requires an unprecedented level of collaboration among the OEMs.

Approach

This study used a combination of targeted secondary research, covering both English and targeted foreign language sources, in conjunction with in-depth primary source interviews to assess the current state and trends in the NA automotive PE supply chain. The integrated primary and secondary research strategy featured a flexible approach to enable rapid adjustments as new information or insights warranted.

Synthesis finds that the literature on the NA traction drive PE supply chain is often outdated and frequently lacks objectively validated data sources. Valid data relevant to the NA PE supply chain (e.g., empirically-based distinctions between and among company positions, investment plans, product offerings, technology offerings) was found to be lacking.

Primary source contacts engaged with Synthesis under agreements to protect proprietary information. These contacts included foreign-based transplant companies with extensive NA operations. Accordingly, all information derived from these sources is presented anonymously. As a set of core data from which to draw general conclusions and perform analysis, Synthesis maintains confidential records for all information developed.

The sources and interviewees contacted in the course of this study provided many constructive comments and suggestions. However, the conclusions and key findings in this study are the result of Synthesis' independent assessment of the combination of primary and secondary information collected over approximately eight months, ending in August 2013.

Interviewees, independent experts and DOE personnel were not asked to endorse the conclusions or recommendations contained herein, nor did they review the final draft of the report before its release to the DOE-VTO.

Synthesis has made good faith attempts to ensure this study is accurate, up-to-date and as comprehensive. Nonetheless, SP looks forward to working with DOE stakeholders to identify gaps and refinements so that the results of this activity are precise, accurate, and provide the needed inputs for DOE decision-making.

Results

NA PE Supply Chain

Research identified more than 330 companies in the NA PE supply chain.

This study is focused on the NA supply chain for automotive traction drive PE, which includes:

- Automotive suppliers operating in the contiguous US, Canada and Mexico
- Automotive traction drive PE
  - A sub focus is on PE suppliers that are deemed to have sufficient capability or expertise to become linked to automotive traction drive PE supply chain activities in North America.

For brevity, all of the above information is frequently conveyed by the phrase, "NA PE Supply Chain."

Companies in the automotive sector are labeled according to their position in the supply chain, which extends from the top OEM, for example Ford or General Motors. The OEMs manufacture the final completed product for the consumer market. The Tier 1 through Tier 4 terms describe the level of the supply chain below the OEM that the company inhabits. Tier 1 companies are direct suppliers to OEMs. Continental, Delphi, Magna International and Denso are Tier 1 companies. Tier 2 companies are direct suppliers to Tier 1 suppliers; for example, Nichicon and SBE Electronics. Tier 3 companies are direct suppliers to Tier 2 companies, and generally supply advanced materials or basic components that are further processed, integrated or assembled into a key component by the Tier 2. For example, Dow Corning, Cree and Fairchild Semiconductor are direct suppliers to Tier 2 companies.

Tier 4 companies are direct suppliers to Tier 3 companies. These companies are suppliers of basic raw materials, such as ceramics, glass, composites, steel and other specialty materials.

The automotive supply chain is complex and many companies maintain supplier relationships at multiple levels in the supply chain, and are labeled accordingly. This means that some companies represent themselves as being in multiple Tiers at the same time.

Companies and Organizations in the NA PE Supply Chain

Synthesis endeavored to identify engineering, service, system integrators, assembly, manufacturing and developers of hybrid and all-electric powertrain related PE systems,

components and sub-components located in the US, Canada and Mexico.

This work was intended to portray 1) the NA supply chain for automotive traction drive PE, and 2) companies with product or engineering skill-sets of particular relevance to automotive-grade PE systems and components. These companies could provide components, engineering services and manufacturing capability related to traction drive electrical and electronic components to the automotive supply chain in NA. However, further analysis is required to validate their potential involvement and interest in the supply chain.

The following list includes organizations that:

- Have manufacturing, assembly or engineering service operations in NA
- Are considered mainstream contributors to traction drive PE
- Have PE manufacturing, engineering or technical service-related capabilities
- Could offer significant capabilities for any future expansion of the PE supply chain, even if they are not considered as part of a formal traction drive PE supply chain today.
- This list does not include:
  - Organizations that do not have manufacturing, assembly, or engineering service operations in NA
  - Battery manufacturers or developers
  - A complete list of heavy-truck/off-road hybrid electric vehicle product development and engineering companies

List of NA PE Supply Chain Organizations

Select NA OEMs, Including PEV and HEV Final Assemblers:

- AMP Electric Vehicles, Inc
- BYD America Corp.
- Chrysler LLC
- Electric Vehicles International
- Emerald Automotive LLC
- Ford
- General Motors
- Honda of America Manufacturing, Inc.
- John Deere
- Kleenspeed Technologies, Inc.
- Mercedes Benz R&D NA–A Daimler Co.
- Proterra
- Renault/Nissan
- Smith Electric Vehicles
- Tesla Motors
- Toyota

Select NA PE Tier 1 Suppliers:

- Allison Transmission, Inc.
- Baldor Electric Co. (ABB Subsidiary)
- Calsonic Kansei North America, Inc.
- Continental Automotive Systems U.S. Inc.
- Delphi Automotive LLP
- Denso International America
- Hyundai Mobis
- KollMorgen

- LG Chem Power, Inc.
- Mabuchi Motor America Corp.
- Magna Electronics, Inc.
- Mitsubishi Electric Automotive America, Inc.
- Odyne Systems LLC
- Protean Electric
- Quantum Technologies
- Remy International, Inc.
- Robert Bosch, LLC
- Rueland
- Saminco/American Traction Systems
- Siemens
- TDK Corp. of America
- TM4 Inc.
- Toshiba America Electronic Components, Inc.
- XL Hybrids, Inc.

Select NA PE Tier 2 Suppliers

- Arkansas Power Electronics International, Inc.
- AVX Corp.
- CEPCOS
- Fairchild Semiconductor
- Fuji Electric Corp. of NA
- General Atomics
- HRL Laboratories, LLC
- IBM Microelectronics
- Infineon
- International Rectifier Corp.
- Kemet Corp.
- Microsemi Corp.
- Mitsubishi Electric Automotive America, Inc.
- ON Semiconductor
- Phoenix International Corp.
- Powerex
- Renesas Electronics America Inc.
- Rohm Semiconductor
- SBE, Inc
- Spansion, Inc
- Taiyo Yuden (USA) Inc.
- Texas Instruments
- Toshiba America Electronics Components, Inc.
- Universal Semiconductor
- Vishay Americas

Select NA PE Tier 3 Suppliers:

- A2Mac1
- Analog Devices, Inc.
- Ansys
- Autocam Corp.
- Cree, Inc.
- EFC International, Inc.
- Electron Energy Corp.
- FEV, Inc.
- General Electric
- Hitachi Automotive Systems America, Inc.
- Honeywell Int.
- Keystone Electronics Corp.

- Kostal of America, Inc.
- Multicraft International
- OPAL-RT
- Orion Manufacturing, Inc.
- PWO de Mexico S.A. de C.V.
- Southwall Technologies, Inc.
- Superior Essex Inc.
- TRW Automotive U.S. LLC
- UT-Battelle, LLC
- Worldwide Manufacturing USA Inc.
- Xerow Research Centre of Canada
- ZF Electronics Corp.

Select NA PE Tier 4 Suppliers:

- Arnold Magnetic Technologies, Corp.
- Cree, Inc.
- Dow Corning
- Johnson Matthey, Inc.
- Kyocera America, Inc.
- Melexis Inc.
- Mirwec Film
- Sapa Extrusions
- Silicon Materials, Inc.
- Toray Plastics (America), Inc.

Lessons Learned from Global Automotive PE Production Leaders

This section addresses the tasking to determine the current PE production leaders, how they succeeded (in terms of volume), and their actions and strategies relevant to NA PE supply-network expansion activities.

Synthesis developed limited scope case studies concerning three global PE production leaders: Denso, Mitsubishi Electric and Continental. Synthesis selected these companies from among the global PE production leaders in the 2012 Top 10 inverter manufacturer list. These companies consist of the two largest Japanese Tier 1s (Denso and Mitsubishi Electric) and the lead European Tier 1 (Continental). The following analytic results are extracted largely from these studies.

These case integrated information from hundreds of secondary sources on each company, including from academic and business journals, public press announcements, targeted Japanese and Chinese language research, and selected insights obtained from primary sources. The purpose of the case studies is to research and analyze how the current PE production leaders came to be among the top-ranked among automotive traction drive PE producers.

Table II-7: Top 10 Inverter Manufacturers.

Manufacturer	2012
Toyota	1,017,178
Mitsubishi Electric	294,868
Denso	261,895
Hitachi	156,065
Continental	85,585
Bosch	56,153
Hyundai Mobis	53,762
Toshiba	42,320
Calsonic Kansei	37,980
TDK	22,271

The difference in approach taken to supplier relations by these companies is striking, while the success of each is undeniable. The following are the specific lessons learned relevant to NA PE suppliers, covering the core ingredients to success that were found apply across each of the three companies' growth:

- Long-term, sustaining relationships with OEM(s)
- Intent and capability to deliver global top-ranked quality, competitiveness and volume, and for a broad portfolio of automotive and beyond-automotive products
  - PE-only does not work!
  - Automotive-only is not sufficient!
- Capability to invest $100s of millions over decades
  - Patient capital linked to global growth strategy required
- Capability to build and sustain competitive facilities wherever the market demands and rapidly achieve proximity to fast-growing markets
- Capability to produce consistent engineering reliability and product quality standards–communicated throughout a global supply chain–to achieve optimal supply chain value management

In terms of manufacturing volume, the three selected companies are top players in the inverter market and are also major players in terms of OEM sales. However, Mitsubishi Electric is not nearly as dominant in terms of OEM sales for automotive parts other than inverters. The three companies are top inverter producers and key players in global OEM supply of parts ranging from fan belts to complete electronic systems. The NA OEMs are major customers of these companies.

Top Constraints Affecting NA Tier 1-4 PE Producers

Key Findings

The automotive PE supply chain is brittle in that disruption to a limited number of material or component suppliers (Tier 4 and below) can have significant negative impacts. This finding is key to understanding the context in which NA PE producers seek to achieve high volume production in the future.

Why the PE Supply Chain Is Brittle

The supply chain for many industries is commonly represented in the shape of a pyramid with the final product manufacturer at the top of the pyramid, followed by the number of Tier 1, Tier 2, Tier 3 and other suppliers in order as the pyramid shape widens out until the base of the pyramid is reached, representing the raw materials suppliers.

In contrast, as depicted in Figure II-118 above, the automotive PE sector supply chain is more appropriately represented in the shape of a diamond.

Similar to the more familiar pyramid supply chain diagram, the diamond supply chain diagram starts out at the top with the point representing the OEMs, then widens out as the Tier 1, Tier 2 and Tier 3 suppliers are represented. However, around the Tier 3 level, at the widest part of the diagram, a gradual narrowing of the diagram begins to take place, representing the smaller number of suppliers at the Tier 4 and below levels. This narrowing continues until the diamond shape is completed again at a point at the base, representing the raw material suppliers. The narrow point at the bottom of the diamond could represent a critical weakness in the automotive PE supply chain.

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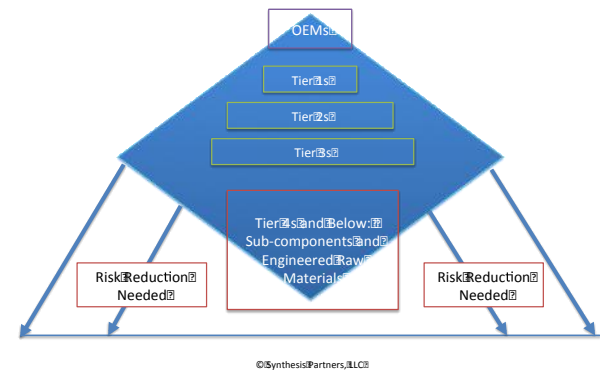
Figure II-119. Risk Reduction Needed to Address Brittleness in PE Supply Chain.

The figure above underscores where risk reduction strategies are needed to address the empty space–that is, in the space between 3 supplier levels and the far more limited number Tier 4 level suppliers.

Several examples of the negative impacts of brittleness in the automotive supply chain include the recent natural and man-made disasters that have had serious impacts on the mid- and lower levels of the automotive supply chain. Sources contacted for this project discussed the devastating affects of the tsunami that struck Japan in March 2011, and the massive flooding in Thailand and their impacts on future growth possibilities on the NA PE supply chain.

Nonetheless, there appear to be at least three factors contributing to the persistence of the diamond-shaped supply chain:

- An insufficient understanding of both the nature of the problem and the level of the risk. The combination of these factors directly reduces the participants' motivation

and capability to spur growth in the numbers and quality of Tier 4s and below companies.

- Formidable barriers-to-entry for would-be new Tier 4s, as the incumbents are companies are niche players, have deep connections to the Tier 2 and 3 automotive suppliers, and are extensively certified and warranted for automotive work.

- Profit margins in automotive supply are in general low relative to many other industries,. There are significant alternative markets with higher volumes and/or higher profit margins, particularly for PE suppliers. This makes it difficult to attract investment and new entrants.

Key Findings from Primary Research Sources

Each table/figure below addresses a key question that was discussed in the interviews during this research task. Synthesis' assessment is not attributed to any particular interview source, but is rather the result of Synthesis' integrated assessment of all the information developed during this task.

Table II-8: Discussion Results: "Is the Traction Drive Inverter Market Important to Your Firm?"

Type of Respondents	# of Respondents	Answer: YES	% of Total	Answer: NO	% of Total
OEM	10	7	70%	3	30%
Tier 1	17	12	71%	5	29%
Tier 2	9	2	22%	7	78%
Tier 3	1	0	0%	1	100%
Other	6	3	50%	3	50%
ALL	43	24	56%	19	44%

Analysis:

- In response to the question "Is the traction drive power inverter market important to your firm?" a slight majority of respondents, or 56%, (24 of the 43 interviewees)–stated that it was.

- Approximately 70% of the OEMs and Tier 1s interviewed stated it was. This is not surprising given the primary role that each of these types of organizations play in advancing the development of key components used in hybrid and electric vehicles. Their business and planning interests require that the core components needed for hybrid and electric vehicles are available and economical.

- Tier 2 and 3 companies exhibited significantly less interest (~25% responded in the affirmative) in the traction drive power inverter market. This response indicates the challenge that exists in terms of growing the participation of Tier 2 through 4 organizations in the marketplace for automotive traction drive power inverters.

- Approximately 44% of all respondents (19 of the 43 interviewees) stated that the traction drive inverter market is not important to their firm. These respondents are essentially stating that they are not interested in making significant investments in this market at this time.

- A minority of OEMs and Tier 1s (30%) do not believe that the traction drive inverter market is important to their firm,

while a majority of the Tier 2 and other companies (50–75%) take this view.

- The responsiveness and responses of the Tier 1s queried indicates that these companies are deeply committed to sustaining the NA PE supply chain. Synthesis assess that a strategy to enhance the NA supply chain diversity and capability would be well-served by engaging these companies.

- Secondary sources indicated that Tier 1s are hedging their bets and seeking to expand to industries beyond automotive to diversify their markets, even while they are committed to automotive OEM customers.

The bar graphs below provide rankings of companies based on the number of times interviewees cited these companies as investment leaders in the NA PE supply chain.
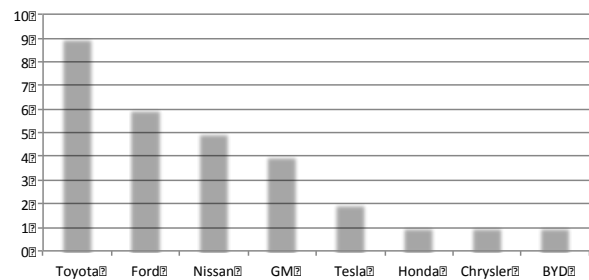
Figure II-120. Frequency that OEMs were mentioned during interviews regarding PE Investment Activity in NA.
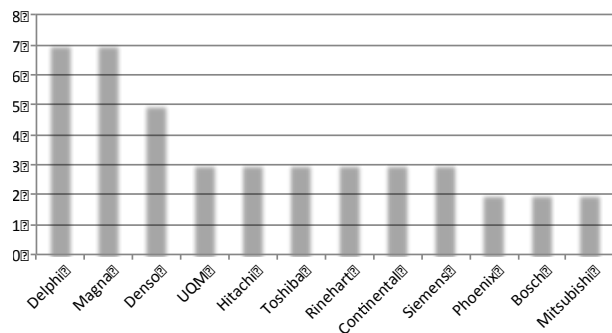
Figure II-121. Frequency that Tier 1-3s were mentioned during interviews regarding PE investment activity in NA.
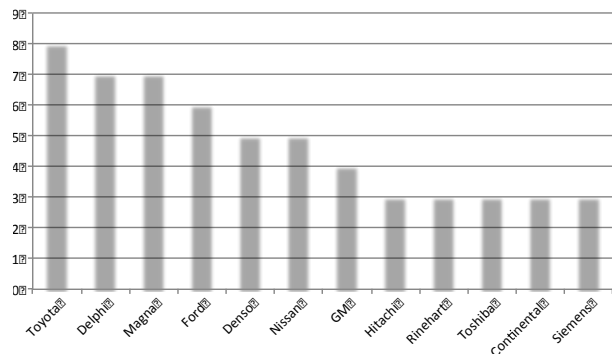
Figure II-122. Frequency that all companies were mentioned during interviews regarding PE investment activity in NA.

Analysis:

- The above three figures depict the most-cited companies, by category, in interviews regarding NA PE supply chain investment activity.
- Investment leaders in the NA PE supply chain appear to be either 1) among the global leaders in HEV/EV production, including PE components, or 2) NA-based automotive suppliers that are exceptionally focused on building a sustainable PE supply chain in NA.
- Three of the top five companies in the All Company category are headquartered in NA. This may be attributed to the size of the U.S. market for EVs and HEVs.
- Research did not indicate that any of the companies listed are planning strategic-level coordination.
- There is a lack of representation of Tier 2 through 4 companies in the above rankings. This is an additional factor in exacerbating the already brittle supply chain.
- Numerous respondents noted Delphi's NA investment activity, despite the fact that Delphi is not in the top tier of global PE suppliers.
- The frequency with which UQM was referenced is notable, as it is a motor, not PE supplier. UQM's intensive engagement with DOE is apparently having an impact on community perceptions.

Table II-9: Distribution of Positive Responses: "Is a US-Based PE Supply Chain Critical to Your Firm's Future Success?"

Number of Respondents	Number of Respondents That Agree	Rationales for Agreement	Share of total Respondents That Agree
36	11	Reduce inventory costs, increase competitiveness, protect IP	50%
	5	To continue process of expanding NA supply base	23%
	6	Other rationales	27%
TOTAL:	22	All of above rationales	61%

Analysis:

- In a wide-ranging set of in-depth interviews, Synthesis identified a small number of rationales for supporting a NA-based PE supply chain.
- A strong majority of companies (61%) that engaged in these discussions with Synthesis believe that a U.S.-based PE supply chain is critical to their firm's future success. This would appear to augur well for initiatives designed to expand participation of current and new players in NA PE supply chain developments.
- Among respondents answering positively, 50% cited the desire to increase competitiveness by reducing logistics and inventory costs and protecting IP.

- – Proximity to markets reduces costs, and any cost reduction is notable in that it can deliver a competitive advantage in a very competitive global market.
- – There is a significant potential benefit for suppliers if their IP can be protected to some extent. This could catalyze innovation since the innovators can be more confident that their inventions will accrue a reasonable ROI.
- Among all the respondents, Synthesis found an understanding that the U.S. is at a crossroads in terms of both the need for, but absence of a globally competitive NA automotive PE supply chain.
- Companies that are investing in the NA PE production, naturally support investment in similar activities by other organizations and the USG in order to support a more diverse, higher capitalized set of participants.

Table II-10: Distribution of Negative Responses: "Is A U.S.-Based PE Supply Chain Critical To Your Firm's Future Success?"

Number of Respondents	Respondents That Do Not Agree	Rationales for Disagreement	Share of Total Respondents That Do Not Agree
36	9	Supply chain is global; environmental regulations are too strict in NA; in any case, external factors such as shipping costs, exchange rate fluctuations and market volumes determines location of suppliers	64%
	4	Overseas suppliers are currently the source of necessary engineering, technology and components.	29%
	1	Other rationales	7%
SUBTOTAL:	14	All of above rationales	39%

Analysis:

- 39% of the respondents (14 of 36) do not believe that a US-based PE supply chain is critical to their firm's future success. This may be a large enough cohort to have a negative impact on the development of a NA PE supply chain. Their rationale:
  - The current supply chain is global and sufficiently large to address demand
  - Environmental and other business regulations are too heavy in North America. This view is voiced particularly in comparison to low-cost Asia-Pacific nations.
  - External factors, which suppliers have no control over (e.g., exchange rate fluctuations, shipping costs, market volume) will determine location of suppliers
  - The development, engineering, technology and components needed are primarily sourced from overseas suppliers
- The challenge of establishing automotive PE IP positions– and protecting these positions–in order to generate a sustainable competitive advantage is a topic of concern and discussion.
- These responses point to a recognition that current market conditions are not sufficient to drive extreme changes in the PE supply chain.
- Real-world constraints, such as exchange rate fluctuations, shipping costs, trends in EV/HEV market volumes and demand are all considered beyond the control of automotive suppliers. Among the responses who answered negatively, Synthesis found a "work with what we have" mindset. These companies do not appear to push for new approaches to achieve significantly different PE supply chain dynamics in NA
- Among the major benefits of the current global supply chain are the ability to leverage, through outsourcing arrangements, the high-level PE development, engineering and technology development capabilities resident among dominant overseas suppliers.
- Respondents uniformly recommended a careful and cautious and gradual development strategy for the NA supply chain.

43 interviewees were queried concerning their assessment of the key advantages and disadvantages of a NA PE supply chain. Each interviewee could provide one or more response, or no response. The results are depicted in the following analyses.

- The most frequently cited advantage of a NA-based PE supply chain is proximity to market. This includes time-to-market advantages (in which hours and days count) and cost advantages resulting from reduced shipping and inventory charges.
- The second most frequently cited advantage of a NA PE supply chain is the US' industrial-base's capability to generate knowledge and break-through technology and produce reasonable ROI.
- The third most frequently cited advantage is the EV/HEV market potential in NA The NA market size is discussed in the secondary source sections of this report. This

interview finding underscores how economic and market conditions are the ultimate determining factors for automotive supply chain investment decisions.

- The fourth most frequently cited advantage of a NA PE supply chain are the opportunities to develop and leverage partnerships between industry and government.
- Other advantages mentioned less frequently included factors such as exchange rate fluctuations, IP protection and ease of communication. This is not an indication that these are not important to a small, but vital, set of companies.
- The most frequently cited disadvantage–by far–of the NA PE supply chain is the perceived high cost of the products produced. Economics factor on both the pro (proximity to market) and con side of the NA PE supply chain issue.
- Any investment activity in NA which does not include plan to meet globally competitive cost benchmarks will not succeed in the long run.
- The frequency of responses is similar among the second through fifth disadvantages listed above. This points to a level of agreement among sources regarding market demand instability and risk-averse investment planning in the NA automotive PE market.
- Specifically, the following factors were suggested to Synthesis as carrying equivalent weight as disadvantages in the NA context:
- Unstable/insufficient market demand.
  - Risk-averse investment planning: numerous sources highlighted the negative implications for building and sustaining a new industry, e.g., automotive PE supply, when business planning is focused on quarterly returns. This point is raised in the HEV/EV supplier community, noting the contrast with the long-term– though reportedly loss-leading–large-scale, long-term investment strategy pursued by Toyota in HEVs.
  - USG picking winners and losers: this comment reflects frustration with outcomes when USG investments are understood to be "helping only certain companies succeed." This view comes from sources that are supportive of USG involvement when it is focused and understood to investing in broad technology approaches, integration or development of standards, or pre-competitive technology development activities, regardless of the companies that participate.
  - Lack of availability of key components produced in NA, as the automotive PE industry is a global one dominated by overseas suppliers at present.
- The lack of engineers and skilled workers is the sixth-most frequently mentioned disadvantage. This suggests that the pragmatic economic forces discussed above, whether market-, industry- or government-based, are the critical constraints to expanding the NA PE supply chain and that lack of qualified personnel is not a critical factor at this time.
- The remaining disadvantages were mentioned by single respondents, and therefore do not achieve sufficient weight for discussion as broad consensus findings.

Figure II-123 below depicts the responses collected from 21 of the 43 interviewees who provided their specific views on the role that NA-based suppliers play in automotive PE supply chain activities.
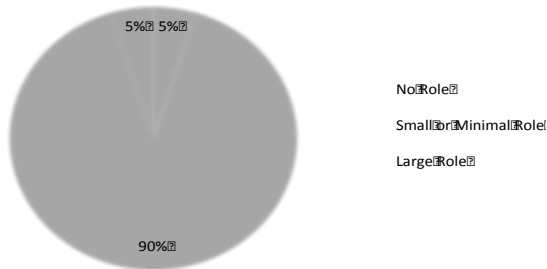
Figure II-123. Responses to: "How Large a Role do NA PE Suppliers Play?"

Consistent with global power inverter supplier rankings presented by Synthesis in this and other studies, NA suppliers make a relatively small contribution at present. The automotive PE supply chain is a global one, with NA suppliers playing a small or minimal role at the present time.

Figure II-124 below depicts the responses collected from 24 of 43 interviewees who provided specific views on whether or not NA PE suppliers are planning to expand production in the next five years.
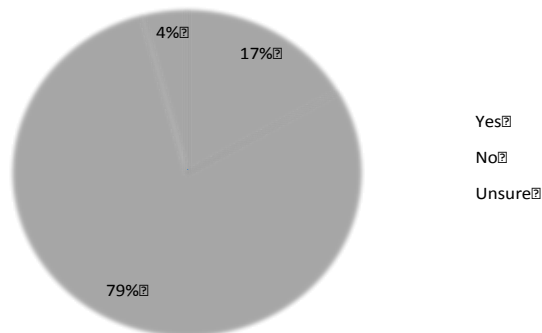
Figure II-124. Responses to: "Are NA PE Suppliers Preparing to Expand Production in the Next Five Years?"

A strong majority of the respondents believed that NA PE suppliers are not planning on preparing to expand production in the next five years.

This consensus view appears to indicate that those organizations now anticipating or planning on a diverse set of NA-based companies expanding or entering the PE supply chain may be disappointed.

The 17% of the respondents stating that suppliers are preparing to expand production, are with, or know of, the companies that are actually making investments. Secondary sources corroborate their information. This is notable because individuals are discussing highly capable, globally managed and committed companies focused on building a supply chain in pursuit of the most important advantages of a NA supply chain identified above. Despite the fact that they are a minority they can have significant impacts on future outcomes in automotive traction drive PE supply.

Alternative scenarios and singular issues that could be potentially leveraged to achieve a significant expansion in NA power inverter manufacturing volume.

Note that this section does not address demand-side activities such as private and public actions designed to increase the market demand for EVs, HEVs and plug-in EV/HEVs through rebates and other incentives, as they are outside the scope of this study.

Primary and secondary research indicates that a significant expansion in the NA power inverter manufacturing volume is extremely unlikely in the foreseeable future due to:

- Current insufficient market demand to lead to shift a significant portion of the global supply chain to NA
- Globally competitive suppliers can satisfy current and expected demand for high quality products
- Profit margins in traction drive PE applications are low relative to PE applications in other markets (e.g., oil and gas, industrial motors, wind, solar)
- Industries other than automotive offer larger volumes for power inverter manufacturers
- The higher cost structure of the NA operating environment, including labor and regulatory costs

These factors all contribute to capital and talent flowing to non-automotive PE markets.

Synthesis therefore assesses that identifying paths to a *significant expansion* of NA power inverter manufacturing volume at this time is not a credible exercise. Instead, Synthesis has sought to identify scenarios and singular issues that may be leveraged in order to achieve *a limited expansion*.

Synthesis has previously identified the three critical dimensions (Synthesis' 2012 "Power Electronics Technology Roadmap Analysis Report") that directly affect the evolution of the PE supply chain, as they are key cost drivers:

- Manufacturing Volume
- Investment (Private and Public)
- Supply Chain Integration

These three dimensions are depicted in Figure II-125 below.
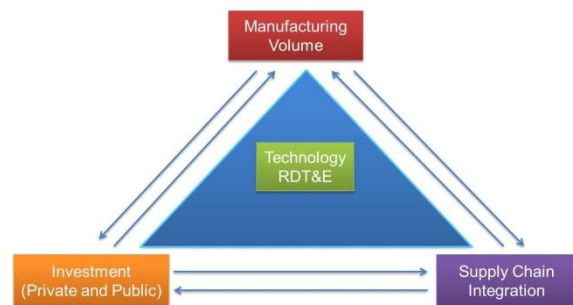
Figure II-125. Critical Dimensions of PE Cost Reduction. © Synthesis Partners, LLC.

The figure depicts the role of DOE's technology Research, Development, Test and Evaluation (RDT&E) activities, which occur in the context of the levels of EV/HEV manufacturing volume, investments, and supply chain integration. As Synthesis found in the 2012 and 2011 reports, NA PE suppliers report that volume, investment, and supply chain

integration are the key drivers of any cost reduction activity. Cost reduction, especially in an industry with low profit margins, is the critical path to expanding market share and supply chain volume in a globally competitive market.

Scenarios

Three distinct scenarios were produced by Synthesis to illustrate pathways to a limited expansion in NA power inverter manufacturing volume. Figure II-125 indicates that scenarios to address increasing volume should include the investment or supply chain integration factors, or both. Synthesis assesses that this approach could enable a transition from the present brittle NA supply chain to a potential future globally competitive NA supply chain.

Further analysis of each scenario could be useful assess their relative plausibility, including viewpoints and counterpoints from key sources. In addition, further analysis could help determine the extent of expansion in NA power inverter manufacturing that these scenarios (or other scenarios) might support.

Following the scenarios is a discussion of singular issues that could potentially be leveraged to achieve a limited expansion in NA power inverter manufacturing volume.

Scenario #1: Increase NA Volume by Increasing Supply Chain Integration

Supply chain integration involves a rationalization of the number of PE architectures, designs, and other aspects to increase supply chain efficiencies. In this case, two OEMs could combine efforts to create common, pre-competitive specifications for classes of traction drive inverters.

This scenario is built on the assumption that OEMs are seeking to realize logistics, flexibility and value-engineering benefits (i.e., the ability of the OEM to be more responsive to market demands through in-house engineering changes at lower costs) and can do so through increased PE product rationalization.

This arrangement would enable suppliers to focus on a smaller number of power inverter requirements, allowing RDT&E and manufacturing resources to be dedicated to fewer designs and products, thus increasing economies of scale and lowering unit costs. Synthesis assesses that the advantages of a NA supply chain could lead some OEMs to require that some of their suppliers locate in NA

A rationalized supply chain could contribute to more effective supply chain management of important factors such as quality, cost, and schedule. OEMs are increasingly requiring robust supply chain management from their Tier 1-4 suppliers.

It is reasonable to expect that additional OEMs would seek to access the NA inverter manufacturing efficiencies realized.

Further, participation by non-automotive manufacturers, (e.g., industrial motors manufacturers, which address a much larger and more profitable market) in specification-setting could lead to a significant expansion of market volumes for PE designs that incorporate specifications for both markets.

Expanding NA supply chain volumes could initiate a virtuous cycle, in which company investments in NA technology, labor, and equipment could generate more NA business.

This scenario has not occurred because the OEMs and Tier 1s consider traction driver inverter design as proprietary information, thus limiting information sharing. Further, at present, no impartial organizations have aggregated information, identified and addressed gaps, and developed roadmaps to achieve common specifications. This would require leadership and funding.

Synthesis considers this scenario as the most likely to occur of the three discussed here. However, achieving this scenario would be difficult.

Scenario #2: Increase NA Volume by Increased Investment, Via a NA-OEM-In-House Inverter Development

In this case, a NA OEM could implement a strategy to develop traction drive inverters in-house to leverage the competitive benefits of in-sourcing production, including speed-of-delivery, flexible engineering in response to real-world inverter RDT&E experience, IP protection, and cost reduction.

This scenario acknowledges the potential key competitive advantages that could accrue to an OEM should it pursue a Toyota-like strategy of performing inverter design and engineering in-house. In order to implement such a strategy, significant investments would be required of the NA OEM. The viability of this strategy relies on the projected ROI.

If the expected ROI is sufficient, NA power inverter manufacturing volume would increase as the OEM in-sources manufacturing previously performed largely overseas. However, this would not increase overall market size, but would simply re-distribute existing manufacturing.

This scenario has not come to pass because insufficient information exists to inform a credible determination of ROI. Further, in-sourcing development, design, and production of major components would be a major cultural shift in business strategy. Only Toyota has implemented this business model on a large scale, and information about its successes, failures, and lessons learned is scant.

Synthesis assess that the likelihood of a NA OEM pursuing this strategy is low.

Scenario #3: Increase NA Volume by Increased Investment and Supply Chain Integration through Multiple OEM Collaboration

In this case, two NA OEMs would in-source the design and production of power inverters. These two OEMs also would collaborate to establish common integrated requirements for traction drive inverter components.

In addition to the benefits outlined in scenarios 1 and 2, this scenario would result in more comprehensive understanding of technology gaps and the required investments and engineering skills.

This scenario has the benefit of focusing greater investment on NA supply chain activities, drives supply chain integration through common OEM requirements and thus

potentially increases NA power inverter manufacturing volume.

Just as scenarios 1 and 2 could have a limited affect on NA supply chain volume, the integration of the two, at a larger scale (2+ OEMs), could be expected to have a commensurately larger impact.

This scenario is judged to be very unlikely, as it incorporates the risks of the first two and further requires unprecedented collaboration among the OEMs.

Singular Issues That Can Potentially Be Leveraged To Achieve A Limited Expansion in NA Power Inverter Manufacturing Volume

Transitioning from the current vicious cycle of low volume high per unit cost to a virtuous cycle of increasing volume and decreasing per unit costs requires new approaches and strategies. New strategies can be informed by identifying singular issues for realizing realistic paths to limited expansion in NA power inverter manufacturing.

The following strategy elements are foci of global PE manufacturing leaders, as determined via the case study research. Each of the following strategy elements point to the issues that can potentially be leveraged to achieve a limited expansion in NA power inverter manufacturing volume:

- Tier 1 organizational leadership focused over the long term on delivering top-ranked quality and increasing revenue year-on-year in the global context. This focus on revenue can come at the expense of profits in the near- and mid-terms.
- Capability and intent to invest hundreds of millions of dollars over decades to build and sustain global leadership in PE.
- Capability and intent to envision, build, and sustain competitive facilities in response to market demand to produce high-volume automotive parts (including PE) accordingly.
- Long-term, sustaining relationships with OEMs–not simply for PE–but for a portfolio of complex automotive parts–to sustain long-term Tier 1 supplier relationships.
- Decades of effective execution of the above points, in conjunction with a balanced portfolio of other automotive parts or components.

Synthesis assesses that there is are a number of opportunities for DOE to affect these and other factors by:

1. Leveraging the above strategic success factors to enable a NA PE supply chain expansion by engaging the NA-based transplant OEMs and Tier 1 companies. Table II-11 provides a summary of their desired engagement points.

2. Identifying specific measures to address the brittleness of the NA automotive PE supply chain. Specifically, targeted capability improvements, technology investments, or other activities could mitigate the risks posed by disruptions to material or component suppliers (Tier 4 and below) to the NA PE supply chain.

3. Providing technology development leadership and/or manufacturing capacity assistance efforts could expand the field of Tier 4 suppliers.

4. Assisting with engagement and collaboration among supply chain companies. Interview sources and secondary research have indicated that targeted efforts to improve communication and collaboration could be helpful in enabling growth by fostering an improved understanding of technology gaps and required investments and engineering skills. This could result in a more diverse, capable, and efficient market.

The table below illustrates the willingness of supply chain companies to participate in increased collaboration.

By way of introduction to the singular issues involved, Synthesis reviewed the content of the full-text interviews to produce the following list of paraphrased statements regarding the type of information exchange that specific NA PE supply chain participants are seeking. Each company listed below represents a unique company.

Table II-11: Synthesis' Assessment Regarding Needs Expressed, by Company.

Company Type	Synthesis Assessment Regarding Needs Expressed
OEM	Assistance in identifying communities who truly want transplant investment; Assistance in identifying incentives, funding, grants, resources, infrastructure appropriate to target manufacturing activities.
Tier 1	Assistance in recruiting engineering talent
Tier 1	Assistance in identifying potential U.S. suppliers
Tier 3	Assistance in obtaining expanded R&D funding for SiC, WBG
Tier 1	Assistance in obtaining WBG R&D funding
Tier 1	Assistance in targeting investments in R&D and manufacturing; Assistance in developing strategy in response to Toyota, Nissan and other OEM's strategy to "look beyond Denso"; Assistance in obtaining expanded R&D funding for Si, capacitors and inductors.
Tier 2	Assistance in expanding manufacturing in U.S.
OEM	Incentives for semiconductor manufacturing in U.S.
OEM	Assistance in identifying common ground for the common good in OEM-supplier relationships; Additional cost analyses for major EV components along lines of what SP did with inverters.
OEM	Assistance in identifying and tracking investment capital, loans, grants and incentives.
Tier 2	Assistance in promoting collaboration between OEMs and suppliers to work together to identify areas of commonality, such as: Assistance with standardized inverter with at least some common automotive and industrial applications; Identify component standardization candidates along lines of Tesla's reported use of discrete IGBTs as standardized component.

Company Type	Synthesis Assessment Regarding Needs Expressed
Tier 1	Assistance in identifying technology acquisition/transfer opportunities from public and private sector—"We are willing to pay very well for technology once the research has been completed and this allows us to focus on what we do best."
Tier 1	Assistance in identifying next steps towards standardization; Assistance in establishing pool of trained engineers
OEM	Assistance in identifying U.S. suppliers with competitive TDC (total delivery cost), performance, quality and reliability to help meet corporate goal of 85% local manufacturing in U.S.; Assistance in generating approaches to cost reduction while maintaining quality through system integration, standards/optimization for high voltage circuits, thermal management for power modules, and development of power modules.
Tier 1	Assistance in identifying competitive suppliers offering cost and quality advantages; Expanded funding of Si
Tier 2	Expanded funding of enabling technologies similar to past funding of motors and high-temp capacitors; Expanded engineering talent pool; Assistance/encouragement/direction in identifying what needs to be done to attract, keep and expand transplant "incumbents".
Tier 2	Assistance in identifying OEM customers

Conclusions/Recommendations

- Develop a USG-industry collaborative approach to systematically collect, store, and provide access to accurate and timely information on companies, products, technology developments and the essential people that make up the NA automotive PE traction drive supply chain.
    - Synthesis discovered significant interest among sources in participating in technical discussions regarding the future of the NA automotive PE supply chain.
- Assess where geographically-concentrated automotive PE activities may be leveraged to achieve expansions in volume of manufacturing.
    - As lower tier companies tend to locate in the general vicinity of the upper tier customers, investments should take location of the intended recipient into account.

- Devise a strategy to engage the Tier 1 and other companies queried during this research to enhance the NA PE supply chain diversity and capability. The responsiveness and responses of the Tier 1s queried indicates that these companies are committed to building the NA PE supply chain.
- Develop roadmaps to show how R&D investments that contribute to NA PE production capacity will address globally competitive cost benchmarks by contributing to specific cost and volume of production milestones. Cost and volume targets are different sides of the same coin and are both needed to achieve success in the long run.
- Identify non-profit, federal and state-level partners to assist NA suppliers to aggressively work to maintain existing relationships and forge new relationships with globally competitive suppliers in automotive PE, even as they pursue opportunities in industries beyond automotive PE.
- Conduct analysis to better characterize the level of market demand that could sustain a specific size of expanded NA automotive PE supply base.
- Conduct analysis to produce quantitative rankings of R&D investment projects based on the expected increase in vehicle fuel efficiency (e.g., in terms of mpg gain per dollar invested) they can deliver for standardized systems. Use this analysis to clarify how R&D investment dollars are optimized toward fuel-use reduction strategies that are most likely to succeed in the marketplace.
- Conduct research to better understand the affect of OEMs' in-sourced vs. out-sourced PE production strategies, including affects on rates of cost reduction, innovation, level of IP generation and other factors of interest to growing the NA PE supply chain.

Leverage the keen interest shown among sources contacted in this round to encourage targeted discussion regarding technical topics of interest to DOE's Vehicle Technologies Office (VTO).

Note: This is a condensed version of the full report, Synthesis Partners' *Assessing the North American Supply Chain for Automotive Traction Drive Power Electronics*. If you would like the full version, please contact Steven Boyd or Susan Rodgers.

III.0 Power Electronics R&D

III.1. Silicon to WBG Inverter Packaging

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Start Date: October 2012
Projected End Date: September 2015

Objectives

- Develop advanced PE packaging technologies for comprehensive improvement in the cost-effectiveness, efficiency, reliability, and power density of automotive electric drive systems.
  - In FY 2013, develop novel packaging technologies for SiC power modules, enabling exploitation of the superior attributes of WBG materials.

Technical Barriers

State-of-the-art automotive power modules and power inverters and converters have disadvantages in electrical performance, cooling capability, thermomechanical performance, and manufacturability. These are barriers to meeting the DOE APEEM 2020 targets for cost, efficiency, and density.

Technical Targets

- Develop all-SiC power modules to replace their Si counterparts in automotive PE systems for high-power-density, high-frequency, and high-temperature operation.
- Advance packaging and manufacturing technologies for SiC power modules with lower thermal resistance, small electric parasitics, and high-temperature reliability that can be manufactured efficiently.

Accomplishments

- Developed advanced power module packaging technologies, based on a directly integrated cold-base plate concept, that feature a 33% reduction in specific thermal resistivity compared with conventional technologies.
- Fabricated a group of phase-leg power modules (50–100 A/1,200 V) with different combinations of power device (Si, SiC) and thermal packages.
- Performed comprehensive characterization and comparative system evaluation. Combining the attributes of the latest SiC power devices and advanced packaging enables an all-SiC power module with a $3\times$ increase in current density and a 50% reduction in power losses compared with an all-Si module.

✧   ✧   ✧   ✧   ✧

Introduction

There has been significant progress over the past decade in developing PE packaging technologies for Si devices/modules for electric drive systems in automotive applications. The focus has been on improving the systems' electrical performance, thermal management, thermomechanical reliability, and manufacturability. Advancements in power module packaging can be briefly categorized into three generations, depending on the materials and processes employed. As a baseline, first-generation packaging features solder die attachment, wire bond interconnection, and interfacial assembly. The second-generation package employs one of the following techniques: a planar bond, integrated cooling, or more reliable bonding materials. The third generation involves further integration of dual planar bond and double-sided cooling concepts, and so on. These technologies have greatly advanced the metrics for cost, reliability, functionality, power density, and efficiency of automotive PE systems. For further advancement, it is generally accepted that WBG semiconductor power devices—such as SiC and GaN MOSFETs—offer superior properties compared with their Si counterparts such as IGBTs, the power semiconductor switches mainly used in PE systems in medium- and high-power applications. A promising development in past decades is that WBG power devices, especially SiC MOSFETs and JBS diodes, have started to penetrate Si application regimes. Following the successful supply of discrete power devices, a group of all-SiC power modules have recently been developed by manufacturers such as CREE, Rohm, Infineon, and Fuji. They typically have a single-phase-leg topology, made up of SiC MOSFETs and SiC JBS diodes, and are rated at 100 A, 1,200 V.

These module packages typically employ the first-generation structure and conventional manufacturing processes. They are assembled into inverter/converter systems in which a thermal interface grease must be used between cold plate and module packages. The attributes of SiC devices, such as high-power-density, high-frequency and high-temperature operation, have not been fully explored yet.

This project emphasizes the integration of an advanced direct liquid cooling concept into all-SiC power module packaging, enabling exploitation of SiC performance. Technical details such as packaging structure and associated packaging process technology were developed. Performance improvements were characterized by experimental measurements; and efficiency, cost, and reliability benefits to a PE system were evaluated.

Approach

Figure III-1 (a) is a schematic of a one-phase-leg all-SiC power module, which is a basic building block for various automotive power converters/inverters. It is made up of two units (upper and lower) of SiC MOSFETs and SiC diodes. Power MOSFETs and diodes are commercially available in the form of bare dies, both rated at 50 A/1,200 V. The current rating of the power module can be increased by paralleling multiple dies. Figure III-1 (b) shows a layout of the die placement and interconnection pattern for a 100 A/1,200 V phase-leg power module. The power switch unit consists of two SiC MOSFETs and two SiC diode dies in parallel. The electrical interconnection is achieved by bonding AL wires to the tops of the dies and soldering the dies on Cu traces of a DBC substrate; electrical insulation is provided by the Al oxide (Al_2O_3) ceramic slice inside. The parasitic electric resistances of the current flow paths cause ohmic power loss and affect the efficiency and junction temperatures of power switches. The packaging interconnection parasitic inductances will cause voltage overshoot on SiC switches, limiting their switching speed and increasing their switching losses. The layout of multiple SiC dies on a DBC substrate, and their interconnections, has been optimized to reduce these parasitic electrical parameters using electromagnetic simulation tools.

In the first-generation packaging structure of the SiC modules shown in Figure III-2(a), the power stage—including SiC dies, interconnections, and substrate—is directly bonded onto a Cu base plate by solder and then encapsulated. All the power and signal I/O terminals/pins are located on the top surfaces of the modules. For thermal management, the module must be mounted mechanically onto a cold plate, which provides coolant flow paths and keeps the SiC die temperature below a safety threshold. In this assembly, a necessary thermal interface material, such as a thermal grease, severely degrades the cooling efficiency. This study proposes a new cooling structure. As schematically illustrated in Figure III-2(b), the SiC power stage is directly soldered to a cold-base plate. This specialized part replaces the base plate, thermal grease, and cold plate in the conventional packaging structure (Figure III-2(a)). The integration not only improves the cooling efficiency but also reduces the volume and weight

of the SiC power module assembly, as well as the manufacturing steps.

(a)

(b)
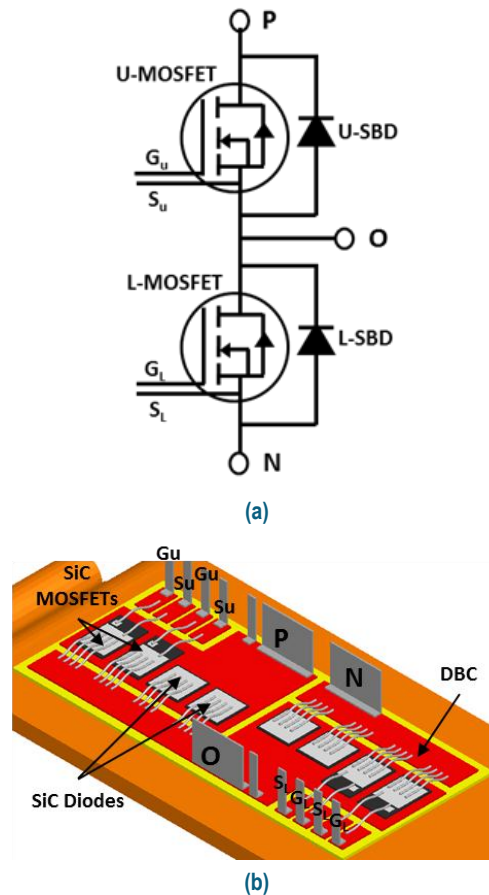
Figure III-1: Electrical design of an all-SiC module: (a) electrical diagram (U-upper unit, L=lower unit) and (b) multiple SiC die layout and interconnection configuration.

(a)

(b)
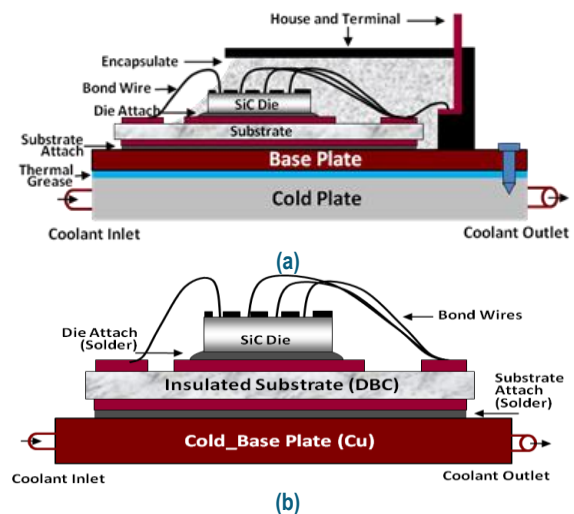
Figure III-2: Schematics of SiC power module packaging structures and materials: (a) conventional interfacial thermal assembly and (b) direct cooling by integrated cold-base plate package.

Figure III-3 (a) shows a photo of a cold-base plate like the one employed in this study. It measures 105 mm (L) by 58 mm (W), including coolant inlet and outlet. Its main body is made of a flat Cu tube with an outline thickness of 3 mm. The effective cooling surface measures 60 mm (L) by 30 mm (W). It contains internal fins to increase cooling efficiency, and they offer excellent thermal uniformity as coolant flows below the entire surface. The x-ray image shown in Figure III-3 (b) exposes the unique internal crisscross fin structure for control of coolant flow. The Cu offers excellent solderability that makes it possible for the power stage (on the DBC) to be directly bonded by solder.

(a)
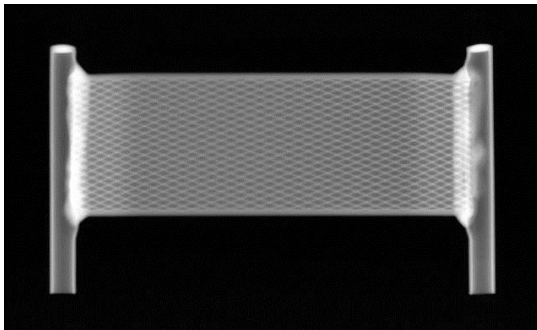
(b)
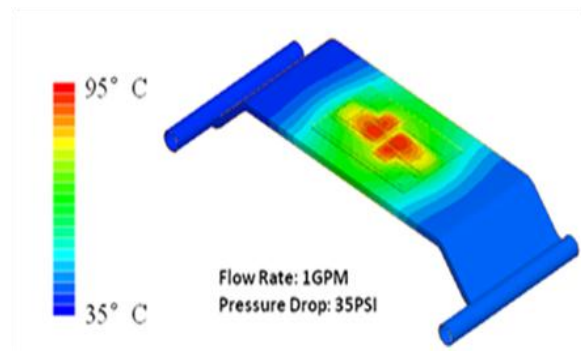
(c)

Figure III-3: Cold-base plate and thermal performance: (a) photo of the integrated cold-base plate; (b) x-ray image of the plate; and (c) temperature distribution of the power module on the integrated cold-base plate.

The thermal performance of this package was investigated via a computational fluid dynamics (CFD) simulation using the computational tool COMSOL. Figure III-3(c) shows the calculated temperature distribution of the whole module under these conditions: each die has a power loss of 12.5 W; inlet coolant temperature is 25°C, flow rate is 1 gpm (308 lpm), and pressure drop is 35 PSI (241 kPa). The effective thermal resistance of an SiC die related to the whole module assembly, including power stage and cold plate, is 0.7K/W, significantly smaller than the resistance in a conventional module assembly with typical thermal grease and a standard Al cold plate.

To manufacture complete power module prototypes, a set of package parts was designed and fabricated using in-house packaging capabilities. They include die attachment solder and the top interconnection wire bond, DBC power substrate, power and signal terminals, baseplate, encapsulate, and so on.

For comparison purposes, the conventional interfacial cooling structures also were manufactured. The conventional cold plate is a solid Cu plate with thermal conductivity [k=400 W/ (mK)] and mechanical strength. Its dimensions are 75 mm (L) × 32 mm (W) × 3 mm (H).

To examine the advantages of this SiC power module applied in an electric drive system, an Si IGBT/ PiN diode phase-leg power module with the same current/voltage rating (50 A/1,200 V) was fabricated. The packaging components in the Si modules are identical to those in the SiC modules except for the power semiconductor dies.

Results

Several SiC and Si power modules were packaged, including samples for special thermal electrical tests. Figure III-4 presents two examples: an all-SiC 100 A/1,200 V phase-leg module with integrated cold-base plate (a) and an all-Si 50 A/1,200 V module with conventional base plate (b).

(a)

(b)
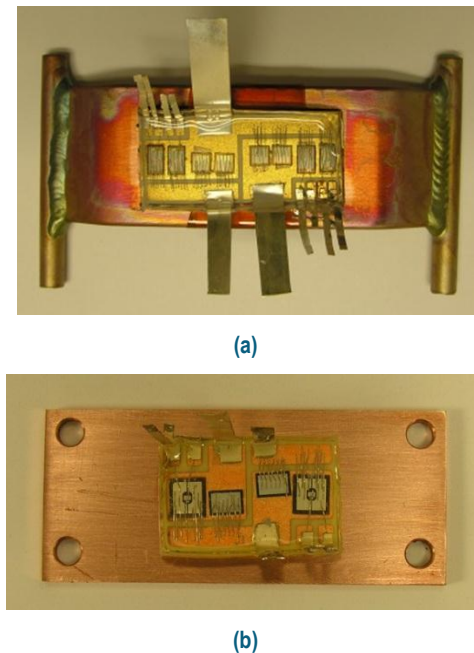
Figure III-4: Photos of representative power modules: (a) all-SiC 100 A/1,200 V module with integrated cold-base plate and (b) all-Si 50 A/1,200 V module with conventional base plate.

The electrical parameters of the modules were characterized using various experimental methods. The static I-V curves were measured at different junction temperatures. Figure III-5 shows the test results for a 50 A/1,200 V SiC MOSFET in the module. Through these tests, the conduction losses of semiconductor devices and packaging parasitic electric resistances were also obtained.
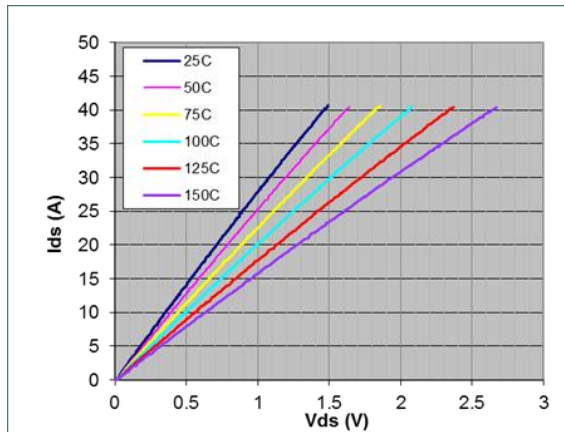
Figure III-5: Static I-V characteristics of 50 A/1,200 V SiC MOSFET.

Figure III-6 shows the typical electrical waveforms of an SiC MOSFET during turn-off transition at a bus voltage of 600 V and current of around 50 A. The fastest switching speed (less than 100 nS) of SiC devices was experimentally identified with a specially designed in-house gate drive circuitry. The package parasitic inductances were measured by switching power devices in a specific testing circuit.
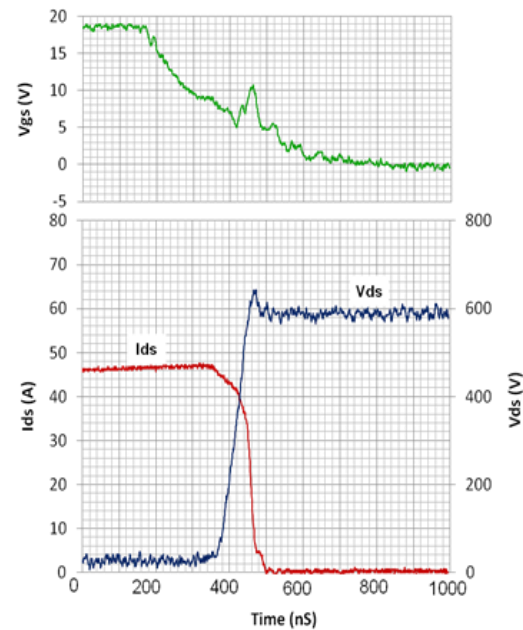
Figure III-6: Switching waveforms of 50 A, 1,200 V SiC MOSFET during turn-off transition.

The switching power losses, including turn-on and turn-off parts, can be calculated from this test at different voltages and currents, temperatures, and so on. Figure III-7 presents the switching power loss of the SiC MOSFET versus current under different operating temperatures (up to 175°C).
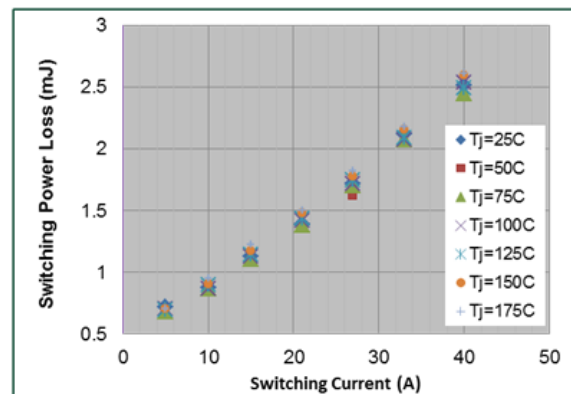
Figure III-7: Switching power loss of 50 A/1,200 V SiC MOSFET vs. current at a different temperature (up to 175°C).

The thermal parameters of the module package were characterized with an established thermal test setup in which the body diode of a SiC MOSFET was used to self-heat. Its forward voltage drop was also used as the temperature sense parameter to measure the junction temperature. The calibration curve of this body diode voltage, Vf, versus temperature at Ifc =1 mA was firstly acquired. The Vf changes linearly with temperature with a temperature coefficient of −2.45 mV/°C. When a larger current Ifp and voltage Vfp are applied to the body diode of the SiC MOSFET for 10 min, the device temperature is increased to a certain level. The corresponding input power equals the product of Ifp and Vfp. Then the input power is quickly turned off, and the current

going through the diode is switched to *Ifc*. A *Vf* variation curve over time can be recorded. After the conversion of *Vf* to the device junction temperature based on the calibration data, a cooling temperature curve (over time) can be obtained. With input electrical power and temperature change, the thermal impedance of the module package can be calculated.

Figure III-8 summarizes the thermal resistance data for both conventional and integrated cooling module assemblies. The specific thermal resistivity is used as an indicator of the thermal performance of the module assembly, which includes the thermal resistivity of all packaging components and the cold plate. The specific thermal resistivity is a normalized thermal resistance to its die area, which represents the thermal performance of a package. It can be seen that the specific thermal resistivity of the integrated cooling packaging is more than 33% lower than that of a conventional package.
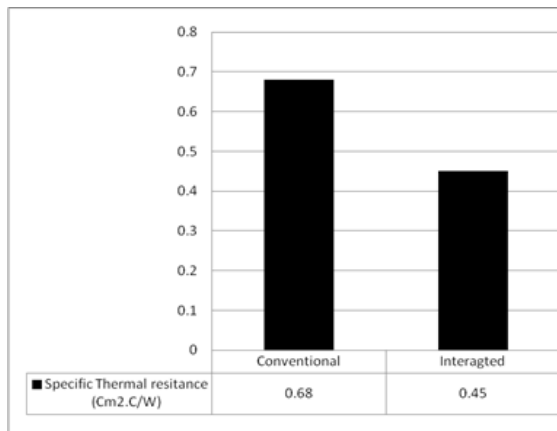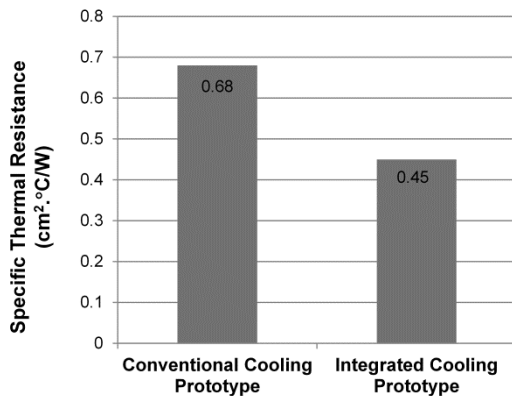
Figure III-8: Comparison of specific thermal resistivity between conventional module assembly and integrated cooling packaging.

In a comparative study, the electrical and thermal performance of Si power modules was also characterized, using the same methodology used for the SiC modules, and the performance of the modules was compared one to one.

Figure III-9 (a) presents a comparison of static I-V characteristics of an IGBT in the Si module and a MOSFET in the SiC module. Their switching losses (sum of turn-on and turn-off parts) are shown in Figure III-9(b). It can be clearly

seen that the SiC MOSFET exhibits less conduction power loss and less switching power loss than the Si IGBT.

As power devices operate in an inverter or converter, the total conduction loss depends on the current, voltage drop, and duty cycle (*D*); the switching loss is related to current magnitude (*Id*), blocking voltage, switching speed, and switching frequency (*f*). As discussed earlier, the electrical power losses in power devices will generate self-heating and cause the device temperature to rise. For thermal management, the power density or heat flux in the die is more directly related to the cooling efficiency, because the thermal dissipation capability depends greatly on the die area (size).

(a)

(b)
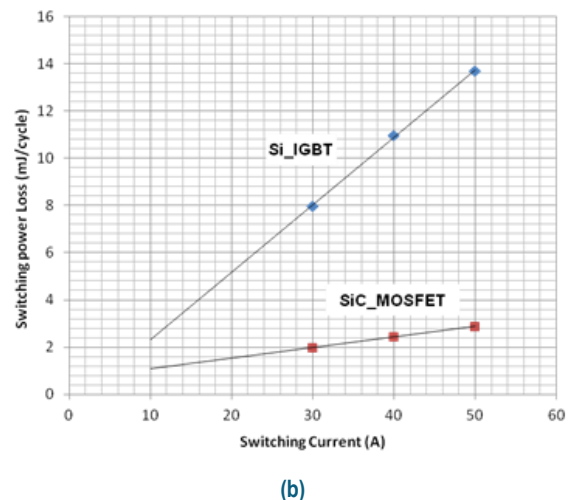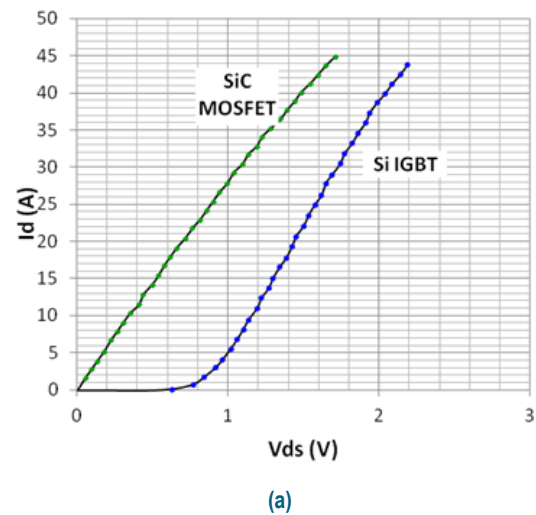
Figure III-9: Comparison between 50 A, 1,200 V SiC MOSFET and Si IGBT switch (at room temperature): (a) static I-V characteristics and (b) switching loss vs. current (at bus voltage of 600 V).

By combining the specific thermal resistivity with different cooling configurations, the temperature rise of a power device can be calculated. Figure III-10 shows the junction temperature increase from the ambient level (here, the inlet temperature of the coolant) versus current for four different device/package combinations. They are an Si IGBT in a

conventional cooling configuration, an Si IGBT on an integrated cold-base plate, an SiC MOSFET on a conventional cold plate, and an SiC MOSFET in an integrated cooling package. The cooling configuration is shown to greatly affect the junction temperatures of power devices. With a fixed current, for example 30 A, the increase in the junction temperature ranges from ~50 to 90°C between the best and the worst combinations. Device temperature is directly related to module reliability and lifetime: higher temperatures lead to a significant reduction of the power module lifetime.
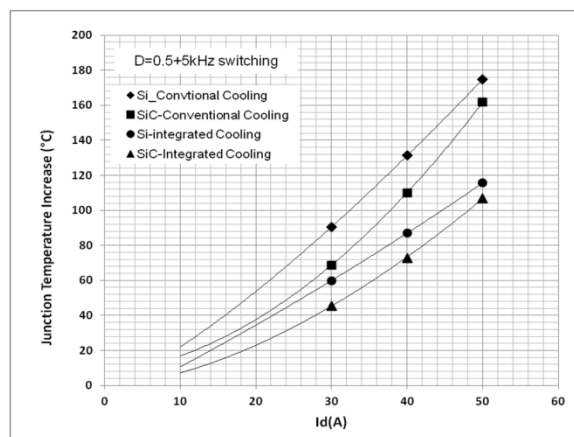
Figure III-10: Comparison of device junction temperature increase vs. current between different power semiconductor and cooling combinations for a typical operation: D=0.5, f=5 kHz.

On the other hand, if the maximum operational boundary is set based on the package reliability and the semiconductor temperature limits, the maximum handling current density of a power switch can be determined accordingly. For instance, as shown in Table III-1, the allowed current density of a power device for four combinations increases from 66 A/cm^2 to 185 A/cm^2 for a 100°C temperature increase, which can be a case for a coolant temperature of 25°C and a junction temperature of 125°C. These maximum current density values define the minimum die size of the power semiconductors for a designed system current (or power) level. It is well known that die size is a dominant factor in power module cost. The 3× die size reduction from the worst combination to the best one is significant for reducing the PE system cost. Furthermore, the data demonstrate that the power semiconductor device type plays an important role in these improvements. For example, the die size can be reduced 1.9 to 2.2 times as a result of changing from an Si IGBT to an SiC MOSFET because of the lower power loss density of the latter. The die size can be reduced 1.3 to 1.5 times by using an integrated cooling package instead of a conventional packaging cooling configuration.

Table III-1: Current density allowed for different power semiconductor and cooling combinations at ΔTj=100°C for a typical opertion (D=0.5, f=5kHz).

Item	Si_ conventional cooling	SiC_ conventional cooling	Si_ integrated cooling	SiC_ integrated cooling
Current density J$_d$ (A/cm^2)	65.35	144.97	97.57	184.98

The analysis and data discussed are closely related to a defined operation condition (here, D=0.5, f=5 kHz). The contributions of the packaging technology and the power semiconductor technology to the improvements in power module efficiency, cost, and reliability can be further analyzed using these performance parameters for any specific application cases.

Conclusions and Future Directions

All-SiC phase-leg power modules fabricated in-house at the ORNL Packaging Laboratory feature the adoption of the latest industrial SiC power devices—MOSFETs and JBS diodes—and second-generation packaging with integrated direct cooling structure. Combining the attributes of SiC and advanced packaging, these modules offer superior performance over Si counterparts.

The module's performance improvements, leading to high-efficiency, high-density system operation beyond the limits of Si, resulted in improvements in system cost, efficiency, and reliability.

Further advancement of WBG automotive PE depends greatly on improvement of power packaging technology through advances in structure, materials, and processing techniques to fully exploit the attributes of WBG power devices: high power density, high frequency, and high-temperature operation. Future development of advanced WBG power modules will include the following:

- Integrate direct double-sided cooling.
- Realize low-parasitic electrical parameters.
- Enable a high-temperature, highly reliable package.
- Provide highly intelligent functionality.
- Allow extensive integration of the converter/inverter system.

These advancements will enable considerable strides in achieving DOE power density and cost targets for PE systems in electric drive vehicles.

FY 2013 Publications/Presentations

Publications

1. Z. Liang, P. Ning, F. Wang, "Development of advanced all-SiC power module packaging," *IEEE Transactions on Power Electronics*, special issue on WBG devices, 2013 (in press).

2. Z. Liang, P. Ning, F. Wang, "Advanced packaging of SiC power module for automotive applications," *Proceedings of the Fifth IEEE Energy Conversion Congress and Exposition*, Denver, September 15–19, 2013.

3. Z. Xu, M. Li, F. Wang, Z. Liang, "Investigation of Si IGBT operation at 200°C for traction applications," *IEEE Transactions on Power Electronics* **28**(5), 2604–2615, May 2013.

4. P. Ning, Z. Liang, F. Wang, L. Marlino "Double-sided cooling design for novel planar module," *Proceedings of the IEEE Applied Power Electronics and Exposition*, Long Beach, Calif., March 17–21, 2013.

Presentations

1. Z. Liang, "Development of automotive power module packaging," SAE Electronic Systems for Vehicle Propulsion/Intelligent Vehicle Systems Symposium, Troy, Mich., September 18, 2013.

2. Z. Liang, P. Ning, F. Wang, "Advanced packaging of SiC power module for automotive applications," IEEE Energy Conversion Congress and Exposition 2013, Denver, September 18, 2013.

3. Z. Liang, "WBG power device packaging," DOE Annual Merit Review, Washington, DC, May 14, 2013.

4. Z. Liang, "Cross-industry reliability: Automotive power module perspective," 2013 PV System Symposium, Santa Clara, Calif., April 30, 2013.

5. P. Ning, Z. Liang, F. Wang, and L. Marlino "Double-sided cooling design for novel planar module," IEEE Applied Power Electronics Conference 2013, Long Beach, Calif., March 17–21, 2013.

FY 2013 Patents

Z. Liang, L. Marlino, P. Ning, F. Wang, "Power Module Packaging with Double Sided Planar Interconnection and Heat Exchangers," U.S. Patent application publication, U.S. 2013/0020694 A1, January 24, 2013.

III.2. WBG Gate Driver and Smart Power Module

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Start Date: October 2012
Projected End Date: September 2015

Objectives

- Develop a highly integrated power module phase leg (rated at 1,200 V and 200 A), incorporating WBG devices, that includes (1) an integrated gate drive, (2) an isolation chip, and (3) a power supply, in a package that allows it to work at high temperatures (up to 150°C ambient) and device junction temperatures of up to 200°C.
- Build a smart gate drive with protection features, high current capability, and active gate control to minimize switching loss and chance of noise-induced gate turn-on that can lead to shoot-through.
- As a final goal, produce 55 kW inverter phase-leg modules that can work at high temperatures and meet 2020 targets of 14 kW/l and 14 kW/kg, and 2015 targets of $5/kW, and 98 % efficiency.

Technical Barriers

PE modules lack the integration necessary to achieve future DOE 2020 VTO cost targets. PE converter components are discrete, bulky, and temperature-limited. Gate drives and packaging for new WBG devices are limited in their ability.

Technical Targets

- Construct an integrated gate-drive solution that can operate at the ambient temperatures seen in an engine compartment.
- Design and fabricate on-chip input isolation prototypes. Determine functionality, blocking voltage, and transient immunity of chip prototypes.
- Develop an isolated power supply on chip (PwrSoC) to power the module.

- Explore a fast, reliable, low-loss, cost-effective overcurrent protection scheme for SiC MOSFETs.
- Develop an active current balancing (ACB) scheme to eliminate the current unbalance of parallel-connected SiC MOSFETs.
- Eliminate cross talk for WBG power devices in a phase-leg configuration, leading to lower switching losses, fast switching speed, and high reliability.
- Integrate a high-temperature gate driver integrated circuit (IC) into an SiC-based phase-leg power module for functionality verification.

Accomplishments

- Developed and experimentally verified a highly integrated gate drive that operates successfully at 200°C.
- Fabricated and verified the functionality of an isolation chip. Demonstrated an input PWM signal frequency of 5 MHz.
- Designed and verified a common mode rejection test printed circuit board (PCB). The design allows for testing in excess of 30 kV/μs.
- Completed the layout of the isolation chip.
- Fabricated a power supply in package, consisting of a boost converter and on-chip inductor for characterization.
- Designed an isolated PwrSoC schematic. Preliminary simulation results are encouraging. A plan for isolated feedback control to regulate the power supply has been established.
- Fabricated the hardware prototype of the SiC MOSFETs with three overcurrent protection methods (solid state circuit breaker [SSCB], desaturation technique, and fault current evaluation).
- Extensively evaluated the performance of the protection schemes under various conditions, considering variation of fault type, decoupling capacitance, and protection circuit parameters.
- Proposed protection schemes capable of clearing a short-circuit fault within 200 ns, irrespective of the junction temperature variation of SiC MOSFETs.
- Based on the testing results, compared each method to explore the benefits and drawbacks of each one and its potential applications.
- Verified the ACB scheme by simulation and experiment, demonstrating the elimination of current unbalance for two parallel SiC MOSFETs.
- Developed an active gate driver to eliminate cross talk for a phase leg using WBG devices, and integrated the logic signal synthesis of the proposed gate auxiliary circuit with the latest version of a high-temperature gate driver IC.
- Developed a board-level integrated power module and conducted the preliminary test for functionality verification.

✧   ✧   ✧   ✧   ✧

Introduction

The EV and HEV have brought significant challenges for PE modules, both for the power devices and for their packaging technologies. One critical design task is to develop highly integrated power modules to reduce the total weight and volume of the power distribution systems.

Input isolation

The control circuitry of the power module requires an isolation barrier for the interface between the logic-level control signal and voltage level of the gate driver that operates the high side of a power phase leg. The isolation solution for the power module must meet the same high-temperature requirements as the power module. The isolation capability must block the rms high voltage across the phase legs and reject the dV/dt transient noise in the power module. The physical layout area of the isolation design should be minimized to reduce the overall size of the power module.

Power supply on chip

To reduce the size of the integrated power module as well as assist in high-temperature operation, an isolated PwrSoC is under development. The power supply receives a dc voltage (9–18 V) from a standard car battery and outputs a +20 V potential and a—2 V potential providing power to the module. The power supply should be operable up to 200°C and be able to supply 250 mA of current.

Overcurrent protection schemes for SiC power MOSFETs

Overcurrent protection of SiC MOSFETs remains a challenge because of a lack of extensive use and testing. Compared with overcurrent protection of Si devices and SiC JFETs, overcurrent protection of SiC MOSFETs is more challenging in the following aspects.

From a thermal point of view, SiC MOSFETs tend to have lower short circuit withstand capability than Si IGBTs and MOSFETs because of their smaller chip area and higher current density.

Besides thermal breakdown, an overcurrent condition also has a negative impact on the long-term stability of SiC MOSFETs, which have traditionally suffered gate oxide reliability issues induced by poor interface quality.

Even when fast fault response time becomes the design focus of the protection scheme for SiC MOSFETs, the objective is quite challenging in a fast-switching environment.

There are no known publications discussing the overcurrent protection of SiC MOSFETs since they have become commercially available. The objective of this research is to help designers select a proper protection method based on the analysis and performance evaluation of different protection schemes.

Active current balancing for parallel-connected SiC MOSFETs

In high-power applications such as HEVs or utility converters, parallel connection of SiC MOSFETs is required, because SiC devices usually have smaller dies than do Si devices as a result of lower yield in this less mature manufacturing process. Current unbalance among the parallel devices can occur when the individual devices or the external circuits are not exactly identical or symmetrical. Unbalanced current can lead to uneven distributed power loss and temperature rise, localized overcurrent, and even the failure of the entire module. To account for that, the current rating of the power module is usually less than the sum of all the devices' ratings, and the current capability of the devices is not fully utilized. This work proposes a novel ACB scheme. The scheme is able to sense the unbalanced current in the devices and continuously adjust the gate delay to eliminate this unbalance. It achieves high speed and arbitrarily fine time resolution that matches the fast switching speed of SiC devices; therefore, it has low circuit complexity and cost.

Cross talk mitigation

SiC devices have an inherent capability for fast switching. However, in the phase-leg configuration, the interaction between two devices during a switching transient (cross talk) might increase switching losses, reduce the reliability of the power device and, eventually, limit the switching speed of SiC devices. Considering the intrinsic characteristics of high-voltage SiC power devices—such as low threshold gate voltage, low maximum allowable negative gate voltage, and large internal gate resistance—cross talk is a serious issue, and a suitable solution for cross talk suppression is essential.

Approach

High-temperature gate driver

A revised multi-chip solution was developed in FY 2013. The functionality of the previous gate driver solution was split across three dies. The decision to split the functionality into several components was driven by our colleagues in the Ampere Lab in Lyon, France. They had purchased an engineering run and provided an area on their reticle. The conditions were that each die would be roughly 3 by 3 mm, which is drastically smaller than in previous efforts; the previous most recent gate drive chip was 9 by 5 mm. The new generation of the gate drive comprises a voltage regulator die, signal management die, and output buffer die. To facilitate a full phase-leg design, the voltage regulator die has two sets of regulators, a 5 V regulator for the low-voltage logic and a 6.4 V charge pump regulator. The charge pump regulator on the past generation had performance issues at high temperatures, but the regulator on this effort was revised to improve its performance over temperature. The signal management die also has two signal paths so that a phase leg may be driven.

The buffer die can be set up so as to double the output current (~10 A) or to drive two power switches.

The entire multi-die solution allows a lot of flexibility for end users in setting up their signal chains. For testing and to mitigate parasitics, the bare die was bonded onto a high-temperature PCB. The experimental validation of the revised gate drive will begin in FY 2014. The test procedure will involve lifetime reliability testing, because part of the revision was to improve the reliability through the addition of redundant metal traces and substrate tie-downs. The substrate tie-downs should provide a low-resistance path for heat to flow off the chip, and the redundant metal traces should improve electromigration immunity.

Input isolation

The input isolation design has been focused on an on-chip-transformer–based input isolation design. The on-chip transformers designed in the chip prototypes are around 200 µm in diameter. This is multiple orders of magnitude smaller than off-chip isolation transformers. The main drawback of the on-chip transformer is the limited dc blocking voltage. The transformer uses stacked coils on a chip metal interconnect to create the primary and secondary windings. There is limited insulating oxide between the two coils. The Si-on-insulator chip prototype 1 uses a three-metal interconnect technology. The maximum oxide insulating thickness of prototype 1 is roughly 0.9 µm. The reported SiO_2 field strength is greater than 700 V/µm. Prototype 2 uses a six-metal interconnect technology. The estimated dc blocking for prototypes 1 and 2 is estimated at 630 and 2440 V, respectively. Although prototype 2 has a much higher dc blocking voltage, the chip technology is not capable of high-temperature operation. Therefore, both prototypes will be tested and the limitations of each will be experimentally discovered.

The on-chip design is implemented in 5 V complementary metal-oxide semiconductor (CMOS) technologies. The design block diagram is shown in Figure III-11. The transformer size is small because of the use of GHz-level voltage pulses passed through the transformer. The transmitter controls the di/dt through the primary transformer winding to create a voltage pulse. The receiver then detects the voltage pulses and recreates the input logic signal.
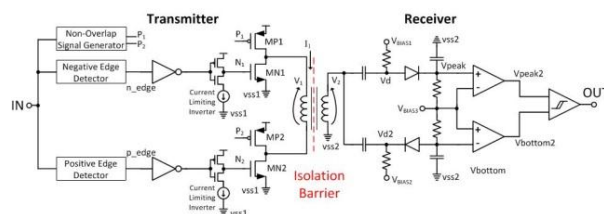
Figure III-11: On-chip design block diagram.

Power supply on chip

To provide the +20 V potential, an active clamp boost converter topology was chosen for its low number of components as well as its wide input range capability. An active clamp flyback converter was adopted to provide the −2 V potential for the same previously mentioned reasons.

Figure III-12 shows the schematic of the power supply. A major difficulty in designing a PwrSoC, let alone an isolated one, is implementing on-chip inductors (or transformers). All inductors have some series resistance that must be minimized for efficient operation of a dc-dc switched mode power supply. This is a challenge because to reduce the series resistance, the size of the inductor must increase. Since size reduction is a design constraint, a tradeoff must be reached that allows implementation of an efficient PwrSoC. The transformers depicted in Figure III-12 are made up of stacked 12 and 23.5 nH inductors with 820 mΩ and 4.5 Ω of series resistance, respectively. The outer diameter of the transformer is 2000 µm. A feedback control scheme is required to regulate the +20 V and −2 V outputs. Since the converter is isolated, the feedback must also be isolated. To accomplish this, a PWM scheme was implemented on the secondary side of each converter. The PWM signal is then transmitted to the primary side, where a controller processes the signal and is used to drive the MOSFET switches of the converter.
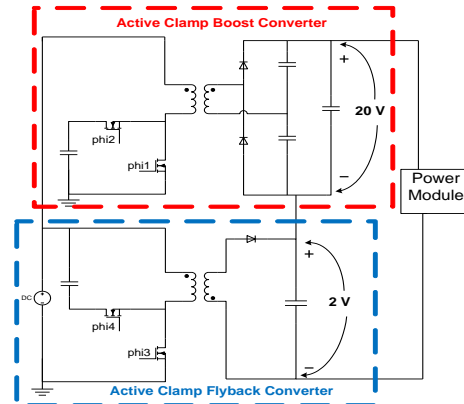
Figure III-12: Schematic of isolated power supply on chip (the feedback control circuitry is not shown).

Overcurrent protection schemes for SiC power MOSFETs

First, the short-circuit capabilities of commercial SiC MOSFETs were determined. Based on this, several candidates, including conventional protection techniques and newly proposed methods, were implemented and evaluated through Saber simulation with real component models. Finally, a step-down converter-based hardware test setup was built to verify and compare these methods through extensive measurements.

Active current balancing for parallel-connected SiC MOSFETs

In high-power applications of SiC MOSFETs where parallelism is employed, current unbalance can occur and affect the performance and reliability of power devices. A novel ACB scheme was proposed. This scheme includes three basic building blocks, as shown in Figure III-13: (1) The current unbalance sensing block senses the unbalanced current in the devices. (2) The current balancing controller generates the correction needed based on the measured unbalance. (3) Then, the active gate control varies the gate drive signal delay according to the instruction from

the balancing algorithm. The three blocks form a negative feedback loop.
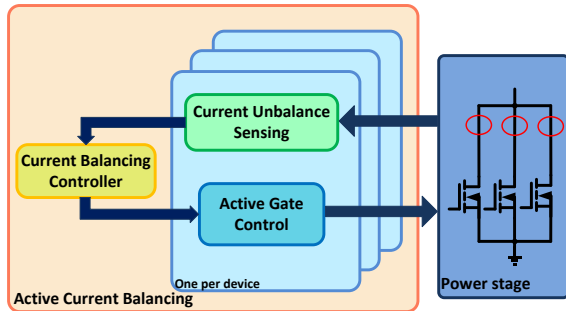
Figure III-13: Block diagram of the proposed ACB.

The proposed current unbalance sensing technique measures the difference instead of the actual value in the two parallel devices, using a differential current transformer (DCT). The schematic is shown in Figure III-14. It has two 1-turn primary windings in opposite directions. If current unbalance exists and the currents in the two windings are unequal, there will be net flux change, and current in the secondary will generate output voltage, *V out*, the polarity of which indicates the polarity of unbalance. The proposed DCT has negligible impact on the system efficiency and component stresses because the 1-turn primary winding has very low resistance and leakage inductance.
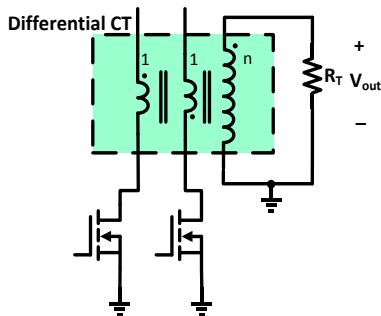
Figure III-14: Schematic of the proposed DCT.

A novel variable gate delay (VGD) circuit is proposed as the core of the active gate control block. The schematic is shown in Figure III-15. During a turn-on transient, M1 is in saturation and its drain current is controlled by its Vgs. Therefore, *Vcontrol* controls the charging current of the power switch gate and thus its turn-on delay. The proposed VGD circuit achieves continuous tuning of gate delay with arbitrarily fine time resolution.

The proposed current balancing controller (CBC) is implemented based on an integrator circuit, as shown in Figure III-16. The output of the DCT is integrated with a gain of $1/sR_1C_1$. The output of the integrator is connected as *Vcontrol* of the VGD. In conjunction with the DCT and VGD, the CBC closes the negative feedback loop and adjusts the gate signal delay so that the output of the DCT is zero; thus the current unbalance is eliminated.
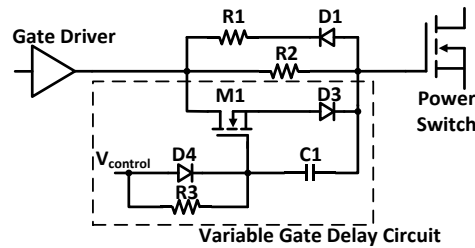
Figure III-15: The proposed variable gate delay circuit.
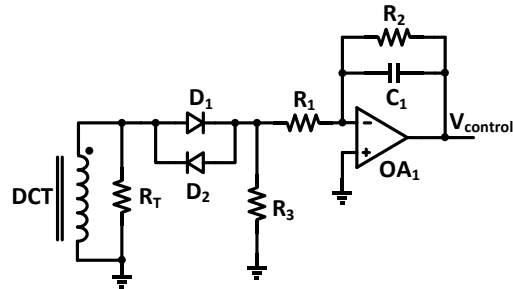
Figure III-16: Simplified schematic of the proposed current balancing controller.

Cross talk mitigation

A gate impedance regulation (GIR)–based active gate driver circuit was developed for cross talk mitigation (it is illustrated in the FY 2012 progress report). To fully avoid cross talk for fast-switching SiC power devices in a phase-leg configuration, a gate voltage control (GVC)–based active gate methodology was proposed, as shown in Figure III-17. Compared with the conventional gate drive circuit (S_{1_H}, S_{2_H} or S_{1_L}, S_{2_L}), two auxiliary transistors (S_{a1_H} and S_{a2_H} or S_{a1_L} and S_{a2_L}) together with one diode (D_{a_H} or D_{a_L}) are added between the gate-source terminals of each device, whereas the commonly used negative isolated power supply is not needed. Figure III-18 displays the active gate driver board with the proposed gate auxiliary circuit.
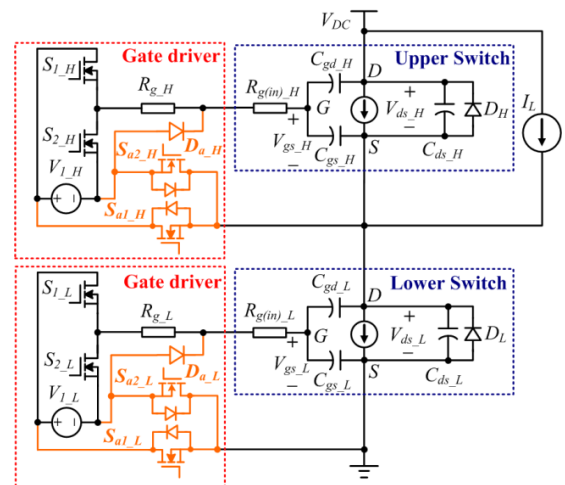
Figure III-17: Active gate driver with GVC assist circuit.
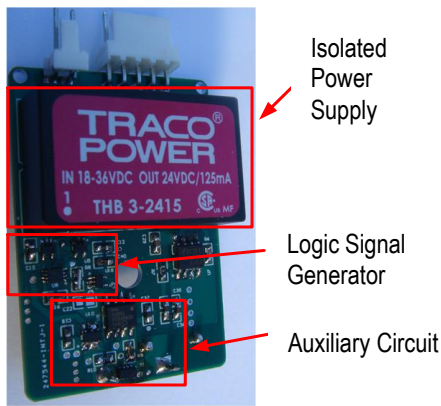
Figure III-18: Active gate driver board.

Board-level integrated power module

Based on a phase-leg power module built with CPM2-1200-0025B SiC MOSFETs and CPW5-1200-Z050B SiC Schottky diode bare dies from CREE (Figure III-19), a board-level integrated power module was developed. It can be seen from Figure III-20 that the smart power module integrates the gate driver auxiliary power supply board, gate driver board, and phase-leg power module in a sandwich structure. Based on chip-on-board techniques, the high-temperature gate driver IC developed by the University of Tennessee is bonded with the gate driver board to switch the power devices.
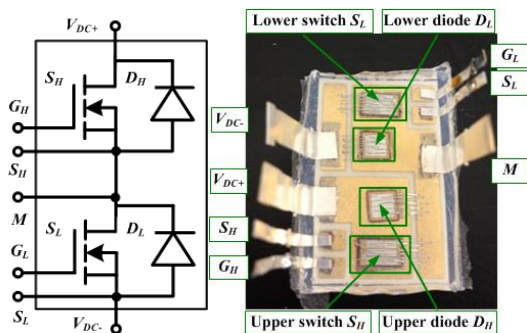
Figure III-19: 1,200 V SiC-based phase-leg power module.
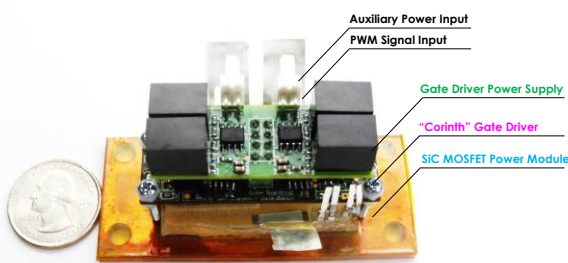
Figure III-20: Board-level integrated power module.

Results

Input isolation

A circuit to test the common mode rejection (CMR) of the input isolation chips was designed. The circuit injects a high-voltage transient to the ground potential of either the transmitter or the receiver of the isolation design. The injected voltage is around 25 kV/µs. This dV/dt can be adjusted by changing a resistor-capacitor network and by adjusting the dc link voltage. The dV/dt ranges from 2 kV/µs to greater than 30 kV/µs. Typical CMR ratings of isolators are around 5 to 50 kV/µs. The discrete components used in the test circuit are rated for 600 V. The setup uses two transmitter/receiver isolation pairs. The first transmitter/receiver pair isolates the PWM signal up to the high-voltage domain, and the second pair isolates the PWM down to the low-voltage domain for measurement. A dynamic CMR test is defined by an injected common-mode voltage while the input and output are switching. A failed test is defined as a false switching of the output signal of the receiver circuit.

A polyimide PCB is used to test the input isolation chips and CMR scheme. Each isolation chip contains both the transmitter and receiver of the isolation design. However, each chip will use only the transmitter or the receiver. The design is a two-chip solution. On the polyimide PCB, four chips are bonded directly to the PCB substrate. The four chips make up two transmitter/receiver pairs.

Test results are shown in Figure III-21 and Figure III-22. Figure III-21 shows the basic functionality of the isolation chips. The frequency of the input logic signal is 1 MHz, well beyond the needed frequency of the power module. The output signal matches the input with a propagation delay of 69 ns. Figure III-22 shows a CMR test. The input signal switches to high, causing the output signal to switch immediately afterward. A common-mode voltage of 6 kV/µs is injected to the ground potential of the high-voltage domain. The output signal is not disturbed by the common-mode voltage pulse.
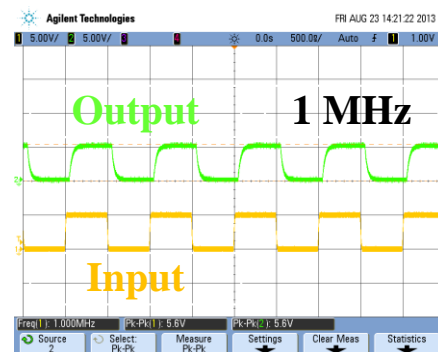
Figure III-21: Functionality test waveform, f = 1 MHz.
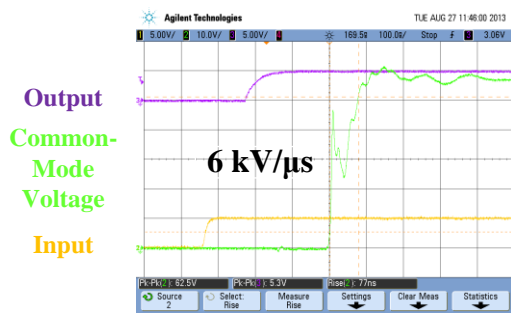
Figure III-22: Dynamic common-mode voltage test.

Power supply on chip

Preliminary schematic simulation results for the power supply without any regulating feedback control are shown in Figure III-23. In Figure III-23, the two potentials in reference to the secondary side ground can be observed. These simulations support Figure III-12 as a viable power supply system.
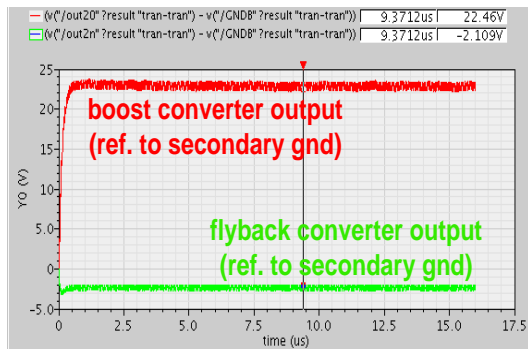
Figure III-23: Preliminary simulation results for the outputs of the boost converter and flyback converter in reference to the secondary side ground.

Overcurrent protection schemes for SiC power MOSFETs

Two conventional candidates were implemented: (1) an SSCB and (2) a desaturation technique. A third protection scheme, based on the fault current evaluation, is also proposed to protect SiC MOSFETs under a short-circuit condition. These were implemented with a special focus on the design optimization, and comparisons of their performance were provided. The fabricated hardware test bed is shown in Figure III-24.
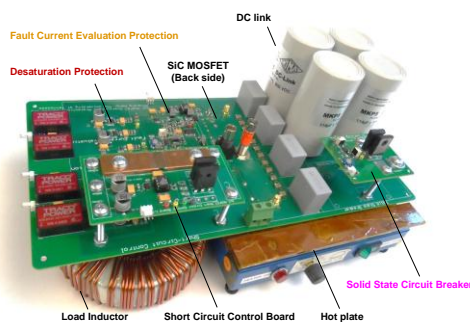
Figure III-24: Hardware testbed of the protection schemes.

1. Solid-state circuit breaker

Figure III-25 describes an SiC MOSFET–based step-down converter with a normally-on SSCB taking advantage of the well-known desaturation protection schemes of IGBTs. The SSCB could be inserted either in series with the energy storage capacitors (position A), or in series with the main power loop (position B). Inserting it into the main power loop can reliably detect and clear overcurrent faults, while considerable power dissipation is a concern. At position A, the loss associated with the SSCB is small, since only ripple current goes through the SSCB in series with the dc link energy storage capacitors. However, SiC MOSFETs could still be destroyed by the short-circuit loop from the dc source V_{dc} or the front-end rectifier to the device.

Figure III-26 and Figure III-27 show the testing results under hard switching fault (HSF) and fault under load (FUL) condition. In both fault types, the fault response time is well below 200 ns, and the fault peak current is below 60 A.
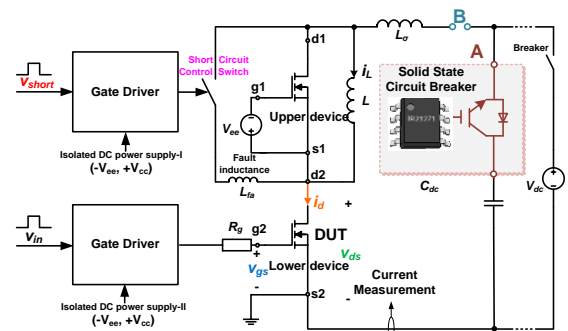
Figure III-25: Step-down converter with an SSCB.
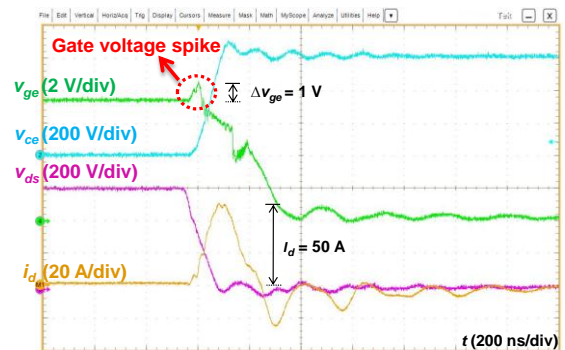
Figure III-26: Protection under hard switching fault condition.
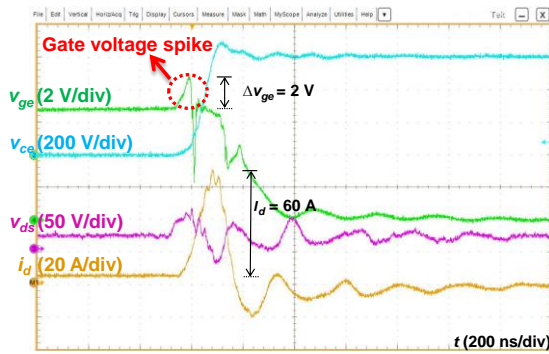
Figure III-27: Protection under fault-under-load condition.

2. Desaturation technique

The desaturation protection circuit implemented in this work is shown in Figure III-28. The drain-source voltage of the device under test is monitored by the sensing diode D_{ss}, and the R-C network (R_{sat1}, R_{sat2} and C_{blk}). When the device is "on" and saturated, D_{ss} will pull down the voltage across C_{blk}. When the device pulls out of saturation under overcurrent condition, the buffer output will charge C_{blk} up and trip the comparator.
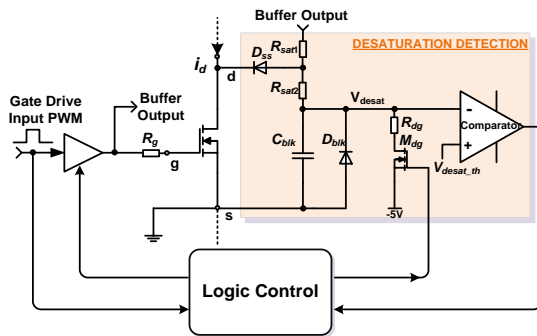
Figure III-28: Implementation of desaturation technique.

Figure III-29 shows experimental waveforms with a desaturation protection scheme under an HSF condition. The blanking time is set at 100 ns. The HSF fault current is limited to 130 A within 210 ns.
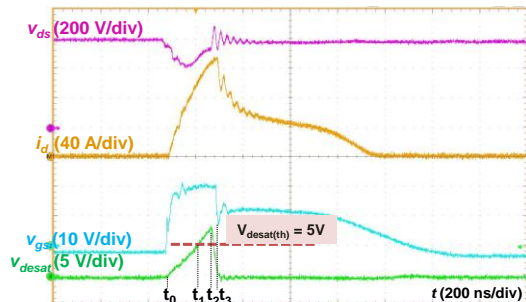
Figure III-29: Protection waveforms under hard switching fault.

3. Fault current evaluation

A novel overcurrent protection scheme is also proposed to realize fast response time and strong noise immunity simultaneously; the circuit implementation is shown in Figure III-30. There are four main function blocks: fault current evaluation, logic control, gate voltage clamping, and soft turn-off.
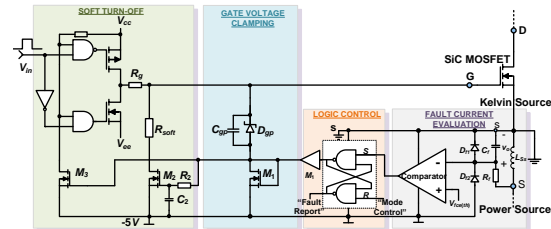
Figure III-30: Fault current evaluation protection scheme.

Fault current evaluation is used to dynamically estimate the fault current by an resistor-capacitor filter during a short-circuit transient. The logic controller could activate/deactivate the protection circuit according to the input fault current evaluation results. Once the protection circuit is activated, the gate voltage clamping could limit the transient short-circuit current, and the device would be softly turned off to suppress the voltage overshoot during a turn-off transient.

Figure III-31 and Figure III-32 show experimental waveforms with the fault current evaluation protection scheme under HSF and FUL conditions. With R_f = 200 Ω, C_f = 1 nF and $V_{fce(th)}$ = −3 V, the current protection threshold is around 100 A. The HSF fault current is limited to 130 A within 140 ns; then it is clamped to around 50 A, with a corresponding clamped gate voltage of 12 V. Following a delay of 400 ns, the device is softly turned off. Similar protection characteristics are also shown under FUL, while its fault peak current (120 A) is a little higher owing to longer protection delay.
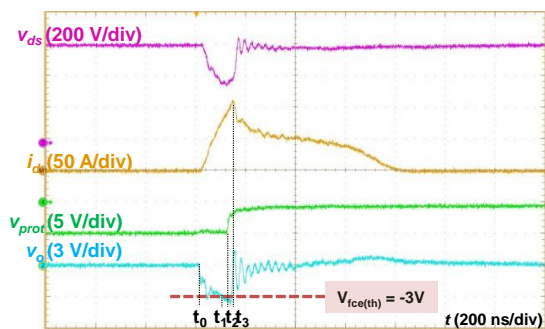
Figure III-31: Protection waveforms under hard switching fault.
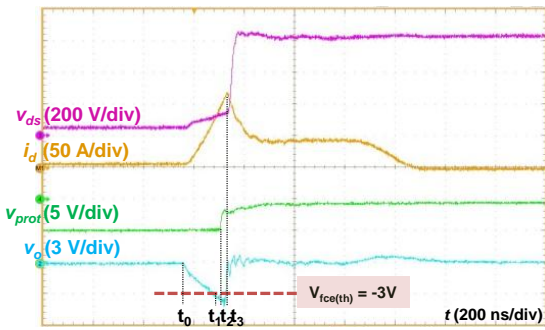
Figure III-32: Protection waveforms under fault under load.

Active current balancing for parallel-connected SiC MOSFETs

The ACB system is implemented with the DCT, VGD, and CBC described earlier and verified in a buck converter with two parallel SiC MOSFETs, model CMF20120D. The simplified schematic is shown in Figure III-33. The V_{th} of M1 is 1.0 V lower than that of M2. The variable delay is applied to M1 while a reference voltage is applied to the M2 VGD so that the relative delay between the two devices can be both positive and negative. Figure III-34 shows the experimental results. The current unbalance during turn-on transition is greatly reduced by the ACB scheme. Since the ACB scheme directly measures the unbalanced current and reduces it by negative feedback, it can reduce any current unbalance, regardless of the cause.
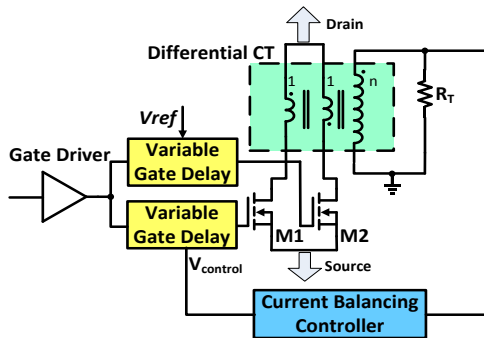
Figure III-33: Simplified schematic of the proposed ACB system.
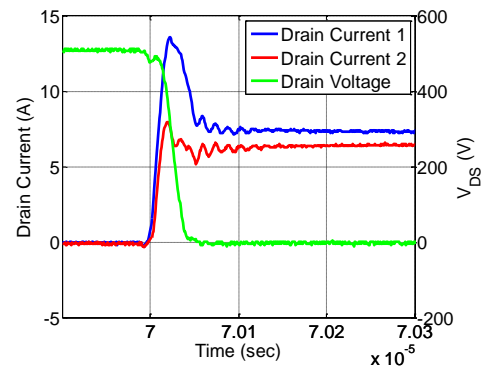
(a)
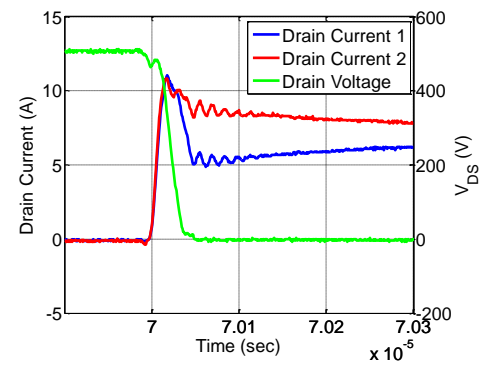
(b)

Figure III-34: The switching waveforms (a) with and (b) without the ACB scheme enabled.

Cross talk mitigation

To evaluate the effectiveness of the GVC-based active gate driver for cross talk suppression, comparison experiments were conducted, using a double-pulse tester with CMF20120D SiC MOSFETs, on three different groups: a conventional gate driver, a GIR-based gate driver, and the latest GVC-based gate driver, as shown in Table III-2. Figure III-35 displays the comparison waveforms under three different groups with the operating condition of 800 V/10 A with 10 Ω gate resistance and load current, I_L, of 10 A. It shows that compared with the GIR-based gate driver, the GVC-based gate driver is more effective at suppressing cross talk: the turn-on energy losses during the turn-on transient of the lower switch are reduced by up to 19% instead of 17%. The slew rate of the drain-source voltage is further improved from 24 to 25 V/ns.

More experimental data under different operating conditions provided in Figure III-36 indicate that compared with the GIR-based gate driver, the GVC-based gate driver can effectively eliminate cross talk and enhance switching performance. Note that to clearly demonstrate the effectiveness of the proposed active gate driver, the experimental data for the second and third groups shown in Figure III-36 are normalized based on data for the first group (Table III-3). In summary, the GVC-based gate driver is a more effective solution for cross talk suppression. Also, considering the all-transistor-based auxiliary circuit, the

auxiliary components of the GVC-based gate driver are suitable for gate driver chip-level integration.

V_{DC} = 800 V, I_L = 10 A (Turn-on transient of the lower switch)

V_{DC} = 800 V, I_L = 10 A (Turn-on transient of the lower switch)
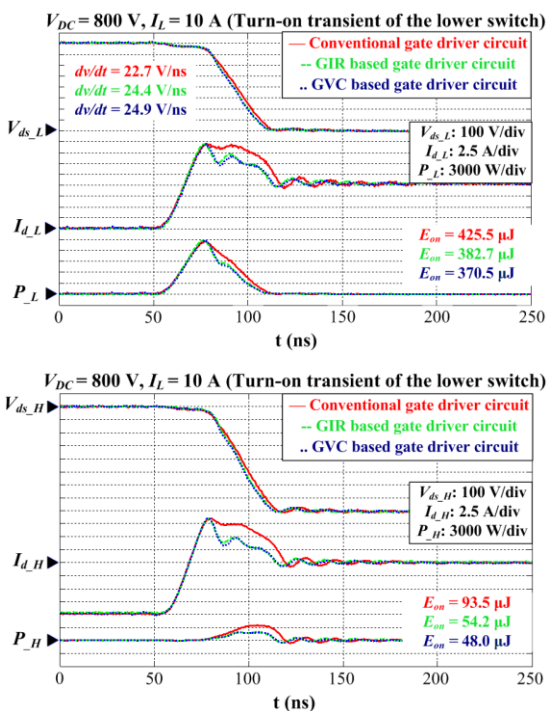
Figure III-35: Lower and upper switch waveforms during turn-on transient of lower switch.

Table III-2: Three comparison groups

1st Group	Conventional gate driver
2nd Group	GIR-based gate driver
3rd Group	GVC-based gate driver

Table III-3: Eon and dv/dt vs. I_L under the first group with Vdc of 800 V and Rg of 10 Ω.

I_L (A)	5	10	20
E_{ON} (μJ)	381.3	519.0	852.6
dv/dt (V/ns)	23.5	22.7	21.1
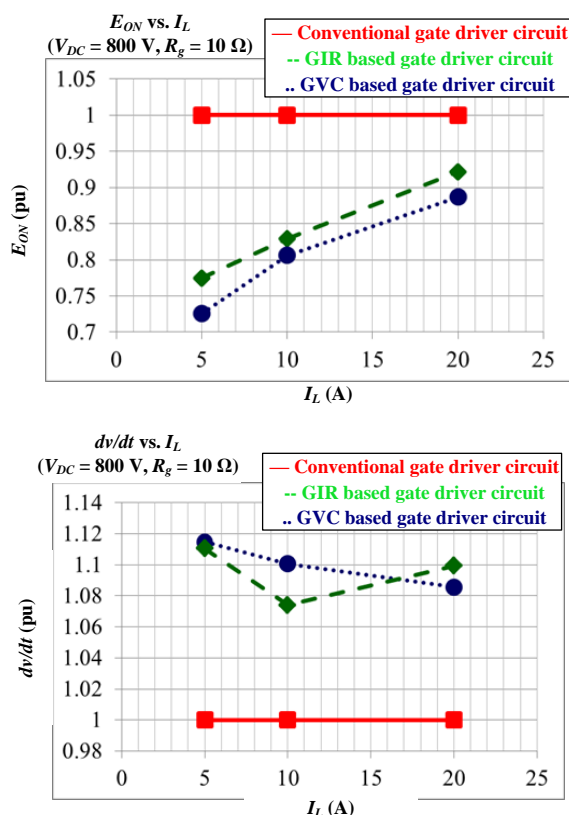
Figure III-36: The GVC-based gate driver is more effective for reducing turn-on energy loss and improving dv/dt under different operating conditions.

Board-level integrated power module

Preliminary testing was carried out to evaluate the switching characterization of the SiC-based phase-leg power module. Figure III-37 displays the drain-current and drain-source voltage of both the upper and lower switches during the switching transient of the lower switch under operating conditions of 800 V/30 A with 5 Ω gate resistance. It shows that with the same gate resistance, the ringing during the turn-on transient is more serious than that during the turn-off transient. In addition, the overshoot voltage of the upper switch during the turn-on transient (902 V) is higher than that of the lower switch during the turn-off transient (642 V). Also, because of the cross talk and its induced shoot-through current, the switching loss of the upper switch (240 μJ) becomes comparable to that of the lower switch (370 μJ) during the switching transient of the lower switch.

More experimental data taken under different operating conditions (Figure III-38) indicate that the cross talk–induced energy losses make up a large portion of the total switching losses. Therefore, it is essential to apply the latest version of the University of Tennessee–developed gate driver IC integrated with the anti-cross talk circuitry for the next version of the 1,200 V SiC-based phase-leg power module.
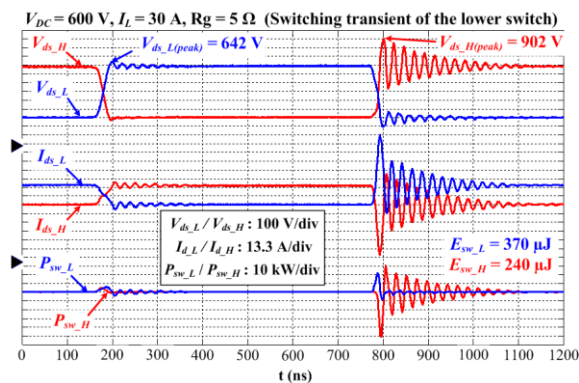
Figure III-37: Typical switching waveforms of power module.
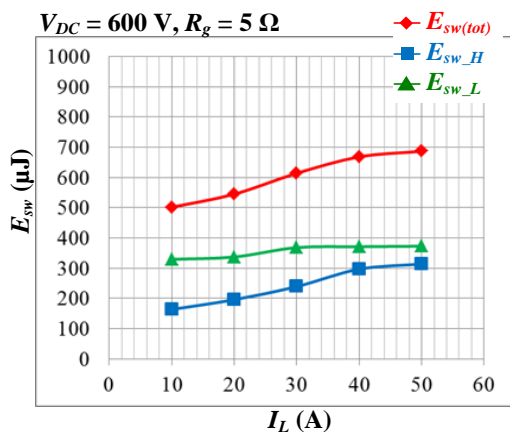
Figure III-38: Switching loss dependence on I$_L$.

Conclusions and Future Directions

Input isolation

A high level of integration is desired for the input isolation and other components of the project. An on-chip solution for input isolation is the current focus for integration with the power module. Two chip prototypes have been designed. The first prototype has been fabricated and tested. The chips have performed well and operate above 1 MHz signal transmission. The CMR of the isolation chips has been demonstrated at 6 kV/μs. The second chip prototype is designed to improve the CMR and rms isolation voltage. This design will be fabricated in October and arrive for testing in early 2014.

Power supply on chip

An isolated PwrSoC schematic has been developed, and a feedback control scheme for regulating the output voltages has been established. Currently, the transmitter and receiver for the PWM feedback signal are being designed. In the near future, the power supply schematic will be combined with feedback control and the completed system will be fine-tuned. Future effort will be spent on shrinking the size of the on-chip transformer and improving the efficiency of the dc-dc converters.

Overcurrent protection schemes for SiC Power MOSFETs

Three overcurrent protection methods have been presented for SiC MOSFETs under both HSF and FUL conditions. The design considerations and associated issues of these methods were analyzed and verified through experiments. A qualitative comparison of these techniques was made for fault response time, temperature-dependent performance, and their potential applications to help the designer select an appropriate protection scheme. The experimental results based on a step-down converter indicate that the proposed protection schemes have the capability to clear a short-circuit fault within 200 ns, irrespective of the junction temperature variation of SiC MOSFETs. The integration of the protection method into a gate driver chip will be investigated.

Active current balancing for parallel-connected SiC MOSFETs

An ACB scheme was proposed. Experimental results show that the proposed DCT is able to accurately measure the unbalance current despite its small size. And the novel, simple VGD circuit is able to continuously adjust the gate delay with arbitrarily fine resolution for fast-switching SiC MOSFETs. The proposed ACB system can automatically adjust the gate signal and remove current unbalance. Based on this work, ACB for multiple SiC devices in parallel will be investigated in the future.

Cross talk mitigation

A GVC-based gate assist circuit using two auxiliary transistors together with a diode is proposed for cross talk suppression in a phase-leg configuration. The test results with CMF20120D SiC MOSFETs verify that without the negative turn-off gate voltage, this gate assist circuit has the capability to fully suppress cross talk under different operating conditions. It also improves switching performance compared with the conventional gate drive, even with −2 V turn-off gate voltage: turn-on transient becomes fast; turn-on switching loss can be reduced by up to 19.4%; and spurious negative gate voltage is always suppressed within its required range. Accordingly, this all-transistor–based gate assist circuit offers a simple, efficient, cost-effective solution for cross talk elimination. Also, it is a promising option for gate driver chip-level integration.

Board-level integrated power module

A board-level integrated power module has been developed, including a high-temperature SiC MOSFET power module, an Si-on-insulator gate driver, and a gate driver power supply. The preliminary switching performance of the power module was characterized through double-pulse tests. Experimental results show the fast switching speed of the integrated power module, as well as associated ringing issues.

The high-voltage and high-temperature input signal isolation will be added to the gate driver and integrated with the power module. A ceramic substrate–based high-temperature gate driver will be fabricated to replace the polyimide PCB board, with the aim of further increasing the power density and high-temperature capability of the integrated power module.

FY 2013 Publications/Presentations

1. Z. Wang, X. Shi, Y. Xue, L. M. Tolbert, B. J. Blalock, F. Wang, "Design and performance evaluation of overcurrent protection schemes for silicon carbide (SiC) power MOSFETs," *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept. 15–19, 2013, Denver, Colorado, 2013.

2. Y. Xue, J. Lu, Z. Wang, L. M. Tolbert, B. J. Blalock, F. Wang, "Active current balancing for parallel-connected silicon carbide MOSFETs," *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept. 15–19, 2013, Denver, Colorado, 2013.

3. Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, "A novel gate assist circuit for cross talk mitigation of SiC power devices in a phase-leg configuration," in *Proceedings of IEEE APEC*, pp. 1259–1265, March 2013.

4. Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, "A gate assist circuit for cross talk suppression of SiC devices in a phase-leg configuration," in *Proceedings of the IEEE Energy Conversion Congress and Exposition*, Sept. 15–19, 2013, Denver, Colorado, 2013.

5. Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, "Active gate driver for cross talk suppression of SiC devices in a phase-leg configuration," accepted for publication in *IEEE Trans. Power Electronics*.

6. Z. Wang, X. Shi, L. M. Tolbert, F. Wang, B. J. Blalock, "A di/dt feedback-based active gate driver for smart switching and fast overcurrent protection of IGBT modules," accepted for publication in *IEEE Trans. Power Electronic*.

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Start Date: October 2013
Projected End Date: September 2016

Objectives

- Overall project objective
  - Develop low-cost, high-efficiency, high-power-density all-WBG dc-dc converters and OBCs. The aim is to reduce charger converter cost by 50% and weight and volume by a factor of 2 compared with the state of the art and provide charger efficiency of more than 96%.
- FY 2013 objective
  - Research architecture candidates for a dc-dc converter and charger best suited for functional integration and target power throughput levels of 2.2 kW for a 14 V dc-dc converter and 6.6 kW OBC. The efficiency of both functions should be greater than 95% at 75% of the rated power.

Technical Barriers

- Reducing OBC and dc-dc converter cost, weight, and volume
- Achieving high efficiency
- Overcoming the limitations of existing semiconductor and magnetic materials to address charger and converter cost, weight, volume and efficiency targets

Accomplishments

- Completed a modeling, analysis, and simulation study for several isolation converter architectures and down-selected one for prototype development.
- Developed a control strategy for the isolation converter to reduce the battery ripple current of twice the ac main frequency that is inherent in single-phase ac-dc converters. Simulation results show the control strategy enables a 60% reduction in the ripple current and thereby a significant size reduction in the bulky dc link capacitor in the front ac-dc converter.
- Completed a DBC substrate design for WBG switch phase-leg modules for Cree SiC MOSFETs and Schottky diodes.
  - DBC cards based on the design were fabricated.
  - Several SiC MOSFET phase-leg modules using the DBC cards were assembled.
- Conducted testing and evaluation of Efficient Power Conversion (EPC) low-voltage (<200 V) enhancement mode GaN (eGaN) switches for possible use in the 14 V dc-dc converter.
- Conducted testing and evaluation of International Rectifier (IR) 600 V GaN switches packaged by Delphi for use in high-voltage converters.
- Completed a design for a 6.6 kW isolation converter using ORNL-designed SiC phase-leg modules and planar ferrite cores.
- Completed tests of a baseline 5 kW Si-based integrated charger, using the selected isolation converter candidate, that demonstrated an isolation converter peak efficiency of 98% and a charger system (ac line to dc output) peak efficiency of 93% at 65% rated load.

✧   ✧   ✧   ✧   ✧

Introduction

The stand-alone OBCs and 14 V dc-dc converters that currently dominate plug-in EVs and AEVs are not cost-effective and have performance limitations that stem from limitations in existing semiconductor and magnetic materials. The result is a plateau in charger and converter performance because (1) Si switches constrain switching frequencies to typically 100 kHz, and (2) inductors and transformers based on soft ferrite magnetic materials further limit power density and efficiency because of low saturation flux densities (~0.38 T) and high core losses at high frequencies. The limitations in switching frequency and material properties result in bulky and expensive passive components—including ac filter capacitors, inductors, and transformers—in currently available OBCs. As shown in Figure III-39, passive components contribute more than 30% of the charger cost in state-of-the-art Si-based technology.

As a result, OBCs

- Add significant cost (~$106/kW), weight, and volume (e.g., the 2012 Nissan LEAF 6.6 kW OBC weighs 16.2 kg and has a volume of 10 L)
- Are relatively inefficient (85–92%)

- Are unidirectional (can charge the battery but are incapable of vehicle-to-grid support, a highly desirable function in future smart grids)
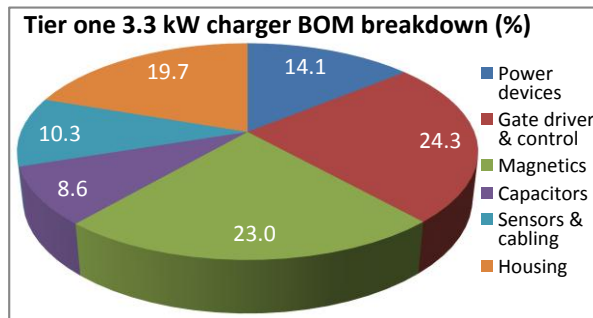
Figure III-39: Bill-of-material breakdown for a tier one 3.3 kW OBC.

Emerging WBG devices, including SiC and GaN and advanced soft magnetic materials, are poised to offer significant improvements in ac-dc and dc-dc converters. Their ability to operate with enhanced efficiency over higher frequencies and temperatures minimizes passive component requirements and reduces cooling demands, providing opportunities for revolutionary strides in PE.

This project is targeted at leapfrogging existing Si-based charger technology to address charger and converter cost, weight, volume, and efficiency requirements. It proposes to overcome the limitations of existing semiconductor and magnetic materials by using WBG devices, advanced magnetic materials, and novel control strategies to significantly increase power density, specific power, and efficiency at lower cost.

Approach

Our strategy to address the limitations of state-of-the-art OBCs and dc-dc converters is multifold:

- Push the envelope on functional integration of the traction drive, 14 V dc-dc converter, and OBC.
- Take up the challenge of introducing WBG materials, specifically GaN, into automotive applications to determine what performance, packaging, cost, and efficiency benefits can be gained.
- Perform analysis, modeling, and simulation that lead to a functional prototype meeting VTO OBC specific power, power density, and efficiency requirements while significantly reducing the current cost levels.
- Design, build, test, and demonstrate prototypes.
- Work with U.S. DRIVE to develop insights and lessons learned from the automotive community pertinent to dc-dc converters and OBCs.
- Collaborate with industry stakeholders, universities, and other national laboratories to maximize the impact of this work.

Three technical approaches are being pursued. First, integrated bidirectional WBG OBCs will be developed that (a) provide galvanic isolation; (b) provide an integrated function

for dc-dc conversion of high voltage to 14 V; (c) use soft switching at the dc-dc stage to reduce electromagnetic interference (EMI) and improve efficiency. Figure III-40 shows an integrated dc-dc converter and charger architecture consisting mainly of an ac filter, a WBG front active converter, a dc bus capacitor, and a WBG isolation converter. The isolation converter integrates the functions for charging both the high-voltage traction battery and the 14 V battery for vehicle accessory loads. It includes high-frequency transformers and dc filters as well as WBG switches. A topology for the front end active converter and isolation converter was selected via simulation and experimental verification.
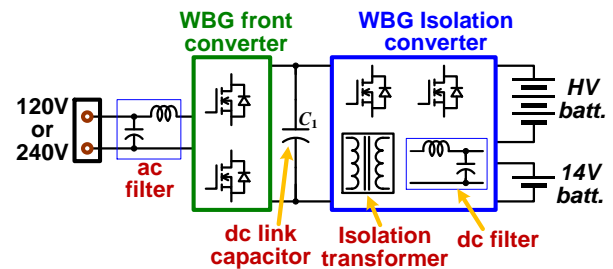
Figure III-40: An integrated dc-dc converter and charger architecture.

Second, increasing power density and specific power without sacrificing efficiency is aggressively pursued by exploiting high switching frequency with WBG devices (especially GaN switches) and using advanced soft magnetic materials (nanocomposites) to drastically reduce the cost, weight and volume of the ac and dc filters and isolation transformer. Because the availability of WBG power modules is limited, SiC and GaN devices are purchased or obtained directly from device vendors, tested, characterized, and packaged for use in converter design and prototype development. Prototypes will be built and tested first using SiC devices—for which wafer processing and device fabrication technologies have advanced to the stage that SiC MOFETs and other switches are available commercially—and then GaN switches as that technology matures and devices with high current ratings become available.

Finally, a control strategy for the isolation converter will be developed to shrink the bulky dc link capacitor. This is necessary to filter out the large voltage ripple—with twice the grid supply frequency—inherent in single-phase ac-dc converters.

Three front end active converters were studied through simulation. The first is based on an ac/ac matrix converter that employs four pairs of switches of reverse blocking capability (Figure III-41). The main advantage of the ac/ac matrix converter is the elimination of the dc bus capacitor. However, because reverse blocking WBG switches are not available, the ac/ac matrix converter requires a switch and a diode connected in series for each of the switches shown in Figure III-41, significantly increasing conduction losses. We found that the efficiency penalty of existing SiC diodes makes it difficult to achieve the required charger system efficiency.
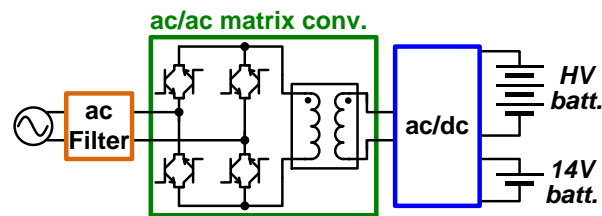
Figure III-41: Using ac/ac matrix converter to eliminate the dc bus capacitor.

The second approach (Figure III-42) employs an H-bridge ac-dc converter and uses a ripple energy buffer to eliminate the ripple voltage. The ripple energy buffer uses a buck-boost converter to remove the pulsating ripple power from the main dc bus capacitor, C_1, and dump it to the energy buffer capacitor, C_2, significantly reducing the capacitance of C_1. This approach shifts the cost of the bulky dc bus capacitor to the additional switches and passive components of the ripple energy buffer. Therefore, the cost, weight, and volume savings in the dc bus capacitor must exceed the cost, weight, and volume added to the other components for this approach to be beneficial in reducing charger system cost, weight, and volume. Our simulation study shows this is not the case.
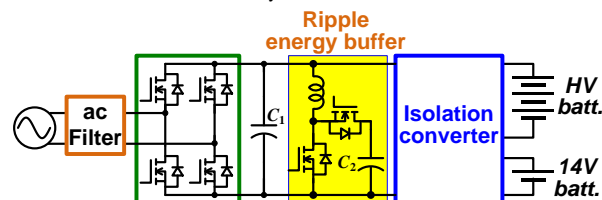
Figure III-42: Use of a ripple energy buffer to eliminate the ripple voltage.

In the third approach, instead of using a ripple energy buffer, we developed a battery ripple current reduction control strategy for the isolation converter to reduce the bulky dc link capacitor (Figure III-43). Simulation results (see Results section) show the control strategy reduces the ripple current by 60%, enabling a significant reduction of the bulky dc link capacitor in the active front ac-dc converter.

Further, WBG traction drive inverters and motors will be operated as the active front converter and used to replace the ac filter inductor, significantly reducing the OBC cost, weight, and volume.
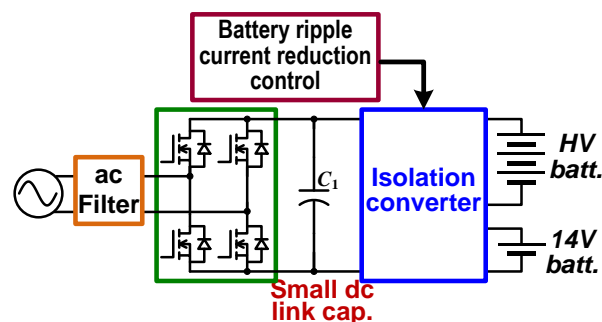
Figure III-43: Using a battery ripple current reduction control strategy for the isolation converter to reduce the bulky dc link capacitor.

Figure III-44 shows the integrated isolation converter topology selected through simulation. It is made up of a dual H-bridge phase shift dc-dc converter and a 14 V buck converter coupled through a high-frequency transformer. One H-bridge is connected to the high-voltage traction battery and the other to the active front ac-dc converter. Sharing of the transformer (for galvanic isolation) and other switch components between the OBC and the 14 V converter leads to substantial cost, weight, and volume savings for the OBC compared with a stand-alone counterpart. Other features of the integrated charger include these:

- It provides bidirectional power flow and thus can offer additional desired functions such as vehicle-to-grid and vehicle-to-home applications.
- It can charge the 14 V battery from the grid in addition to normal operation from the high-voltage traction battery.
- It uses the parasitic capacitance of the switches and the transformer leakage inductance to achieve zero-voltage switching for EMI noise reduction and efficiency improvement.
- The dual H-bridge converter enables the OBC to charge the battery over a wide range of voltages by providing a voltage buck and boost function through phase shift and duty ratio control.
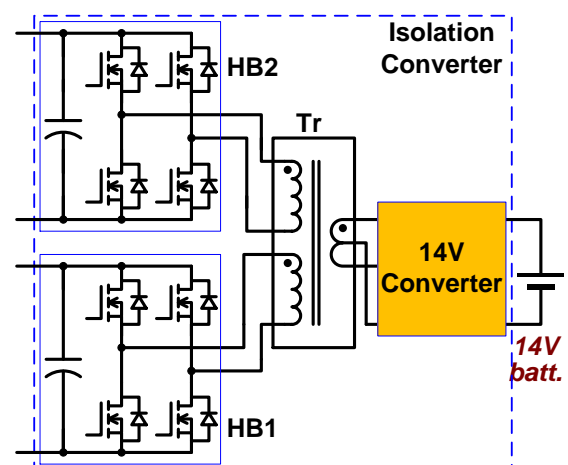
Figure III-44: Isolation converter topology.

An Si-based 5 kW prototype consisting of an electrical drive system and an isolation converter was built to test the charging function and verify the selected topology. The isolation converter and the experimental results will serve as the baseline for comparison with WBG-based prototypes to be developed in the next phase of this project. The TDS consists of two inverters (one rated at 55 kW for the traction motor and one at 30 kW for the generator), a 10.9 kW induction motor, and a PM motor (used as a generator) rated at 8.2 kW. Figure III-45 shows the inverters and test motors. The 55 kW inverter was fabricated with a 600 V/600 A six-pack intelligent IGBT module, and the 30 kW inverter was assembled with a 600 V/300 A six-pack IGBT module. The dc bus capacitor bank was constructed using four 375 µF film capacitors rated at 600 V. These components are mounted on a 12 by 7 in. water-cooled cold plate. Because of their relatively low power ratings, the measured zero-sequence

resistances of the generator and motor are quite large—23.8 mΩ and 165.74 mΩ, respectively—compared with those of production HEV/EV motors. For example, the measured zero-sequence resistances of the 2007 Toyota Camry generator and motor are 21.58 mΩ and 10.75 mΩ, respectively. The combined zero-sequence resistance value of the test motors is thus 189.54 mΩ, more than five times that of the two motors in the Camry (32.32 mΩ). These high-resistance motors (manufactured by General Electric) will have a significant impact on the measured charger system efficiency in the following test results.

The isolation converter prototype, rated at 5 kW, was fabricated using superjunction Si power MOSFETs and a planar transformer with two high-voltage and one 14 V PCB windings. The parasitic capacitances of the MOSFETs, along with the transformer leakage inductance, are used for zero-voltage switching. Figure III-46 shows the isolation converter prototype. All the components are mounted on an Al cold plate with a 6 by 7 in. footprint. Gate driver PCBs are mounted directly over the MOSFETs to eliminate wire connections between them. A control PCB using a TI TMS320F2808 fixed-point DSP controller is used to implement the dc bus voltage, grid current, battery charging voltage, and current control blocks. It is located on the top. Figure III-47 shows the planar transformer, which is constructed using a flat ferrite core and heavy Cu PCBs for primary and secondary windings. The planar transformer measures 5×2.5×0.78 in.

(a) Inverters

(b) Induction motor (c) PM motor

Figure III-45: Photos of Si-based traction drive inverters and motors used in the charger tests.
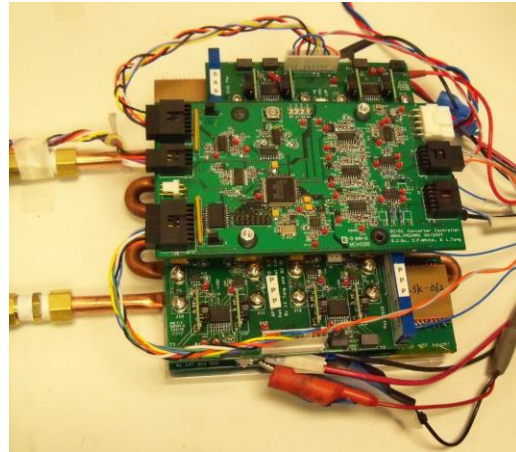
Figure III-46: Photo of the 5 kW charger dc-dc converter.
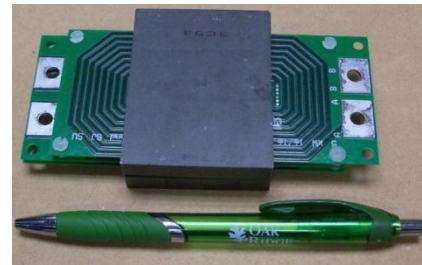
Figure III-47: Photo of the planar transformer (footprint: 5 by 2.5 in.).

Results

Battery ripple reduction control

Figure III-48 and Figure III-49 show simulated waveforms of the grid source voltage, battery charging current, and dc bus voltage in the selected topology shown in Figure III-43, with and without the battery ripple current reduction control. The control reduced battery ripple current by 60%, demonstrating the effect of the control strategy to use the isolation converter to reduce the bulky dc link capacitor.

Si-based isolation converter and charger system tests

The Si-based isolation converter prototype was first tested with a resistive load bank. Figure III-50 gives typical operating waveforms, in which V_{bat}, v_{Tr1}, v_{Tr2}, I_{bat}, i_{Tr1}, and I_{in} are output dc voltage, transformer primary voltage, transformer secondary voltage, output dc current, transformer primary current, and input dc current, respectively. Smooth transitions in the transformer voltage waveforms indicate soft switching operations. Figure III-51 plots measured isolation converter efficiency vs. output power. The efficiencies are greater than 97% for output power levels up to 5.2 kW, and the maximum value is 98.0 %.
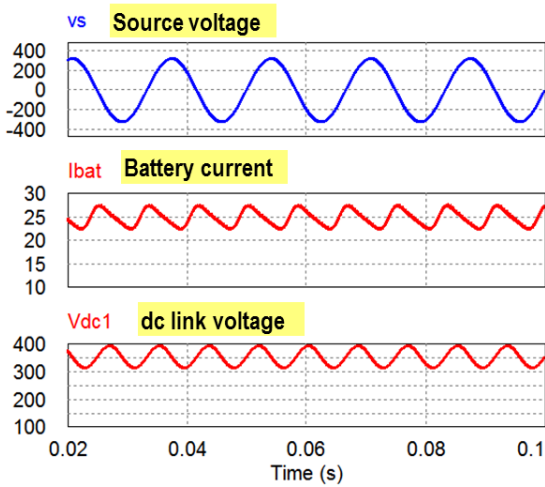
Figure III-48: Waveforms showing large ripple in battery current without ripple reduction control.
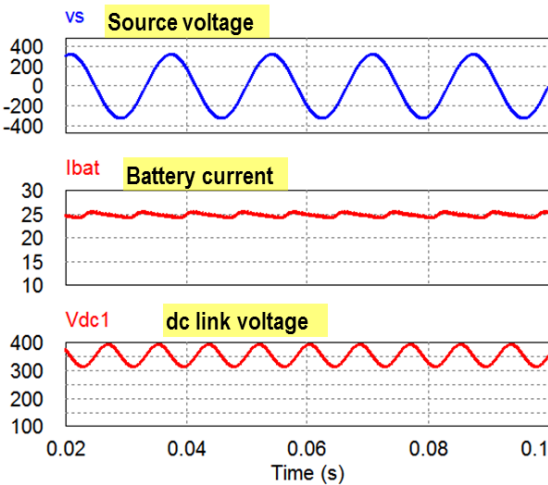
Figure III-49: Waveforms showing significant reduction of battery ripple current with the ripple reduction control.
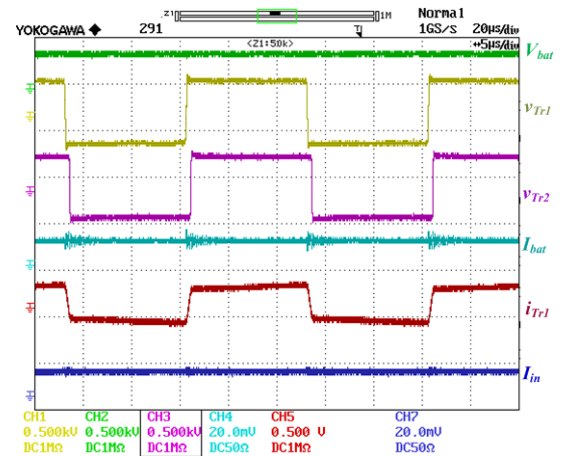
Figure III-50: Isolation converter operating waveforms showing, from top, output dc voltage, V_{bat}, 500 V/div; transformer primary voltage, v_{Tr1}, 500 V/div; transformer secondary voltage, v_{Tr2}, 500 V/div; output dc current, I_{bat}, 20 A/div; transformer primary current, i_{Tr1}, 25 A/div; and input dc current, I_{in}, 20 A/div.
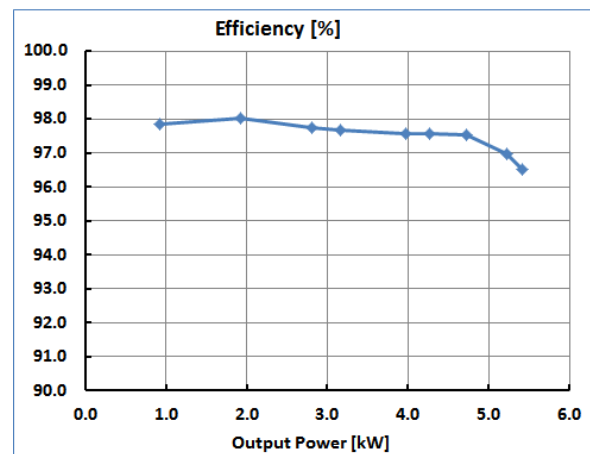
Figure III-51: Measured efficiency of the 5 kW Si-based isolation converter.

The isolation converter and the traction inverters and test motors were then combined to function as an OBC, and the whole charging system was successfully tested at both 120 and 240 V grid voltages. Figure III-52 shows typical operating waveforms of the system with a 120 V input voltage and 3 kW charging power.Figure III-53 illustrates waveforms of the system with a 240 V input voltage and 5 kW charging power. Figure III-54 plots the measured system efficiency of the charger at a grid voltage of 240 V. The maximum efficiency is 92.8%, which dropped to 90.0% at 120 V grid voltage. This efficiency reduction illustrates the impact of the Cu losses in the high-resistance test motors. It is thus reasonable to expect higher efficiencies for production EV/HEV motors, which have much lower stator winding resistances.
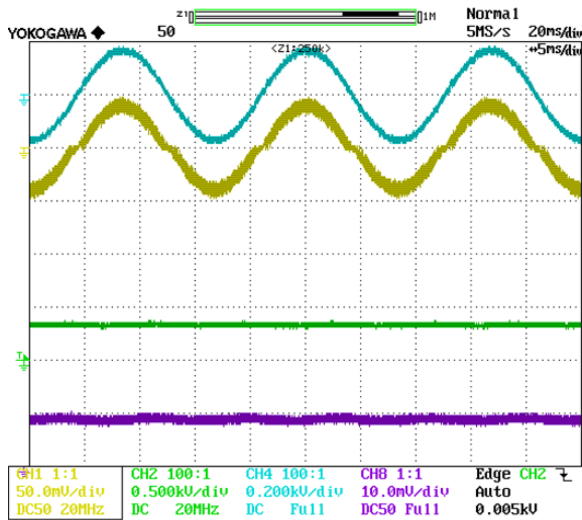
Figure III-52: Waveforms of the charger system with 120 V input and 3 kW charging power. From top, grid voltage (200 V/div), grid current (50 A/div), charging voltage (500 V/div), and charging current (10 A /div).
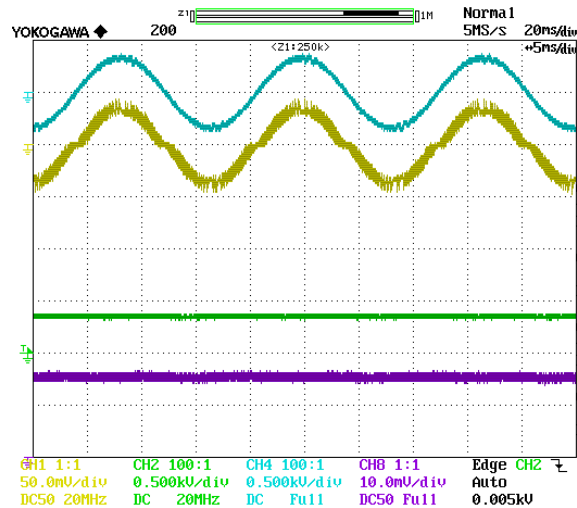
Figure III-53: Waveforms of the charger system at 240 V input and 5 kW charging power. From top, grid voltage (500 V/div), grid current (50 A/div), charging voltage (500 V/div), and charging current (10 A/div).
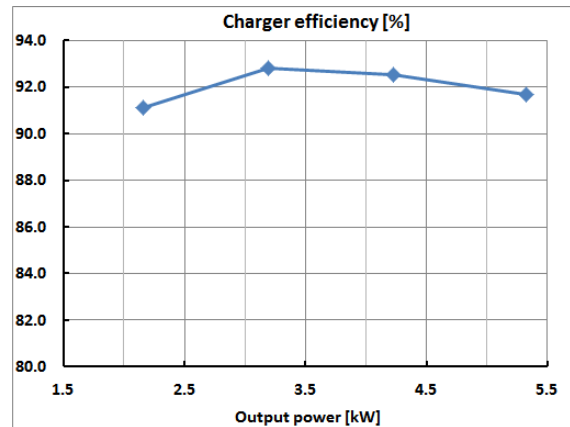
Figure III-54: Measured charger system efficiency at a grid voltage of 240 V.

GaN device tests

Several low-voltage (<200 V) eGaN switches made by EPC were tested and characterized for possible use in the 14 V dc-dc converter. Using evaluation boards, a test setup was assembled for testing the eGaN switches in different 14 V converter topologies, including synchronous buck, boost, and full bridge converters. Test results were incorporated into the GaN switch simulation model for the 14 V dc-dc converter. The resultant converter model should produce more accurate results, enabling use of the simulation results for iterations of converter design optimization while reducing the need for experimental verification.

Figure III-55 shows the EPC eGaN test setup and Figure III-56 shows typical EPC eGaN switching waveforms in a full-bridge dc-dc converter with 12 V output. Measured turn-on and turn-off times are 22 and 29 ns, respectively. A maximum efficiency of 94.7% was recorded at a switching frequency of 370 kHz with a resistor load.

Figure III-55: EPC eGaN test setup.

(a)

(b)

(c)
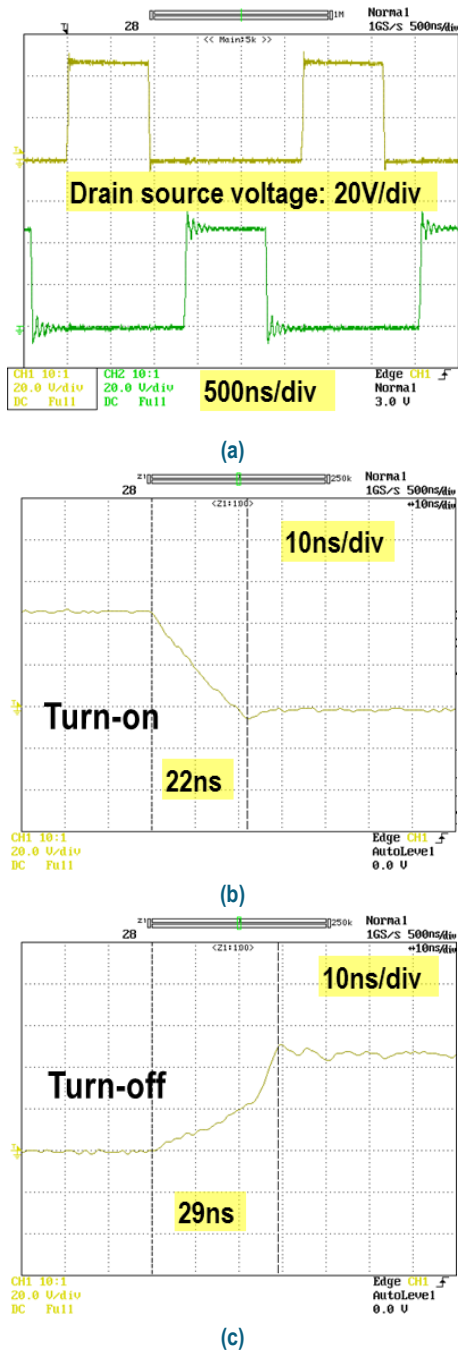
Figure III-56: EPC eGaN voltage switching waveforms in a full-bridge dc-dc converter.

IR 600 V GaN switches were tested and evaluated for use in the high-voltage charger converters. A test board (Figure III-57) for characterizing the IR GaN switches packaged by Delphi was designed and fabricated. The test setup (Figure III-58) is flexible and can be reconfigured for double-pulse tests to measure switching losses and test loads in a half-bridge configuration for efficiency measurement. The test circuit includes an SiC Schottky barrier diode (SBD) in parallel with each of the IR GaN switches. The IR devices are packaged in a cascade connection of a normally-on GaN high-electron mobility transistor (HEMT) fabricated on a Si

substrate and a low-voltage Si MOSFET, which makes them operate as normally-off switches.
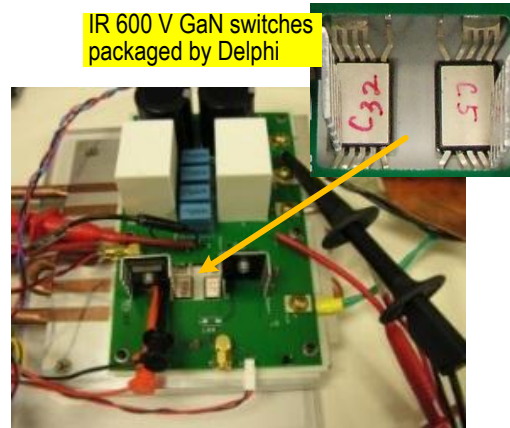
Figure III-57: IR 600 V GaN switch test board.
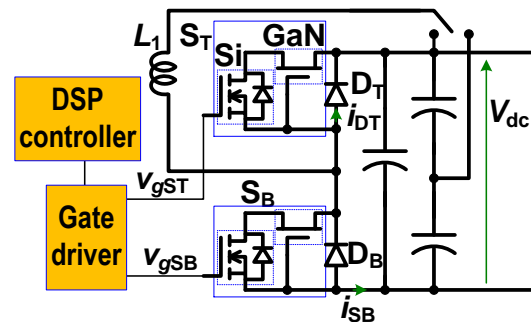
Figure III-58: IR 600 V GaN switch test circuit.

Double-pulse tests were first performed with the top switch, S_T, kept off or switched complementarily. Figure III-59 shows double-pulse test results with S_T kept off and V_{dc}=300 V. Measured switching losses are 91.6 µJ for turn-off and 17.35 µJ for turn-on. Figure III-60 shows double-pulse test results with S_T switched complementarily. Observing the diode current, i_{DT}, it is apparent that the GaN device can conduct current in the reverse direction at a lower voltage drop than the SiC diode. This indicates that the IR GaN switches can be used for synchronous rectification operation by turning on the switch while current is passing through the antiparallel SiC diode. The transition of current between the SiC diode and the GaN switch was also investigated for optimizing the gate control signals. The transitions took a rather long time, measured at about 500 ns.
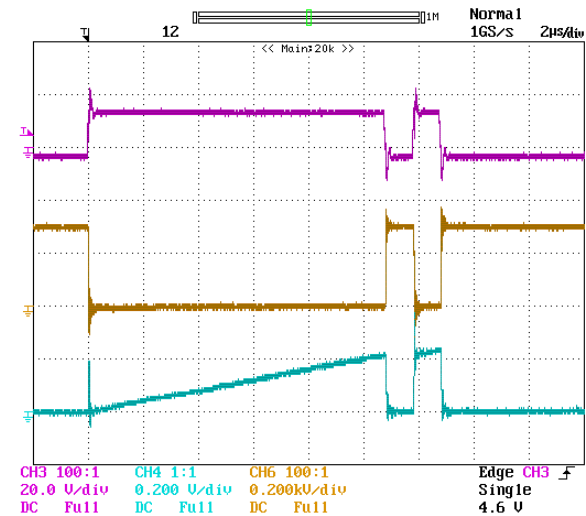
(a) Full test cycle waveforms
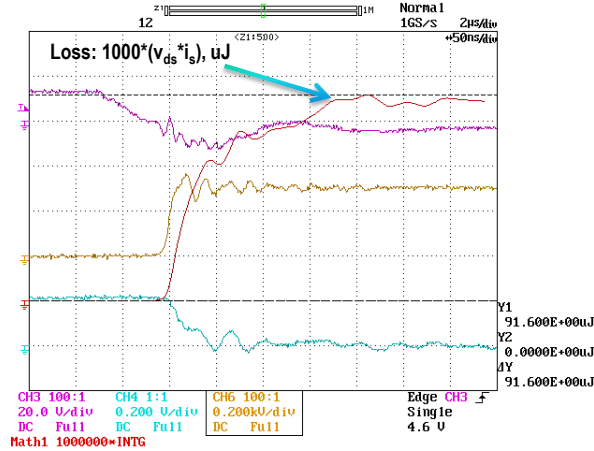
(b) Turn-off
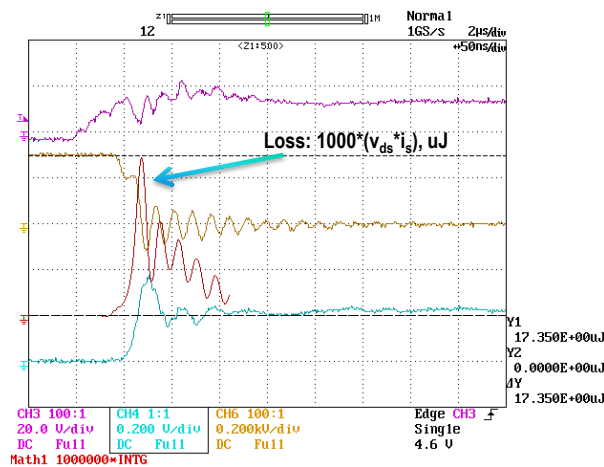
(c) Turn-on

Figure III-59: Double-pulse test results with S_T kept off. CH3: v_{gSB}, 10 V/div; CH4: i_{SB}, 10 A/div; CH6: v_{DSB}, 200 V/div; 2 us/div.
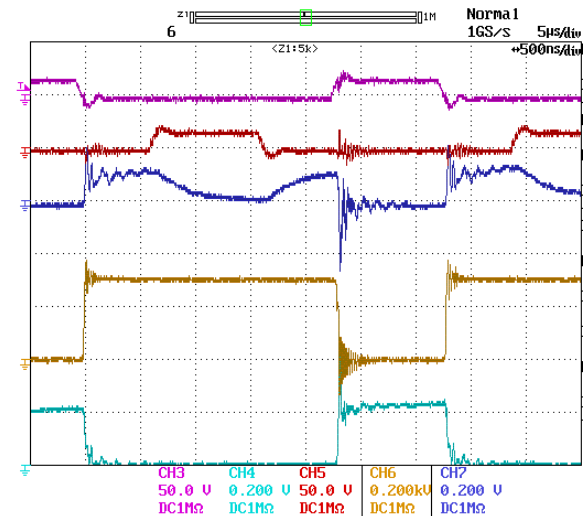
Figure III-60: Double-pulse test results with S_T switched complementarily. CH3: v_{gSB}, 50 V/div; CH4: i_{SB}, 10 A/div; CH5: v_{gST}, 50 V/div; CH6: v_{DSB}, 200 V/div; CH7: i_{DT}, 10 A/div; 500 ns/div.

After the double-pulse tests, further experiments were carried out by operating the IR GaN switches in a half-bridge inverter with an inductor load at a dc bus voltage of 300 V and switching frequencies of 100–300 kHz. Figure III-61 shows typical operation waveforms at a switching frequency of 300 kHz. Estimated efficiency is about 98% at an output power level of 1 kW.
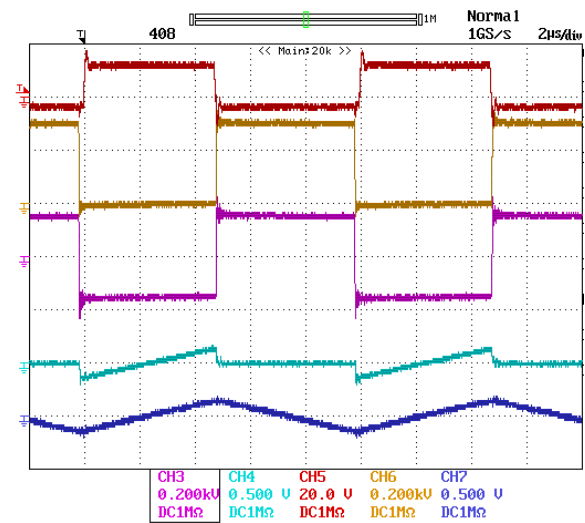
Figure III-61: IR GaN switch operation waveforms in a half-bridge inverter with an inductor load. CH3: v_{out}, 200 V/div; CH4: i_{SB}, 25 A/div; CH5: v_{gSB}, 20 V/div; CH6: v_{DSB}, 200 V/div; CH7: i_{L1}, 25 A/div; 2us/div.

SiC-based isolation converter design

SiC switch phase-leg modules rated at 1,200 V/100 A were fabricated on ORNL-designed DBC substrates using Cree SiC MOSFETs and SBDs (Figure III-62).

Incorporating the results from the simulation study, a power circuit design for a 6.6 kW isolation converter using the

ORNL-designed SiC phase-leg modules and planar ferrite cores was completed. Figure III-63 is a 3D drawing of the isolation converter design. It comprises a primary switch PCB and its gate driver board, a secondary switch PCB and its gate driver board, a 14 V converter board, a DSP control board (top), and a planar transformer assembly. All the components are mounted on a 7 by 5 in. heat exchanger. At a switching frequency of 200 kHz, the transformer core size was reduced by 50% and the power module footprint by 15%, compared with the Si-based 5 kW baseline; a high converter efficiency of 98% was maintained.

| (a) DBC card | (b) Assembled SiC MOSFET module |
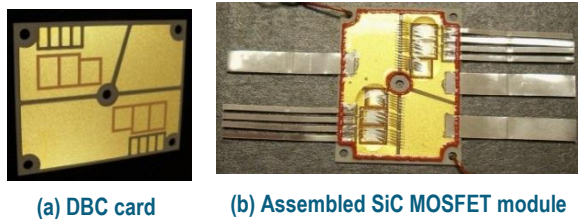
Figure III-62: DBC design and SiC switch phase-leg modules fabricated using the DBC cards.
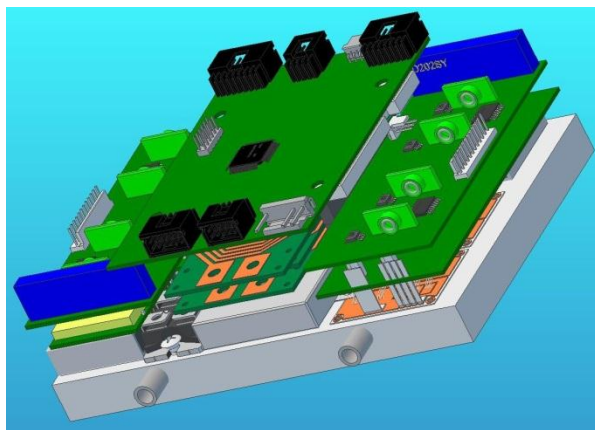
Figure III-63: Three-dimensional drawing of the SiC isolation converter design.

Conclusions and Future Directions

This project is aimed at leapfrogging existing Si-based charger technology to address charger and converter cost, weight, volume, and efficiency. It proposes to overcome the limitations of Si semiconductor and magnetic materials by using WBG devices, including SiC and GaN; using advanced magnetic materials; and employing a novel integrated charger architecture and control strategy.

ORNL has developed a new integrated OBC and dc-dc converter architecture that significantly reduces the number of components (power circuit components alone are reduced by 47%, not counting savings in gate driver and control logic circuits). ORNL has built and tested a 5 kW Si-based prototype demonstrating an isolation converter peak efficiency of 98% and charger peak efficiency of 93%. Test results validated the new integrated charger and dc-dc converter architecture and provide a baseline for measuring the benefits

of WBG counterparts. ORNL also developed a control strategy for the charger isolation converter to reduce the battery ripple current—twice the ac main frequency—inherent in single-phase ac-dc converters. Simulation results show the control strategy reduces the ripple current by 60%, enabling a corresponding reduction of the bulky dc link capacitor in the active front end converter.

Emerging GaN devices fabricated on Si substrates are poised to offer significant improvements in power converters at a cost comparable to Si device costs. Their enhanced switching speed and reduced switching and conduction losses may enable these switches to minimize passive component requirements, a major driver of cost, weight, and volume in charger and dc-dc converters. ORNL has characterized both low-voltage (<200 V) and high-voltage (600 V) GaN switches, which generated valuable design data for hardware development of OBCs and dc-dc converters.

Incorporating the simulation results, ORNL completed a power circuit design for a 6.6 kW isolation converter using the ORNL-designed SiC phase-leg modules and planar ferrite cores.

Future work will be directed at building and testing prototypes for a 6.6 kW SiC isolation converter and OBC, a 6.6 kW GaN isolation converter and OBC, and a 2 kW GaN 14 V converter.

FY 2013 Publications/Presentations

1. G.J. Su, "WBG dc-dc and on-board charger," presented at the DOE Vehicle Technologies Program Advanced Power Electronics and Electric Motors R&D FY 2013 Kickoff Meeting, November 13–15, 2012.

2. G.J. Su, "WBG converters and on-board charger," presented at the 2013 DOE Hydrogen and Fuel Cells Program and Vehicle Technologies Program Annual Merit Review and Peer Evaluation Meeting, May 13–16, 2013.

3. G. J. Su and L. Tang, "An integrated onboard charger and accessory power converter for plug-in electric vehicles," 5th *IEEE Energy Conversion Congress and Exposition (ECCE 2013)*, pp. 1592–1597, September 15–19, 2013.

III.4. Power Electronics and Regenerative Energy Storage Systems Matching

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Start Date: October 2012
Projected End Date: September 2013

Objectives

- Develop a bi-directional buck-boost dc-dc converter between the RESS and the dc link (traction drive inverter input)
- Review and analyze bi-directional dc-dc converter architectures
- Model, simulate, and analyze a battery/ultracapacitor (UC) hybrid energy storage system (ESS)

Technical Barriers

The most important barrier is the boost ratio/range and efficiency that drive dc-dc converter architectural choices. A bi-directional dc-dc converter architecture should be selected depending on the difference between the battery voltage and the reference traction drive inverter voltage. Passive components of a dc-dc converter should be sized to keep the cost low and power density high with respect to the DOE VTO goals. Another significant barrier is the potential cost added by the dc-dc converter and hybrid ESSs. For example, in a battery/UC hybrid ESS, the UC increases the cost; however, it also reduces the battery size and prolongs its lifetime. These advantages are a tradeoff for the up-front cost of the UC.

Technical Targets

- Achieve power density of more than 13.4 kW/L
- Achieve specific power of more than 14.1 kW/kg
- Achieve a service life of more than 15 years or 13,000 h

Accomplishments

- Reviewed, modeled, and simulated bi-directional dc-dc converter architectures that interface the RESS with the traction drive inverter and created a summary review report discussing the operating principles, controls, advantages, and drawbacks of these converter architectures
- Reviewed and analyzed hybrid RESS architectures and created a summary report based on the advantages, drawbacks, control systems, performance, number of components, and other characteristics
- Reviewed, analyzed, modeled, and simulated four battery/UC hybridization strategies
  - Built simulation models of the battery and UC
  - Modeled hybridization architectures
  - Simulated a representative portion of the Urban Dynamometer Driving Schedule (UDDS) that includes acceleration, braking, and idling conditions for t = [690, 760] for these hybridization architectures
  - Collected data and compared the simulation results
  - Created a comparison results table for the RESS hybridization architectures

✧   ✧   ✧   ✧   ✧

Introduction

To provide more efficient propulsion without sacrificing performance or increasing fuel consumption, more than one energy storage device, each with different power/energy characteristics, can be used in PEVs. In such a system, proper power budgeting, based on the specific characteristics of energy sources, should result in higher efficiency, longer life and reduced wear on energy sources, and overall size and cost reduction. The combination of energy sources should be able to store, supply, and recapture high-power pulses in a typical or worst-case drive cycle, as well as supply the steady demands of the car. A hybrid architecture composed of a high-power-density component such as a UC and a high-energy-density component such as a rechargeable battery offers the advantages of both.

The energy storage devices in EVs should be able to meet demands the vehicle may encounter under any condition. Rechargeable chemical batteries are the traditional energy storage source for EVs. However, since the source needs to supply the peak power demands of the traction motor during transients and rapid accelerations, and since existing technologies do not provide a battery with sufficiently high power densities, the size and cost of the battery pack significantly increase if it is required to supply all the load demands.

A PEV traction battery may be sized to successfully meet the energy capacity needs for a given single-charge travel distance requirement. But since the present generation of highly energy-dense lithium-ion batteries has a relatively low power density, this single power source may not be capable of sourcing or sinking large, short bursts of acceleration or regenerative braking energy. Moreover, battery longevity is directly related to both the depth of discharge and the quantity of micro or macro charge/discharge cycles, i.e. the short, powerful charge/ discharge cycles associated with sharp acceleration and hard regenerative braking. Battery C-rate is the parameter that expresses battery discharge intensity; in a battery-powered system, because low C-rates tend to increase battery life span, instantaneous charge/discharge pulses or fast fluctuating currents should be avoided. The problems associated with cycling batteries at high C-rates include decreased capacity, excessive heating (which requires additional cooling), and increased dc resistance (ESR). Capacity and ESR are the metrics used to define battery performance and therefore end of life.

Without a secondary ESS, the battery pack must supply all vehicle power demands. The result may be an oversized system with massive energy density to compensate for power density shortcomings. This may increase the size and cost of the battery pack or, if a smaller pack is used, shorten the battery lifetime and cause thermal runaway problems. For this reason, UCs are proposed, because of their higher specific power and cycling efficiency, to relieve peak power transfer stresses on the battery bank. A hybrid system combining these two energy sources, batteries and UCs, can not only better meet both the energy and power requirements of the drive train but also provide the flexibility of using smaller batteries with less peak output power. Because of their very low internal resistances, UCs have very small time constants and can deliver high-power charge and discharge pulses for relatively short durations. The manufacturer performance ratings for certain UCs state a 20% decrease in initial capacitance and doubling of internal resistance over a period of 1,000,000 cycles. Curves showing whether this wear and tear is linear or nonlinear over time are not provided, but it is not likely that a system with a 1,000,000 cycle rating would see serious degradation for a substantial length of time or energy throughput.

Employing UCs with batteries in a proper, efficient, and cost-effective manner can increase the peak current capacity of the overall architecture. Therefore, the hybrid architecture could benefit from intermediate storage of high power in a buffer stage designed to deliver or receive current for the highest peaks, thus reducing both the number and the depth of battery discharge cycles.

Approach

This section reviews and describes hybrid battery/UC architectures.

Passive parallel hybrid architecture

In the passive parallel configuration, the battery and UC are connected directly in parallel without any interfacing converter. Combining two power sources passively in parallel is the simplest method, as the output voltages of both sources are automatically equalized by virtue of being directly connected to the same bus. The passive parallel connection architecture is shown in Figure III-64 with the bi-directional converter interfacing the common ESS bus to the dc link and motor drive. Since the converter is operated to provide a constant input voltage to the dc link /motor drive, increasing the mechanical load on the machine will tend to increase the motor current, decreasing the dc link voltage. This will cause more power to be drawn from the ESS through the bi-directional converter to return the dc link to its nominal voltage. On the other hand, whenever braking occurs, the motor drive operates as a generator and recaptures the braking energy to the dc link. Therefore, dc link voltage increases during braking or a reduction in mechanical load, and the bi-directional converter is operated in reverse (from dc link to ESS bus) to regulate the dc link voltage.

This architecture provides simplicity and cost effectiveness for hybrid ESSs. In this connection architecture, it is expected that the UC will act faster than the battery because of its lower time constant. Therefore, it is anticipated that the UC will provide transients and fast power variations while the battery supplies a relatively slow varying current as a result of its slower dynamics.
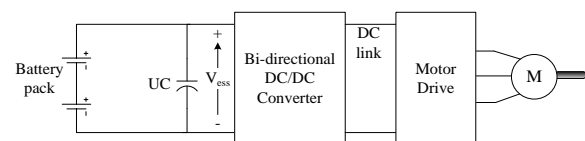
Figure III-64: Passive parallel connection architecture.

However, immediately after current is drawn from the UC, because the UC and battery are directly connected, the battery will supply a similar current profile for voltage equalization, since there is no active battery current waveform shaper, limiter, or controller. The lack of effective control of battery current presents a drawback to the passive parallel connection architecture. In addition, the nominal battery and UC voltages must be sized to match, further restricting the system configuration.

Ultracapacitor/battery cascaded hybrid architecture

The most common UC/battery configuration connects the UC terminals to the dc link through a bi-directional dc-dc converter. In this architecture, the battery is directly connected to the dc link and a bi-directional interface is used for UC connection (Figure III-65). Figure III-66 shows another common view of the same connection architecture. In this case, the power contribution from the UC can be effectively controlled, and the bi-directional dc-dc interface helps to

efficiently and more completely recapture braking energy. Moreover, a UC voltage can be selected that is different from the nominal dc link voltage. This allows the UC energy capacity to be increased or decreased regardless of the system dc voltage, as UC energy capacity varies by the square of its voltage. Since the battery is directly connected to the dc link, input voltage to the motor drive is relatively constant and further dc-link voltage regulation is not required. This provides simplicity of control so that voltage control loops may be eliminated.
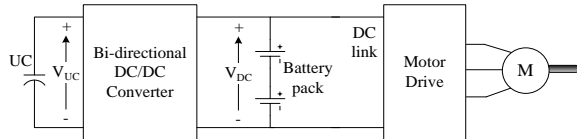
Figure III-65: Ultracapacitor/battery configuration.
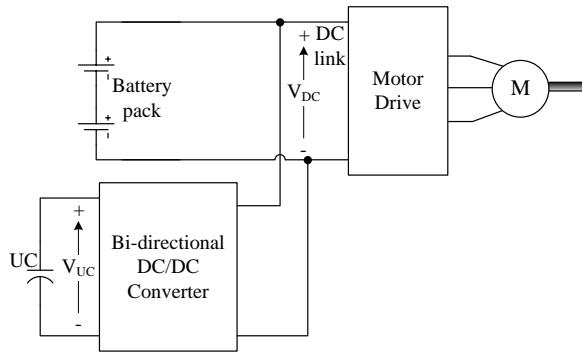
Figure III-66: Another representation of the same ultracapacitor/battery configuration.

The disadvantage of this architecture is that the braking energy captured by the battery is not directly controlled. Braking energy recovered by the battery depends on the power level, battery state of charge (SoC), and amount of energy captured by the UC. The other drawback is that the bi-directional dc-dc converter must operate properly even with low UC voltages and therefore higher current values, so current ratings of the switches and other PE should be chosen appropriately.

Battery/ultracapacitor hybrid architecture

For the battery/UC architecture shown in Figure III-67, the device positions are simply switched compared with the UC/battery configuration.
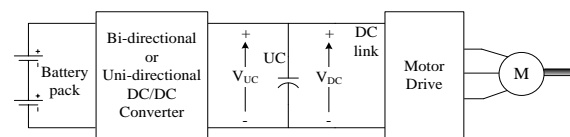
Figure III-67: Battery/ultracapacitor architecture.

The main advantage of this architecture is that the battery voltage can be maintained at a lower level. During braking, the UC is recharged directly from the dc link; and some portion of the braking energy, appropriately current-limited, can be transferred to the battery. Since the UC is directly connected to the dc link, it acts as a low-pass filter and takes care of fast load transients. However, the battery pack should be

controlled so that it continually maintains an appropriate voltage across the UC and dc link. The control strategy for the battery pack may be designed so that it supplies the average and slow-changing load variations while the UC supplies the rest, acting as a buffer with faster dynamics. If the UC is not large enough or charged continually, the dc link voltage will be allowed to fluctuate over a wide range; in this case, the motor drive inverter should be capable of operating over a large input voltage range.

In this architecture, for simplicity and cost effectiveness, the battery pack converter can be unidirectional. Since the overall system is that of a PEV, the battery pack can be configured to receive a charge only from an onboard generator or an external source. The UC can be the only device responsible for capturing braking energy. This scheme would provide a significant amount of simplicity for power budgeting during braking.

Cascaded hybrid architecture with two converters

As another alternative, one energy storage device can be cascaded to the motor drive through a dc-dc converter and the other cascaded through a first and second dc-dc converter. The cascaded converters configuration is presented in Figure III-68.
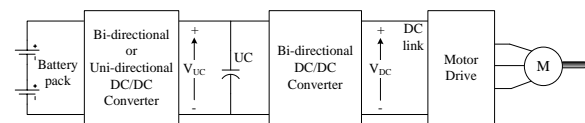
Figure III-68: Cascaded converters configuration.

In this configuration, both battery and UC voltages can be decoupled from the system voltage and from each other. It is preferred that the battery converter control the battery output current and therefore the stress on the battery. If the UC is undersized or the battery converter not appropriately controlled, the UC voltage can vary substantially. At low UC voltages, the input current to the UC converter can be very high, leading to higher conduction losses and a need for switches rated for high current. Additionally, the UC dc-dc converter must provide stable operation over a wide voltage input range.

The major disadvantage of the cascaded converter architecture is that additional losses may be encountered at the battery power flow path because there are two cascaded converters between the battery and dc link. The battery converter can again be a unidirectional converter for control and configuration simplicity. In the case of a boost converter for the battery, the battery power contribution can be controlled easily by current control mode. The UC converter can be controlled for dc link regulation, and the battery can be controlled so that it supplies a smoother current profile during the operation.

As in the battery/UC architecture shown in Fig. 4, the positions of the battery and UC can be switched, leading to a slightly different cascaded converters architecture. However in this case, the power contribution from the UC might result in more fluctuation voltage applied to the battery terminals. On the other hand, since the battery is the dc link–side energy

storage device, dc link voltage regulation could be easily accomplished by the use of a nearly constant battery voltage.

Multiple parallel converters hybrid architecture

In a multiple parallel converter architecture, each energy storage device has its own bi-directional dc-dc converter for interfacing with the dc link, and the output of all converters is held in parallel. A block diagram of this architecture is shown in Figure III-69.
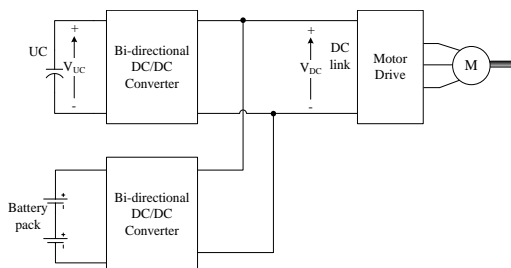
Figure III-69: Multiple parallel connected converters architecture.

Although this architecture is called a multiple input converter, it is not a "true" multiple input converter since each energy storage device has an individual converter and their contributions to the dc link are paralleled. This architecture offers the most flexibility and offers more functionality than the cascaded converters architecture. The battery and UC voltages are decoupled from each other as well as from the dc link voltage. Since the power controls and power flow paths from the energy storage devices are totally decoupled, this architecture is superior in terms of stability, efficiency, and control simplicity. Reliability is also improved because one source can keep operating even if another fails.

The battery can be operated in current control mode, supplying the load variations averaged and smoothened over a period of time. Meanwhile, the UC can be operated in voltage control mode, maintaining a nearly constant voltage across the dc link. Therefore, the UC will supply fast load variations and transients during both rapid acceleration and sudden braking. This is because these load activities directly affect the dc link voltage, and as long as dc link voltage is regulated quickly enough, all load demands will be satisfied.

The bi-directional dc-dc converters discussed for the architectures described in this section could be typical two-quadrant converters, able to operate in boost mode in one direction and buck mode in the other (Figure III-70). This architecture is also called a half-bridge bi-directional dc-dc converter.
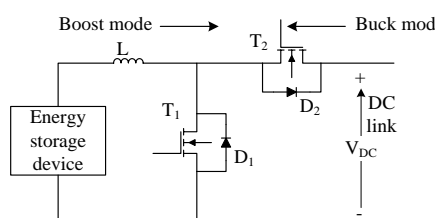
Figure III-70: Bi-directional dc-dc converter.

As shown in Figure III-70 for power flow from an energy storage device to the dc link, inductor L, switch T_1, and diode D_2 form a boost converter. To accommodate power flow from the dc link to an energy storage device, switch T_2, diode D_1, and inductor L form a buck converter. Of course, other types of bi-directional converters could also be used. Some of them are presented in the following subsections.

Multiple dual active bridge converters hybrid architecture

It is known that conventional buck-boost converters can step the source voltage up or down at the cost of inducing a negative voltage output. Therefore, an inverting transformer is usually employed to obtain a positive output voltage. Although the transformer adds cost and volume, it may be advantageous when there are two input sources for both isolation and coupling. Two buck-boost type dc-dc converters for the UC and battery can be combined through the magnetic coupling of a transformer reactor. However, neither conventional buck-boost nor buck-boost with transformer architectures is suitable for vehicle propulsion systems because they are not capable of bi-directional operation. On the other hand, dual-active-bridge dc-dc converters can be employed for the combined operation of batteries and UCs. Although transformers typically add cost and volume to a system, the transformer in the dual-active-bridge converter operates at very high frequency and may therefore be very small and cheap. Having a transformer in the converter architecture may be advantageous when there are two or more input sources because they can be combined through the magnetic coupling of a transformer reactor. A dual-active-bridge converter with two input sources is presented in Figure III-71. Although this architecture completely isolates the input sources from the dc link, it requires a greater number of switches at increased cost. If only isolation is required, the number of switches can be reduced by employing half-bridge inverters/rectifiers instead of full-bridge versions. This dual-active bridge architecture with half-bridge converters would cut the number of switches in half (Figure III-72).
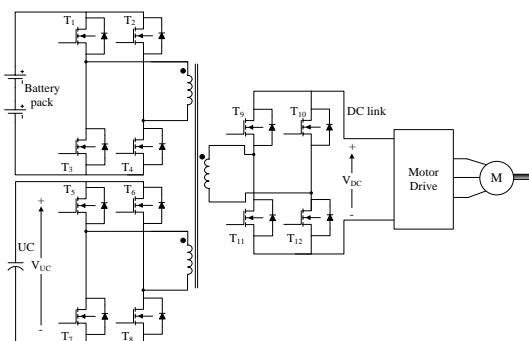
Figure III-71: Dual-active-bridge converter with full-bridge converters.
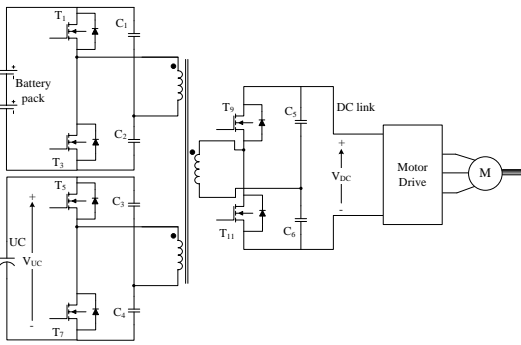
Figure III-72: Dual-active-bridge converter architecture with half-bridge converters.

Dual-source bi-directional converters

In the multiple converters configuration discussed earlier, each converter shares the same output and so the combination of converters occurs at the output. A dual-source bi-directional converter configuration applies the combination at the input, instead of paralleling the converter outputs at the dc link. This configuration is presented in Figure III-73.
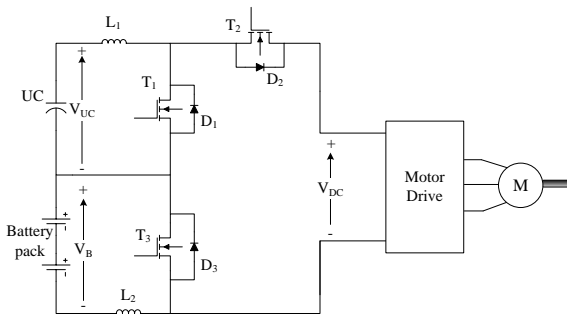
Figure III-73: Dual-source bi-directional converters architecture.

Although this architecture is similar to a multiple parallel-connected converter configuration, there is one less switch in the dual-source input case. For the UC, inductor L_1, switch T_1, and diode D_2 form a boost converter when transferring power from the battery to the dc link. For the battery, inductor L_2, switch T_3, and D_1-D_2 path form a boost converter when transferring power from the UC to the dc link. During regenerative braking, the interface should be operated in buck mode. Switch T_2, diode D_1, and inductor L_1 form a buck converter from the dc link to the UC. On the other hand, some regenerative braking energy can be conveyed to the UC by applying a PWM signal to T_1. In this case, switches T_2 and T_1, diode D_3, and inductor L_2 will form a buck converter from the dc link to the UC. By applying an appropriate duty cycle to T_1 and T_2, braking energy can be properly shared. Although one switch is eliminated, a complicated control system is the main drawback of this configuration compared with the multiple converter configuration.

Multiple modes single converter hybrid architecture

In this design, only one bi-directional converter is required, and the UC voltage is selected to be higher than the battery voltage. The UC is directly connected to the dc link to supply peak power demands, and the battery is connected to the dc

bus through a diode. The bi-directional dc-dc converter is connected between the battery and UC (Figure III-74) to transfer power between them. This converter is controlled to maintain a higher voltage across the UC than the battery; therefore, the diode is reverse-biased for most of the operation.
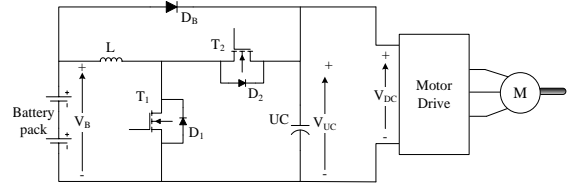
Figure III-74: Single bi-directional converter architecture.

This converter has four different modes of operation: low-power, high-power, regenerative braking, and acceleration.

In low-power mode, it is assumed that the total power demand is less than the power capacity of the bi-directional converter. In this mode, since the UC/dc link voltage is higher than the battery voltage, the diode D_B is reverse-biased. Since the power demand is lower than the capacity of the bi-directional converter, there is not any power flow from the battery to the dc link. The battery only supplies power to the UC to keep its voltage at some pre-determined higher level.

Whenever the power demand of the vehicle is greater than the converter power capacity, the system operates in high-power mode. In this mode, the UC voltage cannot be maintained at that high value since the power from the battery to the UC is less than the power from the UC to the dc link. In this case, diode D_B is forward biased, and battery also directly supplies power to the dc link along with the UC.

In regenerative braking mode, since the UC is directly connected to the dc link, it is recharged by virtue of its position in the circuit, whereas diode D_B blocks the dc link power to prevent recharging of the battery directly. Some portion of the recaptured braking energy can be transferred to the battery through the bi-directional converter. Therefore, this mode provides controlled recharging for the battery; i.e., whenever the UC is fully charged but there is still regenerative energy available, the rest of the energy can be transferred to the battery so long as the regenerative current does not exceed the maximum battery charging current. In the latter case, mechanical brakes could be used to keep the battery current below the maximum limit.

When the vehicle first starts to accelerate, the voltage across the UC is higher than that of the battery and equal to that of the dc link. Power demand on the vehicle is high, and UC voltage therefore drops. During acceleration mode, the UC discharges through the dc link, and the battery supplies power to the dc link through the bi-directional converter. Whenever the dc link voltage decreases to the level of the battery voltage, D_B becomes forward biased and the system switches to high-power mode.

The advantage of this architecture is that it requires only one converter. However, although power is shared between the battery and UC during different modes, the battery current

is not effectively controlled. This is especially the case in regenerative mode, with its potentially sharp transients.

Interleaved converter hybrid architecture

The combination of battery and UC can also be achieved by using interleaved converters. The interleaved converter configuration is composed of a number of switching converters connected in parallel as shown in Figure III-75.
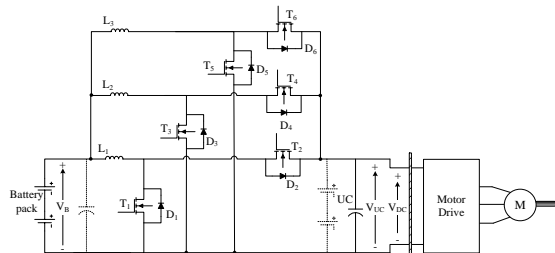
Figure III-75: Parallel interleaved three-stage bi-directional converter.

When low current ripples or very tight tolerances are required, interleaved converters tend to be preferred. Interleaved converters offer much lower inductor current ripple compared with regular bi-directional converters, and the overall efficiency for a given power requirement is greater because each interleaved architecture has a smaller power rating and smaller overall loss. Interleaved converters also have faster transient response to load changes.

As shown in Figure III-75, the battery is interfaced to the UC terminals through the interleaved converters, with the UC directly connected to the dc link. Alternatively, UC and battery positions can be reversed as shown by the dashed lines in Figure III-75. In addition to these two configurations, the interleaved converters can be employed within other architectures presented in this section.

Switched capacitor converter hybrid architecture

Another bi-directional interface that combines battery and UC operation in a PEV is the switched capacitor converter (SCC). An SCC is basically a combination of switches and capacitors. By different combinations of switches and capacitors, these converters can produce an output voltage that is higher or lower than the input voltage. In addition, reverse polarity at the output can be provided if necessary. The capacitor can be charged or discharged through various paths formed by the controlled switches. Four switches, three diodes, and one switched capacitor can be used for a typical SCC. SCCs can have a large voltage conversion ratio with very high efficiency; therefore, they appear to be well suited for automotive applications.

An example of a battery/UC combination through an SCC is provided in Figure III-76.
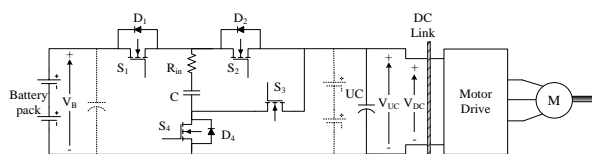
Figure III-76: Switched capacitor converter configuration.

Based on the circuit configuration shown in Figure III-76, battery energy can be delivered to the load side by buck mode operation and the battery can be recharged by boost mode operation. In buck mode, switches S_1 and S_4 are turned ON until capacitor C is charged to some desired voltage level less than that of the battery. At that point C is disconnected from the battery terminal by turning switches $S1$ and $S4$ OFF, and connected to the load by turning switch $S2$ ON to transfer its stored energy through S_2 and diode D_4. In boost mode, C can be charged from the load side through D_2 and S_4. After this stage, S_3 and D_1 become the operating switches and the energy in C is discharged to the battery side. This control strategy offers control simplicity, continuous input current waveform in both modes of operation, and low source current ripple.

As shown in Figure III-76, the battery is interfaced to the UC terminals through the SCC, and the UC is directly connected to the dc link. Alternatively, UC and battery positions can be reversed, as shown by the dashed lines in Figure III-76. In addition to these two configurations, the SCC can be employed within other architectures as a bi-directional converter.

Multiple input converter–based hybrid architecture

In the architectures discussed previously, battery and UC energy storage devices were employed through their individual dc-dc converters. Unlike these configurations, the multiple input dc-dc converter has the flexibility of adding a number of inputs at the added cost of one switch and one diode (two switches and two diodes in the case of bi-directional operation). The multiple input dc-dc converter architecture schematic with battery and UC input sources is shown in Figure III-77.
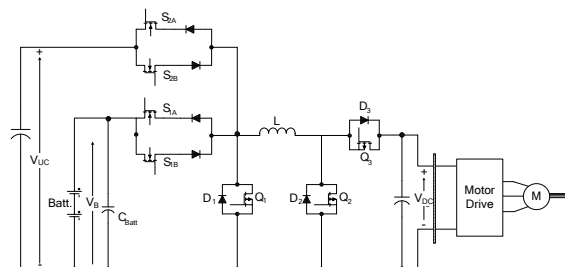
Figure III-77: Multiple input dc-dc converter architecture.

In this converter architecture, the inputs share the same converter inductor and are connected through bi-directional switches. This converter is capable of operating in buck, boost, and buck-boost modes for power flow in both directions. The assumption of continuous inductor current requires that at least one input switch or diode be conducting at all times. The respective input diode is ON if all the input switches are OFF. If more than one switch is turned ON at the same time, the inductor voltage equals to the highest input voltage.

Under acceleration conditions, both sources deliver power to the dc link. Since the UC voltage varies in a wider range than that of the battery, battery voltage can be selected to be higher than UC voltage for simpler operation. Since the battery voltage is higher, S_{2A} is turned ON in boost mode. Switch Q_2

can be switched to control the inductor current, and power flow from the battery to the UC can be controlled by switch S_{1A}. Diode D_3 conducts when Q_2 is turned OFF. During deceleration, the braking energy is transferred from the dc link to the energy storage devices, and the converter is operated in buck mode. Since the UC voltage is less than the battery voltage, S_{1B} is always turned ON. Switch Q_3 can be used to control the inductor current. Power sharing between inputs is accomplished by controlling S_{2B}. Diode D_2 cannot conduct until switch Q_3 is turned OFF.

The main advantage of this architecture is that only one inductor is required for the whole converter even if more inputs are connected. This advantage can decrease the volume and weight of the converter significantly compared with multi-inductor or transformer architectures. Conversely, power budgeting in both boost and buck modes is very challenging and requires advanced control design.

Results

Three example hybridization architectures for the combined operation of batteries and UCs were modeled and simulated: (1) a passive parallel configuration architecture, (2) a battery/UC cascaded connected converters architecture, and (3) a parallel connected multi-converters configuration. The following discussion makes a case for the effectiveness and feasibility of each one. For the simulations, a representative portion of the UDDS was used for the time interval t=[690, 760]. This driving cycle period of 80 seconds includes acceleration, braking, and idling conditions. A typical mid-size electric vehicle was used for the analysis. For the UC, a Maxwell BMOD0165 module was used with a nominal capacitance of 165 F, rated voltage of 48.6 V, equivalent series resistance of 6.3 mΩ, and peak current of 1970 A. Since one of the test architectures calls for a passive-parallel connection, the UC voltage should be chosen so that it is close to the battery voltage. Therefore, seven BMOD0165 modules were connected in series, resulting in 23.57 F capacitance, 340.2 V rated terminal voltage, and 44.1 mΩ of internal series resistance.

Simulation and analysis of passive parallel configuration

In this configuration, the battery and UC are connected directly in parallel without any interfacing converter between them, and the common battery/UC terminals are connected to the dc link through a bi-directional converter. The power demand for the vehicle was obtained through PSAT (Powertrain System Analysis Toolkit) simulations of a typical mid-size sedan vehicle configured as a PEV. Since the motor drive voltage is almost constant, the power demand of the vehicle can be divided by the dc link voltage to obtain the motor drive current; and the motor drive and load demand variation were therefore modeled and implemented as a controlled current source.

During the simulation, the reference dc link voltage was selected as 400 V, and the bi-directional converter was controlled through a double-loop voltage and current controller. A PI controller was used in the voltage loop, and a

peak current mode controller was used in the current loop (Figure III-78).
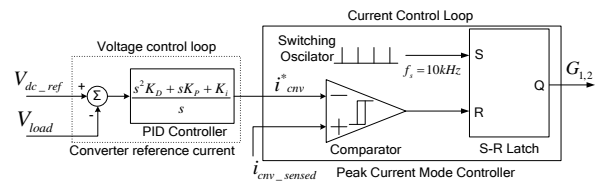
Figure III-78: Control system for the passive parallel connection architecture.

The load current for the t=[690, 760] time interval varies, as shown in Figure III-79. The load current includes positive and negative current variations, simulating acceleration and braking conditions. Based on this load current variation, the bi-directional converter is controlled so that it maintains a constant dc link voltage while supplying power from sources during acceleration and recharging them during braking. The battery and UC current variations are shown in Figure III-80 and Figure III-81, respectively.
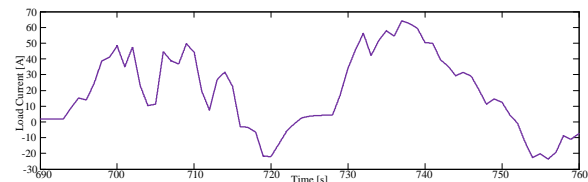
Figure III-79: Load current variation.
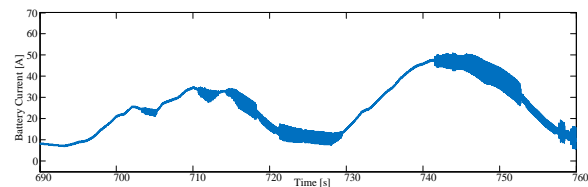
Figure III-80: Battery current variation in passive parallel configuration.
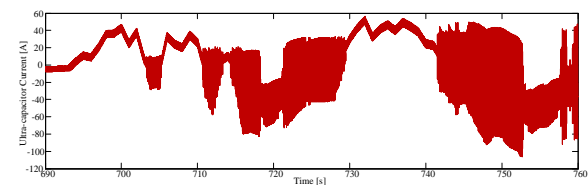
Figure III-81: Ultracapacitor current variation in passive parallel configuration.

The battery inherently supplies a smoother current profile than does the UC because of its slower dynamics. However, since no interface controls the battery current, its current has some fluctuations that could likely be eliminated by other connection architectures. Because of the voltage balance between the battery and UC, battery current varies automatically to maintain a terminal voltage similar to that of the UC at all times. If the UC voltage were higher than the battery voltage as a result of a large braking energy recovery, the battery current would reverse direction; but here only the UC receives power from the application of regenerative braking.

The SoC variations of the battery and UC are shown in Figure III-82 and Figure III-83, respectively.
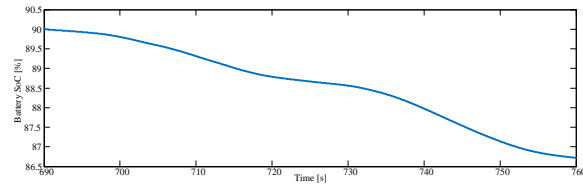
Figure III-82: Battery SoC for passive parallel configuration.
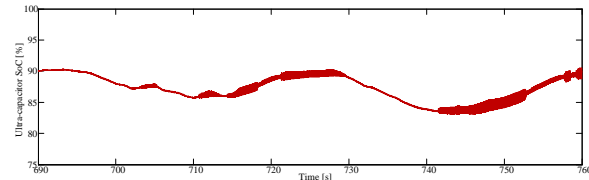
Figure III-83: Ultracapacitor SoC for passive parallel configuration.

The initial SoCs for both battery and UC were selected as 90%. Since the battery voltage is higher than the UC voltage, the battery is always discharging, as was explained for the current variations. However, the SoC of the UC is sometimes increasing as it recharges during braking conditions, i.e., the negative current variations of the UC.

Finally, the dc link voltage variation, to which the motor drive inverter is connected, is shown in Figure III-84. As observed from Figure III-84, the dc link voltage varies steadily around the 400 V reference set point. During periods of high power demand and the operation mode changes of the bi-directional converter, voltage fluctuations increase. For this architecture and control strategy, the maximum voltage seen at the dc link is 405.3 V and the minimum is 395.2 V. Therefore, the maximum amplitude of the voltage fluctuation is 2.5% over the simulation period.
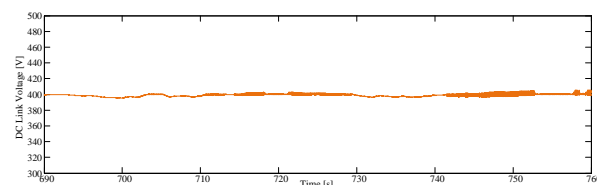
Figure III-84: The dc link (load bus) voltage variation for the passive parallel configuration.

Simulation and analysis of cascaded converters configuration

In the cascaded converter configuration, the battery is connected to the UC through a bi-directional converter, and the UC is connected to the dc link through another bi-directional converter; therefore, the battery, converter 1, UC, and converter 2 are all in cascade connection. The same drive cycle over the same time interval used in the previous simulation was used for load modeling of this architecture. The dc link voltage reference was kept at 400 V. For the UC controls, a double-loop controller was employed for dc link voltage regulation; for the battery controls, only a peak current mode controller was used. The reference current for the battery can be obtained as where I^*_{batt} is the battery

$$I^*_{batt} = \frac{V_{load} \times I_{load}}{V_{batt}} G_{LP}(s)$$

reference current, V_{load} and I_{load} are the instantaneously measured dc link voltage and current, and V_{batt} is the battery terminal voltage, which is nearly constant during the whole drive cycle. The transfer function represented by $G_{LP}(s)$ is a low-pass Bessel filter that is applied to eliminate any spikes and fast transients from the battery reference current. A Bessel filter is a linear filter with maximally linear phase response and minimal flat group delay; it is characterized by almost constant group delay across the entire passband, thus preserving the waveform of the filtered signals with minimal delay. These fast transients come inherently from the variation in instantaneously measured load current. The Bessel filter can make the battery current smoother and reduce the stress on the battery because there is an additional converter regulating battery current. The battery current controller is depicted in Figure III-85.
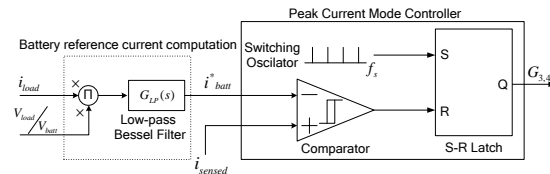
Figure III-85: Battery current controller.

The load current drawn from the dc link varies as is shown in Figure III-79, and vehicle specifications and battery and UC parameters are the same as in the previous example. Based on this load current variation, the UC's bi-directional converter is controlled so that it maintains a constant dc link voltage. The bi-directional converter connected to the battery is controlled so that the battery supplies the average load demand to the converter output. Whenever the dc link sees a reference voltage greater than 400 V, both converters are controlled to change their operating modes from boost to buck so that braking energy can be recovered into the storage devices. Figure III-86 and Figure III-87, respectively, show the battery and UC current variations.
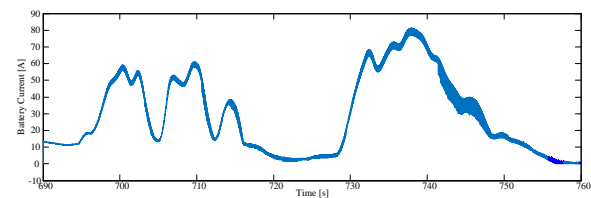
Figure III-86: Battery current variation in cascaded converters architecture.
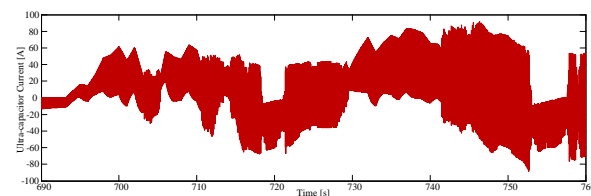
Figure III-87: Ultracapacitor current variation in cascaded converters architecture.

From Figure III-86 and Figure III-87, the battery current ripples are reduced as a result of the control strategy employed. Moreover, the power contribution is greater compared with the previous architecture because the battery current is actively controlled, allowing it to slowly supply the actual load demands. A benefit of this configuration is that at any time, a limitation can be placed on the maximum allowable battery current to reduce the battery contribution and allow the UC to supply more power to the dc link to maintain the 400 V regulation. In this architecture, the current ripple of the UC is greater than in the simpler passive parallel connection, but since it can successfully supply these current variations without reducing its life span, this is not an issue for the UC.

The SoC variations of the battery and UC are given in Figure III-88 and Figure III-89, respectively.
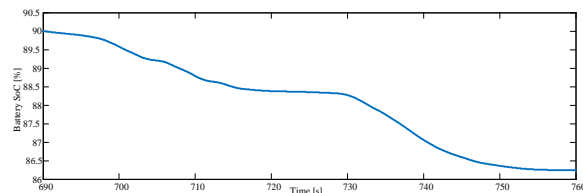
Figure III-88: SoC of the battery for cascaded converters architecture.
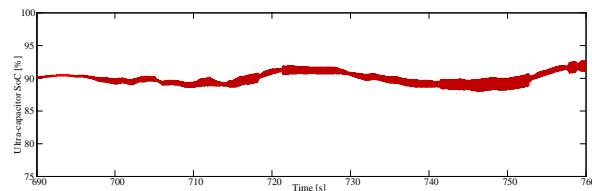
Figure III-89: SoC of the UC for cascaded converters architecture.

In this configuration, the battery is used much as in the passive parallel case. Therefore, the SoC usage window for the UC is smaller because it continually receives charge from the battery. On the other hand, since the battery contributes more charge, its SoC decreases more quickly than in the passive parallel configuration.

The dc link voltage variation for the cascaded converters configuration is represented in Figure III-90. As seen in the figure, the dc link voltage varies around the 400 V reference set point. During periods of high power demand and changes in the operation modes of the bi-directional converters, voltage fluctuations become more apparent. For this architecture and control strategy, the dc link voltage reaches a maximum of 405.0 V and a minimum of 395.3 V. Therefore, the maximum amplitude of the voltage fluctuation was calculated as 2.4% over the simulation period.
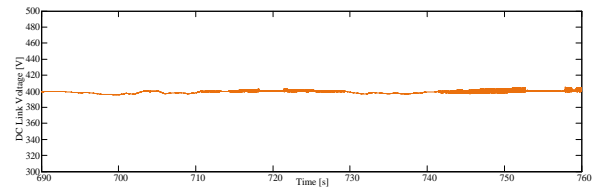
Figure III-90: The dc link (load bus) voltage variation for the cascaded converters architecture.

Since this configuration employs an individual dc-dc converter for the battery, it has the built-in flexibility of tuning and manipulating battery current controls. Therefore, a rate limiter and a saturation limiter can be implemented within the battery current control loop: the rate limiter will limit the slope of the battery reference current, while the saturation limiter will limit the battery current magnitude. The implementation of rate and saturation limiters into the battery controller is shown in Figure III-91.
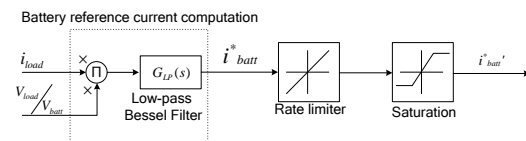
Figure III-91: Battery reference current control modification manipulation.

The rate limiter applied in this work has a rising slew rate of +0.1 and a falling slew rate of −0.1 placed on the rising and falling rates of the battery current. At the same time, the saturation block limits the maximum battery reference current by +50 A and negative battery reference current by −50 A to ensure the further reduction of battery stress and maximum battery charge and discharge current. In this case, the current variations of the battery and UC are recorded as shown in Figure III-92 andFigure III-93.
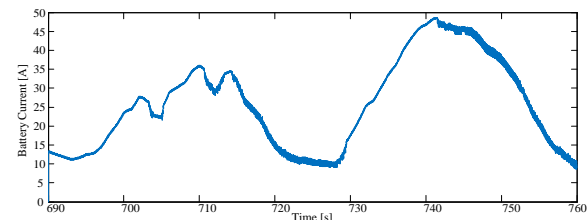
Figure III-92: Battery current variation with modified controls.
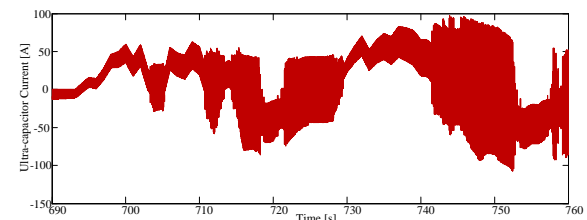
Figure III-93: Ultracapacitor current variation with modified controls of battery.

The battery current given in Figure III-92 resulted from implementation of the rate and saturation limiters within the battery current control loop. This modification improves the battery current waveform by eliminating the natural high slew

rates of the load current (see Figure III-86 vs. Figure III-92). Moreover, maximum charge and discharge current rates can be defined and battery protection can be realized. In this case, the UC tends to vary faster and with a larger amplitude (see Figure III-87 vs. Figure III-93); but again, the selected UC should be capable of supplying this type of current demand. Since battery usage is reduced and more power is supplied from the UC, the modified current controller affects SoC variations as shown in Figure III-94 and Figure III-95.
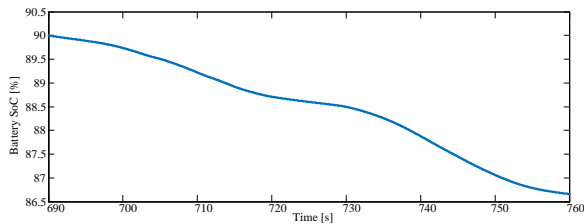
Figure III-94: SoC of the battery for cascaded converters architecture with modified controls.
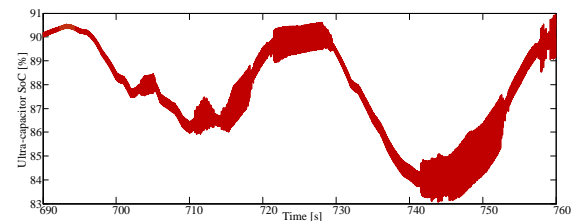
Figure III-95: SoC of the ultracapacitor with modified controls of the battery.

Figure III-94 and Figure III-95 show that the battery SoC remains higher (compare with Figure III-88) whereas the UC SoC drops more drastically (compare with Figure III-89). This occurs because the battery response to power throughput demands is reduced and the UC must deliver more power to the dc link to regulate its voltage during transients.

In any of the architectures discussed, whenever the UC SoC falls below a certain point, the battery controller should bring it back above a certain point while also supplying the load demands. A typical lower limit for the UC can be selected as 20%. Although a deep discharge typically is not a problem for UCs, such a limitation would prevent an associated dc-dc converter from operating in extreme voltage conversion ratios. Moreover, a fully discharged UC would draw an excessively high current at initial charging if the charge current were not appropriately controlled.

The dc link voltage for this architecture with a modification allowing for current-limiting the battery is presented in Figure III-96. Since the UC supplies more power to maintain a constant dc link voltage, the resulting dc link voltage experiences slightly more voltage ripple than in the previous configurations. The maximum dc link voltage for this simulation was 405.2 V with a minimum of 395.2 V and therefore a max/min ripple percentage of 2.5%.
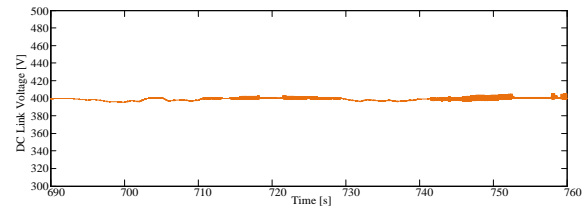
Figure III-96: The dc link voltage variation after modified battery current controls.

Simulation and analysis of parallel connected multiple converters configuration

In this configuration, the battery is connected to the dc link through a bi-directional converter and the UC is connected to the same dc link through another bi-directional converter. The battery and UC are therefore connected to the common dc link in parallel through their individual converters. The same drive cycle was used for load modeling over the same time interval as in the previous simulations, the dc link voltage reference was kept the same, and the same strategies were applied for the battery and UC control loops.

The battery and UC current variations are given in Figure III-97 and Figure III-98, respectively.
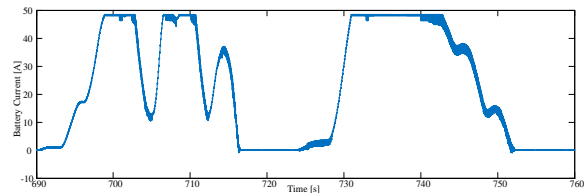
Figure III-97: Battery current with parallel converters architecture.
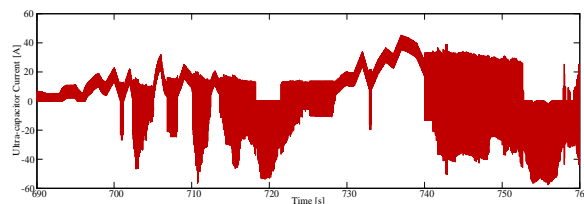
Figure III-98: Ultracapacitor current with parallel converters architecture.

Because of the battery current control strategy used and the parallel-connected individual battery dc-dc converter, the battery current was further smoothed with reduced current ripples. Although the battery current was limited to ±50 A, the battery current remained at less than the maximum limit because of the Bessel reference current filter and rising-falling slew rate limiter controller. The only tradeoff for the lower distortion of the battery current is the huge fluctuations with the UC current. However, the UC is capable of supplying these types of current profiles without sacrificing lifetime and performance.

From Figure III-99 and Figure III-100, it can be observed that the battery is used less and maintains a higher SoC at the end of the drive cycle. Since the UC makes a greater contribution, another mode of operation could be employed so that the battery recharges the UC whenever the UC SoC

drops below a certain lower limit. Figure III-101 shows the final result for this architecture, the dc link voltage variation.
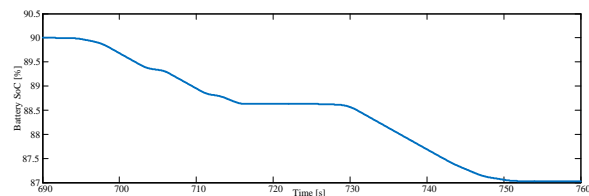
Figure III-99: SoC of the battery with parallel converters architecture.
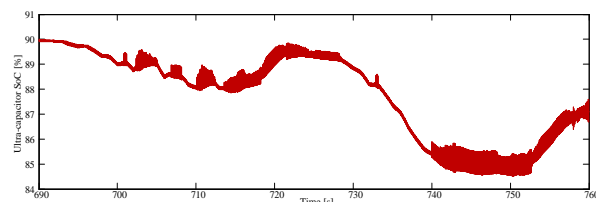
Figure III-100: SoC of the ultracapacitor with parallel converters architecture.
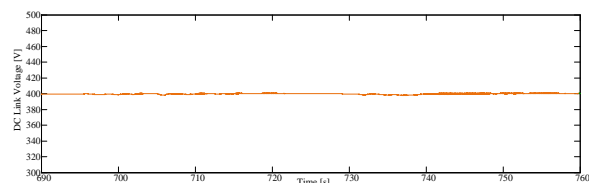
Figure III-101: The dc link voltage variation with parallel converters architecture.

Since the UC and its individual parallel converter are both controlled to maintain a constant dc link voltage, the dc link voltage has a much smaller voltage ripple than in previous configurations. It has a maximum of 400.7 V and a minimum of 397.6 V, resulting in a maximum ripple percentage of 0.8%.

Conclusions and Future Directions

Different architectures offering the combined operation of several ESSs were reviewed. Twelve possible hybridization architectures were described for the combined operation of batteries and UCs. The advantages and drawbacks of the passive parallel connection, UC/battery, battery/UC, cascaded converters, parallel converters, multi-input converters, dual-active-bridge converters, dual-source converters, interleaved converters, and switched capacitor converters were highlighted. Although there is no commercially manufactured PEV powered by a battery/UC combination on the market thus far, the hybridization of these energy storage devices has been shown academically and analytically to be beneficial in terms of battery life, vehicle performance, and fuel economy. However, the hybridization of energy storage devices is a challenging, multi-variable problem requiring appropriate sizing and control of power sharing strategies. Nontraditional forms of ESSs can be promising candidates for PEVs because of their longer lifetimes, higher efficiency, and high specific power and energy densities. Further R&D of these technologies may produce some unforeseen ideal

combination of energy density, power availability, efficiency, and ease of implementation in the future when truly high-energy (low-power) RESS electrochemistries are available, such as lithium-air and others.

This project also modeled and simulated three different hybridization architectures and one of the architectures with a modified controller. The analysis results for these four different configurations are consolidated for comparison in Table III-4. For some comparison criteria, these architectures were graded on a point scale with 1 indicating the best, 2 indicating better, and 3 indicating average.

Table III-4: Comparisons of hybrid energy storage system configurations.

Criteria	PP	CC	CCMC	PC
Control simplicity	1	2	3	3
Structure complexity	1	2	2	2
Number of converters	1	2	2	2
Number of inductors	1	2	2	2
Total inductor mass	2	3	3	2
Number of transducers	5	6	6	6
Cycle-end battery SoC	86.72%	86.24%	86.66%	87.03%
Cycle-end ultracapacitor SoC	89.90%	91.91%	90.45%	87.10%
Maximum battery current ripple	~7 [A]	~9 [A]	~1.7 [A]	~1.8 [A]
Cycle based architectural energy efficiency	95.24%	90.34%	%90.72	%95.25
Maximum dc link voltage variation percentage	2.52%	2.42%	2.51%	0.77%

PP= passive parallel; CC = cascaded converters; CCMC is cascaded converters with modified controls; and PC = parallel converters.

As seen in Table III-4, the control system is the simplest for the passive parallel architecture because there is only one converter current to be regulated. Control of the cascaded converters is more complex because there are two converter currents to be controlled, and the addition of current and slew rate limiters into the cascaded converters controller is obviously more complicated still. Parallel converters have a similarly high level of complexity but with a bit more freedom in control of current magnitude and direction.

The passive parallel configuration has the most basic structure. The other converters have a similar level of structure complexity, as they have a larger number of converters and therefore switches, inductors, bus bars, and so on. The total inductor mass of the passive parallel architecture and of the cascaded converters architecture is higher than that of the parallel converters architecture. In the passive parallel case, 100% of the UC and battery current must pass through a single inductor, requiring inductor wiring with a high current rating. In the cascaded converter architecture, the battery converter carries only the battery current, but the UC converter carries the sum of both the battery and UC current. Although the parallel converters configuration requires two

inductors, they are relatively smaller than the inductors in the other architectures because each converter carries the current of one source, not two.

If the architectures are compared in terms of end-of-cycle battery SoC, the parallel converters case is superior because of the battery current profile. However, the UC is used more in this case, which results in less end-of-cycle SoC. In the cascaded converters case, the battery sustainably recharges the UC; i.e., the battery power is transferred to the UC continually. Therefore, the UC's end-of-cycle SoC is greater. The highest battery current ripple occurs in either the cascaded converter or the passive parallel converters architecture because they do not effectively control and limit the battery current. The cascaded converters with manipulated controls and the parallel converters inherently provide fewer battery current ripples and therefore prolong battery life.

The cycle-based energy efficiencies are calculated by numerically integrating the battery power, UC power, and load power over the drive cycle to obtain the total energy flow from each source to the load. Once the energy levels are obtained, the output energy and input energy relationship defines the cycle-based efficiency. In this case, the cascaded converter

architecture was the least efficient because there are two cascaded converters and one of them should carry all of the current (again, battery current must pass through two converters). In the passive parallel case, there is only one converter, which improves the efficiency. But the most efficient architecture is that of the parallel converters, since each energy storage device has its own converter, and power from a single device never has to pass through multiple converters. The parallel converters architecture is also the best in terms of dc link voltage variation because one of the converters is always used to independently regulate the dc link voltage.

FY 2013 Publications/Presentations

O. C. Onar, J. Kobayashi, and A. Khaligh, "A fully directional universal power electronic inverter face for EV, HEV, and PHEV applications," *IEEE Transactions on Power Electronics* **28**(12), 5489–5498, September 2013

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III.5. Development of SiC Large Tapered Crystal Growth

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Start Date: December 2009
Projected End Date: August 2014

Objectives

- Demonstrate initial feasibility of totally new "Large Tapered Crystal" (LTC) approach for growing vastly improved large-diameter wide-band gap wafers.
- Open a new technology path to large-diameter SiC and GaN wafers with 1000-fold defect density improvement at lower cost.

Technical Barriers

Wide bandgap power semiconductor electronics are widely recognized as critically important to realizing specific cost ($/kW), specific power (kW/kg), power density (kW/liter), and power conversion efficiency goals for electric and hybrid vehicle drive systems. **This project seeks to open a totally new path to lowering 4H-SiC material cost, crystal size, and crystal quality barriers that are significantly hindering realization of these important goals.**

Technical Targets

- Demonstrate initial feasibility of radically new "Large Tapered Crystal" (LTC) approach for growing vastly improved large-diameter SiC semiconductor wafers. In particular, experimentally verify the following required (yet previously undemonstrated) LTC growth physics in a laboratory setting:
  - **Growth of long, small-diameter single-crystal 4H-SiC fibers.** Initial project quantitative metric/milestone is that such fibers exceed 1 cm in length.
  - **Lateral (radial) "M-plane" enlargement of 4H-SiC (simulated) fibers into boules.** Initial project quantitative milestone/metric is that such M-plane

growth enlargement achieve greater than 5 mm diameter miniboule starting from less than 1 mm wide 4H-SiC simulated fiber crystal.

Accomplishments

- Development of totally new source material/feed rod processing technique for Solvent Laser Heated Floating Zone (Solvent-LHFZ) 4H-SiC fiber growth experiments. This advancement enabled:
  - 4-fold reduction in source feed rod diameter.
  - **First demonstration of successful feed rod wetting to a single micro-patterned 4H-SiC seed mesa. This is a critical step needed to initiate growth of desired long 4H-SiC single crystal fiber by Solvent-LHFZ technique.**
- Reduction of parasitic 3C-SiC from lateral CVD epitaxy by implementing TaC coated graphite parts, improving temperature uniformity and altering gas phase chemistry. **Going forward this will enable more prolonged radial/lateral CVD epitaxial growth of larger and higher-quality demonstration mini-boules.**
- Added real-time in-situ thermal imaging of samples and growth environment inside hot-wall CVD reactor. Going forward this capability will accelerate optimization of:
  - Radial/Lateral CVD epitaxial growth process.
  - CVD growth of micro-patterned "hexacone" mesa structures as ideal seeds for growth of long 4H-SiC fibers.
- Procured higher quality 4H- and 6H-SiC seed-slivers needed for improved radial CVD growth.
- Fabricated (via etching and CVD homoepitaxial growth) arrays of micropatterned 4H-SiC hexacone mesas needed for greatly improved seeding of 4H-SiC fiber growth.

✧   ✧   ✧   ✧   ✧

Introduction

Technical Motivation

It is generally accepted that the use of silicon carbide (SiC) power electronics could enable power systems that are significantly more efficient, lighter, and smaller than systems based on silicon (Si) electronics. Although some SiC devices (e.g., Schottky diodes and field-effect transistors (FETs)) have been developed, the energy-saving performance and reliability of SiC power devices are significantly degraded, and device cost significantly increased, because of a high density of dislocation defects (> 1000 per cm^2) in all commercially-available SiC semiconductor wafers. Eliminating these defects economically (i.e., down to densities < 1 per cm^2 while greatly lowering SiC wafer cost) would unlock SiC's enormous (as yet

unfulfilled) promise to revolutionize nearly all high-power electronic systems.

The reason for the high density of defects in commercial SiC wafers is that all current approaches for growing single-crystal SiC boules are fundamentally flawed. The problem with current SiC growth processes is that a high-density of screw dislocation defects (on the order of 10^2 to 10^4 per cm^2) is necessary in order to achieve commercially viable SiC wafer growth rates. Unfortunately, many researchers (including NASA) have now shown that these same dislocation defects harm the yield, performance, reliability, and commercialization of SiC high power devices. If SiC is to fulfill its huge theoretical power device promise, SiC wafer dislocation densities must be brought down 100-1000 fold via a totally new crystal growth approach, yet be able to mass-produce larger-area wafers (at least 6-inches in diameter) and significantly lower both material and device manufacturing cost.

Approach

Introduction to Large Tapered Crystal (LTC) Growth

A NASA Glenn Research Center (GRC) team (J. A. Powell, P. G. Neudeck, A. J. Trunek, D. J. Spry) patented (US Patent 7,449,065) a radically different SiC crystal growth concept that can mass-produce large-diameter SiC wafers wherein each wafer ideally contains only a single screw dislocation (in the center of the wafer). This new growth concept utilizes a revolutionary seed crystal configuration and two simultaneous growth processes in connected chambers for rapidly growing large single-crystal SiC boules with only one centrally-located screw dislocation (SD). Because this new process grows a large crystal with a tapered shape, we have named this the Large Tapered Crystal (LTC) growth process. The crystal growth initiates from a small-diameter fiber (with a single screw dislocation at its core) that is grown in a first chamber, from which it is withdrawn, as it elongates, into a second growth chamber where radial growth on the fiber produces a large tapered crystal. Each growth run produces a low-defect (ideally with a single screw dislocation) SiC crystal boule (100 mm diam.) at the top end of the LTC. A comprehensive technical description of the process and apparatus involved can be found in U.S. Patent 7,449,065 that is now available online at the U.S. Patent Office website http://www.uspto.gov. This section presents a highly condensed summary of the contents of the patent.

Figure III-102 illustrates schematic cross-sections of SiC crystals during steps S1, S2, and S3 of the LTC growth process. Each LTC growth cycle (except the very first cycle, as described in U.S. Patent 7,449,065) starts with an LTC as the seed crystal as shown in Figure III-102(a). The central axis of the LTC seed will be parallel to the crystallographic c-axis. During growth step S1, the small end (the fiber portion in chamber 1), as shown in Figure III-102(b), will be grown in the c-direction and maintained at a diameter of less than 1 mm; the large end of the LTC will be maintained at some designated large diameter (e.g., 100 mm for commercial systems). Simultaneously with the axial growth of the small-diameter fiber in chamber 1, radial epitaxial growth

enlargement of the large tapered section takes place in a growth chamber 2 during a growth step S2. Ideally, only a single screw dislocation (along the central axis) will be present in the entire crystal. This single screw dislocation provides the necessary crystal stacking sequence for a given SiC polytype. This stacking sequence also establishes the sequence of atomic steps that propagate radially during growth in chamber 2. It is important to note that defects (i.e., screw dislocations) are not required for the radial growth in chamber 2. Indeed, the bulk of the crystal boule (except for the very small volume of the central fiber) is deposited by "step-flow growth" in chamber 2 (utilizing the crystal stacking sequence established by the small-diameter fiber).

Because of the large surface area of the tapered portion, moderate radial growth rates (e.g., about 0.1 mm/hour) will yield rapid bulk growth of the LTC in chamber 2. As growth proceeds in steps S1 and S2, the top of the tapered crystal enters an isothermal chamber 3 of inert gas atmosphere where no additional SiC is deposited. This enables a cylindrical (hexagonal cross-section) crystal boule to form as the large end continues to exit chamber 2 into the "no-growth" isothermal chamber 3. The top of the crystal is physically moved upward during growth steps S1 and S2 so that the bottom of the downward-growing small-diameter tip is maintained at the same position inside chamber 1.
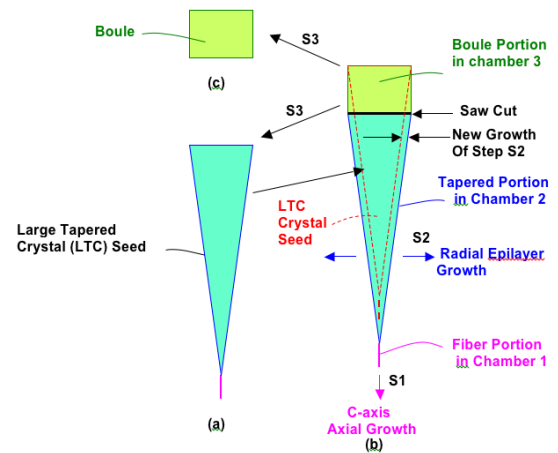
Figure III-102: Simplified Cross-Sectional Illustration of Large Tapered Crystal (LTC) Growth Process.

The LTC growth process as presented herein relies on two separate high-quality SiC growth processes taking place on different surfaces/regions of the same crystal, namely (S1) c-axis fiber growth and (S2) radial epilayer growth. Neither of these processes has been experimentally attempted nor demonstrated for SiC in the manner or configuration that is proposed above. Therefore, the critical first objective of this work is to separately demonstrate, for the first time, that both of these two new SiC growth processes can be successfully carried out.

Results

Fiber Growth via Solvent-Laser Heated Floating zone (Solvent-LHFZ)

A key (and most challenging) aspect of demonstrating the viability of the LTC process is the demonstration of rapid growth (on the order of 1 mm/hour in the crystal c-axis direction) of a single-crystal SiC small-diameter fiber containing a single screw dislocation (i.e., demonstrating growth S1 of Figure III-102). The basic feasibility goal of initial fiber growth work under this project is to demonstrate single crystal 4H-SiC fibers of at least 1 cm in length.

To achieve this, a growth method has been chosen that combines the advantages of two well know growth methods: Laser Heated Floating Zone (LHFZ–proven for oxide-based crystals) [1] and Traveling Solvent Method (TSM–demonstrated for SiC) [2], which we have named Solvent-Laser Heated Floating Zone (Solvent-LHFZ). Growths are initiated by melting the end of the feed rod followed by wetting to the end of a 4H-SiC seed crystal (preferably with a single screw dislocation at the tip) to the melt. In a nominal process material transport and dislocation-mediated growth enlargement occurs on the 4H-SiC tip, so that an elongating single-crystal 4H-SiC fiber can be continuously pulled out from the melt as illustrated in Figure III-103.
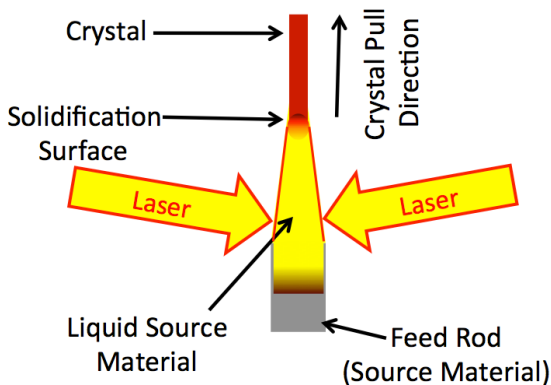
Figure III-103: Simplified Cross-Sectional Illustration of Solvent-LHFZ Single-Crystal Fiber Growth Process (see text).

To perform Solvent-LHFZ experiments, a custom system (more fully described in FY11 annual report) was constructed during the first year of DOE funding consisting of a CO_2 laser (λ=10.6 μm) and associated optics, vacuum chamber, sample translation system, optical pyrometer and video capture/data collection/experimental control system and vacuum/gas management system.

Figure III-104 (reproduced from the FY12 annual report) shows one of the first 4H-SiC seeded crystal film depositions grown using the Solvent-LHFZ growth apparatus. In particular, a 4H-SiC epitaxial layer was grown by dipping a saw-cut 4H-SiC seed sliver into the melt. While the grown crystal represents initial confirmation of the general concept of seeded 4H-SiC growth via Solvent-LHFZ, it is far from being a demonstration of long and high-quality fiber growth. In particular, multiple growth domains eminate from multiple

screw dislocation defects in the seed crystal. As growth proceeds, these multiple small growth fronts collide trapping solvent rich material in the crystal, which in turn create additional defects. The undesirable compounding of defects nucleating from such a chaotic growth surface precludes the ability to grow a long single crystal fiber of acceptable high quality needed to realize LTC. Thus (as described in the LTC patent), **long high-quality fibers need to initiate from a much smaller 4H-SiC seed crystal surface that contains only a single screw dislocation**, rather than the relatively large (> 0.5 mm^2) flat seed crystal surface (that contained abundant screw dislocations) used in these first-ever Solvent-LHFZ demonstration experiments.

300 μm
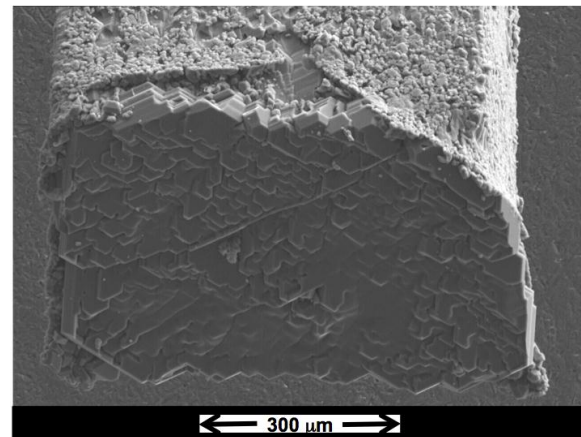
Figure III-104: Scanning Electron Micrograph of 4H-SiC homoepilayer grown via Solvent-LHFZ.

In order to grow a high-quality single crystal fiber, a seed crystal with a single dominant well-ordered growth front is needed. Figure III-105 shows an example of such a seed crystal that we have been producing. We refer to this as a faceted "hexacone" SiC seed crystal. These hexacone seed crystals are produced via hot-wall CVD epitaxy carried out on patterned mesas lithographically dry-etched into SiC wafer substrates. The pointed peak feature is the result of desired and well-ordered defect-assisted CVD growth at a single dominant screw dislocation. It is important to note that the non-pointed mesas in Figure III-105 were subjected to the same process, but did not form pointed hexacones due to the random location of screw dislocations found in the 4H-SiC substrate. Further discussion for the reasons for this are given in U.S. Patent 6,783,592 as well as U.S. Patent 7,449,065. **Only the pointed hexacone mesa is useful for fiber growth, because it contains the single screw dislocation at its center producing the peak.** During the past year considerable effort has been spent fabricating and growing a much larger inventory of these special hexacone crystals (in a newly designed pattern) needed for proper seeding of fiber growth experiments.
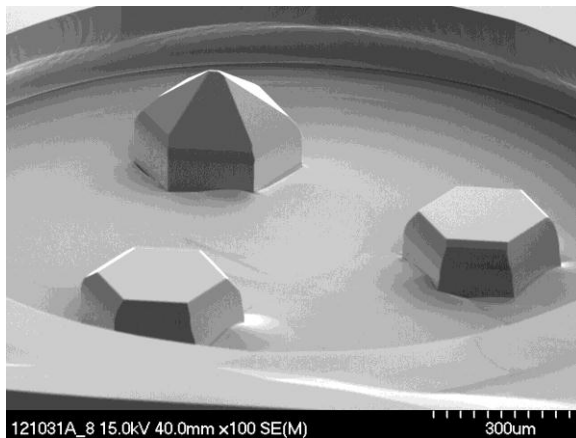
Figure III-105: 4H-SiC "hexacone" seed crystal grown via hot-wall CVD epitaxy on dry-etched patterned 4H-SiC substrate.

To successfully seed a Solvent-LHFZ fiber growth, a 3:1 to 1:1 ratio of the feed rod diameter to seed mesa diameter must be achieved in order to maintain the dynamics of the growth method. Also, the source feed rod melt must only make contact with the desired mesa without contacting any other 4H-SiC mesas in the patterned array. The NASA Glenn Solvent-LHFZ growth system was designed and constructed with sufficient optical monitoring and micopositioning capability to accomplish this precise positioning of the feed rod and seed crystal sample. However, such controlled wetting is not physically possible if the feed rod diameter is much larger than the width of the hexacone seed mesa. **However, the diameters of source feed rods employed for initial Solvent-LHFZ experiments over the last two years were on the order of 2 mm in diameter, physically too large to maintain growth dynamics or meet positioning requirements necessitated by a single 4H-SiC hexacone mesa.** As better described in [3], these prior feed rods were formed via cold isostatic press (CIP) and sintering. **Despite much effort, we were unable to sufficiently shrink the CIP + sintered feed rod diameter to the size needed for Solvent-LHFZ on a single hexacone mesa while simultaneously achieving/maintaining other necessary feed rod material properties (composition, melting, wetting, etc.).**

In order to realize the needed small-diameter source feed-rods, an entirely new feed rod synthesis approach had to be developed starting from scratch. After much work (including a number of trial and error experiments), an extrusion-based feed-rod synthesis process was developed. Public disclosure of the experimental details of the new feed rod preparation process will have to wait until future reports. **Nevertheless, this new process enabled a 4-fold shrinkage in diameter of the Solvent-LHFZ feed rod.**

Figure III-106 shows successful laser-melting of an extruded feed rod, and subsequent successful wetting to a single 4H-SiC hexagonal mesa. Figure III-106(a) is an optical image of the un-heated feed rod underneath an array of hexagonal mesas patterned across the 4H-SiC substrate.
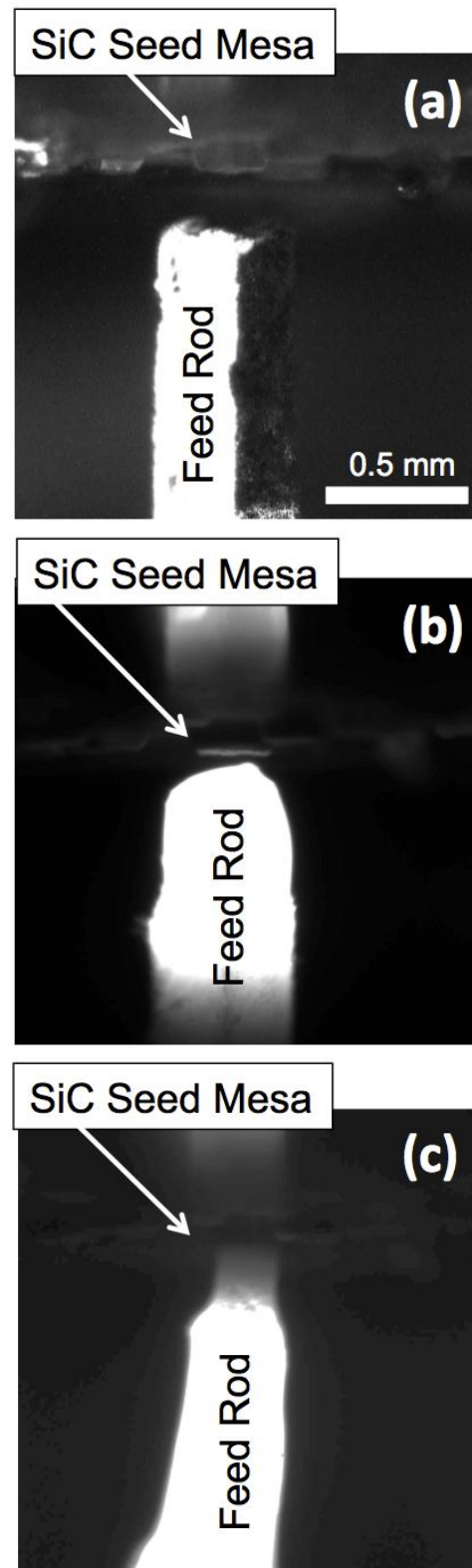
Figure III-106: Optical images of (a) extruded feed rod and 4H-SiC hexagonal mesa array prior to heating, (b) laser-melted tip of source feed rod approaching hexagonal mesa, and (c) successful wetting of melt to single 4H-SiC mesa.

Figure III-106(b) shows the optical image of the laser-melted feed rod tip approaching the targeted hexagonal seed mesa in the array, just prior to physical contact. Figure III-106(c) shows the optical image recorded a few minutes after contact and successful wetting of the feed rod to the targeted hexagonal patterned seed mesa. Note that there is no wetting or contact of the source-melt with other nearby mesas in the array.

This wetting of a single micro-patterned 4H-SiC seed mesa is the necessary first step in properly initiating desired Solvent-LHFZ single screw dislocation growth of long fibers needed for realizing LTC growth. With the improved feed rods and 4H-SiC seed mesas now demonstrated, further experiments during FY14 can proceed towards the demonstration goal of growing increasingly thick layers and fibers of high crystal quality (nominally containing only one screw dislocation defect).

SiC Radial Growth via CVD Epitaxy

The vast majority of the LTC boule will be formed by epitaxial radial growth on the seed fiber via CVD during step S2 (in chamber 2, Figure III-102). As the small diameter fiber expands, the LTC boule is expected to evolve towards a hexagonal cross-section whose outer surfaces will be "m-planes". Maintaining commercially viable radial growth rates (on the order of 50-100 um/hour) are essential to the LTC process. However, the most fundamental question to be addressed by this early stage of research is to determine if the radial epixatial growth expansion of a fiber introduces additional crystalline defects. Previous efforts to grow in the (radial) a-direction by sublimation growth resulted in increasing stacking fault density [4], but these previous studies grew crystals in environments of much higher temperatures and stress (thermal and seed-mounting) than is proposed for the LTC process.

At this time, there is no known source of high-quality single crystal SiC small-diameter fibers to use as seeds for experimental investigation of the radial expansion epitaxy of the LTC process. Therefore, the initial development experiments of the radial growth process have been conducted on simulated "pseudo-fiber" SiC crystals prepared from commercially purchased wafers and saw-cut into long rectangular fiber-like shape with both "a-face" and "m-face" radial growth surfaces as schematically illustrated in Figure III-107. Despite the fact that these pseudo-fiber seeds are far from ideal in terms of their defect content and growth surface quality, significant radial growth enlargement has nevertheless been achieved, including growth of the 4 mm diameter mini-boule shown in Figure III-108. The growth and characterization of this crystal is described in much greater detail in the FY12 annual report.

Towards the end of growing significantly larger and higher quality demonstration mini-boule crystals, three important upgrades for the radial hot-wall CVD experiments were implemented during FY 2013. The first upgrade was procurement and installation of TaC-coated sample carriers. These new carriers are expected to greatly suppress the parasitic nucleation and growth of 3C-SiC that occurs where the seed sliver is held by the carrier [5]. The potential importance of this improvement is readily evidenced

by the predominance of undesired yellow-colored 3C-SiC crystal in the lower portion of the Figure III-108 mini-boule, which was produced using an uncoated graphite carrier. Because this 3C-SiC interferes with desired 4H-SiC radial expansion, its suppression (using TaC coated carriers) is vital towards realizing larger mini-boules of higher crystal quality.
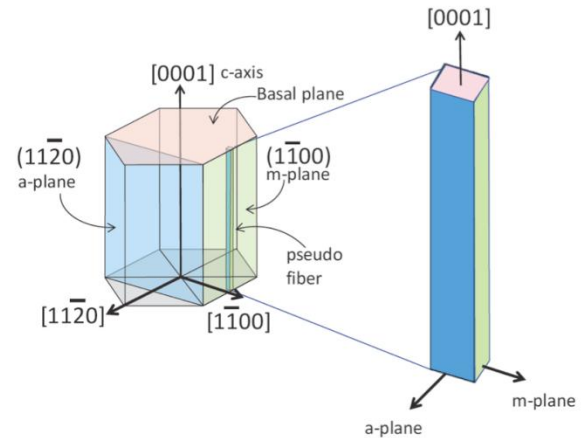
Figure III-107: Schematic illustration of saw-cut "pseudo-fiber" sliver used to seed radial CVD epitaxial growth experiments.
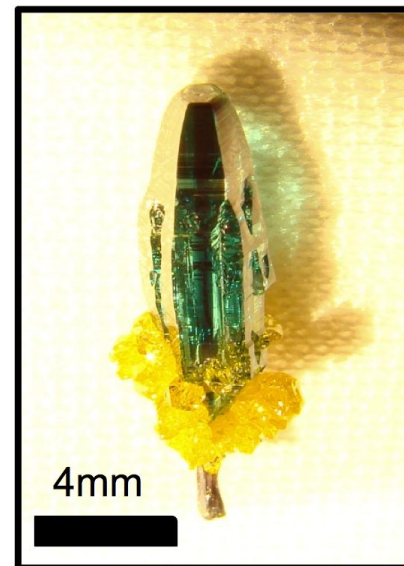
Figure III-108: Optical image of ~4mm diameter "mini-boule" crystal produced via CVD radial epitaxial growth expansion from an imperfect "pseudo-fiber" seed.

Another important upgrade implemented during FY13 was procurement and installation of in-situ thermal imaging for the interior growth zone of the hot-wall CVD reactor. This new thermal imaging capability enables real time monitoring of the spacial temperature profile throughout the reactor, which is vital to radial CVD growth process condition optimization. It also enables monitoring of the changing size and shape of the crystals during growth runs. Figure III-109 shows the acquired thermal image of two 4H-SiC seed slivers during a high-temperature pre-growth etching experiment.
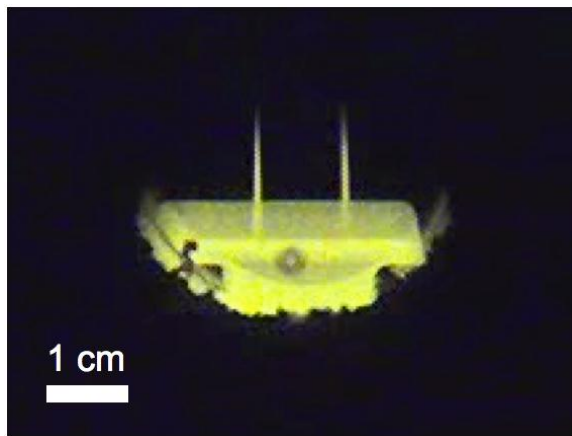
Figure III-109: Thermal image of TaC-coated carrier and 4H-SiC seed slivers inside NASA hot-wall CVD reactor during T > 1400°C pre-growth H$_2$/HCl etch.

Last year's annual report showed X-ray topgraphic characterization of the 4H-SiC mini-boule shown in Figure III-108. A high density of defects was observed in the radially grown epilayer, but the vast majority of these defects were observed to have originated in the poor-quality 4H-SiC seed sliver. This initial result obtained on a relatively small crystal (< 0.5 cm diameter) is generally a positive indication that radial enlargement of via CVD without generation of new defects is possible. As the abundance of seed-originated defects interferes with critical (to determining LTC feasibility) observation of epilayer-originated defects, it is important going forward to carry out radial epitaxial growth experiments starting from significantly higher quality seed slivers. Towards this end, seed slivers of significantly higher crystal quality have been procured from two separate sources. These new seeds will be used for almost all radial CVD growth experiments going forward.

With the above improvements in place, radial growth enlargement experiments were just re-starting when a toxic gas detection alarm occurred in the NASA SiC CVD growth laboratory on 21 May 2013. Subsequent investigation revealed that alarm was real but successfully confined to the protective sample loading glovebox of the CVD system. The root cause was determined to be a partial failure of multiple components (including a defectively manufactured subsystem) that allowed residual HCl to escape the reactor during SiC sample loading/unloading. Safety-related repairs, facility upgrades, procedural revisions, and testing were undertaken. All experimental progress on radial CVD growth was halted until these activities were completed (and approved) in late September 2013.

Fiber Growth via Laser-Assisted CVD (NASA-funded SBIR Phase III)

Since the inception of the LTC growth process for SiC, it has been understood that successfully implementing single-crystal 4H-SiC fiber growth would likely prove the most difficult and challenging technical advancement. Thus, when additional NASA Glenn funds became available in April of 2012 to augment continuing (Dept. of Energy funded) LTC development efforts, a parallel technical path towards realizing

4H-SiC fiber growth was initiated. In particular, a NASA SBIR contract with Free Form Fibers, Inc. (FFF) in Saratoga Springs New York that specializes (and holds patents) in laser assisted CVD growth of ceramics (including polycrystalline SiC) was initiated in June of 2012. NASA Glenn supported these efforts by providing hexagonal-patterned arrays of 4H-SiC mesas for use in the work and also characterized many of the SiC samples following FFF experiments. While details of this SBIR work remain proprietary as of this writing, **the contract concluded in June of 2013 without any experimental realization of 4H-SiC single-crystal fiber growth.** However, the results did make tangible technical progress on the path towards realizing successful laser assisted CVD growth of 4H-SiC single crystal SiC in the future.

Conclusions and Future Directions

If successfully implemented, Large Tapered Crystal (LTC) boules promise to greatly improve the cost and quality of wide bandgap wafers that will become the basis for realizing much more advanced high-power semiconductor switches. These devices in turn offer high-impact benefits to power conversion/management systems including utility power transmission and electric/hybrid vehicles.

Over the past year NASA Glenn has continued progress towards experimental implementation of the two critical (previously un-attempted) "fiber" and "radial" growth processes needed to realize Large Tapered Crystal (LTC) SiC boules. In the area of fiber growth via Solvent-LHFZ, greatly improved source rods have been developed. Combined with newly micro-patterned seed mesas, we are now in a position to initiate LTC fiber growth in its preferred embodiment (namely from 4H-SiC seed crystal mesa with a single screw dislocation at its center). Substantial improvements to the radial CVD process have also been implemented. These are expected to advance the size and quality of radially grown demonstration crystals over the next year, hopefully to a size in excess the 0.5 mm diameter project milestone metric. Therefore, continued experimental progress in fundamental LTC growth demonstations is expected during FY2014.

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2. L. B. Griffiths and A. I. Mlavsky, "Growth of α-SiC Single Crystals from Chromium Solution", J. Electrochem. Soc., 111, 805 (1964).

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4.   J. Takahashi & N. Ohtani, "Modified-Lely SiC Crystals Grown in [1100] and [1120] Directions", Phys. Stat. Solidi B, vol. 202, p. 163 (1997).

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FY 2013 Publications/Presentations

A.A. Woodworth, P.G. Neudeck, A. Sayir, "SiC growth by solvent-laser heated floating zone method", invited presentation at Sixth International Symposium on Advanced Science and Technology of Silicon Materials (JSPS Si Symposium). Hawaii, on November 19-23, 2012.

III.6.   Glass Dielectrics for DC Bus Capacitors

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Start Date: July 1, 2012
Projected End June 30 2014:

Objectives

- Characterize the high temperature electrical properties of flat panel display glass. Relevance–APEEM capacitor goal 140°C and 650V.
- Fabricate and test coiled glass capacitors.
  - Addresses the DOE PEEM requirements for low cost.
  - Leverage the substantial investment has occurred in flat panel display glass for the development for high-temperature capacitors.
- Demonstrate the long-term reliability of glass capacitors through highly accelerated life testing (HALT). Relevance–APEEM capacitor life goal of >13,000 hrs. under EV/HEV operating conditions.

Technical Barriers

- Critical Assumption: 10 µm thick glass will be required to meet the DOE APEEM volume requirements for DC bus capacitors. Currently, glass manufacturers are selling 30 µm thick sheet and have produced glass with thicknesses down to 5 µm. A viable production method for thinning glass at the large scale needs to be established.
- For continued investment in the development of glass for high temperature capacitors, the long–term reliability concerns must be addressed.

Technical Targets

- Develop a glass capacitor to meet the APEEM temperature specifications of 140ºC. Glass has a substantially higher melting point (1400°C) than the melting point of plastics (150ºC) that are presently used in capacitors.
- Determine failure modes and predict life of a glass DC BUS capacitor based on highly accelerated life testing.

Accomplishments

- Coiled glass capacitors were fabricated and tested under high AC voltage.
- Capacitor life was estimated for a capacitor made from flat panel display glass.

◇   ◇   ◇   ◇   ◇

Introduction

There is general agreement within the automotive and power electronics communities that revolutionary approaches, drawing on diverse disciplines, will be necessary to develop the next generation of power systems. In addition to renewable energy sources (solar, wind, etc.), hybrid electric vehicles rely on power converters to transform energy from batteries to motors and to the grid. A major component within the powder converter is a DC bus capacitor which occupies a significant fraction of the inverter volume. The competing material technologies for this application are shown in Table III-5. As a comparison, batteries have energy densities of 300 J/cm^3 and significantly lower power densities of 0.5 MW/cm^3.

Table III-5: Energy Storage Comparison at the Materials Level.

	Relative Permitti v-ity	Break-down Field MV/cm	Energy Density J/cm^3	Power Density MW/cm^3
Glass	5-6	10.5	35	25
Polypropy-lene	2.2	7.3	5	35
PVDF co-polymer	11-12	5	35	3
Polyimide	3.2	5.7	5	3

The research challenge for new materials can be distilled into a single figure-of-merit–**energy density**–which captures the vital materials parameters of relative dielectric permittivity (ε_r) and dielectric breakdown strength (electric field). For linear dielectric materials, energy density varies as $U_e = \frac{1}{2}\varepsilon_r\varepsilon_0 E^2$, where ε_r is relative dielectric permittivity, E is applied electric field, and ε_0 is the vacuum permittivity. Energy densities of nonlinear dielectrics must be derived from the relationship $U_e = \int E dD$, where D is the dielectric displacement. The power density is derived from the energy density and the dielectric loss [5,6]. As shown in Table III-5, glass has the best combination of power and energy density of all of the competing materials.

Another enormous benefit of glass is high temperature endurance. The alumino-borosilicate glasses that are used in flat panel displays have a melting temperature of 1400°C, which is significantly higher than the melt temperature of any polymer. Consider an application in which MW-scale power

converters are 98% efficient, leaving 20kW of wasted power to heat the circuitry. High temperature power components are certainly an advantage in this case and there have been recent breakthrough in SiC based switch components for power circuits [7]. High temperature glass capacitors will provide the complementary high-temperature passive components for these high power circuits.

The combination of new manufacturing methods and new glass materials for the display industry has led to entirely new applications. Thin glass sheet formed by unconventional manufacturing processes has generated an unexpected application in energy storage.

Approach

Commercial capacitors for hybrid electric vehicles (HEVs) and plug-in hybrid electric vehicles (PHEVs) do not meet U.S. automaker's specifications for high temperature operation, cost and reliability. The objectives of this project are to develop high temperature capacitors that go beyond what is commercially available and to eliminate costly coolant systems within the HEVs and PHEVs. Ceramic capacitors have excellent high temperature performance and meet a majority of HEV and PHEV specifications for power electronic converters; however, catastrophic failure modes and cost are primary impediments to their use in hybrid vehicles. The goal of this project is to produce reliable glass capacitors without compromising the energy density (related to capacitor volumetric efficiency). Specific goals include:

- Characterize fundamental electrical properties of flat panel display glass that are related to DC bus capacitor reliability and ultimately the cost and performance of power converters for HEVs.
- Collaborate with Sandia National Laboratory and Argonne National Laboratory to understand breakdown strength and reliability of materials underdevelopment for DC bus capacitors.
- Scale-up glass capacitor technology by teaming with glass manufacturers and capacitor companies.

There has been a substantial world-wide expansion in flat panel display glass over the past decade. This plentiful material has excellent high temperature electrical properties. To use glass capacitors in HEVs the following approach is taken:

- Characterize glass materials at high temperature to predict reliability in DC bus capacitors.
- Develop self-healing modes in glass to avoid catastrophic failure power converter operation.
- Manufacture prototype capacitors for HEVs in collaboration with industrial partners.

There is general agreement within the automotive and power electronic communities that revolutionary approaches, drawing on diverse disciplines, will be necessary to develop the next generation of power systems for electric vehicles. New active and passive components need to be developed and manufactured which can operate at high temperature for

long periods of time. In addition, component miniaturization is important to reduce the total volume and cost of the power electronic circuitry on board an electric vehicle. A summary of the results of this study is shown in Figure III-110.

Current Capacitor Technology Volume = 1.4 Liters 85ºC Rating

DOE Specification Volume =1.2 Liters 140ºC Rating

Current High Temperature Capacitor Technology Volume = 21.6 Liters 125ºC Rating

Glass Dielectric Volume =0.007 Liters 25ºC Projected from Results

Glass Capacitors Projected Volume <2 Liters 140ºC Rating Projected from Results
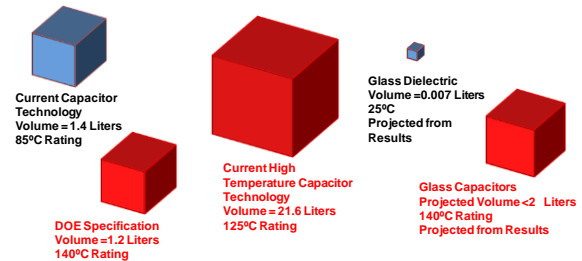
Figure III-110: Volumetric comparison between DOE capacitor specifications, commercial capacitors and the projected capacitor volumes from the research at Penn State. All volumes shown are for a 1000 µF and 1000 V capacitor.

The DOE specifications (Figure III-110 lower left corner) were derived from discussions with the EE Tech Team and component manufacturers. Presently, high-temperature film capacitors (middle of Figure III-110) have 18 times the volume of the DOE specification. The glass dielectrics explored in this study have the potential to operate above 140ºC and the volume is much smaller than commercial high temperature capacitors (Figure III-110 right side).

Results

The flow diagram for producing the coiled glass capacitors is shown in Table III-6. The fabrication process for the prototype capacitor begins with flexible glass ribbon (5 µm to 50 µm thick) and lengths of 3 m. Longer glass ribbons (100 meters) have also been produced by glass manufacturers. The glass surfaces are very smooth (RMS surface roughness values less than a nanometer) and the pristine glass has excellent mechanical properties. Previous reports have shown that a 5 µm thick glass ribbon is able to be wrapped around the diameter of a pencil, which is important for coiled glass capacitor designs.

After receiving the glass ribbon from the manufacturer, electrodes are placed on the both sides of the ribbon. Silver electrodes are deposited by spraying silver nanoparticles on the glass surface and no heat treatment is necessary to produce an electrode with low resistivity. The silver electrodes in this study have sheet resistances in the 10 Ω /$\square$ range, which is similar to evaporated aluminum resistances found for polypropylene capacitors. For large-scale production of glass capacitors, evaporated aluminum conductors will also be used for the conductor. Foil tabs are attached to the electrode along the length of the ribbon every 10 cm, so that the current paths are short. The electrode and tab configuration was designed to minimize the loss and equivalent series resistance.

Capacitor packaging is a critical step for meeting the demanding thermal, electrical and mechanical performance requirements of the capacitor for HEV applications. The glass ribbon is wrapped around the mullite mandrel which is a high

Table III-6: Fabrication process for manufacturing DC bus capacitors.

Draw Glass Ribbon
- Thin glass ribbon is manufactured by a down-draw process and redrawn to reduce the ribbon thickness.
- The key challenge is to produce glass ribbon from 50μm to 10 μm.

Deposit Electrode
- Electrodes are placed on top and bottom surfaces of glass ribbon and candidate electrodes include copper foil, aluminum and silver film.
- Equivalent Series Resistance (ESR) and self-healing mechanisms are controlled by the electrode properties.

Wind glass
- Glass ribbon up to a 100 meters in length has been produced by glass manufacturers, which will need to be coiled into a capacitor configuration.
- Coil diameters of 10 cm have been demonstrated for 50μm thick ribbon. Substantially smaller diameters (1 cm) are possible with thinner glass.

Package
- Packaging includes end termination, lead attachment and encapsulation.
- Thermal, mechanical and electrical performance must be considered in package design.

Test
- The capacitance and loss is characterized as a function of frequency, temperature and AC voltage strength.
- Reliability tests to predict capacitor performance under operating conditions.

temperature insulating material. After the winding step, a wire is attached to each of the conductor tabs and then terminated to the side of the capacitor. There are terminations on the top and the bottom of the capacitor. A high temperature capacitor was manufactured from flat-panel display glass and is shown in Figure III-111. The specific conductor and winding configuration will need further improvement. For the prototype capacitor, a spacer glass layer is used to isolate the positive and negative sides of the conductor-coated glass layer.

The capacitor design was optimized for low equivalent series resistance, low inductance, and high temperature operation. The electrical properties (capacitance and loss) were characterized as a function of frequency and temperature with an Agilent impedance analyzer. High voltage properties were characterized with a high voltage power supply.
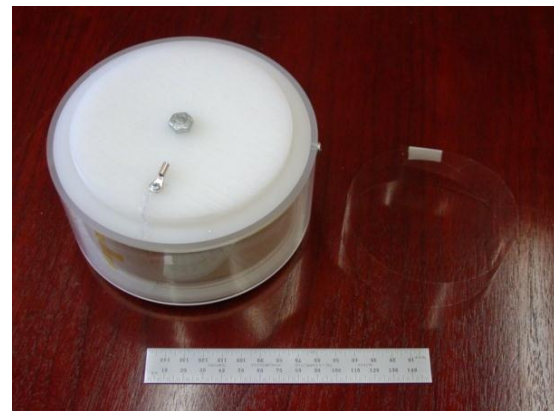
Figure III-111: Top view of a functional DC bus capacitor (left side of figure) and a section of the wound glass ribbon (right side). Ribbon dimensions: 2.9 m long, 30 mm wide and 50 μm thick.

Flat panel display glass has shown excellent electrical performance and is a promising material for DC bus capacitors; however, the long-term material reliability is unknown. A series of electrical tests has demonstrated that the materials will withstand HEV operation conditions for the life of the vehicle. Tests include the characterization of life through a test chamber at 400ºC and using equation 1 to predict performance in vehicles (Figure III-112).

Acceleration Factor (Determined from space charge distribution in glass)

Activation Energy (Determined from ionic transport in glass)

Predicted time to Failure

Measured time to Failure

$$\frac{t_1}{t_2} = \left[\frac{V_2}{V_1}\right]^n \exp\frac{E_A}{K}\left[\frac{1}{T_1} - \frac{1}{T_2}\right]$$

Voltage

Temperature

where the subscripts *1* and *2* describe the test conditions, *t* is the median time to failure, *V* is voltage, *n* is the voltage acceleration factor, E_A is the activation energy for failure, *K* is the Boltzmann constant, and *T* is absolute temperature. The acceleration factor, *n*, and activation energy, E_A, will be determined by performing HALT at different temperatures and voltages.
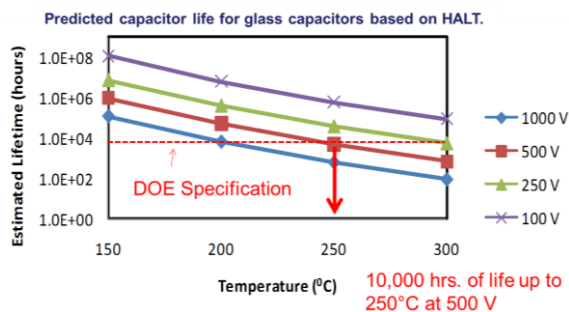
Figure III-112: Life prediction for capacitors that are made from flat panel display glass.

Conclusions and Future Directions

DC bus capacitors must go beyond commercially available polypropylene (PP) in order to minimize the need for costly coolant systems within the electric drive vehicles (EDVs) and meet the DOE cost target for power inverters (from $7.9/kW in 2010 to $3.3/kW in 2020) Material innovations for power electronic components, including SiC/GaN for switches and high temperature dielectrics for capacitors, are key to bringing disruptive progress to meet DOE cost, size, thermal, and other performance specifications in future EDV inverter capacitors.

Penn State has been investigating alkali-free glass (AFG) for high temperature and high energy density capacitor applications with support from DOE, as well as major glass manufacturers (Corning, NEG and Schott). These early R&D efforts and recent manufacturing progress at the major flat panel glass manufacturers provide very promising results including; the superior electrical and thermal performance of commercially available glass compositions, the self-healing feature, the capability to directly manufacture 5 μm thick glass

sheet, and the feasibility to metallize the glass in a continuous roll-to-roll (R2R) process.

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1. P. Dash, E. Furman, C. Pantano, M. T. Lanagan, "Space Charge Formation and High Field Properties of Low Alkali Glasses," 2013 Material Research Society Spring Meeting & Exhibit, San Francisco, California, Apr 1-5, 2013.

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Start Date: FY05
Projected End Date: FY13

Objectives

- Develop ceramic dielectric films that have potential to reduce size, weight, and cost, concomitant with increased capacitance density and high temperature operation, for capacitors in electric drive vehicle inverters.

Technical Barriers

- This project addresses the overall size, cost, and high-temperature operability barriers of the presently used polymer-based capacitors in automotive power inverters. Current DC bus capacitors occupy a significant fraction of volume (≈35%), weight (≈23%), and cost (≈23%) of the inverter module, cannot tolerate temperatures >85°C, and suffer from poor packaging, and inadequate reliability. Traditional capacitor architectures with conventional dielectrics cannot adequately meet all of the performance goals for capacitance density, weight, volume, and cost.

Technical Targets

- Achieving APEEM targets for capacitance density, weight, volume, and cost requires a dielectric material that has high permittivity, shows good performance at high temperature, can be packaged in an architecture with high volumetric efficiency, and exhibits benign failure.
- Technical targets of this project is to demonstrate Pb-La-Zr-Ti-O (PLZT)-based dielectric films with permittivity (k) that is ≈30 times that of presently used polymer-based film capacitors over the temperature (-40°C to +140°C), voltage (450 V nominal) and frequency (≈10 kHz) ranges required for automotive power electronics.

Accomplishments

- Demonstrated fesibility of PLZT and approach to meet APEEM project objective.
- Measured k ≈110 and dielectric loss ≈0.004 (0.4%) at 300 V bias on a ≈3.0 μm-thick PLZT film.
- Dielectric properties at 300 V bias show an increase in k and decrease in dielectric loss with temperature increasing from -50°C to +200°C.
- Measured energy density of ≈85 J/cm^3 on a ≈3.0 μm-thick PLZT film at room temperature.
- Demonstrated PLZT films with dielectric breakdown field >2.6 MV/cm, and leakage current density <10^{-8} A/cm^2.
- Demonstrated graceful failure mode by self-clearing method in single layer PLZT films.
- Dielectric films are thermally cycled (about 1000 cycles) between -50°C and +150°C with no measurable degradation in k.
- Evaluated residual stresses in PLZT films deposited on various substrates.
- Fabricated a ≈8.5 μF (unbiased) and 3.0 μF (at 100 V) prototype capacitor by stacking PLZT films. The multilayer stack was characterized as function of bias voltage, temperature, frequency and measured its ESR.
- The spin-coating process used to demonstrate material properties requires many processing steps and is slow. An aerosol deposition (AD), a high-rate, room-temperature film deposition process, is being developed to reduce capacitor cost.
- Recently demonstrated that a ≈3-μm-thick PLZT film can be deposited at room temperature in significantly shorter time (vs. 1$^1/_2$ days by spin-coating) using AD process.
- Developed solution chemistry and synthesized and characterized PLZT submicron powders required for high-rate deposition processes.
- In FY13, published eleven papers in peer reviewed international journals, three papers in conference proceedings, and presented results at seven scientific conferences.
- Filed five patent applications.

✧　　　✧　　　✧　　　✧　　　✧

Introduction

Power inverter modules are a critical subsystem within electric drive vehicles (EDVs) and their performance directly affects fuel efficiency and battery life. Capacitors occupy ≈35% of the inverter volume and account for ≈23% of the weight in current designs. Thus, even if all other components in an inverter are reduced significantly, the capacitor requirement is a serious impediment to achieving the required volume and weight reduction. In addition, the use of high-temperature coolants further exacerbates the situation because existing film capacitors lose their capability to absorb ripple currents at elevated temperatures, necessitating the addition of extra capacitors. Increasing the volumetric performance (capacitance per unit volume) of DC bus capacitors is required, and their maximum operating temperature also must be increased to assure reliability requirements. Ceramic capacitors have the greatest potential for volume reduction; they could be as small as 20% of the volume of an aluminum electrolytic capacitor. Ceramics offer high dielectric constants and breakdown fields and, therefore, high energy densities. They also can tolerate high temperatures with a low equivalent series resistance (ESR), enabling them to carry high ripple currents even at elevated temperatures, although the capacitance may vary strongly with temperature.

Driven by the increasing demand for passive power electronics with improved performance, high reliability, and reduced size and weight, much attention has been paid to the so-called "film-on-foil" technology, in which ceramic films deposited on metal foils are embedded into a printed circuit board (PCB). Our research [1-4] had shown that the lead lanthanum zirconate titanate ($Pb_{0.92}La_{0.08}Zr_{0.52}Ti_{0.48}O_3$, PLZT) films deposited on base metal foils possess excellent dielectric properties, which are promising for high power applications such as plug-in hybrid electric vehicles. Use of base-metal foils reduces the cost of the capacitor. The stacked and embedded capacitors approaches significantly reduces component footprint, improves device performance, provides greater design flexibility, and offers an economic advantage for commercialization. This technology will achieve the high degree of packaging volumetric efficiency with less weight. Device reliability is improved because the number and size of interconnections are reduced. The vision of embedded DC bus capacitors is compelling and offers U.S. automotive companies a substantial technological advantage over their foreign counterparts.

In power electronics, capacitors with high capacitance are required to work under high voltages. This requirement imposes the additional challenge of fabricating thicker (>3 μm) films. However, due to the well-known critical thickness effect, per-layer thickness that can be achieved by conventional sol-gel method is generally limited to ≈0.1 μm, thus making the conventional method less attractive to industry when thicker films are needed to meet the operation voltage requirement.

Our approach uses ferroelectric thin films (PLZT) on base-metal foils (film-on-foils) that are either stacked on or embedded into PCBs. Embedded film-on-foil capacitors

reduce the component footprint area, shorten interconnect lengths, and reduce parasitic inductive losses and electromagnetic interference. Reliability is improved because the number and size of interconnects are reduced. Solder joints that are most susceptible to failure are no longer needed.

Our R&D efforts focus on examining the underpinning issues of film-on-foil capacitor performance and reliability, developing low cost capacitor designs, making multilayer film-on-foil capacitors, fabricating high-voltage-capable film-on-foil capacitors defined by the inverter application requirements, establishing robust fabrication protocols that are commercially and economically viable, and transferring the technology to industry for manufacturing.

Approach

Develop high-dielectric constant, high-temperature, low-cost ferroelectric PLZT dielectric films on base-metal foils and establish high-rate deposition process to economically make the advanced high-temperature capacitors. Ferroelectrics possess high dielectric constants, breakdown fields, and insulation resistance. With their ability to withstand high temperatures, they can tolerate high ripple currents at under-the-hood conditions. Stacked and/or embedded capacitors significantly reduce component footprint, improve device performance, provide greater design and packaging flexibility, achieve high degree of volumetric efficiency with less weight, and offer an economic advantage. A high-rate room-temperature deposition process, aerosol deposition (AD), has been identified as an economically attractive process to make PLZT-based capacitors. Future effort will be focused on developing the AD process to fabricate PLZT-based capacitors.

Results

We have developed a core technology for fabricating PLZT on Ni foils with $LaNiO_3$ (LNO) buffer layers by a chemical solution deposition (CSD) process [5]. CSD solutions were synthesized and films were deposited by spin coating. High purity (99.98% pure) nickel substrates with dimensions of 25 mm × 25 mm × 0.4 mm were obtained from MTI Corp. (Richmond, California). They were polished by chemical-mechanical planarization (CMP) process. A root-mean-square surface roughness of ≈2 nm was measured by atomic force microscopy (AFM) in the tapping mode with 5 μm × 5 μm scan size. Prior to being coated, CMP nickel substrates were ultrasonically cleaned in distilled water, and then wipe-cleaned with acetone and methanol in sequence. The detailed procedure is reported elsewhere [5,6]. The LNO solution was spin-coated onto the substrate at 3000 rpm for 30 sec, pyrolyzed at ≈450°C for 5-10 min, and crystallized at ≈650°C for 2-5 min. This process was repeated five times to build the desired thickness with a final annealing at ≈650°C for 20 min. The PLZT stock solution was spin-coated onto the LNO-buffered substrate at 3000 rpm for 30 sec. Films were then pyrolyzed at ≈450°C for 10 min and crystallized at ≈650°C for

2-5 min, followed by a final annealing at ≈650°C for 20 min after repeating the coating steps to build up layers of sufficient thickness. By this process, we have fabricated PLZT films with thicknesses up to ≈3 μm. Platinum top electrodes were then deposited by electron beam evaporation using a shadow mask. These electrodes had diameters of 250 μm, 750 μm, 5 mm and 20 mm and thickness of ≈100 nm. Films with top electrodes were annealed at ≈450°C in air for 2 min for electrode conditioning. A Signatone QuieTemp® probe system with heatable vacuum chuck (Lucas Signatone Corp., Gilroy, CA) was used for electrical characterization. For the electrical measurements, the Pt/PLZT/LNO/Ni hetero-structure was contacted by a Pt top electrode pad with one probe and the substrate (bottom electrode) with the other. A positive applied voltage corresponds to the configuration where the top electrode is at a higher potential than the bottom electrode. An Agilent E4980A Precision LCR Meter measured the capacitance and dissipation factor under applied bias field. A Radiant Technologies' Precision Premier II tester measured the hysteresis loops. The capacitor samples were immersed in Fluka silicone oil (Sigma-Aldrich) during high-field hysteresis loops and dielectric breakdown measurements. A Keithley 237 high-voltage source meter measured the current-voltage characteristics. The leakage current density was determined by fitting the current density relaxation data to the Curie-von Schweidler equation [7]. Residual stress in the film was studied by X-ray diffraction [8] method using a Bruker AXS D8 diffraction system.

The PLZT films grown on LNO-buffered Ni foils were phase pure with no preferred crystallographic orientation, and no crack or delamination was observed from SEM [5]. The use of LNO buffer allows the film-on-foils to be processed in air without the formation of a parasitic interfacial nickel oxide layer. The LNO also compensates for the roughness of the Ni foil and provides a smooth interface for the PLZT films, resulting in higher breakdown strengths. In addition, the LNO buffer helps to reduce the compressive strain in the PLZT films deposited on nickel substrates due to the thermal expansion coefficient mismatch between PLZT and metal foils [9,10].

To investigate the effect of film thickness on residual stress, PLZT films of 3, 6, 12, 18, and 27 layers of coatings were grown on platinized silicon (PtSi) substrates by chemical solution deposition. Their corresponding thicknesses are 0.35, 0.69, 1.38, 2.07, and 3.1 μm as determined from SEM. All samples were dense and well crystallized, and were free of impurity phases and microcracks. Figure III-113 shows the regular 2θ scan XRD patterns of PLZT films with various thicknesses grown on PtSi substrates. The XRD patterns of a PtSi substrate without PLZT coating exposed to the same heat treatment (marked by "PtSi") and that of bulk PLZT 8/52/48 (marked by "Bulk") are also shown in Figure III-113 for reference. Bulk PLZT material exhibits a tetragonal structure [11] with lattice parameters a = 4.042 ± 0.002 Å, c = 4.068 ± 0.005 Å, and tetragonality c/a = 1.0065. While diffraction peaks of PLZT films can be indexed according to a pseudocubic perovskite structure (JCPDS 56-0900). The two tiny peaks (at 2θ ≈34.5° and ≈36°) marked by open triangles are associated with Cu-K$_\beta$ diffraction peaks of PLZT (111) and

Pt (111), while the small peak (at 2θ ≈28°) marked by open square belongs to Cu-K$_\beta$ peaks of PLZT (110). Pt (111) diffraction peaks are visible from diffraction patterns of all samples used in this study, indicating that x-ray probed through the entire thickness for all PLZT films during XRD measurements.
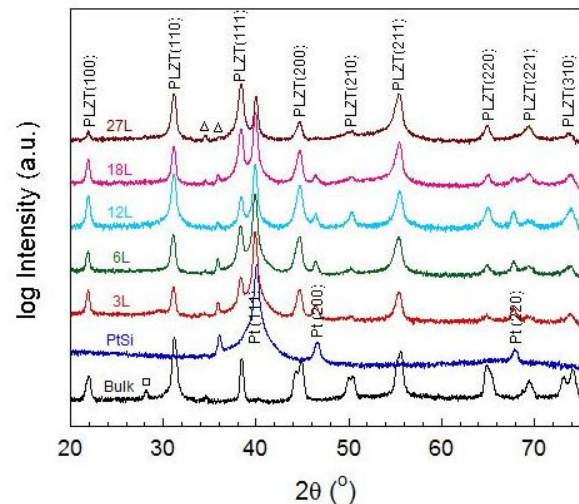
Figure III-113: Room temperature x-ray diffraction patterns of PLZT films of different thicknesses grown on PtSi substrates.

Figure III-114 shows the in-plane lattice parameter and lattice strain as a function of film thicknesses for PLZT films. The pseudo-cubic lattice parameter of bulk PLZT was also plotted in the figure for reference (shown by dashed line). We assumed that unstressed PLZT film adapts the pseudo-cubic lattice parameter of bulk material. The in-plane lattice parameters were determined by off-axis diffraction. We found that in-plane lattice parameter a decreased from 4.072 Å to 4.058 Å when film thickness increased from 0.35 μm to 3.1 μm, gradually approximating the pseudo-cubic lattice parameter of 4.051 Å for the bulk PLZT. This indicates that PLZT films grown on PtSi substrates are under tensile stress, and accordingly the strain (as defined as relative change in lattice constant) decreases with increasing film thickness from ≈0.5% to ≈0.2% during the same increase in film thickness. It is worth noting that the strain or stress determined from XRD is an average across the thickness of the films under investigation. The microscopic stress in a film may actually vary across the thickness, with higher values at the film-substrate interface and lower values at the free-standing top surface.
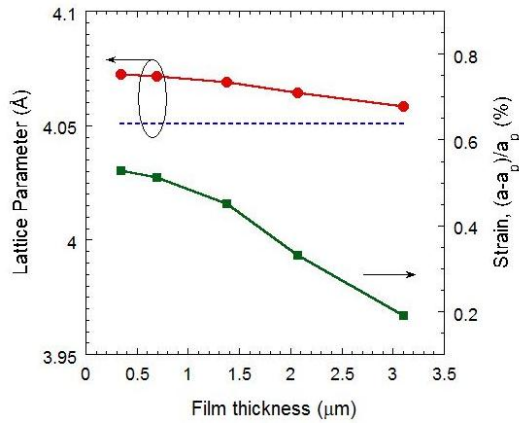
Figure III-114: In-plane lattice parameter and lattice strain of PLZT films of various thicknesses grown on PtSi substrates.

Figure III-115 shows XRD patterns measured with sample tilt angle ψ = 0, 15, 30, 45, and 60° for a 12-layer (1.38 μm thick) PLZT film grown on PtSi substrate. The intensities of the PLZT peaks are nearly independent of the tilt angle, indicating that the PLZT film is not textured. On the other hand, the intensity of the Pt peak varies with the sample tilt angle. For example, we observed a maximum intensity at ψ = 30° for the Pt (220) peak and at ψ = 60° for the Pt (200) peak. This is consistent with the fact that Pt film is textured with (111) planes parallel to the substrate surface. Due to the fact that the angle between the (111) and (110) planes is ≈35° and the angle between (111) and (100) is ≈55°, we observed the highest diffraction peak intensities at ψ = 35° and 55° for the Pt (220) and the Pt (200) diffraction planes, respectively. A similar trend was observed for samples with different thicknesses. A careful look at the diffraction peaks revealed that PLZT diffraction peaks shift to lower 2θ angle with increasing ψ, indicating an overall tensile residual stress in the PLZT film grown on the PtSi substrate. Residual stress σ_ϕ can be estimated with the following formula [8],

$$\sigma_\phi = \left(\frac{E}{1+\nu} \right)_{(hkl)} \cdot \frac{1}{d_{\phi 0}} \cdot \frac{\partial d_{\phi\psi}}{\partial \sin^2 \psi} \tag{1}$$

where E and ν are Young's modulus and Poisson ratio of the thin film, and $d_{\phi 0}$ and $d_{\phi\psi}$ are the lattice d-spacing in a stressed sample that was measured at tilt angles of zero and ψ, respectively. Experimentally, stress in the thin film sample can be calculated by performing a linear fit of the d-spacing measured at various tilt angles as a function of $\sin^2\psi$, then plugging the measured slope into Eq. 1. Values for Young's modulus, Poisson ratio, and coefficient of thermal expansion (CTE) of the thin film materials used in our study are listed in Table III-7. In general, stress in a thin film can come from various sources, such as lattice mismatch stress due to epitaxial growth (σ_{epi}), intrinsic stress (σ_{int}) introduced by a particular growth process, thermal stress (σ_{th}) due to sample heating and/or cooling, and transformational stress (σ_{tr}) caused by structural phase transformation [12].
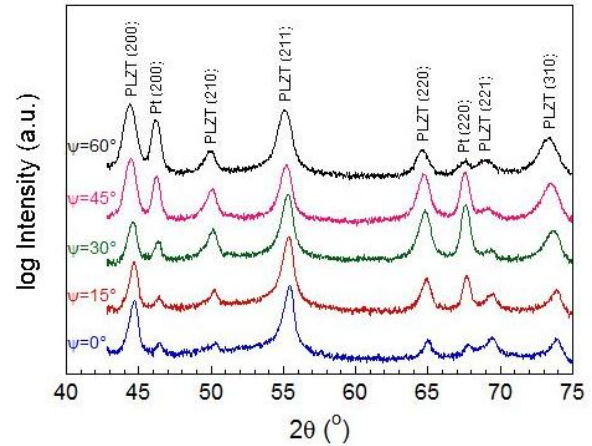
Figure III-115: X-ray diffraction patterns measured with various tilt angles on 1.38-μm-thick PLZT grown on PtSi substrate.

Table III-7: Young's modulus (E), Poisson ratio (ν), and coefficient of thermal expansion (CTE) of relevant materials.

Material	E (GPa)	ν	CTE, α (x10⁻⁶/k)
Ti	116	0.32	8.6
Ni	200	0.31	13.4
Pt	168	0.39	8.8
Si	130	0.28	3.6
SiO$_2$	70	0.17	0.55
TiO$_2$	230	0.28	8.2
PLZT	72	0.30	5.4

The total stress is a sum of all contributing factors σ_{tot} = $\sigma_{epi} + \sigma_{int} + \sigma_{th} + \sigma_{tr}$. The polycrystalline PLZT films fabricated by chemical solution deposition are not textured, and the materials did not undergo phase transformation during our study. Therefore, out of those four identified factors, only intrinsic stress σ_{int} and thermal stress σ_{th} are relevant to our investigation. The intrinsic stress (also known as growth stress) originates from the cumulative effect of structural imperfections that appear on the film during deposition. Its magnitude is largely determined by the processing conditions. Thermal stress in a film can be expressed as [13],

$$\sigma_{th} = \frac{E_f}{1 - \nu_f} \varepsilon_{th} \tag{2}$$

and the corresponding thermal strain is determined by,

$$\varepsilon_{th} = \int_{T_0}^{T_{ann}} (\alpha_f - \alpha_s) dT \tag{3}$$

where E_f and ν_f are the Young's modulus and the Poisson ratio of the thin film material, and ε_{th} the thermal strain, and α_f and α_s are the coefficient of thermal expansion for the film and the substrate, respectively. Due to difference in CTE between PLZT film and its substrate, a tensile strain is formed in PLZT grown on PtSi substrate and a compressive strain is generated in PLZT grown on nickel substrate, during cooling of the sample from annealing temperature, T_{ann}. As shown in Figure III-116, we measured tensile stress in PLZT frown on PtSi and compressive stress in PLZT grown on LNO buffered nickel. Our experimental results agree with predictions derived

from Eqs. (2) and (3). A compressive strain in PLZT dielectric is benefitial to enhanced dielectric strength [14].
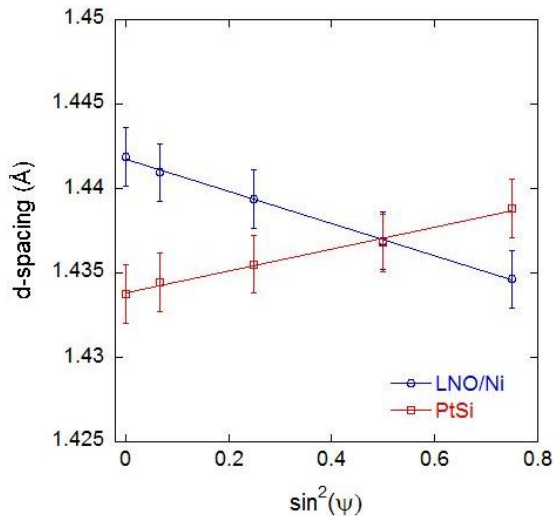
Figure III-116: Lattice d-spacing as a function of $\sin^2\psi$ measured from PLZT (220) diffraction peaks.

Figure III-117 illustrated the correlation between the mean breakdown strength and residual stress for PLZT films. Breakdown strength decreases with increasing residual stress. Mean breakdown strength of $\approx 1.8 \times 10^6$ V/cm can be predicted for PLZT films with no residual stress. If we could make a sample bearing a compressive stress of -800 MPa, it should exhibit breakdown strength of $\approx 3 \times 10^6$ V/cm. On the other hand, breakdown strength of $\approx 1 \times 10^6$ V/cm can be expected for PLZT film bearing a tensile stress of 500 MPa. This experimental finding is instructive for packaging design of multilayer embedded capacitors.
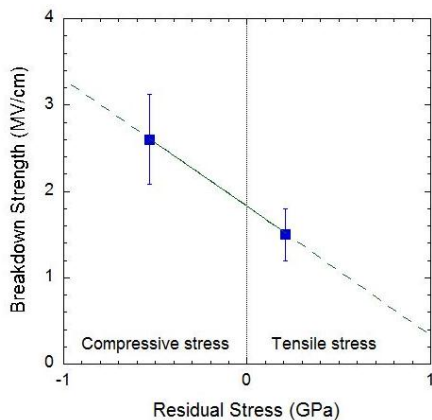
Figure III-117: Correlation between breakdown strength and residual stress in PLZT films.

We investigated the effect of ultra-thin (≈ 5 nm) insertion layer on dielectric properties and breakdown strength of PLZT film capacitors. Figure III-118 showed cross-sectional SEM images of PLZT films grown PtSi substrates with and without ZrO$_2$ insertion layers that were deposited by magnetron sputtering [14]. These films do not contain any obvious defects or other secondary phases, which is also confirmed by x-ray diffraction pattern.
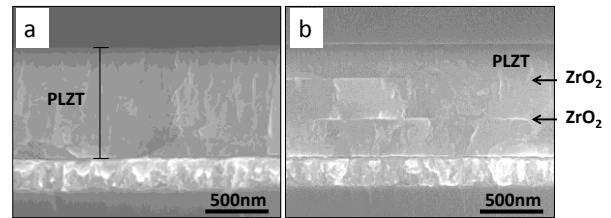
Figure III-118: Scanning electron microscopy cross-sectional images of (a) pure PLZT film and (b) PLZT/ZrO$_2$ film on Pt-Si substrates.

Figure III-119 shows the frequency dependence of the dielectric permittivity and loss tangent measured for PLZT thin films grown on PtSi substrates with and without ZrO$_2$ insertion layers at room temperature. At 10 kHz, dielectric permittivity for Pt/PLZT/Pt and Pt/PLZT/ZrO$_2$/PLZT/ZrO$_2$/PLZT/Pt are ≈ 1370 and ≈ 820, respectively; the corresponding values for dielectric loss are 0.033 and 0.026. The lower permittivity and dielectric loss for the PLZT/ZrO$_2$ films is likely due to the introduction of the low-permittivity ZrO$_2$ insertion layers. The effective permittivity of multilayered films can be determined by series combination of capacitors, while assuming that the interdiffusion between PLZT and ZrO$_2$ is negligible. The effective permittivity ε_{eff} can then be calculated via the series capacitor model,

$$\frac{t_{total}}{\varepsilon_{eff}} = \frac{t_{plzt}}{\varepsilon_{plzt}} + \frac{t_{ZrO_2}}{\varepsilon_{ZrO_2}} \qquad (4)$$

where t_{total} is the total thickness of PLZT/ZrO$_2$ multilayered films, and t_{plzt} and t_{ZrO_2} are the thickness of PLZT and ZrO$_2$, respectively. Also, ε_{eff} is the effective permittivity of, whereas ε_{plzt} is the permittivity for PLZT films, which is about 1370 at 10 kHz in this study, and ε_{ZrO_2} is the permittivity of ZrO$_2$, which is near 25 [15]. The calculated ε_{eff} from equation (4) is 780 for PLZT thin films with two insertion layers of ZrO$_2$, which is very close to the experimental value of 820. Over the frequency range 0.1-1000 kHz, measured values are in good agreement with the calculated ones. This finding indicates no significant interdiffusion between the PLZT and ZrO$_2$ layers.
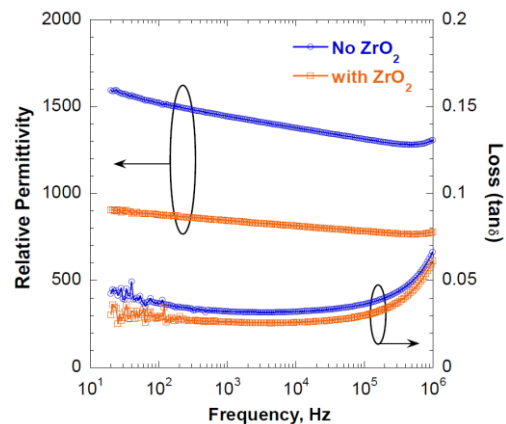
Figure III-119: Frequency dependent dielectric properties of (a) pure PLZT and (b) with ZrO$_2$ insertion layers.

Figure III-120 shows time relaxation leakage current density measured under E ≈60 kV/cm load at different temperatures for the PLZT film with and without ZrO_2 insertion layers. The leakage current density of PLZT/ZrO_2 multilayered films is lower than that of pure PLZT films at all temperatures. Upon increasing the temperature from RT to 300ºC, the leakage current density increased for both samples. For example, over this temperature range at 100 s, the leakage current density increased from ≈4.3 × 10^{-8} A/cm^2 to ≈1.3 × 10^{-5} A/cm^2 for PLZT/ZrO_2 films and ≈6.0 × 10^{-8} A/cm^2 to ≈2.1 × 10^{-5} A/cm^2 for pure PLZT thin films without ZrO_2 insertion layers.
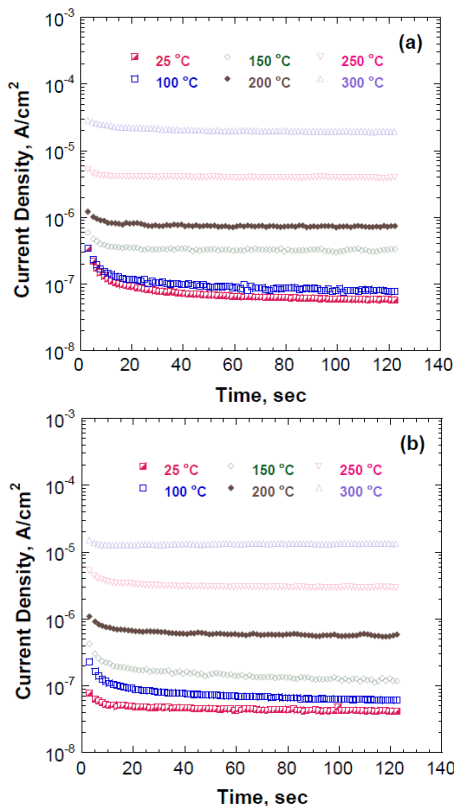
Figure III-120: Leakage current density at different temperatures for (a) pure PLZT and (b) PLZT/ZrO_2 on Pt-Si substrates.

Dielectric breakdown strengths were measured at room temperature for PLZT films grown on PtSi substrates with and without TiO_2 insertion layers. Measurements were conducted with 20 specimens for each type of samples and the results were shown in Figure III-121 in Weibull plot. For samples with two insertion layers (Figure III-118b), we measured a mean breakdown strength that is more than 50% higher than that of samples without insertion layers.
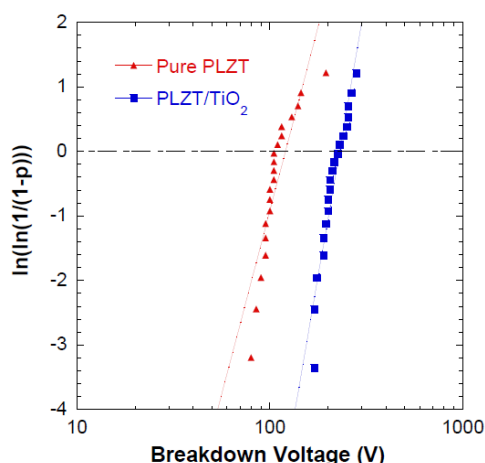
Figure III-121: Weibull plot of breakdown voltage measured for (a) pure PLZT and (b) PLZT/TiO_2 grown on Pt-Si substrates.

Figure III-122 showes the dielectric constant and loss measured as a function of bias field for an antiferroelectric PLZT (4/98/2) grown on PtSi substrate. At room temperature, we observed antiferroelectric to ferroelectric transition field of E_{AF} ≈310 kV/cm and the reverse transition (ferroelectric to antiferroelectric) field of E_{FA} ≈210 kV/cm. At zero bias and frequency of 10 kHz, the dielectric constant ≈350 and the dielectric loss ≈0.03 were observed.The antiferroelectricity was confirmed by the PE hysteresisloop as shown in Figure III-123.
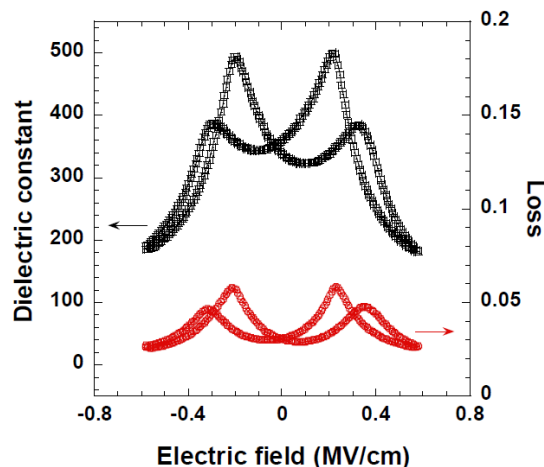
Figure III-122: Dielectric properties measured as a function of bias field for an antiferroelectric PLZT (4/98/2) film grown on PtSi substrate.
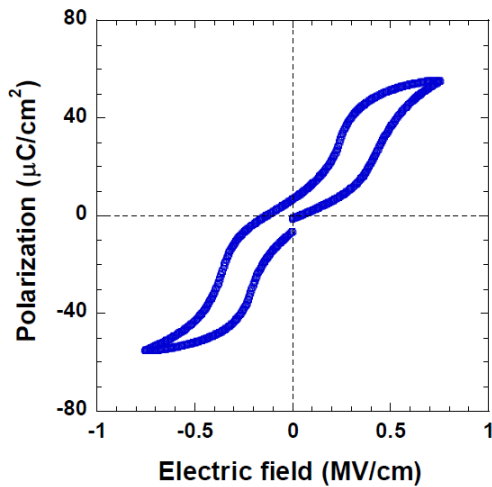
Figure III-123: PE hysteresis loop of an antiferroelectric PLZT (4/98/2) film capacitor grown on PtSi substrate.

Figure III-124 plotted the transition fields E_{AF} and E_{FA} as a function of temperature determined from the field-induced state transition. ΔE is the difference between these two phase transition fields ($\Delta E = E_{FA} - E_{AF}$). The difference between E_{AF} and E_{FA} decreases as the temperature increases. At room temperature, AFE-to-FE and the reverse FE-to-AFE transition occurs at DC bias field $E_{AF} \approx 310$ kV/cm and $E_{FA} \approx 210$ kV/cm, respectively. A thermal-induced AFE-to-PE phase transition occurs at a temperature $T_c \approx 225°C$, above which $\Delta E = 0$ and the material is paraelectric. Below this temperature, the materials exhibit antiferroelectric property which is desirable for energy storage applications. We have measured energy density of 61 J/cm^3 for the AFE PLZT (4/98/2) film capacitor grown on PtSi substrate.
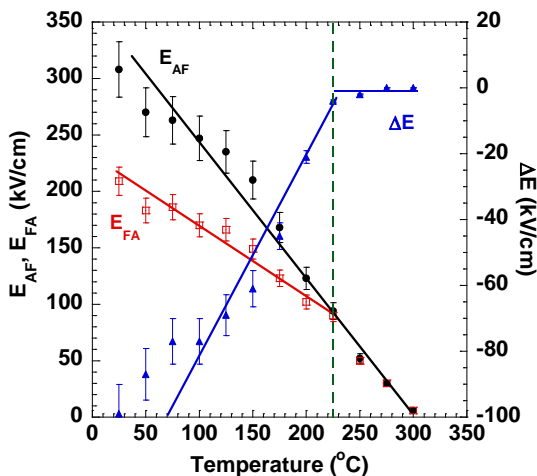
Figure III-124: Temperature-dependent phase transition fields E_{AF}, E_{FA}, and ΔE.

Figure III-125 shows the capacitance and dielectric loss of a stacked capacitor with copper ribbon termination. Each film-on-foil capacitor has two copper ribbons attacked as electrical leads. Testing was conducted at room temperature as a function of applied bias up to 100 V. We measured capacitance of ≈8.6 μF and dielectric loss of ≈0.05 for this

stack at room temperature under zero bias. Both capacitance and dielectric loss decrease with increasing bias voltage. At 100 V bias, we measured capacitance of ≈2.5 μF and dielectric loss of <0.01.
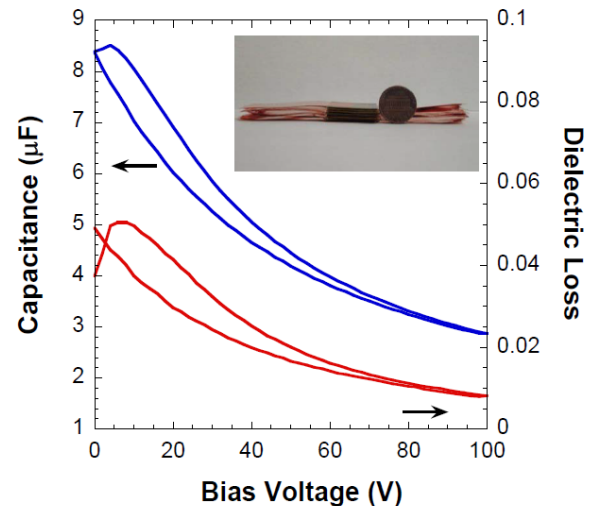
Figure III-125: Capacitance and dielectric loss measured as a function of bias voltage for a stacked capacitor.

Capacitance and dielectric loss tanδ measured as function of frequency for the multilayer stack is plotted in Figure III-126. The test was conducted at room temperature under 70 V and 100 V applied bias. The blue line is for data measured with 70 V bias; and the black line shows data measured with 100 V bias. ESR decreases with increasing frequency as expected from the following equation,

$$ESR = \frac{\tan\delta}{2\pi f \cdot C} \tag{5}$$

where tanδ is the dielectric loss, f the frequency, and C the capacitance. We observed decrease in ESR as the bias voltage was increased from 70 to 100 V in the frequency range 1 to10 kHz, as shown in Figure III-127. At higher frequencies (>10 kHz), the measured ESR with 70 V and 100 V bias are virtually identical. Also shown in Figure III-127 is the ESR for a 1000 μF capacitor (shown in red color) calculated from the ESR measured on the small multilayer stack. We found the ESR for a 1000 μF capacitor to be ≤1 mΩ at frequencies >1 kHz. This meets the APEEM goal of <3 mΩ for applications in advanced power inverters.

The research done in this phase of the project demonstrated that the dielectric constant of spin-coated PLZT film-on-foil is ≈30 times that of the currently used polypropylene-based materials over the temperature, voltage and frequency ranges required for automotive power electronics. PLZT's temperature capability also meets or exceeds the temperature requirement for today's automotive environment; however, the spin coating process requires over thirty depositions, more than thirty annealing steps, and many hours to produce a simple 3-μm-thick PLZT coating suitable for a capacitor. The spin-coating process is simply impractical on an industrial scale. Therefore, effort was focused on developing a high-rate deposition process. We have identified
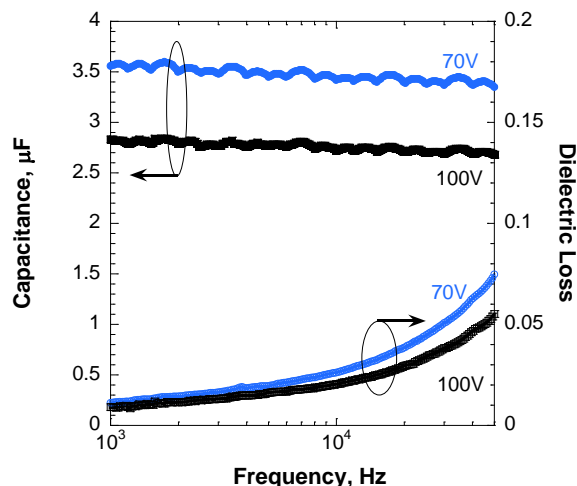
Figure III-126: Frequency dependent capacitance and dielectric loss measured for a stacked capacitor at 70 V and 100 V bias.
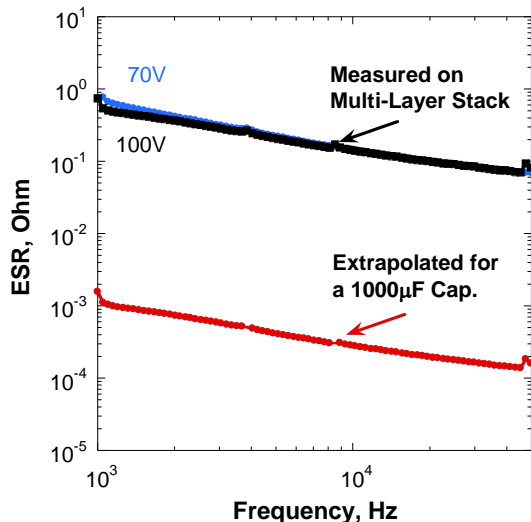
Figure III-127: Frequency dependent ESR measured for a stacked capacitor at 70 V and 100 V bias along with that calculated for a 1000 µF capacitor.

aerosol deposition (AD) as a high-rate deposition process to fabricate PLZT films. During AD, PLZT particles areaccelerated toward the substrate and, if their speed exceeds a critical value, the particles consolidate upon impact without-additional heating of the substrate. Because AD is done without heating the substrate, flexible materials such as polymers, plastics, thin metal foils, glass, etc. can be used as the substrate. By using flexible substrates, PLZT-based capacitors can be produced in a wound configuration, which would allow APEEM's requirement of benign failure to be engineered for the capacitor. Recent work at Argonne demonstrated that a ≈3-µm-thick PLZT film can be prepared in about 20 minutes by AD process. Sample of similar thickness deposited by spin-coating process would take more than a day and half to make.

Figure III-128 a shows a photograph of the AD system built at Argonne. AD process can produce dense PLZT films at room temperature on virtually any type of substrates. Figure III-128b and Figure III-128c showed plan view and cross-sectional SEM microimages of a 3.2-µm-thick PLZT film deposited on PtSi substratea. This 3.2-µm-thick film was made by AD process in approximately 20 minutes.
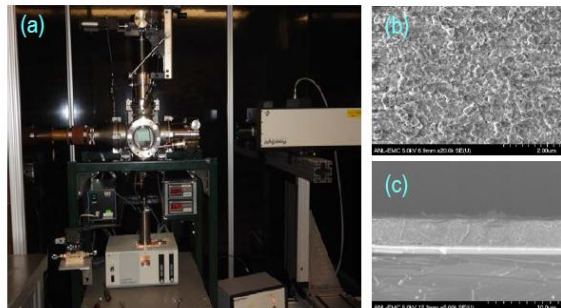
Figure III-128: (a) Photograph of an aerosol deposition system built at Argonne, (b) plan-view and (c) cross-sectional SEM images of PLZT film deposited using the AD system.

Figure III-129 shows a photograph of a PLZT film-on-foil capacitor fabricated using the aerosol deposition process. PLZT film of ≈4 µm thick was deposited on 8-µm-thick aluminum foil. Top electrodes were deposited by electron-beam evaporation before being wound on a pencile for electrical property testing, as shown in the photograph. This demonstrates the potential of using PLZT film-on-foils to fabricate wound/rolled capacitors similar to the currently used polymer film capacitors in power inverters for electric drive vehicles. PLZT ceramic films deposited on metal foils can withstand high operation temperatures without degradation in property. In addition, the high dielectric constant of ceramic dielectrics enables superb volumetric efficiency.
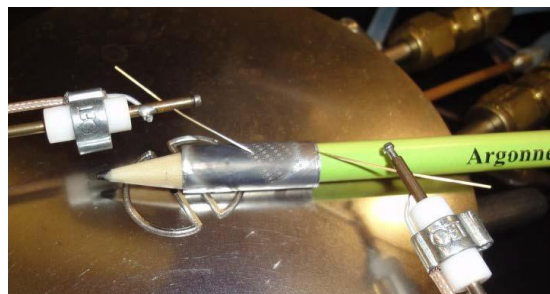
Figure III-129: Photograph of a wound PLZT film-on-foil capacitor on testing stage.

Figure III-130 shows the frequency dependent dielectric properties measured at different temperatures on a PLZT film-on-foil capacitor made by aerosol deposition process. We measured slight decrease in both dielectric constant and loss with increasing frequency. Dielectric constant increases while loss decreases with increasing temperature. We measured dielectric constant of ≈90 and loss ≈0.03 at 1 kHz and 150°C. This meets the APEEM goal of 150°C operation temperature requirement for application in advanced power inverters.
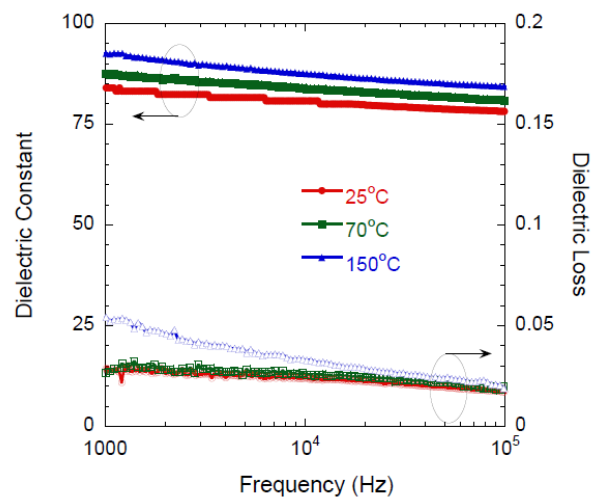
Figure III-130: Frequency dependent dielectric properties of PLZT film-on-foil capacitor deposited by AD process.

Figure III-131 shows the dielectric properties of an aerosol deposited PLZT film-on-foil capacitor measured at room temperature as a function of applied bias field. Dielectric constant exhibits weak dependence while dielectric loss is nearly independent of bias field. With 300V bias, we measured dielectric constant of ≈80 and loss <0.03 at room temperature. This dielectric constant value, under high electric field, is substantially higher than that of the polymer dielectrics (dielectric constant of ≈2.2) that are currently in use in power inverters. Our results demonstrate the great potential of PLZT capacitors meeting APEEM power inverter specifications.
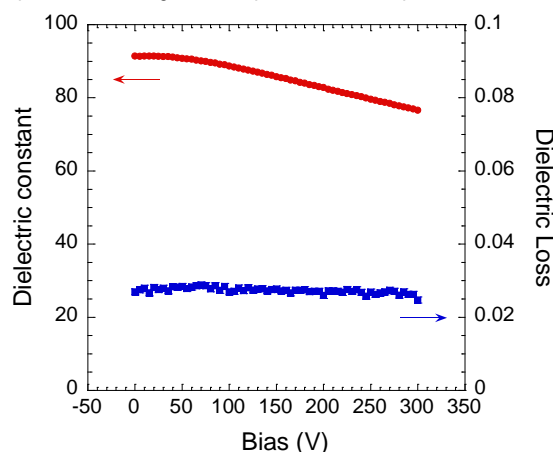
Figure III-131: Field dependent dielectric properties of PLZT film-on-foil capacitor deposited by AD process.

Figure III-132 shows a PE hysteresis loop measured for a PLZT film-on-foil capacitor deposited by AD process. Hysteresis data confired low-loss and weak dependence of dielectric constant on applied field. The sample retains its paraelectric behavior even at high applied field which is desirable for high power applications. From the hysteresis loop, we calculated a recoverable energy density of ≈12 J/cm³, as shown by the shaded area in Figure III-132. This energy density value measured for AD ceramic film is more than 6 times higher than that of the polypropylene thin films

(<2 J/cm³) [16]. Thus, it can potentially lead to superior volumetric efficiency when used in power electronic devices.
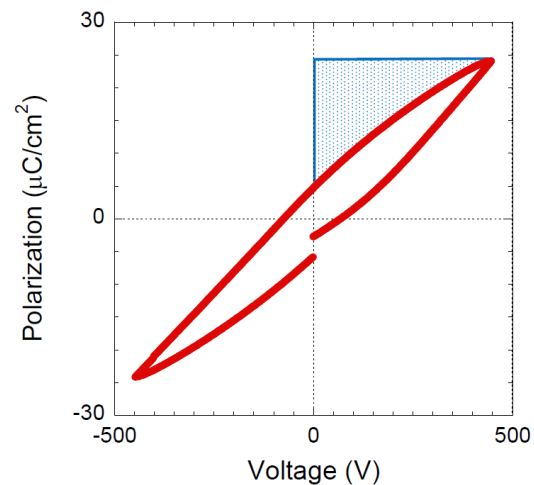
Figure III-132: PE hysteresisloop measured for a PLZT film-on-foil capacitor deposited by AD process.

Conclusions and Future Directions

We have developed a core technology for fabricating high capacitance density, high temperature ceramic PLZT films on base metal foils, called "film-on-foil" technology. PLZT film-on-foils have been fabricated by chemical solution deposition with LNO buffer layers atop Ni foils, allowing the capacitors to be processed in air. At 1 kHz and zero bias, we measured dielectric constant of ≈700 and dielectric loss of 0.04 at -50°C, dielectric constant of ≈1150 and dielectric loss of ≈0.05 at room temperature, and dielectric constant of ≈1900 and dielectric loss of ≈0.03 at 150°C, respectively. Film-on-foil samples were characterized under high bias fields. We measured dielectric constant of ≈230 and loss of ≈0.008 (0.8%) at 100 V bias, dielectric constant of ≈140 and loss of ≈0.005 (0.5%) at 200 V bias, dielectric constant of ≈110 and loss of ≈0.004 (0.4%) at 300 V bias on a ≈3-µm-thick PLZT film-on-foil sample. Film-on-foil capacitors with copper ribbon electrical leads were fabricated and characterized as function of temperature, applied bias, and frequency. At room temperature, we measured capacitance of ≈8.5 µF (unbiased condition) and ≈3 µF with 100 V bias. The properties measured show that these ceramic film capacitors have potential to meet the APEEM goals. Our results and the research plans were presented at the VT program's APEEM project kickoff, Annual Merit and Peer Review, and EE Tech Team meetings. The spin-coating method currently used to make PLZT films requires too many processing steps. During FY13, we have developed an aerosol deposition (AD) system at Argonne National Laboratory. AD technology allows deposition of dense ceramic films at room temperature with high deposition rate. Our initial investigation demonstrated that a ≈3.2 µm thick PLZT film can be deposited in about 20 minutes which is significantly faster than the spin-coating process which required more than a day and half to make. Preliminary characterization of film-on-foil capacitors fabricated by AD process revealed high dielectric constant,

low dielectric loss, weak-dependence on field, high recoverable energy density, and suitable for high field and high temperature operation. The AD process offers the greatest potential for producing low-cost, reliable, high temperature operational, compact and light-weight ceramic film capacitors for power electronics. The emphasis of FY14 effort is on developing and optimizing the AD process to make PLZT capacitors at faster rate to reduce manufacturing cost.

FY 2013 Peer Reviewed Publications

1. B. Ma, Z. Hu, S. Liu, S. Tong, M. Narayanan, R.E. Koritala, U. Balachandran, Temperature-dependent dielectric nonlinearity of relaxor ferroelectric $Pb_{0.92}La_{0.08}Zr_{0.52}Ti_{0.48}O_3$ thin films, *Appl. Phys. Lett.* **102**, 202901, 2013.

2. S. Tong, B. Ma, M. Narayanan, S. Liu, U. Balachandran, D. Shi, Dielectric behavior of lead lanthanum zirconate titanate thin films deposited on different electrodes/substrates, *Mater. Lett.* **106, 405, 2013.**

3. U. Balachandran, M. Narayanan, S. Liu, B. Ma, Development of film-on-foil ceramic dielectrics for embedded capacitors for power inverters in electric drive vehicles, *Jpn. J. Appl. Phys.* **52, 05DA10, 2013.**

4. S. Tong, M. Narayanan, B. Ma, S. Liu, R.E. Koritala, U. Balachandran, D. Shi, Effect of lanthanum content and substrate strain on structureal and electrical properties of lead lanthanum zirconate titanate thin films, *Mater. Chem. Phys.* **140, 427, 2013.**

5. S. Liu, B. Ma, M. Narayanan, S. Tong, Z. Hu, R.E. Koritala, U. Balachandran,Dielectric properties of lead lanthanum zirconate titanate thin films with and without ZrO_2 insertion layers, *J. Appl. Phys.* **113, 174107, 2013.**

6. B. Ma, S. Liu, S. Tong, M. Narayanan, R.E. Koritala, Z. Hu, U. Balachandran, Residual stress of $(Pb_{0.92}La_{0.08})(Zr_{0.52}Ti_{0.48})O3$ films grown by sol-gel process, *Smart Mater. Struc.* **22, 055019, 2013.**

7. S. Tong, B. Ma, M. Narayanan, S. Liu, R.E. Koritala, U. Balachandran, D. Shi, Lead lanthanum zirconate titanate ceramic thin films for energy storage, *ACS Appl. Mater. Interfaces* **5, 1474, 2013.**

8. B. Ma, Z. Hu, S. Liu, S. Tong, M. Narayanan, U. Balachandran, Temperature dependent polarization switching properties of ferroelectric $Pb_{0.92}La_{0.08}Zr_{0.52}Ti_{0.48}O_6$ films grown on nickel foils, *Appl. Phys. Lett.* **102, 072901, 2013.**

9. M. Narayanan, S. Tong, S. Liu, B. Ma, U. Balachandran, Estimation of intrinsic contribution to dielectric response of $Pb_{0.92}La_{0.08}Zr_{0.52}Ti_{0.48}O_3$ thin films at low frequencies using high bias fields, *Appl. Phys. Lett.* **102, 062906, 2013.**

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11. B. Ma, S. Liu, M. Narayanan, S. Tong, U. Balachandran, Development of high dielectric strength ceramic film capacitors for advanced power electronics, *J. Micro. Elect. Pack.* **10, 1, 2013.**

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III.8. High Temperature Dielectric Film Capacitors

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Start Date: September 2010
Projected End Date: April 2014

Objectives

Our project goal is to develop an inexpensive replacement high energy density, high temperature polymer-based dielectric for DC bus capacitors for use in next generation hybrid electric vehicles (HEVs), plug in hybrid electric vehicles (pHEVs), and electric vehicles (EV). The improved capacitors will be based on novel inexpensive, high temperature polymer thin film dielectrics that have much of the chemical functionality of the known high temperature polymer Kapton®.

Technical Barriers

DC bus capacitors are currently the largest and the least reliable component of fuel cell and electric hybrid vehicle inverters. Capacitors represent up to 23% of both inverter weight and inverter cost and up to 35% of the inverter volume. Furthermore, existing DC bus capacitors cannot tolerate temperatures greater than 120°C and require the use of a cooling loop to maintain proper operating temperatures. High temperature polymer dielectrics would remove the need for thermal management and lower packing costs.

Technical Targets

Our technical goal is to enhance high temperature performance and volumetric efficiency compared to present dielectrics. Specific metrics include the development of polymer film dielectrics with dissipation factors of 0.02 or less at 150 °C. Synthesis, fabrication, and high temperature (room temperature to 150 °C) characterization of these dielectric materials is an integral part of the material development program. This year, we investigated inexpensive organic molecules to increase dielectric breakdown voltages in order

to reduce capacitor size, by increasing the overall energy storage density. In addition, work has commenced on polymer extrusion of our novel high temperature dielectric film in order to verify its compatibility to industrial processes. Unfortunately we were unable to optimize the polymer extrusion of our dielectrics due to thermal degradation and limited molecular weight ranges. However, we have identified a path forward to polymer extrusion by slightly modifying the backbone of our original material and resulted in superior dielectric and physical properties.

Accomplishments

- Investigated voltage stabilizing agents to improve energy density and resulted in nearly doubling the energy density
- Purchased and installed stand-alone extrusion equipment at Sandia in order to produce rolls of polymer dielectrics
- Polymer extruded several kilograms of material and fabricated capacitors of extruded films
- Identified another polynorbornene-based material as a possible next generation dielectric with better physical properties and more suited for polymer extrusion

✧   ✧   ✧   ✧   ✧

Introduction

Our R&D is important to the DOE Office of Vehicle Technologies since we are reducing the size of the largest component in the inverter: the dc bus capacitor. Further, we are increasing the operating temperature of the dc bus capacitor to 150 °C. Studies by Semikron indicates that the operating temperatures of 150 °C will eliminate the need for the cooling loop in the inverter and lead to a potential cost savings. Our goal is to reduce the size of presently available polypropylene, polyphenylene sulfide and barium titanate based capacitors by a factor of two. Presently, polyphenylene sulfide (PPS) is the highest performance, high temperature polymer film dielectric. It has a dielectric constant of 3.1, however, a major limitation of PPS is that the material is relatively expensive and has a tendency to fail as shorts.

Recently we have developed polymer chemistry that has resulted in flexible polymer films with a dielectric constant of 3.1 and a dissipation factor of 0.008 at 170°C meeting DOE FreedomCAR requirements. These high energy density dielectrics will reduce capacitor volume and weight significantly. Reduction in the size and weight of the DC bus capacitor will help meet FreedomCAR peak power to weight and volume ratios.

Approach

Sandia National Laboratory's (Sandia) capacitor research and development (R&D) program addresses the high temperature capacitor technology gap in an innovative manner. We are developing high performance, high temperature, low cost capacitors that are based on novel Sandia developed polymer chemistry. Capacitors fabricated using this polymer technology will achieve a high degree of packaging volumetric efficiency with less weight while maintaining a cost of less than $0.03 per µF. Our R&D specific efforts focused on two targets 1) Inexpensive nanoparticle fillers that increase dielectric breakdown strength to further decrease capacitor volume to meet the DOE APEEM program goals 2) Investigate low cost film production of the Sandia dielectric by polymer extrusion, which will help verify commercial feasibility of these materials.

Results

1.0. Voltage stabilizing agents to increase energy storage density

For the past three years Sandia has been developing a novel high temperature dielectric based on a co-polymer of N-phenyl-7-oxanorbornene [poly(PhONDI)] and norbornene [poly(NB)]. The composition of the polymer was selected due to the presence of the polar imidie functionality that increases the dipole moment and thus the dielectric of the material. The imidie unit is attached to a norbornene, which are readily polymerized via Grubbs catalysts and are low cost materials. Early work found that the unsaturated positions (double bonds) were causing film casting issues so reduction of the polymer was performed and resulted in improved polymer solubility and stability (Scheme 1)
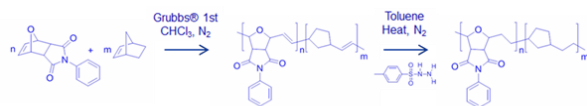
Scheme 1: Synthesis of hydrogenated co-polymer poly(PhONDI)-poly(NB).

The dielectric constant of the co-polymer at a 75%-25% poly(PhONDI)-poly(NB) was found to be 3.08 with a breakdown strength of 350 V/µm and an energy density of 1.62 J/cm3. The Tg of the material was measured at ~175°C, which allows temperature stability of greater than 150°C.

Initially the dielectric was solvent cast into thin films and the capacitors were fabricated using a stacked process. A series of prototype capacitors were developed using a drawdown-based solvent casting technique with a layering of the films (~20 µm thick) and thin films of aluminum foil (~6 µm). Two layers of polymer dielectric were used to minimize the possibility of film defect causing a short. The packaged capacitors (Figure III-133 top) has a scaled volume of 9.6 liters (based on initial packaging results) for a 1000 µF capacitor; far smaller than the 21.6 liters of current high temperature capacitors. More recent work has demonstrated the use of a

rolled form to produce high temperature capacitors with reduced volume (reduced by five times) relative to the stacked capacitors (based on initial packaging results). The volume reduction of the rolled capacitors is readily apparent in a comparison of the prototype forms, each with a similar capacitance of ~1 µF as shown in Figure III-133 bottom. While the initial volumes of the capacitors fabricated using the Sandia developed polymer are a great improvement in cost, volume, and weight relative to commercially available dielectric materials, they do not meet the VT volume goal.

Figure III-133: Stacked capcitor (top) Stacked vs. rolled.

Hunt *et al.,* discusses a series of certain chemicals that act as voltage stabilizers and offer protection from the effect of small defects in insulation materials such as polyethylene. Therefore, four additives were chosen from this series of organic chemicals and examined in an attempt to increase the breakdown strength of the 75%-25% poly(PhONDI)-poly(NB) by acting as protection from these imperfections. Dielectric permittivity and breakdown testing were performed to determine the effect of the additives; 2- and 4-nitrodiphenylamine (NDPA), 4-nitrophenol and 2- nitroaniline.

Due to the brevity of this report, only the highest performing additive will be discussed, which was 2-nitrodiphenylamine (2-NDPA). The incorporation of 2-NDPA showed an increase in breakdown strength (Figure III-134) of greater than 50 V/µm at 0.2% and 1.0% (w/w) and an increase of ~25 V/µm at 0.5% from the control 75%-25% poly(PhONDI)-poly(NB) without a significant increase in dielectric constant or dissipation factor but an increase in energy density in the three aforementioned samples (Table III-8).

The 0.2% and 1.0% (w/w) compositions were compared to 75%-25% poly(PhONDI)-poly(NB) control films using various thermal and mechanical characterization techniques. Differential scanning calorimetry (DSC) and thermogravimetric analysis (TGA) were performed to determine the effect of the additive on Tg and decomposition temperature (Td) respectively. 2- NDPA was not found to have any significant deteriorating effect on either value as clearly shown in Figure III-135. Characterization was performed to investigate the effect of 2-NDPA in 75%-25% poly(PhONDI)-poly(NB) on the films' mechanical properties. A stress-strain

curve was developed using dynamic mechanical analysis (DMA) for
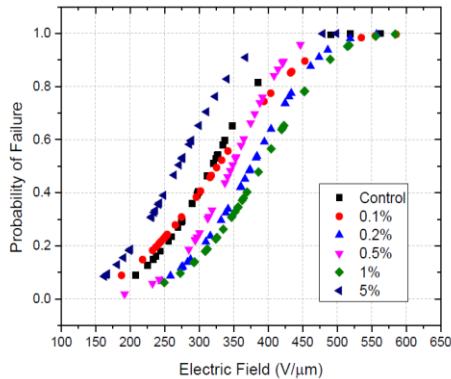
Figure III-134: Breakdown results for 2-NDPA polymer-additive.

Table III-8: Measured breakdown strength and calculated energy density of additive/polymer film.

2-NDPA Concentration (w/w)	Breakdown (V/μm)	Energy Density (J/cm^3)
0	345	1.62
0.1	365	1.36
0.2	405	2.53
0.5	370	1.76
1.0	415	2.37
5.0	290	1.18

the 75%-25% poly(PhONDI)-poly(NB) additive films as found in Figure III-135. Slight improvements in modulus were observed with the additive and no negative consequences were observed.

The incorporation of 2-NDPA generated significant improvements in the dielectric properties of 75%-25% poly(PhONDI)-poly(NB) by increasing the breakdown strength of the material and leading to an increase in energy density.

2.0. Polymer Extrusion

In order to be a feasible option for the automobile industry, high temperature thin film polymer dielectrics must meet specific criteria. The materials and methods of developing these dielectrics must be inexpensive and simple to meet demand. Solvent casting of films would be cost-prohibitive on a large scale, and these films commonly have many defects when compared to melt-extrusion films. In order to withstand extrusion, the polymer dielectrics must be thermally stable at high temperatures (~220°C). In-house extrusion was performed on 75%-25% poly(PhONDI)-poly(NB) using the extruder purchased from Dr. Collin® shown in Figure III-136, but the resulting films were extremely brittle and were unable to be successfully rolled into prototype capacitor without shorting during dielectric permittivity measurements. Figure III-137 shows the comparison of a solvent cast 75%-25% poly(PhONDI)-poly(NB) film with an extruded film of relative thickness (~15 μm). Upon visual inspection defects are not apparent in solvent cast 75%-25% poly(PhONDI)-poly(NB) films and a relatively transparent film is produced via the drawdown method despite no special care being taken to prevent

particulates from accumulating in the polymer films. A clean room would be
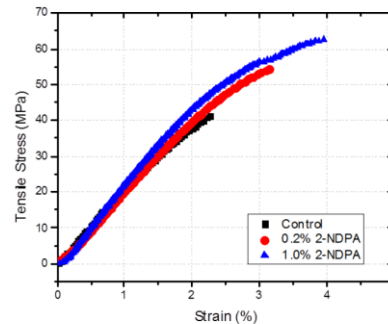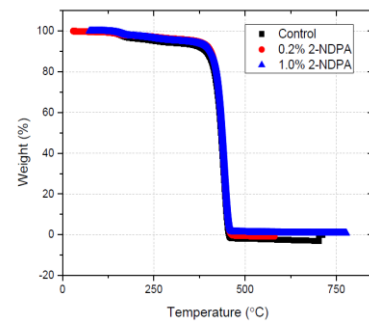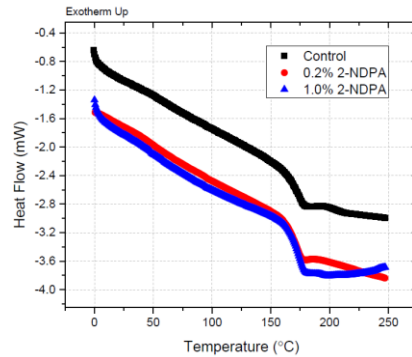
Figure III-135: DSC, TGA and DMA of 2-NDPA additive-polymer film.

Figure III-136: In house Dr. Collin extruder.
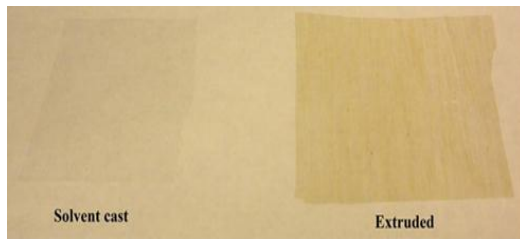
Figure III-137: Solvent cast vs. Extruded films.

necessary to completely limit this effect. Physical defects were initially observed in the extruded films as well as a color change when compared to solvent cast. As shown in Figure III-138, TGA was performed to determine if decomposition of the polymer was occurring during extrusion; however, no significant Td difference between extruded and solvent cast was observed. Additionally, dielectric permittivity measurements on the extruded film were not able to be performed due to the lack of quality of the film. Studies were performed evaluating the use of plasticizers in extruded polymer to increase flexibility. Plasticizers work by penetrating unused space of the polymer and increasing intermolecular distance resulting in swelling and increased free volume. The plasticizer essentially acts as a lubricant within the polymer allowing more chain mobility and therefore better flexibility. Additionally, the plasticizers allow the polymer to remain more ductile at lower temperatures by reducing the Tg. However, in order for the plasticizers to be beneficial for the purpose of high temperature polymer dielectrics, a significant reduction of Tg is not acceptable.
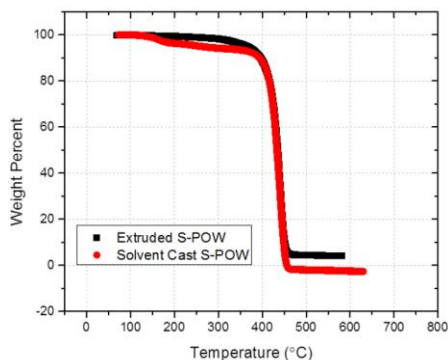
Figure III-138: TGA curves of solvent cast and extruded films.

Several plasticizers were screened including phthalates, terathanes, and trimellitates to improve the mechanical performance of the 75%-25% poly(PhONDI)-poly(NB) and optimize extrusion of the material. Plasticizers trioctyl trimellitate and 650, 1400, and 2900 terathanes were examined to improve the properties of the solvent cast films based on improved mechanical characteristics without a detrimental decrease in Tg. Ultimately, 650 terathanes and trioctyl trimellitate were chosen for in-house extrusion studies and optimization. Several prototype capacitors were developed using the extruded polymer with the incorporation of these plasticizers. Photographs of one capacitor (10% (w/w) trioctyl trimellitate)

are provided in Figure III-139. Figure III-140 shows that a concentration of 12% of both plasticizers resulted in severely diminished breakdown strengths in the extruded films while 10% (w/w) of the trioctyl trimellitate showed no adverse effect on the breakdown.
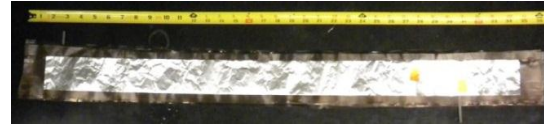
Figure III-139: Rolled capacitor of extruded film.
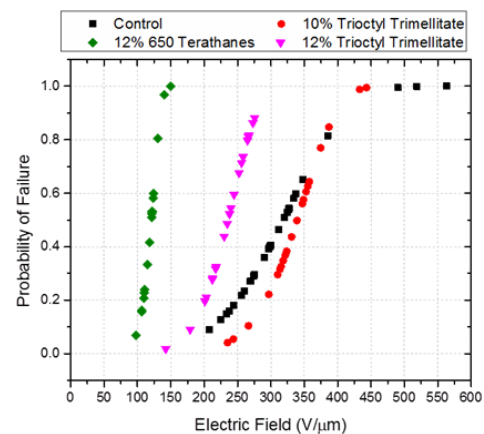
Figure III-140: Breakdown results for plasticizers incorporated in extruded films.

While the introduction of plasticizers showed some improvement in mechanical properties, incorporation of the plasticizers into the polymer proved difficult and posed a significant limitation in the optimization of in-house extrusion

3.0 Optimized polymer dielectrics

As discussed in the previous section, the limitations of 75%-25% poly(PhONDI)-poly(NB) extrusion lead the development of an improved chemical structure with higher thermal and mechanical stability. Recently Yoon et al. demonstrated a greater thermal stability and Tg of poly(N-phenyl norbornene 5,6-dicarboximide) [poly(NDI)], the carbon analog of poly(N-phenyl-7- oxanorbornene) poly(PhONDI) and it was found that the carbon bridged polymer exhibited a higher degradation and glass transition temperatures than poly(PhONDI) (Scheme 2).

Therefore it was suspected that the oxygen bridge in the backbone of the poly(PhONDI) was causing degradation during the hydrogenation of the polymer into 75%-25% poly(PhONDI)-poly(NB). Initially a 75:25 ratio of NDI to NB copolymer was synthesized and hydrogenated in order to make a relevant comparison to 75%-25% poly(PhONDI)-poly(NB) in an attempt to confirm the dielectric properties of the new polymer. A significant increase in breakdown strength of greater than 50 V/μm was observed for the PhNDI:NBE copolymer (Figure III-141). Due to the higher thermal stability of the poly(PhNDI) and impressive improvement in energy
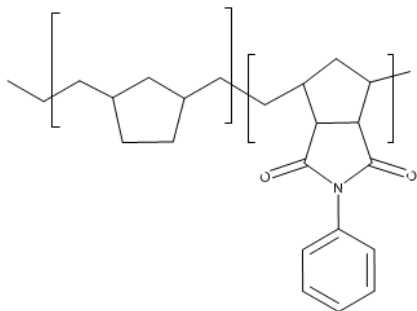
Scheme 2: Structure of poly(N-phenyl norbornene 5,6-dicarboximide) [poly(NDI)].
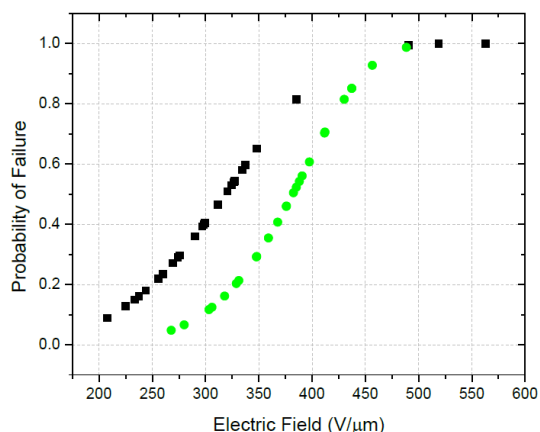
Figure III-141: Breakdown voltage of poly(PhONDI) /poly(NB) [black], poly(NDI)/poly(NB) [green].

density of the hydrogenated 75:25 poly(NDI):poly(NB) when compared to 75%-25% poly(PhONDI)-poly(NB) control, various ratios of NDI and NBE were synthesized and characterized to determine the effectiveness of poly(NDI) for use as a high temperature polymer dielectric.

The homopolymer of poly(NDI) was prepared in addition to three NDI:NB copolymers as provided in Table III-9.

Table III-9: Stoichiometry of co-poly(NDI)-poly(NB)

% NDI	% NBE
100	0
90	10
50	50
30	70

Figure III-142 shows the DSC curves for the copolymers as well as the poly(NDI) homopolymer. The homopolymer provided the highest Tg (as expected); however, the films were brittle and difficult to work with. The 30 and 50 NDI demonstrated an unfavorable Tg of ~90°C and ~125°C while the 90 NDI matched the Tg of 75%-25% poly(PhONDI)-poly(NB) (175°C).

In Figure III-142, DSC curves of homopolymer of poly(NDI) and three PhNDI:NBE copolymers are plotted. In Figure III-143, stress-strain curves for the homopolymer of poly(NDI) and three NDI:NBE copolymers vs. 75%-25% poly(PhONDI)-poly(NB) are plotted.
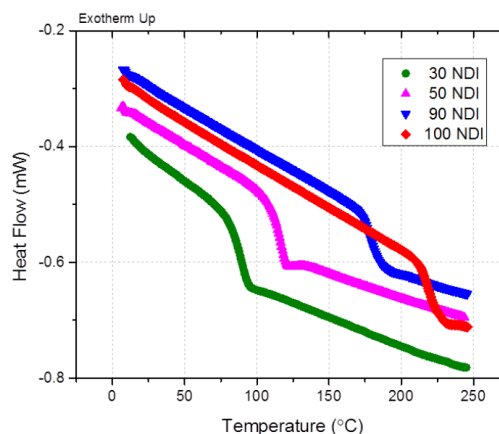
Figure III-142: DSC curves of various co-poly(NDI) poly(NB) ratios.
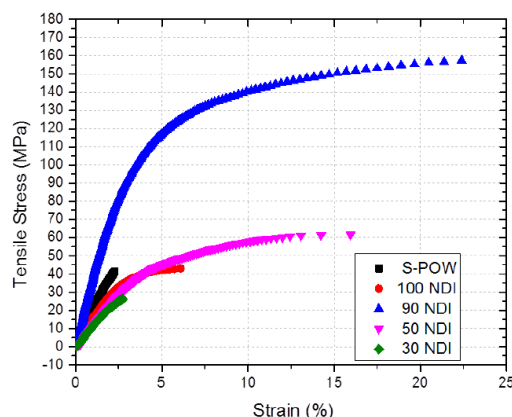
Figure III-143. Stress-strain curves of various co-poly(ND)-poly(NB) ratios.

By increasing the NDI monomer content in the copolymers showed an increase in the stress and the elongation at break. The NDI homopolymer does not follow this trend and has values significantly lower than the 50 and 90 NDI copolymers. The 90 NDI displayed an impressive tenfold increase in elongation as well as a rise in tensile stress of 100 MPa when compared to 75%-25% poly(PhONDI)-poly(NB) (175°C). The overwhelming improvement in the mechanical properties should greatly improve processability of the dielectric polymer and permit melt extrusion into films allowing for the transition to industry.

Conclusions and Future Directions

This year our overall objectives were to push our R&D efforts towards commercialization. In order to further reduce the volume of current inverters our first goal was to increase the overall energy storage capacity of our materials through the use of organic additives which act as voltage stabilizers. We examined four additives; 2- and 4-nitrodiphenylamine (NDPA), 4-nitrophenol and 2- nitroaniline. The best results were observed with 2-NDPA which displayed breakdown

voltage increases of nearly 20% and increasing the storage energy density by nearly 40%! Commercialization of new polymer dielectrics will require the ability of extrusion, due to the low cost of film production using this technique. This year we are also worked on extruding our material with a recently acquired polymer extruder. We have extruded several Kgs of our material and have formed several rolled capacitors, unfortunately, the extruded films were of poor quality and modification of the polymer backbone was required to improve its extrusion ability. The final accomplishment that was achieved this year was optimizing the backbone structure which increased the mechanical strength by a factor of 10 and improved the breakdown voltage by 20%. This new material should easily be able to be extruded without the incorporation of plasticizers. The Sandia has developed polymer film and additives that are critical components that should enable high temperature, thin film, polymer dielectrics which will be used to fabricate high temperature DC bus capacitors with significantly reduced size and weight, and improved performance and reliability

FY 2013 Publications/Presentations

1. Dirk, S. M.; Sawyer, P. S.; Wheeler, J.; Stavig, M.; Tuttle, B., High Temperature *Polymer Dielectrics from the Ring Opening Metathesis Polymerization (ROMP)* Proc. - IEEE Int. Pulsed Power Conf., 2009.

2. Dirk, S. M., Cicotte, K. N., Sawyer, P. S., Johns, K. S., Mahoney, P., Tuttle, B. A. *Thiol-ene coupling modifications of polynorbornene polymers for the synthesis of novel dielectric materials.* Polymer Preprint, 2010, POLY-442.

3. Dirk, S.M., et al., High temperature polynorbornene copolymer dielectric materials. PMSE Prepr., 2009. **100**: p. 331-332.

III.9. Next Generation Inverter

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Subcontractors:
Hitachi, Delphi, Infineon, HRL, Panasonic, AVX, Freescale, Oak Ridge National Laboratory, and National Renewable Energy Laboratory

Start Date: 2011
Projected End Date: 2016

Objectives

- Develop the technologies and the engineering product design for a low cost highly efficient next generation power inverter capable of 55 kW peak/30 kW continuous power.
- The Inverter is to improve the cost of the power electronics to $3.30/kW produced in quantities of 100,000 units, and the power density to 13.4 kW/l, and a specific power of 14.1 kW/kg to meet the DOE 2020 goals.

Technical Barriers

Traction inverter cost is the key barrier to economic viability of electric traction drives. Achieving the cost goals though must be done simultaneously with increasing efficiency, decreasing mass and volume, and maintaining reliability. Current materials used in today's inverters for automotive application are expensive and require multiply processes to be performed to construct a complete inverter. Additionally because of instability in the EV/HEV market commitment from the supplier base is difficult because the cost of introducing new technologies and their validation are high.

Technical Targets

- The Inverter is to improve the cost of the power electronics to $3.30/kW produced in quantities of 100,000 units, and the power density to 13.4 kW/l, and a specific power of 14.1 kW/kg to meet the DOE 2020 goals.

Accomplishments

- Detailed Design
  - Conventional module based design
  - Meets all vehicle constraints
  - Design flexibility for all vehicle applications

  - Assessment of critical characteristics to meet 2020 targets
- Power Module
  - Thermal cycling
  - Power cycling
  - R theta
- Capacitor Evaluation
  - Traditional and individual bobbin
- Gate Drive and Controller
  - Built and tested

✧   ✧   ✧   ✧   ✧

Introduction

The goal of this Cooperative Agreement is the development a Next Generation Inverter. The key goal is to reduce the production cost of a traction drive inverter while still making improvements in mass, volume, and reliability/durability. Traction inverter cost is a key barrier to economic viability of electric traction drives. This program is divided into four budget periods: technology assessment, technology development, technology build, and non-destructive confirmatory testing. The technology assessment phase includes the investigation through experimentation and evaluation of all key elements of the inverter. Technology development includes the concept and breadboard, and a final detailed design of the inverter. Technology build includes the procurement, fabrication of components, and the assembly of the inverter. Non-Destructive confirmatory testing includes environmental test setup, electrical verification, temp/vibe characterization and margining, and test support at national lab. The National Energy Technology Laboratory (NETL) awarded GM a Cooperative Agreement in October 2011. Budget period 2 started on January 16, 2013 and work is in progress on all tasks.

Approach

Engage with Tier 1, 2, and 3 suppliers along with National Labs to co-develop technology that reduces cost and increase efficiency, without increasing volume or mass. An Inverter design will be done that ensures modularity and scalability of inverter to meet all vehicle applications. This dictates that packaging will fit in all vehicle applications and have these additional characteristics:

- Consistent electrical parameters and mechanical structure
- Has to adhere to global manufacturing processes
- Has to provide adequate cooling for the capacitor
- Has to have low inductance

Then demonstrate technology to verify feasibility and cost. Multiple units will be built and tested over the complete automotive operating envelop.

Results

Technology evaluation and testing in FY13 was drawing to a close. A design concept was complete and a design review was held with DOE. The detailed design of the concept was initiated and completed. First unit builds were scheduled and build process development began along with material purchasing. Parts have started to be received.

Inverter Evaluation and Assessment of three technologies for the inverter power module are being considered: Conventional, Transfer Molded, and Encapsulated. Testing is nearing completion. Tests included thermal cycling, power cycling and R theata. Thermal cycling has been completed on transfer molded and to failure on the encapsulated, with conventional in process. Power cycling has been completed on transfer molded and to failure on encapsulated, with conventional in process. R theta has been completed on all units.
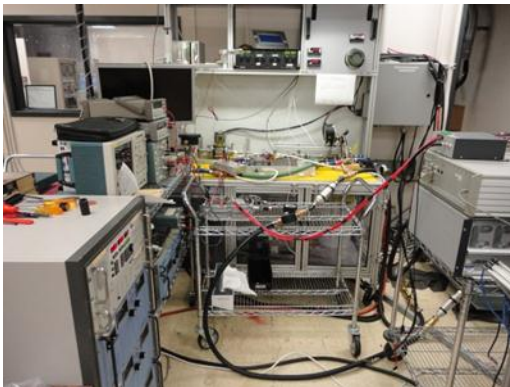
Figure III-144: Thermal Cycling Tests.
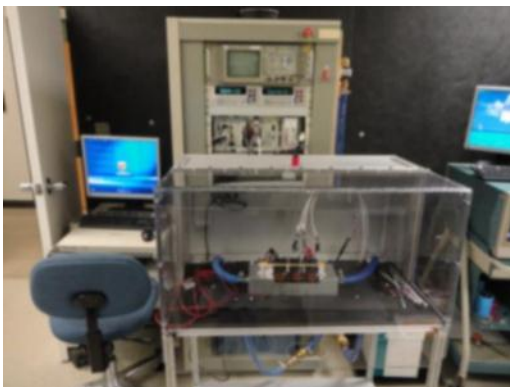
Figure III-145: Power Cycling Test.

WBG (Wide-Band-Gap) power device work has continued during this reporting period. Devices from Rohm, Cree, and Infineon have been acquired. Simulations have been performed to determine vehicle level benefits from the introduction of these devices. Tests are being performed on the devices to determine actual performance data.

Figure III-146: Wide Band Gap Modules.

Capacitor work has continued with testing of two types of traditional and individual bobbins. Two tests are being run on these types. A temperature and a life test are being run. Temperature testing is 75% completed with life tests complete on the individual bobbing and 45% on the traditional.
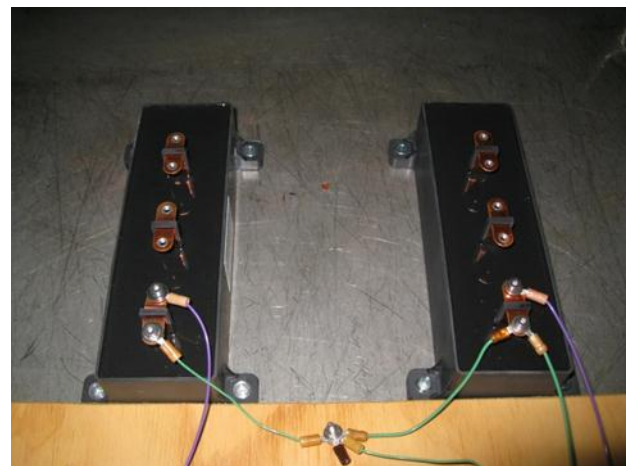
Figure III-147: Traditional Capacitor.
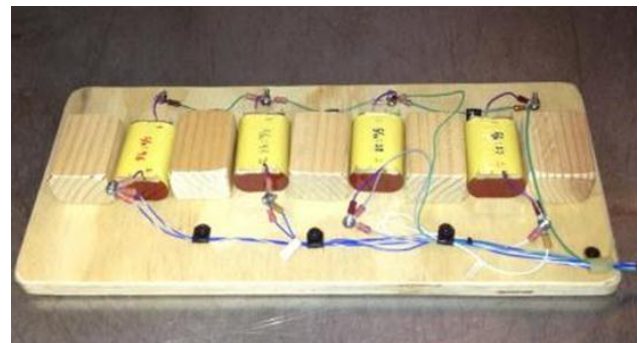
Figure III-148: Individual Bobbin Capacitor.

Gate Drive and controller board was designed and fabricated. This design incorporates new processor and gate chips.
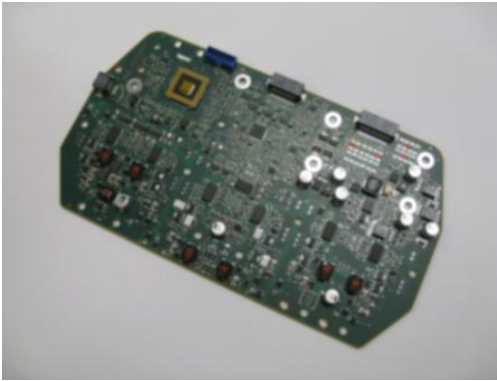
Figure III-149: Gate Drive and Controller.

Unit materials have been built for the purpose of understanding and evaluating manufacturing process choices and unit assembly. Coolant manifold construction, substrate, and their attachement have been the focus.

Figure III-150: Coolant Manifold.

Figure III-151: Substrate to Coolant Manifold Attachement.

Detailed design was completed. This design meets all vehicle constraints. Design flexibility allows for scalable voltage and current to meet all vehicle applications needs while maintaining consistency in manufacturing and performance characteristics. Cost objectives though have yet to be fully accomplished at this time, but work still continues.
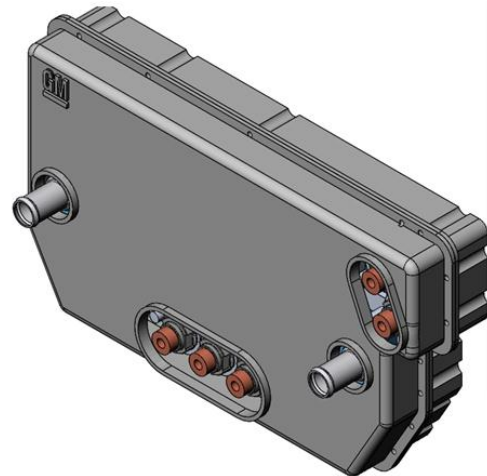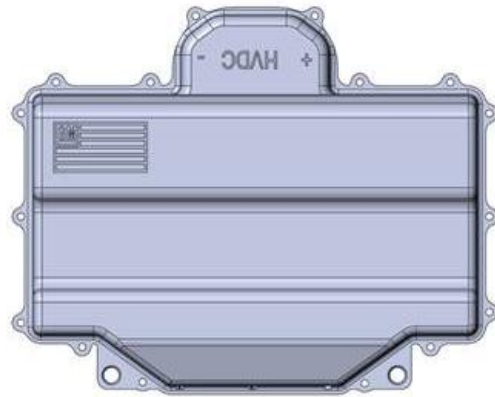
Figure III-152: Next Gen Inverter.

Conclusions and Future Directions

During FY13 an inverter detailed design was completed. Development work with each respective supplier has gone on to evaluate and determine appropriate process options for each part. Evaluations of these process options and their impact on the final unit assembly have taken place, but are still continuing. Parts have been received and used for mechanical checks and assembly process development. An early build is scheduled for the 1st quarter of 2014 and final evaluations will then be completed. The early build will provide data on assembly processes, tolerance stackups, materials, and inverter performance.

FY 2013 Publications/Presentations

1. 2013 DOE Vehicle Technologies Program Review March 21, 2013.
2. DOE Annual Merit Review Vehicle Technologies Program May 14, 2013.
3. DOE Vehicle Technologies Program Kickoff November 5, 2013.

III.10. High Temperature Inverter

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Subcontractor: Delphi Automotive Systems, LLC
(Delphi)

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Subcontractor:
Argonne National Laboratory, Argonne, IL

Start Date: September 26, 2012
Projected End Date: September 30, 2013

Objectives

- Develop, test and demonstrate a 30 kW continuous, 55 kW peak inverter that can operate from the vehicle's existing coolant system and be 4.6 liters or less in volume, 4.6 kg or less in weight, manufacturable in high volume and meet DOE's cost target if produced in quantities of 100,000 units/year.
  – Determine root cause failure of previous high temperature PEI capacitors
  – Build, test and demonstrate an inverter using a PEI dc-link capacitor
  – Develop process concepts for forming capacitors based on sub-micron PLZT particles
- The targeted application for these capacitor technologies is the dc-link capacitor used in Electric Drive Vehicles (EDVs), where this technology can substantially lower the size, weight and cost of power inverters.

Technical Barriers

Delphi and GE, working with GE partner Dearborn Electronics, used PEI film and formed capacitor bobbins which were integrated into the bobbins to create dc-link capacitors for Delphi's inverter. Two previous attempts at forming capacitors using this process had failed. The root cause appeared to be a high impedance on the capacitor winding. The challenge was to determine where the high impedance originated, implement a corrective action to fix the problem, finish the builds of the dc-link capacitor and the high temperature inverter, and finally execute the inverter test plan and provide the results to ORNL.

In Delphi's joint effort with Argonne National Laboratory (Argonne) to form capacitors based on sub-micron PLZT particles, after working with a solution-based PLZT chemistry, it was agreed to focus on ways to form PLZT powders such

that a single-step deposition process could be used to lower process cost. To facilitate single-step deposition, Argonne is developing a combustion synthesis process to form sub-micron PLZT particles. Keeping the sub-micron PLZT powders from agglomerating is a challenge. The team has considerable experience/expertise in dispersing sub-micron sized ceramic powders in slurry for ink-jet printing and tape casting of fuel cell materials. This know-how will be used to keep the sub-micron PLZT powders in a well-dispersed state. Another challenge to overcome will be porosity resulting from improper/incomplete removal of organics from thicker films deposited using PLZT slurries. Porosity in the PLZT films will degrade their dielectric properties. Thermal treatment conditions (heating/cooling rates, peak temperature, hold-time, and atmosphere) will be optimized for thicker PLZT films to eliminate porosity and form dense, thick PLZT films. Delphi and Argonne are working to define a low cost deposition process to form dc-link capacitors using Argonne's sub-micron PLZT particles. Efforts are focused on producing a film to understand the sub-micron PLZT material properties to better define the process. Since the properties of sub-micron PLZT particles are not known, films are being produced and characterized to determine sub-micron PLZT properties. Since the process of forming films with sub-micron PLZT particles is different than the previous sol-gel process for making films, the process parameters for forming films with sub-micron particles are also of being developed.

Technical Targets

The primary technical target has been to develop a process to make sub-micron size PLZT powders suitable for high-rate deposition to reduce the manufacturing cost for a very compact, high energy-density PLZT capacitor.

Accomplishments

- A tested PEI dc-link capacitor was delivered the week of December 17th allowing Delphi to resume its build and test of the high temperature inverter.
- Delphi demonstrated a non-optimized, scalable high temperature inverter for multiple applications.
- Delphi applied the demonstrated PEEM inverter technologies in a production intent inverter design that met or exceeded the APEEM 2015 R&D targets.
  – Assuming production at a rate of 100,000 units/year, DOE's $5/kW cost target was achieved; cost would be somewhat lower toward the upper end of 55-120 kW power range and somewhat higher toward the lower end of the power range
  – Specific power achieved of 17 kW/kg and power density of 15 kW/kg would be somewhat higher toward the upper end of the power range and lower toward the lower end, exceeding 2015 targets in all cases

- Delphi is going to production with an inverter based on the technology innovations developed with this DOE project.
- National lab expertise and facilities supported this project, including: capacitor development / testing, power device characterization, system modeling, thermal/heat exchanger experiments, thermal interface material characterization, and inverter system testing.
- Argonne developed an approach to form sub-micron size PLZT powders suitable for high-rate deposition processes.
- Argonne prepared PLZT-based inks using sub-micron powders .
- Argonne installed a system that enables high-rate PLZT film deposition.
- Argonne demonstrated that a ≈3 μm-thick PLZT film can be deposited at room temperature in significantly shorter time (20 min. vs. 11/2 days by spin-coating) using AD process.
- Delphi is producing un-optimized films using the sub-micron PLZT powders to understand their material properties.
- Delphi has defined deposition process concepts to form capacitors using Argonne's sub-micron PLZT particles.

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Introduction

Delphi and GE, working with GE partners, Dearborn Electronics, and GE's film metalizers, completed their joint investigation to determine why the GE PEI capacitors were failing. The investigation focused primarily on determining the origin of "scratches" in the capacitor film and implementing corrective actions, to be able to manufacture the PEI capacitors needed to create the dc-link capacitor required by Delphi's inverter. Using the results of this investigation, GE and Dearborn were successful in delivering a dc-link capacitor to Delphi 2012, which passed Delphi's verification testing in late-December. ORNL performed confirmation testing of Delphi's inverter system on DOE's behalf, utilizing Delphi's facilities, at the targeted higher ambient temperature (140°C) with 105°C coolant.

Delphi and Argonne are developing a fabrication process to reduce the manufacturing cost for a very compact, high temperature, film-on-foil high energy-density PLZT (Pb-La-Zr-Ti-O) capacitor. The targeted application for this capacitor technology is the dc-link capacitor used in EDVs, where this technology can substantially lower the size, weight and cost of power inverters. This will help to broaden the market for these more fuel efficient vehicles and, in turn, lower U.S. dependence on foreign oil, reduce greenhouse gas emissions, and advance U.S. manufacturing's competitiveness for the global EDV market. The spin-coating process used in our work until this time, to establish PLZT's properties and potential to meet APEEM's high-temperature and high-volumetric efficiency targets, requires over 30 depositions and over 30 annealing steps and many hours of time to produce a single 5 μm coating. For example, ceramic films of thicknesses over 5 μm are produced in a single coating step. However, sub-

micron sized particles are essential for the success of these very fast deposition processes. To provide these sub-micron particles, this project focused first on the preparation of sub-micron-sized PLZT powders, and will be followed by developing one of the above mentioned processes to fabricate thicker PLZT films in one single deposition step. By reducing processing steps and time, the energy input and overall cost for the manufacturing process will be reduced.

Over the past several years, Delphi has been collaborating with Argonne on Argonne's PLZT dielectric material. This material has shown strong promise of a very high dielectric constant (Dk) and high temperature capability. The PLZT's temperature capability has been shown to meet and exceed the temperature requirements for today's automotive environment and Argonne has estimated that, over the temperature, voltage and frequency ranges required for automotive power electronics, the Dk of the PLZT material will be ≈40 times that of today's polypropylene (PP) capacitors. It has also been shown that as the PLZT material gets hotter, the performance improves, rather than declining as with today's PP capacitors. Delphi has verified Argonne's claims for dielectric withstand voltage, Dk, benign failure mode, and the potential for low-cost processing. Therefore, Delphi feels this material has strong potential for producing a very small, much lower cost, reliable and durable high-temperature bulk capacitor for automotive power electronics, as well as for other applications. The spin-coating process used to demonstrate these attributes of the PLZT, however, is too slow and not practical for mass production of large area capacitors. In short, a high-rate film deposition process is required to economically manufacture PLZT-based high Dk, high-temperature capacitors.

This project has identified a high-rate deposition process to fabricate PLZT films. With flexible substrates, PLZT-based capacitors can be produced in a wound configuration that should enable APEEM's requirement of benign failure to be met.

Approach

GE PEI Capacitor

The approach used was to verify root cause of the failed PEI capacitors, institute corrective action, build and test capacitor bobbins, form bobbins into a dc-link capacitor, build, test and demonstrate the high temperature inverter with the high temperature PEI dc-link capacitor.

Sub-micron PLZT Capacitor

PLZT-based ferroelectrics possess high Dk and breakdown field. With their ability to withstand high temperatures, they can tolerate high ripple currents at under-the-hood conditions. Our approach has been to develop a process to produce sub-micron sized PLZT powders and a deposition process to economically make PLZT-based capacitors for power inverter applications.

The current focus in this regard is to utilize the developed powder production and deposition processes to form capacitor film, to understand the resulting material properties. This

understanding will enable us to optimize the sub-micron PLZT powder production and deposition process to achieve the high performance of the spin-coated PLZT films but at low overall production costs.

Results

During the October–December 2012 quarter, Delphi and GE, working with GE partners Dearborn Electronics, and GE's film metalizers, completed their joint investigation to determine why the GE PEI capacitors were failing. The investigation focused primarily on determining the origin of "scratches" in the capacitor film and implementing corrective actions to be able to manufacture the PEI capacitors needed to create the dc-link capacitor required by the inverter. Using the results of this investigation, GE and Dearborn were successful in delivering a dc-link capacitor to Delphi, which passed Delphi's verification testing in late-December.

It was agreed during the previous quarter that two rolls of extruded PEI film would be provided by for the final capacitor build. It was also agreed, based on discussions between all parties, that each roll of film would have a different metallization. One roll would have the same web metallization as the previous two builds, metallization, while the second roll of film would have a different metallization.

To verify that the root cause problem with the previous builds had been corrected, Ralph Taylor, Delphi's PI, spent one week at Dearborn Electronics at the start of the build process. It was agreed that 4 rolls of film would be used to first wind capacitors, to be followed by the use of 4 rolls of film to wind caps. It was expected, and later proven correct, that enough caps could be built and tested in the first week to give confidence that a dc-link capacitor could be successful.

In general, the process steps were: wind caps – end spray prep – end spray – end spray cure – dump test – lead attach – test (cap/Df/ESR sample flash/IR) – condition – test (cap/Df/ESR flash/IR) – build modules – test modules – build dc-link capacitor – test dc-link capacitor – ship dc-link capacitor.

For each process, there were 4 lots of capacitors. The week's goal was to complete the build process for 4 lots of caps that to go into the conditioning process, as follows:

- Lot 1: 78 capacitors completed
- Lot 2: 74 capacitors completed
- Lot 3: 76 capacitors completed
- Lot 4: 73 capacitors completed

Initial test results were as follows:

- ~99% of all Df is less than 1%
- All caps passed the dump test (with no initial shorts)
- Yield of samples: ~90%

During the conditioning process, it was noted that ~10% of one metallization of the capacitors failed short during the flash test (600 Vdc bias and 140˚C). None of the other metallization of capacitors failed. The failure of the parts was attributed to the thickness of the Al metallization and the inability of the capacitor to vaporize (clear) the short.

After the initial testing, capacitors were selected to form (6) six, 12-cap modules that were used to select the four (4) 12-cap modules utilized to form the dc-link capacitor. This was done with both the metallizations of capacitors.

The pictures below (Figure III-153) are before assembling into the first PEI prototype dc-link capacitor.

Figure III-153: Assembled capacitor pairs.
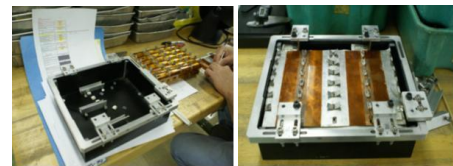
Figure III-154: Blocks attached to bus bars and fitted to housing.

Figure III-154 shows the first PEI dc-link cap in the case and attached to the fixture before bus bar soldering.The blocks that were selected by Delphi were bundled together to form two dc-link caps. The first PEI prototype cap, before potting, passed all the electrical tests at room temperature with good results.

Before installing the bus bars on the dc-link caps, the bus bars of each cap were clamped together and placed in a 140°C oven followed by applying a voltage up to 800 Vdc to test bus bars' insulation strength. IR test of the assembly showed 160 MΩ of resistance. Then, the first set of bus bars were installed on the first dc-link cap by soldering of all the tab-stocks, followed by insulating the soldered areas first with the high temperature tape (2 mil Kapton) and then Nomex sheets.

After completing the bus bars insulation, the assembly was electrically tested at 25°C before placing it in 140°C for a 600 Vdc flash test at temperature. The PEI dc-link cap (before potting) was placed in 140°C oven and 600 Vdc was applied to the dc-link cap, in increments of 50 Vdc. The cap withstood each increase of voltage up to 600 Vdc, at which time it electrically shorted. Checking the dc-link cap showed that one pair of caps from block #2 failed at higher temperature. Investigating further revealed only one of the paired caps failed with blisters evident on its outer surface. (Figure III-155) The short did not clear.

Figure III-155: Blisters on shorted cap.

Since there was a possibility that other pairs in the dc-link cap had some damage, it was decided to insulate all the pairs and electrically check each pair. The result of this test at room temperature showed no other pair has been damaged during the higher temperature flash and IR test.

After replacing the failed pair, the assembly of the dc-link capacitor was completed and it was electrically tested at room temperature. Then, the dc-link cap was placed in a 140°C oven and, after initial heating for 2.5 hours, it was flash tested and its IR was checked. While the dc-link cap was still warm, immediately after removing from the 140°C oven, it was electrically tested in the lab environment. In addition, the dc-link cap was electrically tested after it was cooled down to room temperature, and then tested one more time before the potting (encapsulation) process.

The dc-link cap was potted using a high temperature epoxy. Due to the difficulty of working with high temperature epoxy, the dc-link cap was potted in several steps. However, one step before final pour of the dc-link cap, the epoxy bubbled in the oven and stuck to the potting fixture, forcing us to machine down the epoxy surface in the machine shop (using end mill) before re-potting and finishing. After completing all work on the cap (including rounding cap's corners), it failed final electrical tests during flash test after reaching 300 Vdc.

After the dc-link cap failed flash test at 300 Vdc (25°C), we discharged the cap and tested all other electrical characters. We applied voltage to the cap again in increments of 10 Vdc up to 500 Vdc expecting that the cap would "clear." However, it did not clear, so it then showed it was "short" at 10 Vdc. A "high current" power supply (Sorensen) was used to apply 30V, 0.5 Amp for 5 minutes in conjunction with a Fluke (Ti 32) thermal fusion reader to measure "hot spots" in the dc-link cap. (Figure III-156) Using the Fluke during the test, we could measure the temperatures of the cap's body to be about 25°C and the hot spot to be about 43°C.
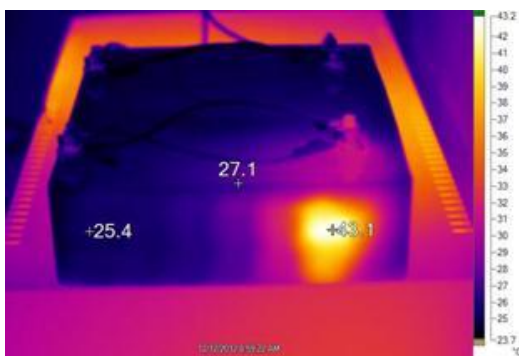
Figure III-156: Shorted Module in dc-link Capacitor.

The hot spot indicated a shorted cap in the higher temperature area. While this cap had not gone through root cause analysis, based on earlier testing of the capacitors, we knew that if an internal short appears in the capacitor, the cap is unable to clear. It is possible that there was some "defect" in the film that was exasperated by the potting process (perhaps by the pressure), which, though not evident before potting, caused the short to appear after potting.

Assembly and test of the second PEI dc-link capacitor followed shortly after assembly of the first dc-link capacitor. After installing the bus bars, the second dc-link capacitor was electrically tested and showed good results. The dc-link capacitor was fully tested before a flash test at 140°C, followed by a test immediately after the "hot" flash and IR tests. After the high temperature tests, the dc-link cap was fully tested at room temperature before potting. The potting of the second dc-link capacitor was performed in several steps, which included curing of the epoxy at each step. The dc-link cap passed flash test at 140°C and 400 Vdc. We checked IR at voltage and temperature (hot IR) and it was the same as before potting, about 20 MΩ.

In conclusion, one (bad) and one (good) dc-link capacitor were received at Delphi on December 17, 2012. (Figure III-157) Verification testing of the good dc-link capacitor was done at Delphi at 140°C, room temperature and at -40°C. The good dc-link capacitor passed all the tests. The good second dc-link capacitor was integrated into Delphi's DOE PEEM High Temperature Inverter starting in early-January 2013.

Figure III-157: Delivered Capacitors.

High Temperature Inverter Packaging and Test

During the January–March 2013 quarter, Delphi successfully completed the build and test of the high temperature inverter, with ORNL visiting Delphi in March to observe and confirm the testing for the DOE.

After installing the GE high-temperature dc-link PEI capacitor, Delphi completed the build and debug of its high-temperature inverter. This high temperature inverter was then connected to an inductive load for testing on March 7, 2013 in the configuration shown in Figure III-158 below.
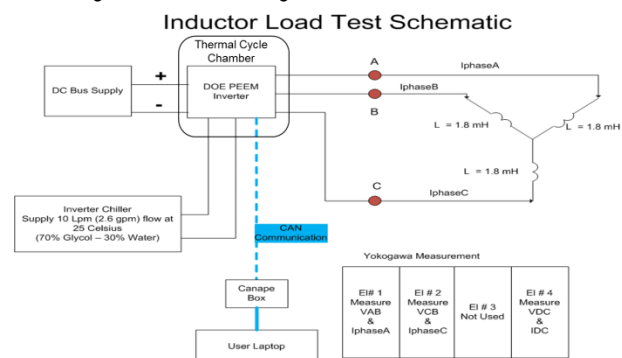
Figure III-158: Inductive Load Test Block Diagram.

For the confirmation test, testing was carried out in accordance with the test plan provided by ORNL. The data from this testing was reviewed and documented and, after the initial testing was successfully completed, ORNL was invited to visit Delphi in Kokomo to witness the confirmation testing for the DOE.

In an effort to make best use of ORNL's time at Delphi, it was agreed by both parties to have two setups: (1) an inductive load setup for thermal testing, and (2) a dyne setup for inverter performance testing. In addition, specific operating test points from ORNL's test plan were selected for the verification / confirmation testing. The inductive load test had the high temperature inverter with the GE PEI capacitor installed. For the dyne testing, we used our lab tested high temperature inverter, consisting of the same hardware as the high temperature inverter, except the inverter was opened up to allow initial debug of the high temperature hardware and it included a GE PP cap rather than the GE high temperature PEI capacitor. The PP capacitor was made with the same thickness film, as the PEI capacitor. The PP capacitor was made to verify the capacitor manufacturing process, to establish a packaging concept for the PEI capacitor and to establish a baseline for comparison with the PEI high temperature capacitor. Note: While only one GE PEI dc-link capacitor was successfully produced, the process is now well understood and it would not be difficult to produce many more of the same capacitors.

Testing of the high temperature inverter was witnessed, documented and successfully completed during March of 2013. Delphi R&D of advanced inverter with integrated controller met APEEM 2015 R&D targets based on production intent design using PEEM technologies. Assuming a production volume of 100,000 units/year, cost/kW would be lower than the DOE target of $5/kW for the upper end of 55-120 kW power range and somewhat higher for the lower end of power range; kW/kg and kW/L would be higher for upper end of power range and lower for the lower power. Delphi is going to production with an inverter based on technology innovations developed with DOE.

Sub-micron PLZT

Sub-micron particles of PLZT have been successfully made. The sub-micron particles have the same crystal structure as the bulk material. (Figure III-159)
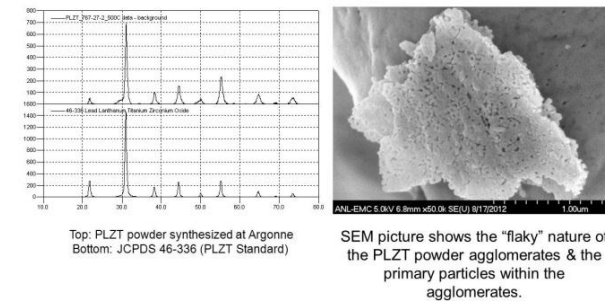
Figure III-159: Characteristics of sub-micron sized PLZT powders.

Un-optimized conditions in preliminary tests at Argonne, we fabricated a 3.2 µm-thick PLZT film on platinized Si substrate (Pt/Si) in ≈20 minutes; the film's dielectric breakdown strength is shown in Figure III-160.
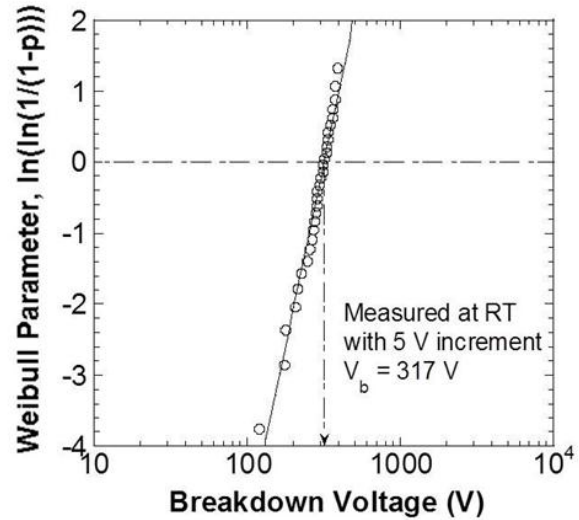
Figure III-160: Breakdown strength of PLZT film (thickness = 3.2 µm) on Pt/Si.

Dielectric constant and loss as function of bias voltage is shown in Figure III-161. Dielectric properties of the PLZT film measured at 25, 70, and 150°C are shown in Figure III-162.
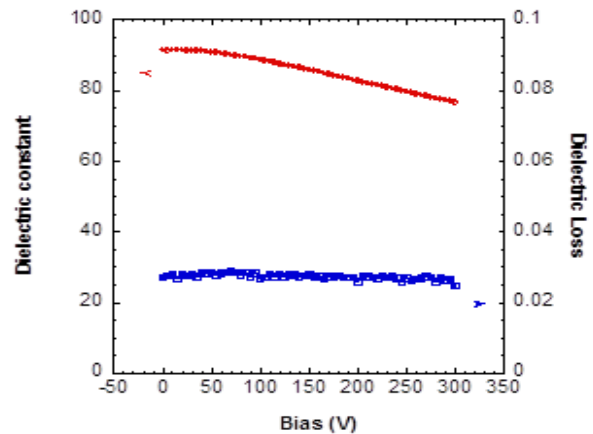
Figure III-161: Dielectric constant and dielectric loss as a function of bias voltage for a PLZT film (thickness = 3.2 µm) on Pt/Si.
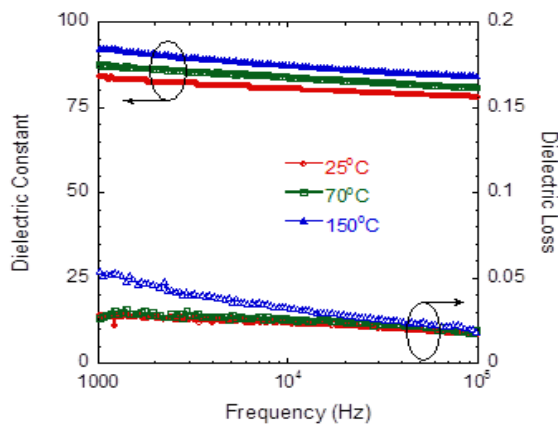
Figure III-162: Dielectric constant and dielectric loss at 25, 70, and 150°C as function of frequency for a PLZT film (thickness = 3.2 μm) on Pt/Si.

As seen in the scanning electron microscopy image (Figure III-163), the as-deposited film appears to be very dense.
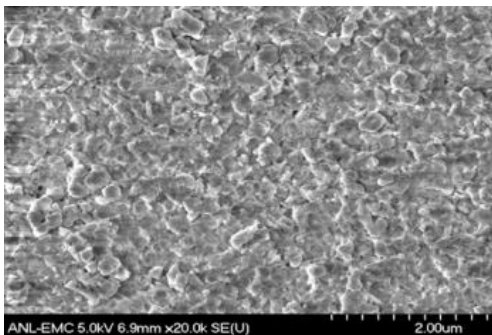
Figure III-163: SEM image of the as-deposited PLZT film (thickness = 3.2 μm) on Pt/Si.

PLZT-based inks were made using the sub-micron powders and delivered to Delphi for ink-jet and flow coating processes. Delphi is continuing to develop PLZT deposition concepts and capacitor material costing.

The cost of forming sub-micron particles can be determined today. Making films with sub-micron PLZT particles is the next step in an effort to quantify the costs of forming capacitors.

The amount of sub-micron particles required to form a capacitor depends upon the dielectric thickness and coverage area of the sub-micron particles. The dielectric thickness depends upon the breakdown strength of the sub-micron PLZT particles, which can be determined by making films, then caps and measurement. Once breakdown strength is verified, surface area coverage of the sub-micron PLZT powders can be calculated and verified by the formation of films. At this time, our effort is focused on the process for forming films with sub-micron PLZT particles. Making films will also determine if the process is a low temperature or a high temperature process and if patterning of the films are required. In addition to using the films to understand process temperatures, the films will also be used to measure the breakdown voltage of the material. This will better define our

process flow and cost models. If successful, the relative breakdown voltage and dielectric constant of the PLZT will be determined. At this time, this will be an un-optimized test.

Delphi is also investigating various base substrate materials (glass, metals and polymers) for forming capacitors.

To determine which process will be required, Delphi and Argonne have been working together to make films, capacitors and to analyze the capacitors. The goal is to determine the breakdown voltage, dielectric constant and capacitance of the film. Delphi has been making capacitors on various substrates to determine capacitor properties. Argonne has supplied the ink and has evaporated electrodes for the glass substrates. Argonne has also performed XRD analysis on two films, one crystallized and one not crystallized.

Using the flow coated films that were made on June 27th, capacitors were made and characterized and the breakdown voltage and dielectric constant of the PLZT were determined. At this time, this was an un-optimized test.

In order to determine capacitance, the thickness of the dielectric was required; this was measured using an electron spectroscopy for chemical analysis (ESCA) to give a depth profile of the capacitor.

An attempt was made at determining breakdown voltage of the applied film. But since this is new material, process and capacitors, it was determined to limit this testing until the first breakdown, to avoid permanently damaging the capacitor, so other data could be taken. Additionally, our top electrodes are very thick, making benign failure difficult to control.

On September 28th, Delphi and Argonne met at Purdue University's Birck Nanotechnology Center in an attempt to measure the piezoelectric properties of the sub-micron based PLZT film. The goal of this experiment was to validate a model Delphi created to predict the performance of the film and enable optimized electrode design. During this day, large amounts of data were created. The analysis of this data is ongoing. The Figure III-164 and Figure III-165 show PLZT displacement, moiré patterns, as a function of the applied voltage.
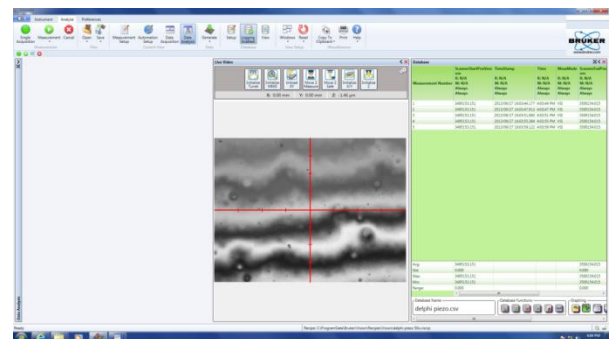
Figure III-164: Ttop electrode 0V time 0 at edge.
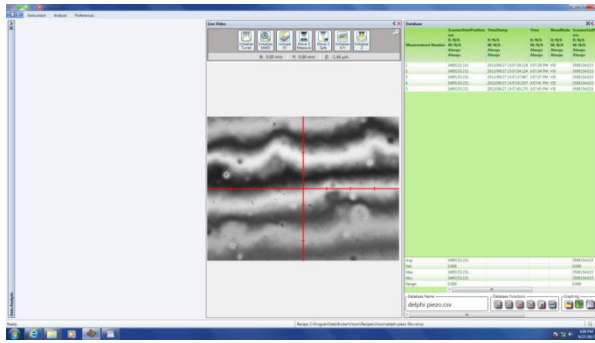
Figure III-165: Top electrode 50V time 0 at edge.

Work is continuing in this area to understand the sub-micron material properties before a final conclusion can be reached.

Conclusions and Future Directions

Process concepts have been presented, supplier materials have been evaluated and specific processes have been identified. To further refine this technologly transfer Delphi, Sigma and Argonne will continue the material and process development. We are developing solution chemistry to synthesize sub-micron powders for high-rate film deposition processes. Our initial investigation demonstrated that ≈3.2 μm thick PLZT film can be deposited in less than 20 minutes,

which is significantly faster than the previously shown spin-coating process. Future effort will be focused on optimizing the parameters to produce PLZT particles with suitable particle size and distribution for high-rate deposition processes and process conditions to fabricate uniformly thick PLZT films on metallized thin film substrates. Work is continuing on understanding crystallization temperature and profile, modeling and analysis of the piezoelectric effect of PLZT and how it affects electrode design, formation and analysis of films and capacitors, costing studies, material development, supplier development and technology transfer. High rate particle deposition is the primary path we will continue to follow until sub-micron film material properties indicate otherwise.

This is the final annual progress report for this extension of the DOE-Delphi High Temperature Inverter APEEM program. These topics and others as they develop will be discussed in the Argonne-led follow-on program "Development of Economically Attractive Manufacturing Process to Produce Advanced High-Temperature Capacitors for Power Inverters in Electric Drive Vehicles."

FY 2013 Publications/Presentations

Annual Merit Review; ape 012 High Temperature Inverter; 14 May 2013.

IV.0   Electric Motors R&D

IV.1.   Traction Drive Electric Motor Development

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Start Date: October 2012
Projected End Date: September 2013

Objectives: Overall

- Develop efficient, low-cost non–RE electric motors that take advantage of lower-loss materials enabled by new processing methods.
- Meet DOE 2020 cost and performance targets for electric motors.

Objectives: FY 2013

- Develop candidate non-RE, motor (induction and switched reluctance, and eventually synchronous reluctance) designs suited to 55 kW peak, 30 kW continuous power.
- Deliver electrical models to APEEM TDS team for computer simulation and performance validation.
- Employ material and process innovations that facilitate meeting DOE 2020 motor efficiency goal.

Technical Barriers

Cost is an overarching concern for electric traction motors. Traction motors for PEVs are on an approximate 3.5% progress curve and their attendant PE on an approximate 7% progress curve. This means that the DOE 2020 TDS cost target of $8/kW will not be met until 2028 or later unless revolutionary changes occur. Furthermore, instability in RE magnet pricing will continue to pace future cost reductions. There is also a pressing need for a consistent definition of efficiency.

Technical Targets

- Improve system efficiency above the DOE 2020 target of 94% for the TDS. Efficiency computations rely on a harmonic average of motor line efficiency at 20% rated torque from 10 to 100% speed.

Accomplishments

- Completed identification of motor R&D candidates.
- Completed comparisons based on DOE 2020 targets for specific power, power density, specific cost, and efficiency (as defined in Technical Targets).
  - Candidate designs include the IM, switched reluctance motor (SRM), and eventually synchronous reluctance motor.
  - Package-efficient (i.e., smaller) motor designs are more challenging thermally. This challenge prompted closer collaboration with the NREL, which was achieved in the complementary task 1.2.
- Developed a more package-efficient traction motor that analysis shows can meet DOE 2020 targets:
  - Minimizes material content
  - Benefits from low-loss, affordable electrical steels
  - Promotes operation at higher continuous power using improved thermal management materials
- Completed mass and cost calculations that show the selected, and commercially available, baseline IPM traction motor will be challenged to meet DOE 2020 targets because
  - RE magnets are a small fraction of the total mass but a very large fraction of cost.
  - IPM designs are close to or at their rotor structural stress limits; therefore, moving to much higher speeds will be challenging.
- Achieved success in a new process for low-loss, potentially cost-effective electrical steel that is suitable for high-volume manufacturing.
  - In FY 2012, this project validated the performance benefits of low-loss electrical steel and demonstrated, in static testing, substantial improvement in core loss reduction in the baseline IPM test motor (temperature rise at the same operating point was 22°C lower than in the comparator).
  - Subsequent dynamic testing of the same IPM stators in FY 2013 validated earlier findings and showed core loss was reduced by 86% for commercial high-Si steel at a 7000 rpm test condition (speed at which the resultant electrical frequency matches that of the earlier static tests).
  - The new metallurgical process for 6.5% Si steel (Fe 6.5 wt. % Si-500 ppmB) with trace amounts of boron was successfully demonstrated at ORNL using

successive strain softening during warm deformation (first reported by Fu et al. [1]) that leads to ease of cold formation, i.e., rolling into thin sheets.

- Completed the design of a high-speed IM that analysis shows can meet DOE 2020 targets for performance and cost. Efficiency will be challenging and requires the use of low-loss steel.

✧   ✧   ✧   ✧   ✧

Introduction

The DOE VTO APEEM program has the charter to develop alternatives to RE PM motors. Alternatives to RE magnets, such as enhanced Alnico, are being developed at Ames Laboratory under the aegis of the Beyond Rare Earth Magnets (BREM) program for application to automotive traction motors and other industrial and commercial motors. The ORNL PEEM group supports the VTO APEEM mission through electric motor research on non-PM motors that lessen dependence on critical materials, specifically dysprosium (Dy) and neodymium (Nd). To facilitate the quest for alternatives to non-PM traction motors, this project explores in considerable depth the application of novel materials and their processing as enablers for better performance, efficiency, and cost. This report summarizes APEEM electric motor research for FY 2013 with emphasis on high-speed IM and SRM candidates. Both IM and SRM designs require very low-loss electrical steels to minimize core heat generation and higher thermal conductivity (TC) coating and potting materials that facilitate more rapid heat removal. Low-loss lamination electrical steel and coatings are essential because the absence of RE magnets means that the motor core and working air gap(s) may be magnetized only by an externally applied magnetizing current, either as a component of the stator current in the case of an IM, or phase current injection in the case of the SRM. Figure IV-1 highlights the mass and volume challenges of replacing the magnetizing strength of a typical RE magnet with that of a current-carrying Cu coil. In Figure IV-1 the NdFeB+Dy magnet (N35SH) has a nominal coercivity of 15.4 kOe (1.22×10^6 A/m) and a length of 7.163 mm for an equivalent strength of 8800A. A Cu wire bobbin having the same face areas as the magnet is wound with 1,760 turns of #22 AWG magnet wire. When the Cu bobbin is excited with a 5 A current (15.3 A/mm^2), an equivalent 8800A strength is realized.

The purpose of Figure IV-1 is to quantify the challenge this project faces when it comes to non-RE alternative motor architectures. The challenge is very significant, including the attendant heat removal burden that injection of external magnetizing current has on the motor's thermal management system. The coil, for example, requires a 100 V_{dc} supply to drive 5 A of excitation current with an attendant 500 W of heat dissipation and rapid temperature rise. The Figure IV-1 inset (1) defines an equivalent current sheet for the coil, since this current is spread over an approximately 50 mm quasi-annular region. Above this current sheet (the coil), an expected flux density (2), B(z=0)=110 mT, is in fair agreement with the

measured flux density over the coil window. Similarly, taking the coil as an equivalent magnetic dipole moment (3), m, and calculating the flux density at z=100 mm above the coil window area shows fair agreement with measured data. The discrepancy can be accounted for by noting the coil is not an infinite current sheet (2), and in (4), z>>a is necessary to satisfy the dipole moment field, which is not the case here.

Magnet dimensions: L49.35xW17.88xH7.163 mm
Coil dimensions: OD150xH15.9 mm

	Magnet	Coil	Units
Core area	882	882	(mm^2)
Mass	52	999	(g)
Mmf	8800	8800	(A)
B(z=0)	260	74	(mT)
B(z=100)	1.53	7.8	(mT)

$$H_x = \frac{K}{2}\,(A/m), where\ K = \frac{8800A}{0.05m} \quad (1)$$
$$B_x = \mu_0 H_x = 110\ mT \quad (2)$$
$$m = \pi a^2 I = 172.5 Am^2, given\ a = 79mm\ (3)$$
$$B(z = 100mm) = \frac{\mu_0 m}{2\pi d^3} = 3.45\ mm\ (4)$$

Figure IV-1: Comparison of NdFeB magnet to copper coil of same magnetomotive force rating.

This illustration of replacing a high-energy PM with a Cu winding puts into perspective why RE magnet traction motors have such high performance metrics. This also illustrates why wound field alternatives to PM motors are challenged in meeting specific power and power density.

Approach

- Develop performance and cost assessment for candidate electric traction motors.
- Use the 2012 NISSAN LEAF AEV traction motor as the baseline IPM motor comparator.
- Present analysis to show present traction motor, PE, and TDS will not meet the 2020 target until ~2028 (given 2010 metric initial conditions).
- Project RE-based motor designs out to higher speeds, using optimized RE content at ~$77/kgRE, to show that potential benefits of higher speed are lost when RE content dominates motor cost.

Results

This project includes four experimental test stators that have been fabricated to be as nearly identical as possible to the baseline IPM motor, a 2010 Prius hybrid 60 kW peak power design.

A. Experimental IPM stator thermal and magnetic material characterization

Figure IV-2a shows the comparison stators that were static tested in FY 2012 with a laboratory 3-phase ac source set at 60V_{rms} line to neutral, and subsequently dynamic tested in FY 2013 using the commercial transaxle case as a dynamometer fixture for FY 2013 characterization work.

Figure IV-2b shows the resultant temperature rise at the applied excitation (~22 A$_{rms}$ line current) for the winding end turns at steady state (20,000 s), relative to the Prius baseline stator, was −7.24°C for the 29M19C5 core, −18°C for the 10JNEX900 Super Core™, and −22.6°C for the potted M19 core. Note also that the core with Cotronics epoxy molding compound (EMC) having a TC of 3.2 W/mK registers a lower temperature at 20,000 s because of the higher thermal mass.
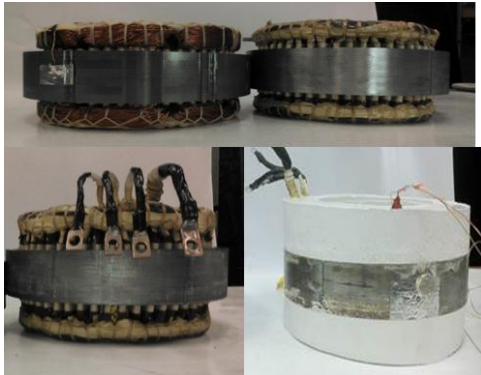
(a)
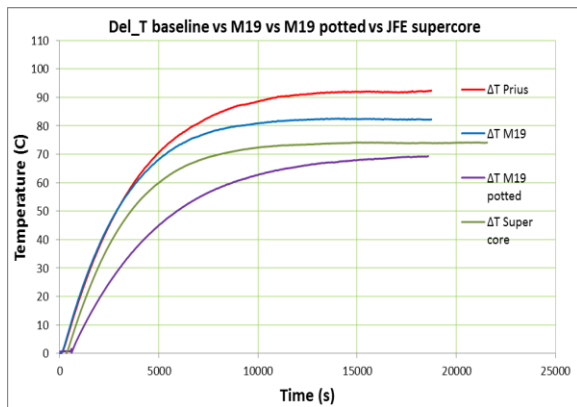
(b)

Figure IV-2: (a) Comparison stators for static testing at 3-phase, 400 Hz excitation (top: 29M19C5 and 10JNEX900; bottom: 2010 Prius and potted M19 cores). (b) Chart shows resultant experimental temperature rise data.

Figure IV-3 is a compilation of core loss comparisons of the M19 and 10JNEX900 cores with the production Prius stator. These are all 48-slot, 8-pole, 3-phase IPMs, so testing at 6,000 rpm results in 400 Hz ac phase voltages that increase to 467 Hz at 7000 rpm. The shaft torque necessary to spin the JFE Super Core 10JNEX900 high-Si steel is virtually identical to spin power for an inert rotor (diamonds).
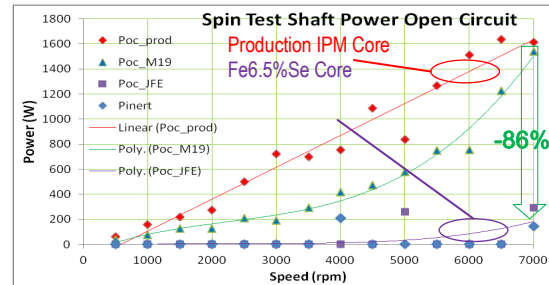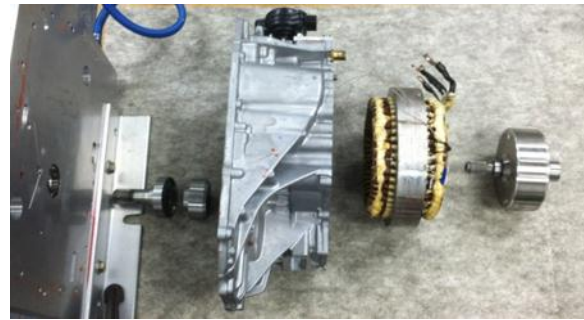
Figure IV-3: Test fixture for prototype stator spin testing (top). Comparison of experimental phase voltages (bottom).

Characterization testing performed on the experimental stators does confirm that the phase resistance, ac resistance, and back electromotive force (bemf) are virtually identical, as expected. However, the short circuit current and d-axis phase inductance are somewhat different compared with the baseline Prius stator, even though the windings are as uniform as is possible. Figure IV-4 compares the expected change in phase resistance for the NIH (number in hand) 12 of #20 AWG, N_c=11 turn coil from its dc value to operation at 400 Hz and maximum of 900 Hz when rotating at 13,500 rpm. From short circuit testing of the experimental stators, the d-axis inductance values compute to L$_{ds}$(Prius)=1.74 mH; L$_{ds}$ (M19)= 1.91 mH; L$_{ds}$(Super Core)=1.96 mH. The error source is most likely the speed signal, since the magnet flux linkage given in Figure IV-4 is virtually identical (i.e., 0.7% error).
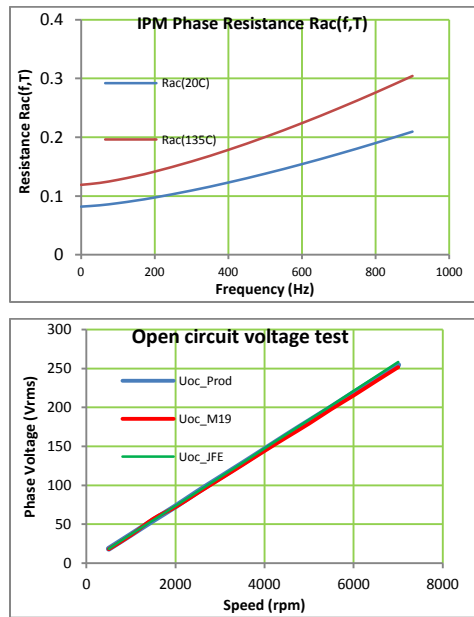
Figure IV-4: Prototype IPM stator characterization data. Top: dc phase resistance R_{ph}(mΩ) Prius 80.3; M19 82.9; Super Core 83.5 and R_{ac} plot at 20°C and 135°C. Bottom: stator bemf test data in V_{rms}/phase (lambda=0.1287; 0.127; 0.1296 Wb, same order).

B.   New processing method for Fe 6.5 wt. % Si-500 ppmB electrical steel

Commercial 6.5% Si steel processed by chemical vapor deposition (CVD) has low loss, as Figure IV-3 shows, but is very expensive—on the order of 20 times the cost of M19 steel. ORNL has pursued an alternative process based on strain softening during warm deformation (first reported by Fu et al. [1]) that effectively destroys lattice ordering (B2 phase), leading to restoration of ductility and subsequent ease of cold formability. This process leads to low-cost Fe-6.5%Si steel sheet for motor laminations with equal or better magnetic properties compared with the CVD processed steel. Scaleup and commercialization of the process is important to industry and motor manufacturing because of the major beneficial impact. More development is needed, specifically in the optimization of boron content and thermomechanical process parameters. ORNL is exploring superimposed ultrasonic vibration during deformation to eliminate the need for warm rolling (Figure IV-5). Other researchers are doing so, also. [2,3].

With the recent addition of a Walker scientific hysteresis graph, the APEEM group has a facility to characterize lamination steel before embarking on the fabrication of experimental electric machines. In prior electric machine fabrication, a significant difference was observed between prototype results and computer modeling and simulation based on the manufacturer's steel characteristics or model library parameters. Procedures for lamination steel characterization are well documented [4–13] and available to guide APEEM group characterization work. These characterization procedures will be applied to any lamination stock that is processed by strain softening at ORNL.
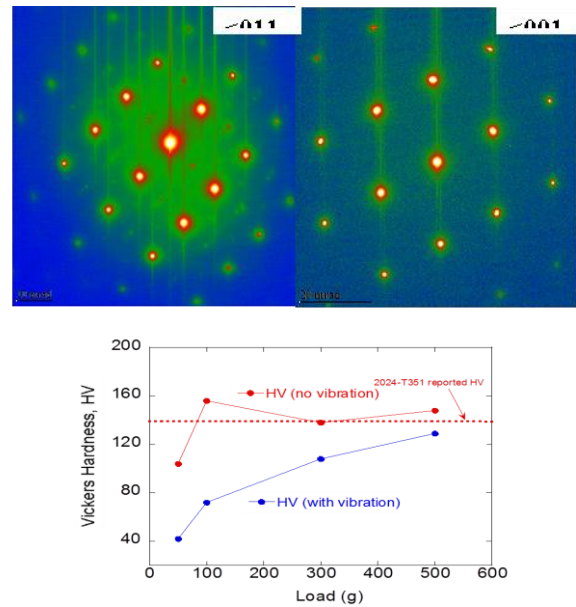
Figure IV-5: ORNL testing confirms prior work [1] and now extends it with trace boron and ultrasonic vibration. Top: superlattice observed <011> BCC and after 44% deformation superlattice eliminated <001> BCC. Bottom: illustration of ultrasonic vibration during strain softening to reduce hardness.

To determine the full benefit of 6.5% Si steel processed by strain softening, it is necessary to continue this work in FY 2014. In particular, it is necessary to accomplish the following:

- Optimize the boron content for maximizing room-temperature ductility without impacting magnetic properties. This may prove challenging because boron has low solubility in iron and tends to entrain into grain boundaries, which may limit ductility reduction.

- Demonstrate formation into thin sheets by cold rolling in size ranges sufficient for traction motors (e.g., 0.20 to 0.35 mm).

- Conduct analytical modeling and simulation to better understand the effect of boron on the stability of ordered precipitates (B2 phase) and the acoustic plasticity in B2 and DO3 ordered Fe-Si domains. ORNL will employ ultrasonic vibration to aide boron solubility.

- Validate the processed sheet magnetic properties as described.

C.   Thermal coating materials

Industrial and automotive electric machines use 0.25 mm thick aramid paper as a slot liner in the stators to prevent contact between magnet wires and the slot walls and core edges. Aramid paper has a TC of 0.05—0.1W/mK. In this project, certain EMCs have been explored for application in electric machines, including processing and application methods such as an electrostatic powder coating process (for conformal coating stator slots) and thermally setting the material in place. Heating converts the deposited powder to a continuous thin EMC coating that has 0.7 < TC < 0.8 W/mK. The 3M paper used in prior project work had a TC of 0.2 W/mK. It is anticipated that powder coating the stators to

replace the slot liner paper should increase the TC of the winding bundle to the stator core by some 300%, substantially improving heat transfer.Figure IV-6 shows one of several 60° segments cut from an experimental 29M19C5 core described earlier but stacked to only 25 mm. The photo in the upper right shows a stator segment that was heated to 200°C for 1 h and then sprayed with SolEpoxy DK15-0984. This process was found to result in a nonuniform, "orange peel" appearance. It was rejected and the coating changed to a 2905-102B material following the same process. The final coating method consisted of the same preheat schedule followed by dipping into a fluidized bed of SolEpoxy DK15-0984 material and then curing at 200°C for 15 min. The fluidized bed process appears viable but may be problematic in thickness control. The sample using the fluidized bed dipping process was wound for high-potential insulation resistance (IR) testing.

Figure IV-6: Illustration of stator segment. Top: uncoated core sample (left); coated with SolEpoxy 2905-102B (right). Bottom: preheated segment dipped in fluidized DK15-0984 and lap wound with 19 AWG magnet wire (right).

The dip-coated stator segment with individually wound coils was tested for high potential by continuous application of 1 kVdc in a thermal chamber with controlled up and down ramp. Figure IV-7 shows the results of the IR for temperature ramp-up and ramp-down from room temperature to 145°C. An interesting phenomenon occurs at approximately 70°C, where a sharp transition in IR occurs having approximately 2 orders of magnitude. This test was repeated for Nomex paper-lined slots using the uncoated segment; and very similar IR results were found in the 55 to 70°C range, indicating some Arrhenius behavior (i.e., related to activation energy) in the insulating materials.
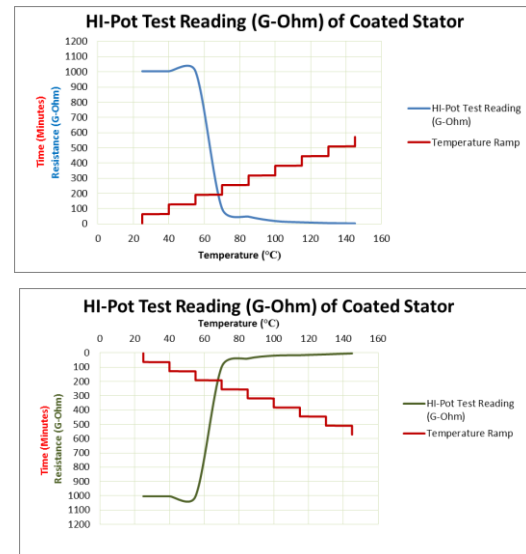
Figure IV-7: IR test results for coated stator segments during temperature testing. Ramp up (top) and down (bottom).

ORNL quantified the thermal properties of the coating materials described. Figure IV-8 summarizes the laboratory tests for TC, diffusivity, and heat capacity for both the DK15-0984 and the MgO–loaded 2905-102B materials that confirm TC in the expected range. Based on the densities (i.e., 2.025 g/cc for the Al_2O_3-filled coating, and 1.934 g/cc for the MgO-filled coating), note that since MgO and Al_2O_3 have similar densities, the volume fraction in the Al_2O_3-filled coating would be higher, so better thermal performance would be expected.

In these characterization tests, the two samples are the (SolEpoxy standard) tabular-alumina-filled coating (DK0984) and the development MgO-filled coating (2905102B). This information is useful because with the quantified thermal diffusivity (lambda) and heat capacity (Cp), the thermal conductivity (kappa) can be calculated as kappa = Cp × density × lambda. The advantage of knowing all the thermal parameters, versus only TC, is that any and all transient and steady-state thermal modeling cases can be considered that use these coatings.
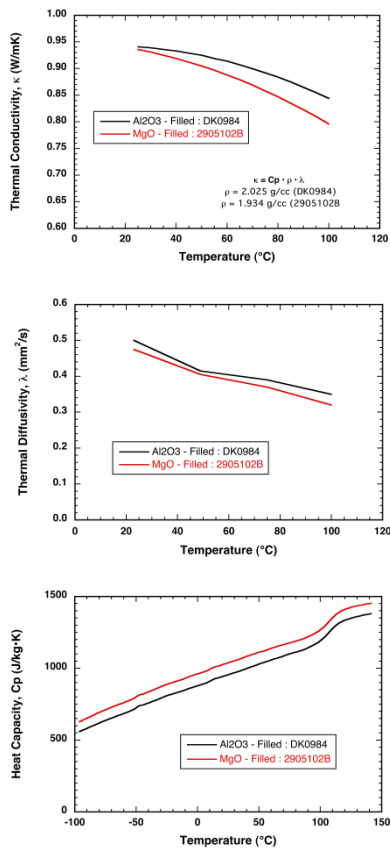
Figure IV-8: Characterization of thermal coating materials used on stator core samples. Top to bottom: TC, diffusivity, and heat capacity.

D. Input requirements for a high-speed induction motor

This project accepts the existing DOE 2020 technical targets for HEVs and concentrates on the design actions required for a non-RE traction motor to meet them, while acknowledging upfront that no electric motor can compete directly against a motor using high-energy magnets, as was illustrated in Figure IV-1. Therefore, a non-RE traction motor must rely on higher speed to achieve these goals and thereby minimize material content. Higher-speed traction motors may require an additional gear stage to match them with the existing gearboxes of conventional all-electric vehicles. This section discusses the ramifications of adding in-line gearing, such as an epicycle (i.e., planetary, or "rotissmo") stage. It summarizes the highlights of the case for an IM operating at speeds above 14,000 rpm and with a high-conductivity Cu rotor in an effort to meet or exceed DOE's 2020 technical targets.

To meet this aggressive set of goals, a cascade of cost reduction actions must be undertaken in TDS design to reduce the cost from the 2012 metric of \$17/kW to the 2020 goal of \$8/kW. For electric motors, this means not using RE magnets—because of politically instigated price volatility and future uncertainty, using alternative magnet materials, and using less

material overall. The goal of reducing the total material content can be partially achieved by operating at higher speeds and higher voltages, which are complementary in electric motors. To develop the attendant PE needed to drive a higher-speed motor and achieve these goals requires a similar minimization of material usage, primarily semiconductors. Lower semiconductor content in the traction inverter is realized by operating at higher voltages that lead to a reduced inverter switching current and, consequently, lower motor line current magnitudes. Input requirements are summarized in Table IV-1 and details of the laminations are shown in Figure IV-9.

Table IV-1: Electric traction motor input requirements.

Requirement	Symbol, (Unit)	Target
Peak power at corner speed for 18 seconds and at nominal dc link voltage and temperature representative of prior continuous duty power	P_{pk}, (kW)	55
Continuous power at nominal voltage & temperature	P_{cont}, (kW)	30
Electromagnetic mass (per BOM)	M_{em}, (kg)	<35
Electromagnetic volume (per BOM)	Vol_{em}, (dm^3)	<9.7
Unit cost @ 100,000 APV (annual production volumes)	C, (\$)	258
Operating voltage, nominal	U_{d0}, (V_{dc})	720
Maximum operating speed	n_{mx}, (rpm)	>14,000
Ambient temperature outside housing	T_a, (°C)	-40 to +140
Coolant inlet temperature	T_{inlet}, (°C)	
Winding insulation resistance, any phase to stator iron at continuous operating temperature	IR, (MΩ)	>1
Peak ripple torque at any speed and any power	δm_{pk}, (% m_{pk})	<5

BOM = bill of materials based on electromagnetic design content

Electromagnetic torque is "m" for moment and no subscripts for derivations except peak.

Elsewhere in this report "m_x" refers to number for phases, x=1 for stator and 2 for rotor.
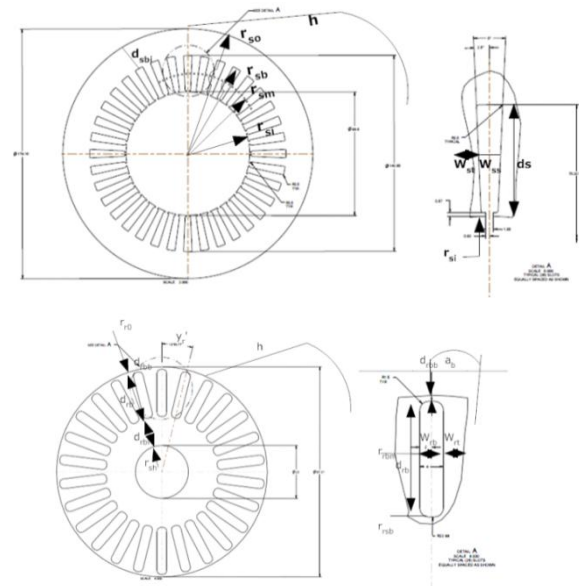
Figure IV-9: High-speed copper rotor, closed-slot IM. Top: stator lamination design and slot detail; bottom: rotor lamination design and slot detail.

Details of this motor design are provided in an ORNL report (see publications list) and supported by related literature on dealing with frequency effects on windings, especially the Cu bar rotor [11, 14]. Motor parameter evaluations are supported by related literature [15–16] and much of the detailed stator and rotor electrical and magnetic design follows refs [17–19]. The resulting design is a 23,000 rpm motor developed to match the axle torque at 1,600 rpm axle speed. Table IV-2 lists the full set of motor parameters (see also ORNL/TM-2013/60 in publications list). The parameter values shown in Table IV-1 are defined by the 4-pole IM equivalent circuit shown asFigure IV-10 along with its slip characteristic vs. frequency.

Table IV-2: Electric traction motor parameter values

n_r	8846	(rpm)	L_m	2.367	(mH)
f_s	295	(Hz)	U_{ll}	485	(V_{rms})
ω_s	1852	(rad/s)	U_s	280.7	(V_{rms})
r_1	87.6	(mΩ)	I_r	-	(A_{rms})
r_2'	36.14	(mΩ)	m_{bd}	196	(Nm)
r_c	-	(Ω)	m_r	59.4	(Nm)
L_{ls}	150.6	(uH)	s_{bd}	0.076	(#)
L_{lr}	114.86	(uH)	s_r	-	(#)
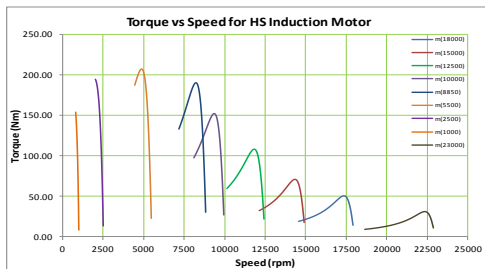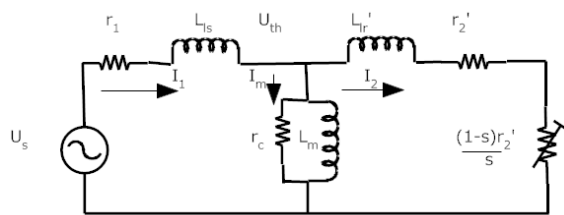
Figure IV-10: High-speed IM model and matching to vehicle axle using in-line planetary gear. Top: Equivalent circuit model for 4-pole, 3-phase IM. Bottom: Slip characteristics at various speeds.

Gear design is based on an in-line planetary shown in Figure IV-11 at the motor output shaft end, and the overall reduction ratio is 1.917 in the planetary stage and an additional 7.9:1 in the final drive for a total ratio of 15:1. This effectively translates the IM 59 Nm of rated shaft torque into 885 Nm and 8850 rpm into 590 rpm at the axle. Peak shaft torque is 2.5 times higher, developing 2,200 Nm of axle torque at the same speed, sufficient to meet grade requirements.
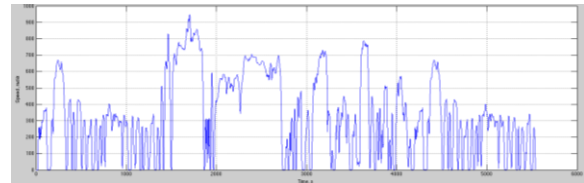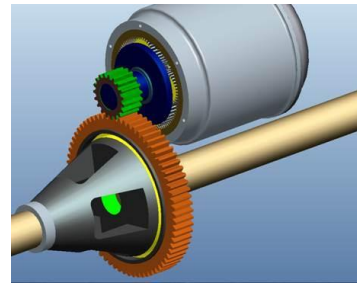
Figure IV-11: High-speed IM with in-line planetary gear. Top: Architecture of in-line planetary to driven axle. Bottom: Combined drive cycle=UDDS+US06+HWFET+ LA92+UDDS.
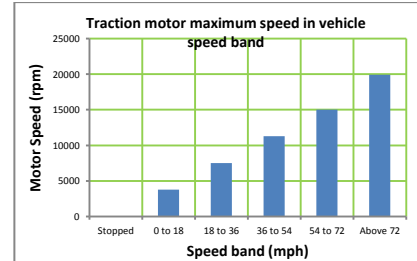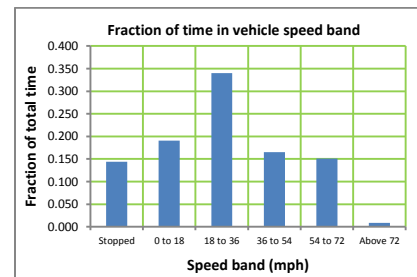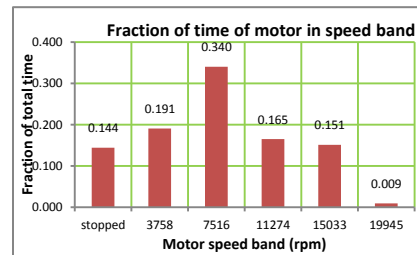
Figure IV-12: Vehicle application: combined drive cycle schedule results. Top: fraction of total time spent in motor speed band. Center: fraction of time spent in vehicle speed band. Bottom: Maximum traction motor speed by vehicle speed band.

It is evident from Figure IV-12 that this high-speed traction motor will spend very little time operating in the band above 15,000 rpm (0.9%), which, mapped to vehicle speed, is in the region above 72 mph. The bulk of operation is in the 3,758 to

15,033 rpm range, 84.7%, and 14.4% stopped. This bodes well for the in-line planetary gear lubrication and gear teeth meshing velocity.

Conclusions

High-speed traction motors are the subject of considerable debate in automotive circles, even though traction motor speeds in both hybrid and battery electric vehicles have steadily increased over the past two decades. It is well known that a low-speed, high-torque traction motor requires low values of gear ratio to match vehicle propulsion needs. At the same time, it is recognized that an electric motor of equivalent power operating at 40,000 rpm for intermittent boosting duty in race cars requires very low torque but high gear ratios. The conundrum is determining where between these two extremes in motor speed is the optimum. This project was designed to explore that space and to identify R&D gaps in motor technology. It is also well established that more compact electric machines have a much more demanding thermal management burden. To mitigate the thermal challenge, this project researched the use of lower-loss mild steel for laminations and higher-TC coating and potting materials. The benefits have been quantified and show 86% lower core loss with 6.5% Si steel and over 300% better TC with MgO-loaded epoxy matrix coatings. Table IV-3 summarizes the performance metrics of electric motors typical of industrial applications, automotive traction, and racing. The distinction between these application classes is motor speed.

Table IV-3: Electric motor comparison by speed.

Vendor	Motor Type	Mass (kg)	Peak Power (kW)	Speed (rpm)	SP (kW/kg)
Baldor	IM	238	75	1800	0.315
NISSAN	IPM	56	80	10,300	1.43
MTS	SPM	4.0	60	40,000	15

In Table IV-3, SPM is a surface PM design suited to high speed and ease of control. This project was motivated by the fact that the optimal specific cost ($/kW) and, by the same token, the specific power and power density of electric traction motors for PEVs remain largely unknown. Figure IV-13 puts this into perspective by noting the major contributors to specific cost—electromagnetic materials and the bearings and gears needed to match commercial gearboxes.

Industrial motors are designed to operate continuously for 20 years at rated power, and at a peak power 2.5 times the continuous power for short periods. EV traction motors are designed to operate intermittently for 7,500 h (13.3 year life of vehicle) and have rated power equal to their peak design power. Racing applications, such as kinetic energy recovery systems, are designed for the highest possible specific power. This project recognizes that reduction of heat generation, rapid heat removal, and adequate thermal management are on the path to the optimized electric traction motor.
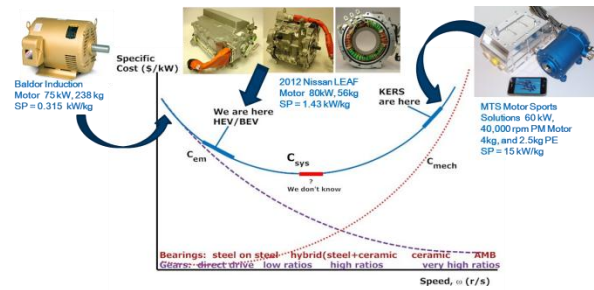
Figure IV-13: Electromagnetic and mechanical contributors to finding the optimal specific cost of electric traction motors.

Future Directions

- Continue design iteration on the high-speed IM stator design, specifically stator slot geometry, and update bill of materials mass and cost breakdown.
- Exercise the same IPM stators fabricated with different materials under PE inverter excitation and compare the core loss results with static and dynamic test results.
- Share the updated IM model parameters with the TDS simulation leader for validation over drive cycles. Share loss data with NREL colleagues for assistance on thermal design and request feedback regarding any concerns relevant to optimizing the motor design.
- Continue design iteration on the SRM and scale it to AEV power levels.
- Proceed into the next phase of Fe 6.5 wt. % Si+B low-loss lamination material and optimize the boron content for the best warm deformation processing, which includes the use of ultrasonic vibration during alloy processing and elimination of ordering phases [20].
- Coordinate the development of a next-generation traction inverter based on WBG semiconductor materials that best match motor designs.
- Perform TDS simulation of motor designs in an AEV simulation environment over combined drive cycles (e.g., UDDS+HWFET+US06+LA92+UDDS) and compare the resulting TDS efficiency with an IPM comparator.
- Address critical assumptions and issues found during FY 2013 program execution.
- Address the cost of currently available low-loss steels, such as JFE Corp. SuperCore™ 10JNEX900 (Fe 6.5% Si):
    – Develop a cost model for the new metallurgical process and compare it with commercial 29M19C5 grade steel.
    – Identify a commercialization partner and initiate technology transfer.
- Seek EMCs with higher TC, 2<TC<5, to promote more rapid heat removal from the traction motor core and windings.
    – Powder-coated cores must meet thermal cycling demands and retain electrical insulation properties in addition to high TC.

– Consider such high TC EMCs as coating alternatives in higher-temperature motor wires.

FY 2013 Publications/Presentations

1. B. Radhakrishnan, A. Shyam, C. M. Parish, and J. M. Miller, "Development of Fe 6.5% Si-B steels for motor core laminations," presented to DOE VTO propulsion materials program manager Jerry Gibbs, August 21, 2013.

2. R. Wiles, A. Wereszczak, C. Ayers, and J. M. Miller, *Powder Coating Motor Stators with Epoxy Molding Compounds (EMCs) to Eliminate Aramid Paper and Increase the Thermal Conductivity of the Winding Slots*, ORNL/TM-2013/44895, August 2013.

3. John M. Miller, "Game changing technologies in power conversion for electrification of vehicles (air, sea, ground)," panel presentation to IEEE International Transportation Electrification Conference, ITEC2013, Adoba Hotel, Dearborn, MI, June 17, 2013.

4. J. M. Miller, C. Ayers, B. Ozpineci, A. Wereszczak, and R. Wiles, *Design and Development of an Asynchronous Traction Motor to Meet DOE 2020 Targets*, ORNL/TM-2013/60, March 2013.

5. J. M. Miller, "Plug-in electric vehicle (PEV) traction motor and traction drive systems," IEEE Industry Applications Society Distinguished Lecture, Dayton PEAL Chapter, University of Dayton Research Institute, March 27, 2013.

6. J.M. Miller, "Tutorial on traction drive system, power electronics and electric motors," presented at DOE Headquarters to Vehicle Technology Program APEEM sponsor and U.S. DRIVE leads, January 17, 2013.

7. J.M. Miller, "Electric traction motors and EV Everywhere initiative," presented at BREM-VII Workshop, Ames Laboratory, Ames, IA, October 30, 2012.

8. J. M. Miller and R. L. Smith, *Vehicle Performance Metrics Applied to Electric Drive Vehicle System Research— Interim Report*, ORNL/TM-2012/305, September 2012.

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10. J. M. Miller, Traction Drive System breakout session (facilitator) for EV Everywhere Chicago Workshop, July 24, 2012.

11. John M. Miller, "Alnico and ferrite hybrid excitation electric machines," APE043, U.S. DOE Hydrogen and Fuel Cells Program and Vehicle Technologies Program Annual Merit Review and Peer Evaluation Meeting, Crystal City, VA, May 15–17, 2012.

12. John M. Miller, "Motor packaging with consideration of electromagnetic and material characteristics," APE035, U.S. DOE Hydrogen and Fuel Cells Program and Vehicle Technologies Program Annual Merit Review and Peer Evaluation Meeting, Crystal City, VA, May 15–17, 2012

13. John M. Miller, "Alnico and ferrite excitation electric machines," Electrical and Electronics Technical Team, U.S. Council for Automotive Research, Southfield, MI, April 26, 2012.

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20. K. Raviprasad, K. Chattopadhyay, "The influence of critical points and structure and microstructural evolution in iron rich Fe-Si alloys," *Acta Metallurgica and Materialia* **41**(2), 609–624, 1993.

FY 2013 Patents/Disclosures

1. B. Radhakrishnan, J. M. Miller, A. Shyam, and C. M. Parish, "Process for Making Fe-6Si Steel Laminations for Electric Motors," IDSA#3160, September 2013.

2. J. M. Miller, C. W. Ayers, and R. H. Wiles, "Cross-field Weakened Surface Permanent Magnet Generator," application S-124,492, disclosure #20120918, August 2013.

IV.2. Electric Motor Architecture R&D

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Start Date: October 1, 2012
Projected End Date: September 30, 2013

Objectives

Overall Objectives

- Support overall driveline system modeling (TDS efficiency and cost)
- Design matching driveline components for ORNL concept motors for test bed demonstration
- Provide modeling to validate speed/dynamics capability of ORNL concept motors, including gearing

FY 2013 Objectives

- Study evolution of driveline systems to benchmark industry direction, determine what changes are needed to reach DOE goals
- Provide study results, finite element analysis (FEA) data, and gear design concept(s) to the APEEM team
- Partner with the motor and gearbox industry to produce advanced concept of integrated gear/motor system for ORNL TDS design

Technical Barriers

- Bearing speeds
- Bearing quality and cost needed to meet speed requirements
- High-speed gear design manufacturing methods and cost
- Mass effect of additional gearing on power density

Technical Targets

- Motor (2020 target)
  - Cost: $4.7/kW
  - Specific power: 1.6 kW/kg

- TDS (2020 target)
  - Cost: $ 8/kW
  - Specific power: 1.4 kW/kg

Accomplishments

- Prepared technical assessment report evaluating benchmarked TDSs and selected state-of-the-art starter motors for high-speed operation
  - 2012 Nissan LEAF®, 2004 and 2010 Prius, 2011 Sonata, 2007 Camry, 2008 Lexus
  - 2010 Camry starter, Dixie Electric starter, Denso starter (planetary gears, gear manufacturing)
- Performed FEA modal analyses on several traction drive rotors, benchmarked units and ORNL concept rotors
  - 2012 LEAF
  - 2010 Prius
  - ORNL multiple isolated flux path (MIFP) SRM
  - ORNL outer rotor generator
  - ORNL IM design
- Performed FEA stress and thermal analysis for concept motors
- Designed gearing for ORNL concept motor(s)

✧ ✧ ✧ ✧ ✧

Introduction

Hybrid vehicle traction driveline gearing has evolved over the last decade to match ever-increasing speeds for HEV motors and generators. Auto manufacturers are using increased speed as a means to increase the power density of their electric traction motors in vehicles. ORNL is also pursuing traction motor designs that have much higher maximum rotor speeds, in the range of 15,000–25,000 rpm.

Improved gearing is needed to reduce the higher rotor speeds to match the final drive and wheel speed requirement, which does not change. Speeds for starters and alternators are also increasing in auto designs, so high-speed rotors and gearing for speed reduction are being developed in that automotive area as well. These efforts focus on increasing power density, making motors and generators smaller, reducing or eliminating the need for magnet material, and reducing the overall amount of materials required to produce these products (e.g., Cu, Si, steel). Accomplishments in those areas can reduce the cost of HEVs as well as reduce their weight.

Replacing conventional oversized motors with smaller motors using speed-reduction gearing has inherent design and cost tradeoffs. ORNL benchmarked drives are being examined, gear designs proposed, and gear manufacturers consulted to develop a concept that supports the ORNL goal of smaller, higher-speed motors. This effort strives to find the

best means of matching new higher-speed motors to existing drivelines in the gear trains of automotive traction drives.

No present technology can be extrapolated to meet DOE 2020 targets. Increasing speeds can enable motors to meet the targets.

Approach

- Assess the evolution of traction and starter motors as designs move from conventional to high-speed
- Analyze state-of-the-art rotors and ORNL rotors, conduct FEA modeling of structural stresses and modal behavior and their impact on high-speed operation
  - Rotor bending modes
  - Centrifugal stresses
  - Bearing loads
- Evaluate material limits for high-speed concept motor(s) and compare them with benchmarked commercial traction motor design limits
  - Cu rotor bar stresses
  - Lamination bridge stresses
  - Rotor end-ring retention
- Develop and deliver driveline designs for ORNL TDS high-speed concept motors to the APEEM team

Results

Rotor modal analysis

Four rotors were analyzed and compared for modal response to see how rotor geometry affects design and speed limitations. The 2010 Prius, the 2012 LEAF, the ORNL MIFP 15,000 rpm SRM, and the ORNL 23,000 rpm IM rotors were examined.

A 23,000 rpm version of the ORNL MIFP is currently being developed, and results from that design are shown as well. The rotor diameter will decrease somewhat to the approximate size of the ORNL IM, and the rotor will stretch axially from its present design.

The two rotors shown in Figure IV-14 are the commercial rotors that were initially modeled to provide baseline information on these mode shapes. Models of the ORNL concepts were analyzed as the designs progressed.
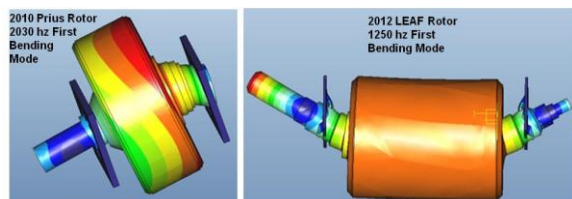
Figure IV-14: Rotor first bending mode analyses for 2010 Prius and 2012 LEAF.

Figure IV-15 shows an analysis of the ORNL IM model and the first bending mode of that rotor design.
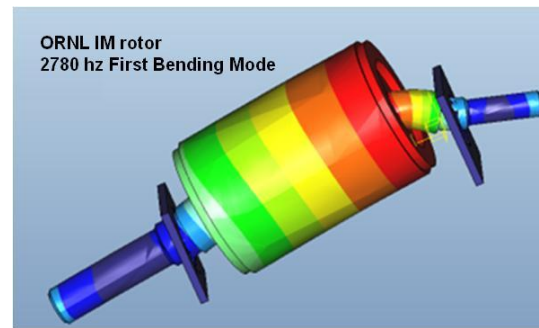
Figure IV-15: ORNL induction machine (Cu rotor) concept machine modal analysis.

Similar bending mode analyses are shown for the first- and second-generation ORNL MIFP SRMs. The first-generation unit was built and tested in FY 2012 at ORNL. The second-generation unit is under design and analysis for operation at 23,000 rpm, similar to the ORNL IM. Figure IV-16 shows the results of the modal analyses for those rotors.
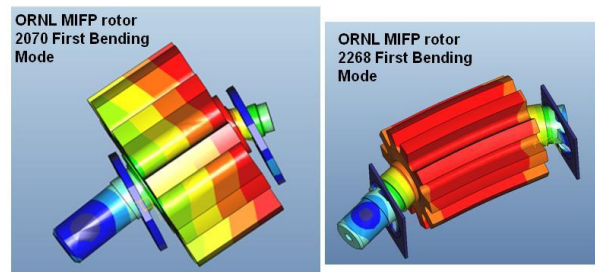
Figure IV-16: ORNL MIFP SRMs. Left: first-generation prototype (built and tested); right: second-generation prototype rotor (concept).

It was found that all the first bending mode frequencies in these various designs were extremely high compared with operating speeds. The results are tabulated in Table IV-4.

Table IV-4: Modal analysis results for several commercial and concept motor rotors.

Rotor	Max Operating Speed	First Bending Mode Frequency
2010 Prius	14000 rpm	122000 rpm
2012 LEAF	10400 rpm	75000 rpm
ORNL MIFP	15000 rpm	124000 rpm
ORNL IM	23000 rpm	167000 rpm
ORNL MIFP	23000 rpm	136000 rpm

An important observation based on these analyses is that the first bending resonance of these shafts is not the limiting factor in high-speed capability. The bending modes are all six to eight times higher than the maximum operating frequency. Speed capability is also typically limited by bearing speeds, magnet retention, rotor bar retention, and other factors; so one or more of these factors will be the major contributors to speed

limitations, as opposed to magnet or rotor bar retention strength.

Rotor /lamination centrifugal stresses were studied on the ORNL concept motors. These rotors do not have the magnet retention stress problem typically found in common IPM motors. The ORNL MIFP has an extremely simple rotor— stamped laminations with rotor pole radial extensions. This rotor has a speed capability of at least 30,000 rpm based on the lamination stress, as seen in Figure IV-17 for the first- and second-generation units.

ORNL Gen1 MIFP stress at 30 krpm
Max stress 49 ksi @ tooth root

ORNL Gen1 MIFP stress at 30 krpm
Max stress 23 ksi @ tooth root
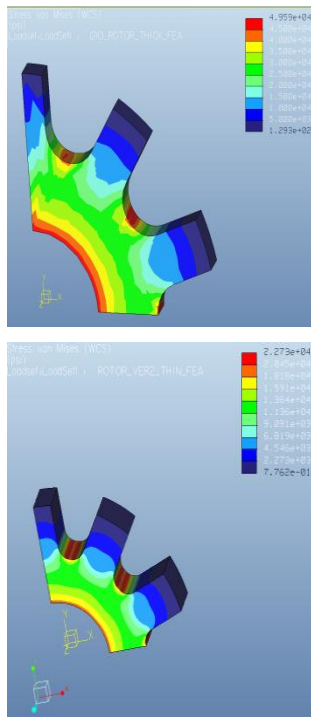
Figure IV-17: Lamination simulated stresses for the generation 1 and 2 ORNL MIFP SRMs.

The rotor in the ORNL IM is somewhat more complex because of the Cu rotor bars inserted through the laminations. This geometry creates a thin area (bridge) in the outer perimeter of the lamination that is similar to the design of PM rotors. The bridge area is the weak link in this design, and FEA simulations (Figure IV-18) show that the stress is highest at the bridge but still acceptable at 23,000 rpm. More information can be obtained for this design in Miller et al. [1].

ORNL IM stress at 23 krpm
Max stress 51 ksi @ lamination bridge
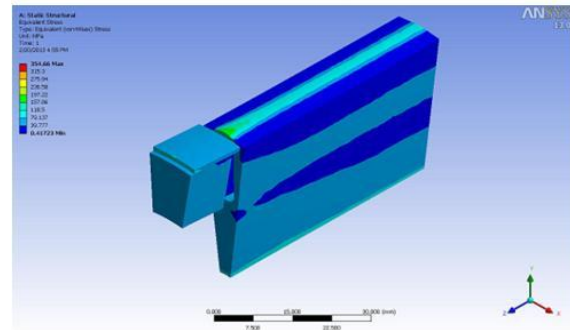
Figure IV-18: Lamination bridge stress from copper rotor bar for the ORNL IM concept.

Driveline matching design work

Gear design is key in the matching of the new higher-speed motor to a generic automobile drive train. The high-speed motor concept includes applying an in-line planetary gear set (sun gear, 3–4 planet gears, planet carrier, and ring gear) and matching the ratio of this set to the remaining gears in the drive train. It has been calculated that a total reduction of about 14:1 or 15:1 will be required for a 23,000 rpm motor to match a 1,600 rpm maximum axle speed. A first-cut design completed by MagnaPowertrain uses a planetary reduction of 4.6:1 and a final gear reduction of 3.7:1. This design for the gear system from motor to axle (represented in Figure IV-25–Figure IV-28 later in this section) is based primarily on the geometry of the 2007 Toyota Camry.)

Gear losses are related to the power transferred through a gear train. Calculations for gear power and losses were based on data from one of the ORNL concept motors.

Representative torque and power curves for the ORNL IM are shown in Figure IV-19. Calculations for gear power and losses are based on these data and can be linearly adjusted based on any final adjustments to this concept motor performance or curves from a similarly designed ORNL concept motor.
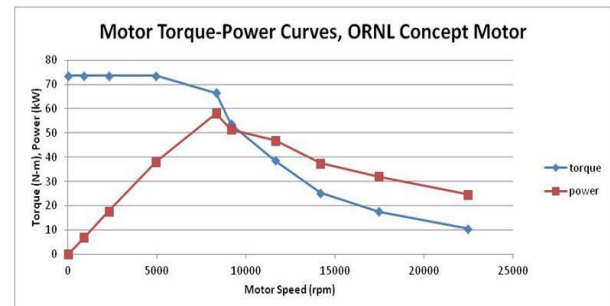
Figure IV-19: Torque/power vs. speed for an ORNL high-speed concept motor.

In a final design, speed and torque range will be interconnected with shaft sizes and thus with available bearing sizes for a given design choice. The graph in Figure IV-20 shows a curve developed from standard bearing inner diameters and the highest speed rating of each size. Overlaid

on this graph is another curve based on the torque capability calculation from torsion in the shaft.
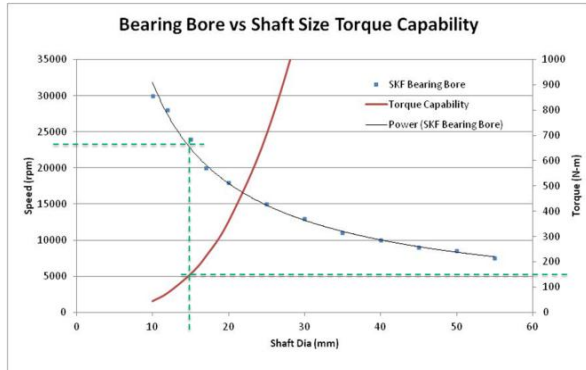
Figure IV-20: Relationship among bearing bore, shaft size, and torque capability for motors.

Shaft diameter for a given torque is based on the equation

$d^3 = (16 * T) / (Pi * \tau_{max})$,

where d = shaft diameter

T = shaft torque

τ = shear strength of the material

The material used for the example represented in Figure IV-20 was AISI 4340 steel, σ_{yield} = 100,000 psi and τ_{max} = 50,000 psi.

The two curves in Figure IV-20 can be used to deduce the torque capability and speed range a particular shaft design can handle. The example shown by the green dashed line is a 23,000 rpm shaft of 15 mm diameter; it can handle about 150 N-m torque. As speed is increased for a given traction motor application, the torque requirement at the motor output shaft is reduced. This reduction allows the motor shaft size to be reduced, allowing the bearing diameters to decrease and thus increasing the bearing speed range.

To further examine an application for a high-speed concept motor, the gear design and the losses associated with it should be addressed. For high-ratio gear reductions, potential power (apparent power) can be used to determine losses associated with a gear design across the speed range of the system.

Potential power (similar to reactive power in electronic circuits) circuits) is based on the product of pitch line force and pitch line velocity for each gear mesh in a gear train (Figure IV-21). Losses can simply be estimated by applying a rule-of-thumb loss percentage to the potential power at each individual gear mesh (1% at each gear mesh is a typical number—this can be adjusted based on empirical testing of the actual motor and gear train). The *shape* of the potential power curve (and the loss curves) will be the same as for the motor power curve, but with varying absolute values depending on the nature of the gear mesh for which it is calculated.

Figure IV-22 shows estimated gear losses in watts for each gear mesh in the concept design (based on Figure IV-19 data). These data can be used in the system model to see

what impacts gear issues have on overall system losses. A related ORNL task is developing models for the overall system using a drive cycle and inputs from the various parts of the TDS. From this task, a couple of inputs for the overall system model can be the gear losses vs. speed, and an estimate of churning losses vs. temperature in the gearbox lubricant.
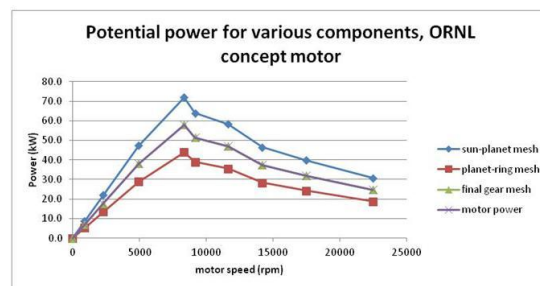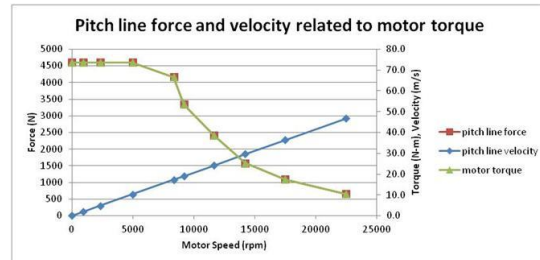
Figure IV-21: Pitch line force/velocity (upper), potential power for components (lower).
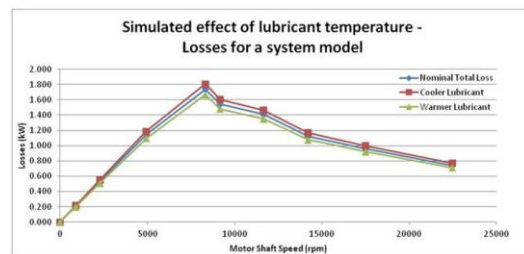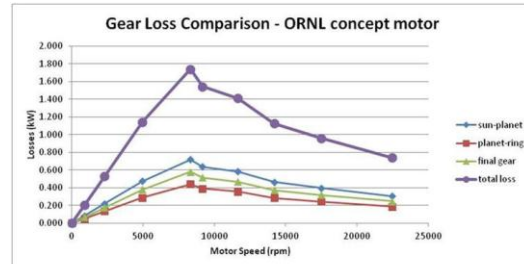
Figure IV-22: Losses for gear mesh locations (upper) and estimated losses due to lubricant temperature (lower).

The ORNL combined drive cycle (CDC) is a close approximation of real world driving. The cycles used are UDDS, HWFET (Highway Fuel Economy Test), US06, and LA92, which are combined in series to form the ORNL CDC. Based on the CDC, calculations were performed to estimate the dwell time for vehicle operation in each of several speed bands. The band stops are 17.9, 35.8, 53.7, and >71.7 mph. Figure IV-23 shows the time fraction in each band and the maximum speed a traction motor would reach in those bands. Only about 1.2% of time is actually spent above 15,000 rpm in

reality, and the vehicle is stopped for around 14% of the time. Most of the time is spent at motor speeds in the 3,500 to 15,000 rpm range.
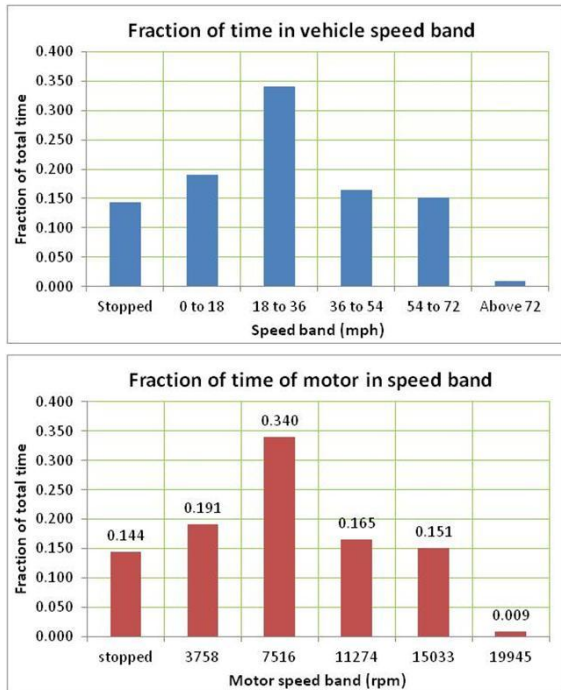
Figure IV-23: Relative fraction of time a 15:1 ratio traction drive system will spend in different speed bands.

To get a feel for how gear losses impact the system over a CDC, an overlay was made using the gear loss graph and the speed bands dwell time, seen in Figure IV-24. It is interesting to note that the dwell times follow the shapes of the power curves fairly well.
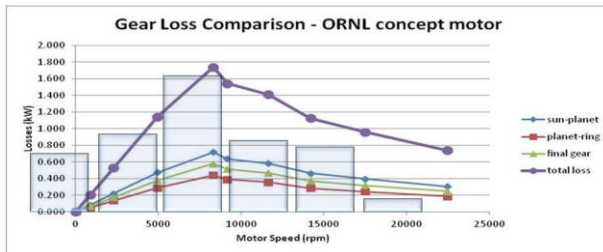
Figure IV-24: Overlay of dwell time estimates (translucent bars) over the gear loss curves.

Approximate gear losses can be calculated using potential power methods. Losses are highest for the first (highest-speed) gear mesh at the motor shaft.

A couple of observations can be made from the analysis of gears and the system geometry.

1. Trading a high-speed, high-reduction planetary for some of the existing conventional gears (as seen in the benchmark drives) can be evaluated. It appears to be a good efficiency and cost tradeoff based on findings.

2. It is possible that this new layout (assuming gears/bearings can be removed) could be as efficient as

or more efficient than existing designs. The gear diagrams indicate that *two gears, one gear mesh, and at least one bearing* can be removed from a typical system.

Based on observation and study of existing systems, and combining this information with the specifications of the ORNL concept motors, a gearing philosophy was chosen to match the higher-speed motor to existing drivetrain speeds for conventional sedans. An in-line planetary was chosen to mount adjacent to the motor output shaft; it would reduce the speed to a reasonable level to drive a pinion and main drive gear at the vehicle axle differential.

MagnaPowertrain calculations provided a gear set design to ORNL, and the resulting specifications were used to assemble a conceptual design for the drivetrain connecting a 23,000 rpm motor to a 1,600 rpm axle. Figure IV-25 shows the overall modeled concept of the motor connected to the differential with an axle.
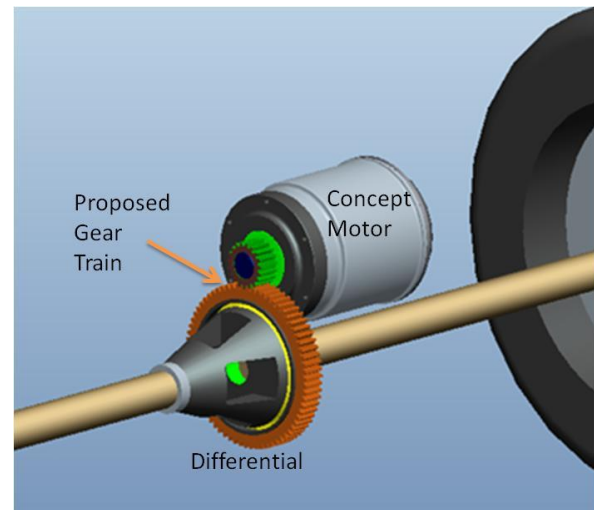
Figure IV-25: ORNL concept matched driveline, 23,000 rpm motor.

The ORNL concept motor has a higher L/D ratio than those used by today's typical HEV traction drives. This allows the motor to lie in closer proximity to the axle centerline and enables the simpler high-speed driveline.

Figure IV-26 is an exploded view of the concept driveline showing the internal parts and how they assemble to one another. Lubrication and cooling are remaining issues that need to be addressed for this design, and they are part of the next steps as this project continues. This work could be done as an integral part of a housing design that contains the motor, gears, and bearings.

Figure IV-27 and Figure IV-28 show additional views giving more detail on the internals of the ORNL driveline concept.
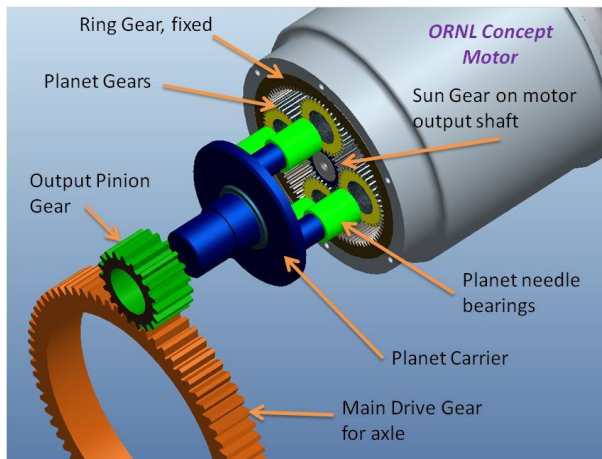
Figure IV-26: Exploded view of ORNL concept driveline with MagnaPowertrain calculated gears.
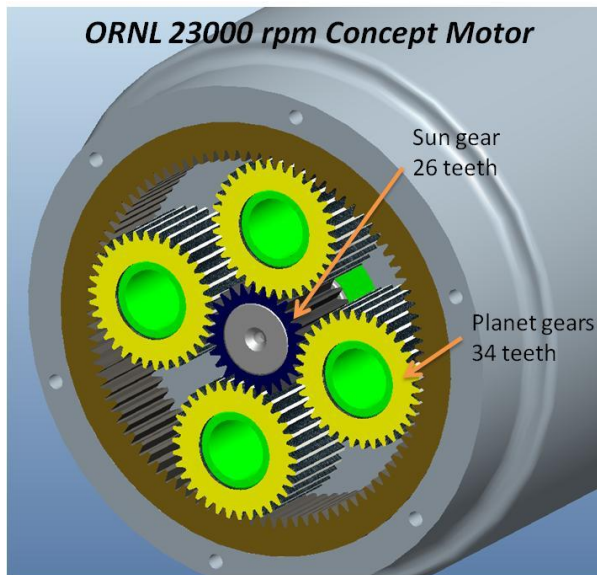
Figure IV-27: Close-up view of in-line planetary at motor shaft.
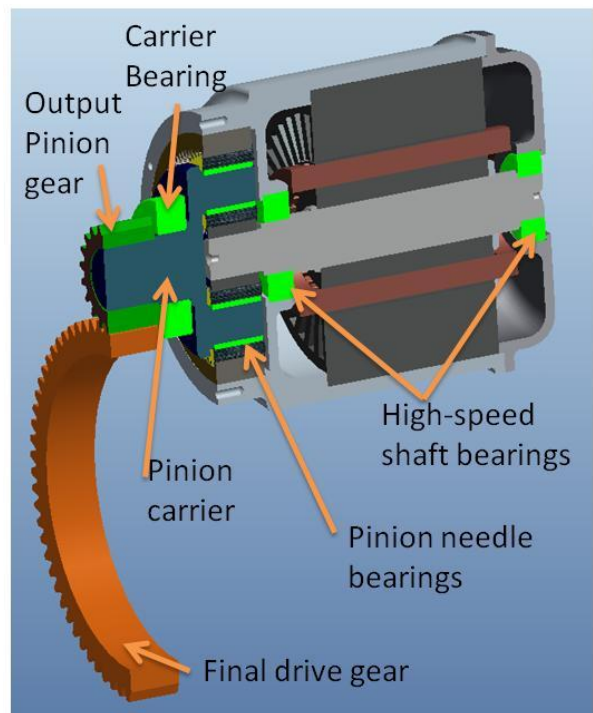
Figure IV-28: Section view of 23,000 rpm ORNL matched driveline concept.

Earlier in the year, consultations with Regal Beloit yielded interest in our high-speed motor, SRM concepts, and high-speed gearing for the traction drive application. Regal Beloit performed some initial calculations to evaluate the concept and determined that it was achievable with reasonable gear designs. Their calculations, using their gear software, for the in-line planetary gear set to be mounted to the ORNL concept motor are shown in Figure IV-29.

KISSSOFT
Calculation programs for machine design

```
——————— KISSsoft - Release 03-2012F ———————
Milwaukee Gear Division of Regal Beloit Corp
——————————————— File ———————————————
Name    : 28NDP-4 planet KissSoft fine size
Changed by : 100088887      on: 09.05.2013      at: 14:19:21


Important hint: At least one warning has occurred during the calculation:
1-> Transverse contact ratio is < 1 !

2-> Mounting in radial direction at
the assembly is not possible!

3-> Notice concerning gear 1:
Dimension over balls is not measurable (facewidth is too small)!

4-> Notice concerning gear 3:
Dimension over rollers is probably not measurable (facewidth is a bit too short)!


CALCULATION OF A HELICAL PLANETARY GEAR

Drawing or article number:
Gear 1:  0.000.0
Gear 2:  0.000.0
Gear 3:  0.000.0

Calculation method  AGMA 2001-D04

                                         ------- Gear 1 --------- Gear 2 --------- Gear 3 ---
Number of planets              [p]              (1)               3               (1)

Power (hp)                     [P]                           73.75
Transmitted power (hp)         [P]                           73.75
Transmitted power (ft*lb/s)    [P]                           40562
Speed (1/min)                  [n]        23000.0                             0.0
Speed difference for planet bearing calculation (1/min)
                               [n2]                          12197.9
Speed planet carrier (1/min)   [nSteg]                        4344.4

Torque (ft*lbf)                [T]          16.8             0.0               72.3
Torque Pl.-Carrier (ft*lbf)    [TSteg]                      89.188

Overload factor                [Ko]                          1.00
Power distribution factor      [Kgam]                        1.00
Required service life          [H]                        20000.00
Gear driving (+) / driven (-)                  +             -/+               -
Gearbox type:  Standard gearing in closed housing


1. TOOTH GEOMETRY AND MATERIAL

   (geometry calculation according to
               ISO 21771:2007)
                                         ------- Gear 1 ----------- Gear 2 ------------- Gear 3 ---
Center distance (in, mm)       [a]                       1.2000, 30.480
Centre distance tolerance                     ISO 286:2010 Measure js7

Normal Diametral Pitch (1/in)  [Pnd]                      19.00003
Normal module (in, mm)         [mn]                  0.05263, 1.3368
Pressure angle at normal section (°)  [alfn]                20.0000
Helix angle at reference circle (°)   [beta]              15.0000
Number of teeth                [z]         17               26               -73
Facewidth (in)                 [b]         0.42             0.42             0.42
Hand of gear                               right            left             left

Planetary axles can be placed in regular pitch.:      120°

Accuracy grade (    AGMA 2015)  [Q-AGMA2015-1-A2001]      A6    A6    A6
Inner diameter (in)            [di]        0.00             0.00
External diameter (in)         [dj]                                          0.00
Inner diameter of gear rim (in)  [dbi]    0.00             0.00
Outer diameter of gear rim (in)  [dbi]                                       0.00
Material
Gear 1:            18CrNiMo7-6, Case-carburized steel, case-hardened
                   ISO 6336-5 Figure 9/10 (MQ), core strength >=25HRC Jominy J=12mm<HRC28
Gear 2:            18CrNiMo7-6, Case-carburized steel, case-hardened
                   ISO 6336-5 Figure 9/10 (MQ), core strength >=25HRC Jominy J=12mm<HRC28
Gear 3:            18CrNiMo7-6, Case-carburized steel, case-hardened
                   ISO 6336-5 Figure 9/10 (MQ), core strength >=25HRC Jominy J=12mm<HRC28

                                         ------- Gear 1 ----------- Gear 2 ------------- Gear 3 ---
Surface hardness                           HRC 61           HRC 61           HRC 61
                                     (lb/in²),(N/mm²)   (lb/in²),(N/mm²)   (lb/in²),(N/mm²)
Allowable bending stress number  [sat]   62366, 430.0   62366, 430.0   62366, 430.0
Allowable contact stress number  [sac]  217887,1500.0  217887,1500.0  217887,1500.0
Tensile strength (lbf/in²)       [Rm]    174046.02       174046.02       174046.02
Yield point (lbf/in²)            [sige]  123282.60       123282.60       123282.60
Young's modulus (lbf/in²)        [E]     29877900        29877900        29877900
Poisson's ratio                  [ny]     0.300            0.300            0.300
Mean roughness, Ra, tooth flank (mil)  [RAH]  0.02        0.02            0.02
Mean roughness height, Rz, flank (mil)  [RZH]  0.19       0.19            0.19
Mean roughness height, Rz, root (mil)   [RZF]  0.79       0.79            0.79

Tool or reference profile of gear  1 :
Reference profile 1.25 / 0.38 / 1.0 ISO 53.2:1997 Profil A
```

Figure IV-29: Gear software calculations from Regal Beloit for ORNL's early in-line planetary concept.

Later in the year, and after more complete designs were developed for the ORNL concept motors, we met with MagnaPowertrain to discuss an overall matched driveline. This company has the capability to manufacture the entire unit from motor to axle, and its representatives expressed interest in working with ORNL to produce a prototype. They provided some effort at no cost to look into the driveline matching and high speed in-line planetary idea for ORNL concept motors. Using a conceptual description of our needed gear system, MagnaPowertrain conducted some preliminary design/ calculations for ORNL. Data from its calculations for the design, showing some of the gear information, are shown in Figure IV-30. Figure IV-25–Figure IV-28 are geometrically correct 3-dimensional (3D) models derived from MagnaPowertrain's calculations.

```
8-> Gear pair  2 - 3 :
The transverse load factor Kha is very high.
The formulae in the standard probably do not suit this case.


CALCULATION OF A HELICAL PLANETARY GEAR

Drawing or article number:
Gear 1:  0.000.0
Gear 2:  0.000.0
Gear 3:  0.000.0

Calculation method  ISO 6336:2006 Method B

                                         ------- Gear 1 --------- Gear 2 --------- Gear 3 ---
Number of planets              [p]              (1)               3               (1)

Power (kW)                     [P]                           55.00
Speed (1/min)                  [n]        23000.0                             0.0
Speed difference for planet bearing calculation (1/min)
                               [n2]                          13777.5
Speed planet carrier (1/min)   [nSteg]                        4983.3

Torque (Nm)                    [T]          22.8             0.0               62.6
Torque Pl.-Carrier (Nm)        [TSteg]                      105.394

Application factor             [KA]                          1.25
Power distribution factor      [Kgam]                        1.00
Required service life          [H]                        20000.00
Gear driving (+) / driven (-)                  +             -/+               -

1. TOOTH GEOMETRY AND MATERIAL
   (geometry calculation according to
               ISO 21771:2007)
                                         ------- Gear 1 ----------- Gear 2 ----------- Gear 3 ---
Center distance (mm)           [a]                            38.025
Centre distance tolerance                     ISO 286:2010 Measure js9

Normal module (mm)             [mn]                          1.2500
Pressure angle at normal section (°)  [alfn]                22.5000
Helix angle at reference circle (°)   [beta]               15.0000
Number of teeth                [z]         26               34               -94
Facewidth (mm)                 [b]         30.00             32.00            30.00
Hand of gear                               left             right            right

Planetary axles can be placed in regular pitch.:      120°

Accuracy grade                 [Q-ISO1328:1995]    7        7        9
Inner diameter (mm)            [di]       25.00            30.00
External diameter (mm)         [dj]                                          150.00
Inner diameter of gear rim (mm)  [dbi]    0.00            0.00
```

Figure IV-30: Gear software calculations from MagnaPowertrain for ORNL's latest in-line planetary concept.

In the effort to look at the entire driveline, MagnaPowertrain looked at the final drive gears in addition to the planetary section (Figure IV-25–Figure IV-28). shows the calculations from that work by MagnaPowertrain.

KISSSOFT
Calculation programs for machine design

```
——————— KISSsoft - Release 03-2012F ———————
Magna Powertrain of America, Inc.
——————————————— File ———————————————
Name    : Final Drive Pinion & Ring
Changed by : wenthen      on: 19.07.2013      at: 16:19:58


Important hint: At least one warning has occurred during the calculation:
1-> Notice to gear 2:
NOT POSSIBLE TO MEASURE BASE TANGENT LENGTH!
The width of the gear is too small, hence the tooth thickness too big,
so that the required length for the measurement exceed the face width.


CALCULATION OF A HELICAL GEAR PAIR

Drawing or article number:
Gear 1:  0.000.0
Gear 2:  0.000.0

Calculation method  ISO 6336:2006 Method B

                                         ------- GEAR 1 -------- GEAR 2 --
Power (kW)                     [P]                           55.000
Speed (1/min)                  [n]         4983.3           1352.6
Torque (Nm)                    [T]         105.4            388.3
Application factor             [KA]                         1.25
Required service life          [H]                        20000.00
Gear driving (+) / driven (-)                  +             -

1. TOOTH GEOMETRY AND MATERIAL
   (geometry calculation according to
               ISO 21771:2007)
                                         ------- GEAR 1 -------- GEAR 2 --
Center distance (mm)           [a]                          135.000
Centre distance tolerance                     ISO 286:2010 Measure js9
Normal module (mm)             [mn]                          1.7500
Pressure angle at normal section (°)  [alfn]                20.0000
Helix angle at reference circle (°)   [beta]               25.5000
Number of teeth                [z]         19               70
Facewidth (mm)                 [b]         32.00            30.00
Hand of gear                               left             right
Accuracy grade                 [Q-ISO 1328:1995]    7        7
Inner diameter (mm)            [di]        0.00            160.00
Inner diameter of gear rim (mm)  [dbi]    0.00            0.00
Material
Gear 1:            SAE8620(20Ni1CrMo2-2), Case-carburized steel, case-hardened
                   ISO 6336-5 Figure 9/10 (MQ), core strength >=30HRC
Gear 2:            SAE8620(20Ni1CrMo2-2), Case-carburized steel, case-hardened
                   ISO 6336-5 Figure 9/10 (MQ), core strength >=30HRC
```

Figure IV-31: Gear software calculations from MagnaPowertrain for the final drive gears for ORNL's matched driveline concept.

Shaft speeds for vehicles benchmarked by ORNL have increased from the 2004 Prius at 6,000 rpm to the 2007 Camry at 14,000 rpm (Table IV-5). In addition, a non-benchmarked vehicle, the Tesla, boasts a 15,000 rpm motor with a direct driveline from motor to axle. The 2010 Prius motor maximum speed is at 13,500 rpm, and a couple of the others are around 10,000 rpm. The industry appears to have

stopped at around 14,000–15,000 rpm, and indications from ORNL studies are that most of the bearings chosen (conventional choices) appear to be near or at design speed limits for their specific applications. Ayers [2] has additional information on this subject.

Table IV-5: Vehicle speeds and related gearing information.

Vehicle (Make/year)	ω_{Motor} (rpm)	Gear Ratio $\omega_{mot}/\omega_{whl}$	# of Clutch Sets	# of Gears mtr-diff'l
2004 Prius	6000	4.11	0	6
2010 Prius	13500	8.61	0	7
2007 Camry	14000	8.78	0	7
LEAF	10400	7.93	0	4
Sonata	6000	6 spd trans.	5 sets	7 (plus idle gears)
2008 Lexus	10200	2 spd trans	2 sets	?
Tesla	15000	8.275	0	?

Conclusions and Future Directions

- Driveline matching for an ORNL high-speed (23,000 rpm) concept motor has been successful. ORNL has two concept motor designs using no PMs that will perform well in this high-speed traction driveline concept.
- A conceptual design was completed showing the concept motor and in-line planetary and main drive gears in conjunction with a drive axle system to demonstrate the geometry of the system and the fit of the motor, gears, and axle. Precise modeling of the final concept system was performed using ProEngineer 3D modeling software based on design models of all the individual components and various calculations.
- Discussions with Regal Beloit early in the year indicated the company's interest in this design and the ORNL MIFP SR concept motor. Regal Beloit provided a potential gear design for the driveline matching gear set (primarily the planetary reduction at the motor). Its research indicated gear speeds were high but not exorbitant.
- Design study and discussions with MagnaPowertrain show strong interest in this area of work and confirm that this design is viable. The company looked further into the gear reduction requirements with ORNL and agreed that the concept using our suggested planetary and two main gears was workable. MagnaPowertrain provided a design for all the gears from

the motor shaft to the axle (differential), and those data were used to produce the motor-to-axle 3D model shown in Figure IV-25–Figure IV-28.

- Losses are on the order of 3% for the whole ORNL concept gear train from the motor output shaft up to the main differential carrier gear. This loss number is based on rule-of-thumb estimation and potential power calculations for the proposed gear train. Follow-on work will confirm exact losses via modeling and ultimately dynamometer testing in the ORNL laboratory using the ORNL concept motor and prototype gear train.
- High-speed motors enable the following:
  – Smaller, lighter, higher-power-density designs (lower cost)
  – Smaller diameter and a thinner structure that allows closer packaging to the axle (enabling elimination of some gears/bearings)

Future

- Downselect TDS matching architecture
- Continue collaboration with Regal Beloit and MagnaPowertrain
- Continue support of APEEM team with design/modeling

FY 2013 Publications/Presentations

1. "Electric motor and driveline matching," presented at the DOE VPT 2013 Kickoff Meeting, November 2012.
2. "Electric motor architecture R&D," presented at DOE VPT Annual Merit Review poster session, Washington, DC, May 2013.
3. "Electric motor architecture R&D," presented at the Electrical and Electronics Technical Team meeting, Dearborn, Mich., June 2013.

References

1. J. M. Miller, C. Ayers, A. Wereszczak, B. Ozpineci, R. Wiles, *Design and Development of an Asynchronous Traction Motor to Meet DOE 2020 Targets,* ORNL/TM-2013/60, March 2013.
2. C. W. Ayers, *Traction Drive and Gearing Design Comparisons*, ORNL/TM-2013-482 September 2013.

IV.3. Permanent Magnet Development for Automotive Traction Motors

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Subcontractors:
Univ. Nebraska-Lincoln, ORNL, Univ. Maryland,
Brown Univ., Arnold Magnetic Technologies, Inc.

Start Date: August 2001
Projected End Date: September 2015

Objectives

- Develop the materials and processes needed to fabricate high performance permanent magnets (PM) that can be used for advanced traction drive motors with an internal PM rotor design to meet APEEM goals for enhanced performance at elevated temperature (180-200°C) and reduced cost.
- Anisotropic magnets should be developed to satisfy the need for magnets with maximum magnetic energy density and minimum content of valuable materials. If possible, improved magnet forming processes and mechanical properties also should be developed to further reduce motor manufacturing costs and extend lifetime in service.
- While magnet materials meeting the technical specifications are currently achieved using rare earth (RE) permanent magnets, the market factors of rising RE demand, uncertain RE cost, and near total foreign control of RE supplies dictate that alternative non-RE magnets must be developed.

Technical Barriers

High energy density permanent magnets (PM) are needed for compact, high torque drive motors for HEV, PHEV, and EV. These drive motors should have reduced cost and be highly efficient, which requires PM of high energy density that are made in net shape (preferably) by simple mass production methods. Although PM made from RE elements are currently used in electric drive motors, the recent history of drastically rising prices of RE elements, a nearly singular source for RE supplies, the uncertain future RE prices, and a looming shortage of RE elements, especially Dy, provides motivation

for research into alternative PM materials. Alternative permanent magnets must have high temperature tolerance and long life in harsh vehicle environments.

Technical Targets

- High energy density permanent magnets (PM) needed for compact, high torque drive motors (specific power >1.4 kW/kg and power density >4.0 kW/L).
- Reduced cost (<$8/kW): Efficient (>94%) motors require aligned magnets with net-shape and simple mass production.
- Greatly reduce or eliminate RE elements: Rising prices of RE elements, price instability, and looming shortage, especially Dy.
- Performance & Lifetime: High temperature tolerance (150-200°C) and long life (15 yrs.) needed for magnets in PM motors.

Accomplishments

- Discovered that Zn (vapor) coating with Al addition to glassy $MRE_2(Fe,Co)_{14}B$ flake could boost by 20% the ambient temperature coercivity and energy product of fully dense anisotropic magnets that were fabricated by single stage hot deformation (SSHD) method, but high negative temperature coefficients forced this approach to be abandoned.
- Found by use of Lorentz microscopy mode in TEM that off axis grains in alnico 8 had pinned domains around orthogonal regions of spinodal pattern that were spaced on order of microns apart, which appeared to be a useful new mechanism to raise coercivity.
- Produced first batch of inert (Ar) gas atomized pre-alloyed powder of alnico 8 with a high yield of fine, spherical powder (average powder dia.=30µm), close control (± 0.1wt.%) of final powder composition, and low oxygen content (420ppmw), even in dia.<20µm powder.
- Fabricated first fully dense alnico 8 bulk magnet from pre-alloyed gas atomized powder by HIP consolidation at solutionizing temperature (1250°C), followed by magnetic annealing (at 810°C) and drawing (at 650°C), based on initial recommendations from industrial partner. Measured magnetic properties with hysteresisgraph and produced comparable properties to sintered alnico 8, e.g., achieved 93% of Br (remanent magnetization) and 62% of Hci (intrinsic coercivity).
- Achieved 20% increase in Br in demonstration of powder alignment in an epoxy-bonded alnico 8 magnet made with a mixture of single crystal and polycrystalline spherical powders, compared to unaligned powders of the same size class.
- Discovered that all size classes (up to 106µm) of as-atomized pre-alloyed alnico 8 solidified as a single α (B2) phase, bypassing γ-phase formation and the α-phase

spinodal "splitting," which presents the intriguing possibility that an expensive high temperature heat treatment can be avoided by developing a consolidation processing approach that maintains single-phase α until decomposition in a magnetically biased spinodal reaction to produce an ideal nano-structure with elongated Fe-Co (BCC) phase within a non-magnetic (L2$_1$) matrix phase for enhanced magnetic properties.

- Performed initial low temperature (770-790°C) consolidation experiment on alnico 8 as-atomized powder by spark plasma sintering (SPS) in attempt to avoid solutionizing anneal prior to magnetic annealing and drawing to produce dense bulk magnets, but did not achieve fully densify (91.5% dense) and observed γ-phase formation within microstructure, pointing the way to improvements in future consolidation methods.

- Developed alloy re-design strategy to replace excess Co that was found to reside in L2$_1$ matrix phase of alnico 8 and 9 and verified effectiveness with cast bulk alloys of matrix phase alone and as fully substituted magnet alloys, where developments based on this will be investigated by theoretical calculations and further experiments, including melt spinning and gas atomization.

- Expanded theoretical work on alnico model systems using theoretical tools based on Monte Carlo calculations with existing computer clusters to explore elemental substitutions in alnico alloys and to establish ability to simulate conditions for spinodal phase separation, albeit with significant error in simulated transformation temperature.

- Established correlations between 2 types of theoretical predictions and the results of thin film combinatorial synthesis work on Fe-Co-X systems, where X=5d and 4d (e.g., W, Ta, Mo) and demonstrated (for X=Mo) formation of an aligned columnar structure (reminiscent of alnico) with nano-metric spacing and "single phase" PM behavior with coercivity of 2 kOe.

- Produced aligned nano-metric exchange coupled magnet samples from separate sources of Fe-Co (soft) and Co$_{11}$Zr$_2$ (hard) nano-particulate with dual beam cluster deposition in an applied field.

<p style="text-align:center">✧   ✧   ✧   ✧   ✧</p>

Introduction

Rare Earth Magnetic Materials

Permanent magnets based on RE$_2$Fe$_{14}$B intermetallic compounds, with Nd$_2$Fe$_{14}$B as a prototype, have had a large technological impact because of their unsurpassed (in bulk form) magnetic energy density. Over the past 30+ years since the discovery of Nd$_2$Fe$_{14}$B, extensive research has been performed to develop and improve the magnetic performance of the family of RE$_2$(Fe-Co)$_{14}$B (2-14-1) magnetic compounds and to reduce their cost of production. Commercially, two 2-14-1 magnet classes; aligned-sintered (microcrystalline) and isotropic-bonded (nano-crystalline), have been successfully developed. It should be noted that

aligned-sintered Nd$_2$Fe$_{14}$B magnets are currently used in hybrid vehicle systems with interior PM motor designs that require high magnetic torque. However, the magnetic torque-dominated motor design and the reduced level of automation during assembly of these motors have been judged (by at least one of the OEM partners) to be impractical for very large-scale mass production at a sufficiently low cost. Alternatively, the opportunity exists to use new motor designs that utilize increased reluctance torque, and, as such, are well suited to the reduced ambient temperature magnetic flux available from alternative magnets that retain strength at higher temperatures, up to 180-200°C. This was investigated in an August 2008 consultant's report, "System Cost Analysis for an Interior Permanent Magnet Motor" from an independent expert, Dr. Peter Campbell. The report evaluated the range of viable rare earth based permanent magnet materials for an interior permanent magnet (IPM) motor at a time when the cost for 2-14-1 magnets were just starting to begin its dramatic rise (to a peak in August of 2011). The report found that there are two viable alternatives for IPM motors that meet the FreedomCar goals; anisotropic sintered magnets with reduced Dy content and anisotropic bonded magnets, if high temperature improvements could be made with decreased Dy. Dr. Campbell's report did anticipate a looming shortage of "heavy" RE elements, like Dy, but did not anticipate the extreme RE price instability that occurred 3 years later. He did certainly encourage continued work on further development of low cost processing of the Ames (mixed rare earth) MRE 2-14-1 magnet alloys.

Based on knowledge of the improved magnetic properties at high temperature of Y substitutions for Nd in the MRE 2-14-1 compound (that can reduce or eliminate Dy), it is possible that the ability to produce a highly aligned (nano-crystalline) structure can result in reasonable room temperature magnetic properties and sufficient high temperature (180-200°C) magnetic strength for improved drive motors. If enough manufacturing advantage can be gained by combining alignment and net-shape forming of extrinsically sintered RE magnets, this could provide an intermediate option for PM motor designers that prefer the familiar 2-14-1 magnets. These concepts are being pursued within the scope of the present project by focusing on generating amorphous ribbon of several types of modified alloys that is devitrified under uni-axial pressure. To enable the maximum energy product to be realized in a finished magnet from particulate of these high temperature MRE-Fe-B alloys, reduced temperature sintering with intrinsic or extrinsic constituents is being developed to promote full consolidation and to lock in the aligned particle assembly.

Non Rare Earth Containing Materials

While rare earth perment magnets display magnetic properties which are superior to non-rare earth containing magnets, there are several drawbacks to the use of rare earth permanent magnets. Of these, uncertain cost and long-term, broad availablity are the primary concerns for application in automotive traction motors. While rare earth elements are not actually rare in the earth's crust, the processing costs associated with mining, beneficiation, separation, and reduction of the rare earth oxide are high. As a result, while

the rare earth components of a RE-Fe-B magnet account for less than one third of its mass, the cost of the rare earths (especially Dy) represent a growing fraction (more than 2/3) of the total materials and processing cost of the magnet. Currently ~97% of the world's supply of rare earth oxides (REO) originate in China in spite of recent efforts to rapidly accelerate development of RE mining and refining in theUnited States and Australia. Recently Chineese companies have pursued agreements to acquire siginificant, if not controlling, interest in rare earth producers outside of China. At the same time China is restricting the export of REO materials by quotas and tarrif-like pricing. Moreover, a number of analysts have concluded that within a few years, the total Chinese production of REO will be internally consumed. This appears to be part of a long term plan to export only high end products moving from oxides to metals to magnets to motors. If this trend is allowed to continue without market resistance, the manufacturing of PM motors ouside of China will be severely diminished and an extreme (nearly) sole supplier dependence situation will become even worse. It is therefore necessary and strategic to seek to develop high performance permanet magnets that do not rely on rare earth elements and have sufficient magnetic strength for high torque drive motors.

The challenges associated with developing non-rare earth (non-RE) containing magnets can be demonstrated by a descriptive comparison of the demagnetization curves for the two currently viable non-RE magnets, alnico and ferrite, along with those of the two classes of rare earth magnets. As deficits of the non-RE magnet types, the remanent magnetization, especially of ferrites, and the coercivity, especially of alnico, are considerably lower than that of the RE magnets. While it is not necessary to equal the performance of RE magnets in non-RE magnets for advanced drive motors, it should be possible to significantly close the gap in magnetic performance while realizing a large gain in magnet material availability and, most importantly, to achieve a reduction in magnet cost and a gain in cost stability. However in order to accomplish this goal, it is unlikely that small improvments either to alnico or ferrites will be sufficient, but alnico does have much more promise due to extremely high intrinsic magnetization and a wide operating temperature range. In fact, the inherent absence of the low temperature operating range for ferrites, generally less than about 0°C, make them a non-starter for this program due to their transformation to an anti-ferrimagnetic phase that effectively eliminates their capability for magnetic anisotropy. On the other hand, the ability to develop major improvements to the coercivity of alnico seems much more within our grasp, if we can obtain sufficient understanding of the current coercivity mechnism(s) and can exploit these mechanisms to a far greater extent with innovative processing and creative alloy design.

New high performance permanent magnets without rare earth elements or reaching "beyond rare earth magnets" (BREM) will be a daunting challenge. Over the last century, while there has been a dramatic increase in permanent magnet performance that has always been achieved by serendipitous discovery of a new compound. Since the discovery of the $Nd_2Fe_{14}B$ compound was such a dramatic advance in properties, some continued effort has been

exerted in looking for new compounds with even higher energy product (and useful temperature range), but without equaling that success. What has been achieved is novel ways of combining materials into exchange-coupled composite "spring" magnet microstructures with a combined energy product that is greater than the initial monolithic hard magnetic phase. Recently, it has been shown that graded interfaces rather than discrete combinations of hard/soft compounds in these spring magnets have superior BH_{max}. The exchange lengths are dictated by the materials chemistry of the particular components.

After the discoveries of Sm-Co and RE-Fe-B, the research efforts in PM alloys using only transition metals had waned, especially. In the 40 years since the discovery of the first PM types with RE (Sm-Co), our ability to predict and experimentally explore materials properties has grown exponentially. Now, first principles calculations are easily accessible and are capable of being adapted to calculation of the electronic and thermodynamic properties of complex unit cells to uncover predictions of intrinsic magnetic properties, i.e., Curie temperature, magnetization and magnetic anisotropy. Techniques are now at the brink of calculating complex structures that are 10's of nanometers in size. Experimental techniques have also blossomed. Combinatorial methods, while limited to thin films, are becoming more useful for rapidly assessing large compositional phase space for stable and metastable structures and for some magnetic measurements. Our ability to characterize the magnetic properties has also increased substantially as has the sensitivity of new quantum interference devices. High brilliance synchrotron X-ray beams can be used to analyze hundreds of samples in a few hours with proper adaptation of multi-sample stages and data acquisition systems. Thus, PM researchers are in a much better position to cast a wider net more efficiently over a wider phase space in non-RE magnetic materials than ever before. In the absence of the large magneto-crystalline anisotropies provided by the rare earth elements, it will be necessary to utilize both magneto-crystalline and shape anisotropy in new magnet materials based on Fe and Co that have the highest saturation magnetization. It is possible that surface and exchange anisotropy may also contribute to the coercivity for properly engineered nano-composites in new non-RE permanent magnets. Actually, to achieve the degree of anisotropy enhancement needed may require novel ways of combining materials, where advances in chemical and metallurgical synthesis methods may hold the key to production of new nanocomposite bulk magnets.

Approach

This program consisted in FY2013 of two major thrust areas.

- **Advanced RE Magnet Thrust Area:** Focused investigation of _**RE anisotropic**_ permanent magnets, driven by industry needs, placing effort on novel processing of anisotropic sintered RE permanent magnets with extrinsic sintering additions, while attempting to

enhance the high temperature tolerance of mixed rare earth (MRE)-Fe-B alloys with a high Y:Dy ratio to minimize the use of Dy.

- Refined processing of anisotropic sintered permanent magnets of MRE-Fe-B alloys with little or no Dy content by single stage hot deformation (SSHD) to enable the maximum energy product to be realized in bulk magnets starting from Zn-coated amorphous flake particulate, using pressure-driven liquid phase densification/crystallization/sintering, and producing aligned nano-grained magnets.

- **BREM Thrust Area:** New high strength *non-RE anisotropic* permanent magnets will be developed that meet the requirements for advanced interior PM electric traction motors. The investigation will involve theory and modeling efforts, as well as experimental synthesis of magnet compounds and bulk prototype magnet fabrication and characterization. This task area is extremely high risk, but if successful it can revolutionize the cost structure of permanent magnet motors and reduce the reliance on foreign controlled commodities for hybrid and electric vehicle production.

- Near-term development of non-RE anisotropic permanent magnets is focused on attempts to improve the best of the non-RE systems, alnico, by using modern high-resolution characterization techniques to gain enhanced knowledge of coercivity mechanisms in existing alnico magnet types and, then, by developing innovative alloying and processing to improve coercivity and magnetic energy product using greater control of nano-structure and microstructure.

- Long-term development of new non-RE anisotropic permanent magnets also is pursued with significant input from theory and modeling, seeking to discover novel phases based on Fe-Co-X with beneficial intrinsic properties, i.e., high Curie temperature, magnetization and magnetic anisotropy.

- If the new non-RE permanent magnet phases have insufficient magnetic properties as single-phase magnets, increased properties will be sought by further extrinsic manipulation, including use of a soft magnetic second phase to produce enhanced exchange coupling.

Results

Of the non-rare-earth magnets, alnico shows the most potential for development based on its large magnetization. However, the coercivity of alnico is lower than that required for motor applications. If the coercivity can be doubled, the energy product of alnico will equal or exceed that of Nd-Fe-B magnets above 180 C. Alnico is a 3-D nano-composite consisting of magnetic Fe-Co elongated nano-particles with a transverse dimension of order 40 nm and a longitudinal to transverse ratio of at least 3:1. These particles are set in a nominally non-magnetic matrix with a matrix "span" distance of order 10 nm, dependent on the alnico type. The elongated shape of the particles provides anisotropy to the otherwise isotropic particles. The coercivity of alnico magnets is heavily dependent on the exact details of the microstructure and these

studies have included 3 of the most advanced types, 5-7 (aligned large-grained), 9 (aligned fine-grained, strongest), and 8 (unaligned fine-grained). The fine nm-scale of the alnico microstructures makes conventional methods of determining the exact composition of the constituent phases impossible. Using 3-D atom probe we have made the first accurate determination of the phase compositions for these important magnet materials. This has allowed us to study in detail the morphology and chemistry of the matrix phase, which play a critical role in determining the magnetic coupling between the elongated magnetic particles and hence a critical role in determining the magnetic properties and most importantly, the coercivity.
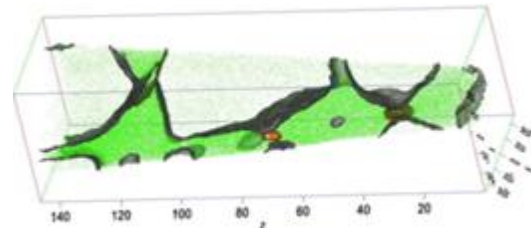
Figure IV-32: 3-D atom probe isoconcentration surfaces 30% Fe and 20% Cu (grey), and atom maps green dots Ti atoms, and orange dots Cu atoms) of alnico 9 showing the location of the Cu-enriched rods at the corners of the Fe-Co phase and the interconnection morphology of the microstructure.

For alnico 8 and 9, which have a significantly larger coercivity than 5-7, the matrix phase exhibits a $L2_1$ structure. Magnetic measurements of single-phase samples at the $L2_1$ compositions for alnico 8 and 9 exhibit large magnetic moments that saturate at high field, consistent with first principles modeling of spin alignment for the measured matrix composition. This implies that there is considerable magnetic coupling of the ferromagnetic Fe-Co nano-particles through the matrix. If it is possible to modify the magnetic properties of the $L2_1$ phase so as to decrease its magnetization as a function of field, the result should be significant increases in coercivity. We have tried two different approaches to modify the $L2_1$. One of these approaches resulted in a significant reduction in the magnetization of the phase while the other did not. Both modifications achieved a significant reduction in Co content that should result in significant cost reductions. Unfortunately, it is not sufficient to control the $L2_1$ phase independent of the overall composition. The modification that resulted in the improved magnetic properties of the $L2_1$ is incompatible with the metallurgical process that results in the formation of the 2 phase microstructure. However the other approach, while not improving magnetic properties, appears to be capable of at least equaling the performance of commercial grades of alnico at a significantly reduced cost.
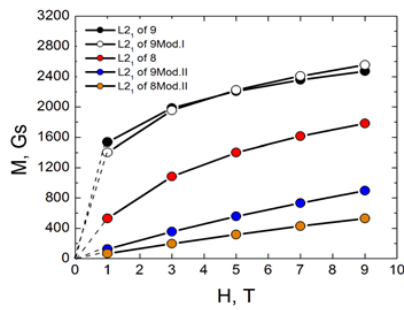
Figure IV-33: Magnetization curves of L2$_1$ matrix alloys in different external magnetic fields.

In addition to redesign of alnico alloys, innovative processing of bulk alnico magnets is in-progress with encouragement from Arnold Magnetic Technologies, our industrial collaborator, and its direction into powder processing is taken partially from results of SEM and MOKE (magneto-optic Kerr effect) analysis of alnico 9 that indicated how a portion of its higher coercivity (compared to 5-7) might be due to micron-scale features, associated with fine grain size. Also, SEM detection of a significant amount of grain boundary impurities in sintered alnico 8 (traditional powder blend processed, highest coercivity/low saturation magnetization) indicated that "cleaner" powder processing may improve its properties. Thus, experiments were conducted to test pre-alloyed powder processing of fine-grained alnico 8 using in-house capability for high-pressure gas atomized powder production with atomization parameters selected for maximum yield of fine spherical powder with high purity. The resulting powder (see Figure IV-35) had an average diameter of 30μm and a low content of satellite particles that promoted excellent flowability and powder packing (tap density). Other important indications of powder quality were a powder bulk oxygen content of only 420ppmw (for dia.<20μm sample) and an almost perfect correspondence (±0.1wt.%) between the nominal ("aim") composition and that of the resulting powder: 32.4Fe-38.1Co-12.9Ni-7.3Al-6.4Ti-3.0Cu (wt.%).
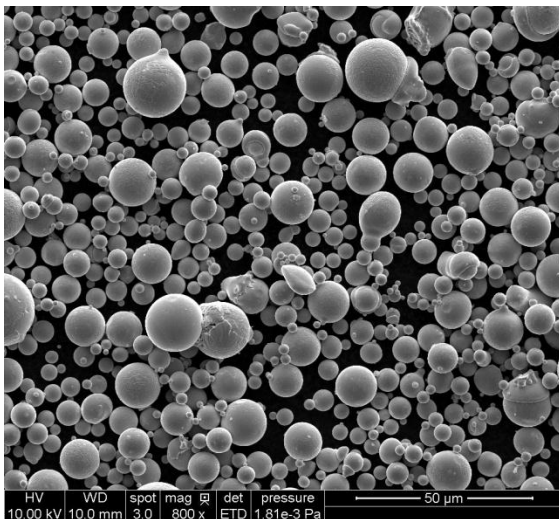
Figure IV-34: SEM micrograph of as-atomized pre-alloyed alnico 8 powder that was sieved to yield powders < 20μm.
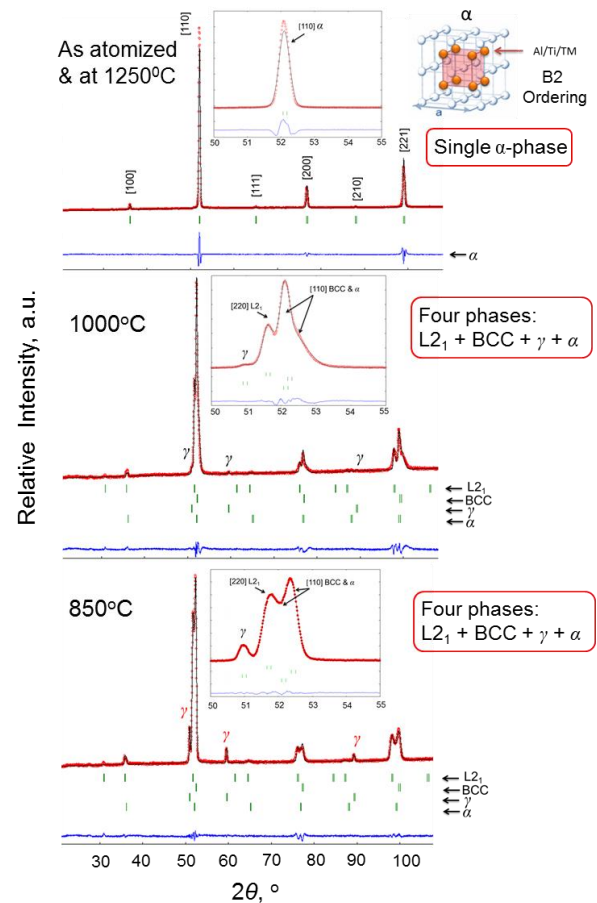
Figure IV-35: Summary of XRD results at high temperature for gas atomized (63-75μm) alnico 8 powder.

Typical cast alnico 8 alloys require annealing at 1250°C to solutionize the as-solidified microstructure into a homogeneous high temperature (B2) α-phase, prior to magnetic annealing and drawing. The normal formation of γ-phase on cooling of an alnico casting can degrade the magnetic properties of the alloy and γ is of primary interest to dissolve during solutionizing. Another objective of the 1250°C anneal is reversal of isotropic spinodal decomposition of α-phase that splits it to L2$_1$+BCC before it can be biased in the magnetic field. Previous reports estimated the γ-phase is confined to higher temperature phase fields, estimated to span about 830-1170°C, which is consistent with the initial results for annealing of the as-atomized powder at 850° and 1000°C for 30 minutes (see Figure IV-35). In other words, for the powder annealed at 850°, the XRD results show that both Υ-phase formed and the spinodal splitting of α-phase to L2$_1$+BCC occurred (Figure IV-35, bottom). For the 1000°C anneal (Figure IV-35, middle), the α-phase was more dominant than the spinodal product phases and the Υ-phase was nearly gone. However, the initial results also showed that due to the benefits of rapid solidification during gas atomization, the as-atomized powder exhibited the same high temperature α-phase, either before (as-atomized) or after solution annealing, as shown in Figure IV-35 (top). Thus, this bypassing of γ-phase formation and the α-phase spinodal

"splitting" in as-atomized pre-alloyed powder presents an intriguing possibility. Perhaps an expensive high temperature heat treatment can be avoided by developing a consolidation processing approach that maintains single-phase α until it can be decomposed in a magnetically biased spinodal reaction to produce an ideal nano-structure with elongated Fe-Co (BCC) phase within a non-magnetic (L2$_1$) matrix phase for enhanced magnetic properties.

To test the temperature tolerance for design of a low temperature consolidation process, as-atomized powder samples were encapsulated and exposed to annealing temperatures from 680-900°C for 45 minutes, before being quenched and characterized by X-ray diffraction. In an example of these new results from the low temperature annealed samples, it can be seen from the minor asymmetry (to lower 2θ) that starts to develop in the [110] peak of the α-phase at annealing temperatures as low as 680°C (Figure IV-36). Thus, it is difficult to tell from the present XRD data if this is peak distortion is caused by initial formation of γ-phase or by spinodal splitting. As the annealing temperature was raised in steps up to 900°C, this preliminary analysis indicated increasing and then decreasing amounts of both phase transformations, consistent with the previous overlapping XRD data. More detailed analysis of this XRD data and high-resolution microstructural observations are in-progress to resolve these questions about the relative progress of both types of reactions to enable our choice of powder consolidation temperatures and types of processes.
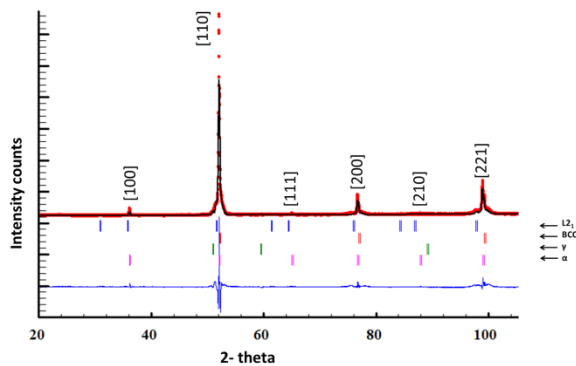
Figure IV-36: XRD pattern obtained from as-atomized alnico pre-alloyed powders, heat-treated at 680°C for 45 minutes.

The initial results from one type of low temperature powder consolidation experiment also can be reported at this time that used spark plasma sintering (SPS) of as-atomized powder (63-75μm) at 770-790°C and 60MPa for 10 minutes. This experiment tried to take advantage of accelerated inter-particle bonding that is promoted by enhanced Joule heating of powder particle contact points, while limiting the time for diffusion and phase transformation. Although full density was not achieved (as expected from this coarse powder with a narrow size range), a compact that could be handled was produced with a density of about 91.5% of theoretical, as seen in the SEM micrograph of Figure IV-37a. Consistent with the indications from our low temperature XRD results, γ-phase formation was detected at inter-cellular and grain boundary

regions of the powder particle interiors (seen most clearly in Figure IV-37b).
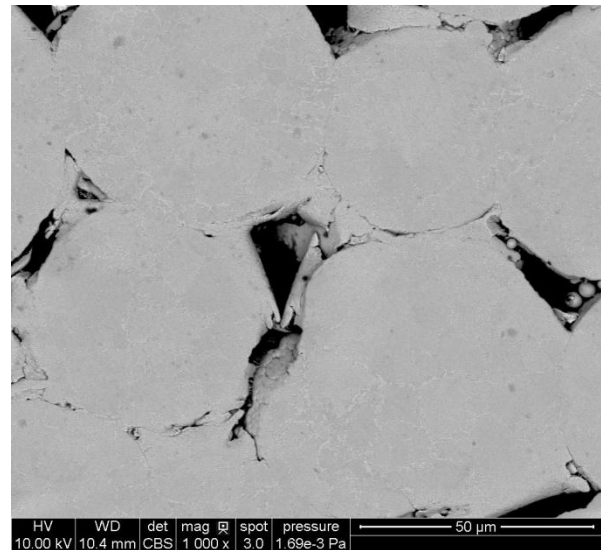
a)
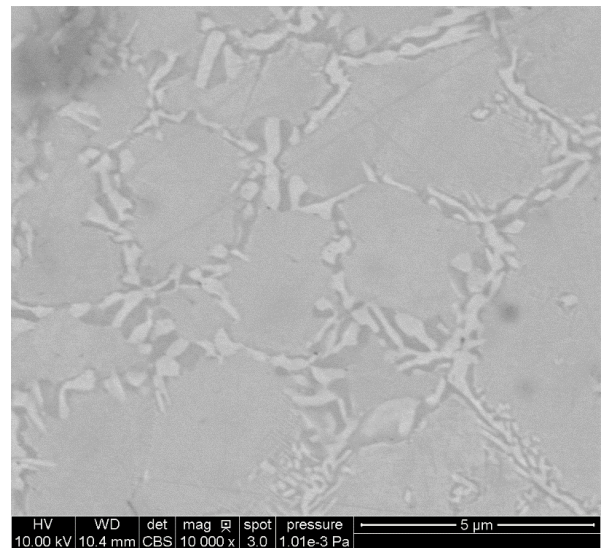
b)

Figure IV-37: SEM of powder particle interior showing cell boundaries decorated by γ-phase.

Obvious in Figure IV-37b is the light/dark contrast of the γ-phase regions, which indicates some further decomposition of γ-phase, but this is not understood at this time. Unfortunately, insufficient formation of sintered neck regions also was observed at the inter-particle boundaries (Figure IV-37a), which lead to brittle mechanical properties of the post-SPS sample. Structural characterization by XRD and detailed microstructural analysis by TEM are in-progress. Based on these results, an extensive series of alternative bulk magnet consolidation experiments also are underway, including SPS at lower temperatures/higher pressures and vacuum hot pressing at similar temperatures/higher pressures.

The Ames project has three closely related tasks for discovery and development of new non-rare earth permanent

magnets. These projects are a cross-disciplinary collaboration involving theorists using first principle calculations and other advanced computational tools to unravel the underlying atomistic to microstructural interactions which give rise to high energy density magnets, materials scientists using advance synthesis tools to investigate and produce new compounds and advanced characterization techniques to unravel the details of these complex compounds and their crystal structures. Information from one group naturally leads to furthering of the whole project through close-working teams.

In the area of permanent magnet material discovery, we are using combinatorial techniques to look for specific compounds within ternary phase space that are rich in Fe, Co and 3d, 4d, or 5d elements that have been previously identified by the theoretical group as promising new compounds. Since many of these complex intermetallics have ranges of stoichiometry, the combinatorial method provides a fast screening tool for discovery of these compounds. Once synthesized, these thin film "libraries" need to be rapidly scanned for promising compounds, as illustrated in Figure IV-38. Here we are using scanning magneto-optical Kerr effect and synchrotron X-ray scattering to indentify and characterize these compounds. Once characterized, the potential of these compounds as a new magnet can be further investigated using advanced computational tools (as shown in Table IV-6) and bulk magnet processing techniques.
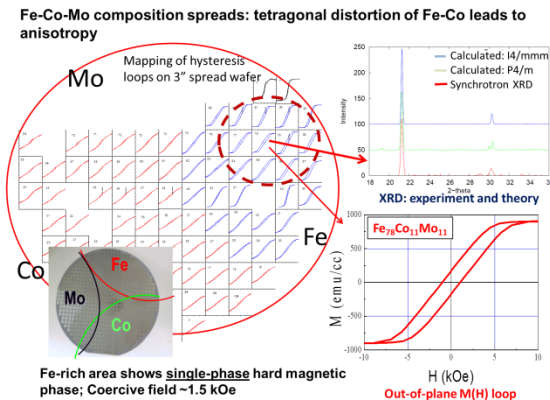
Figure IV-38: An example of the combinatorial process where we have shown that within a limited region of the ternary phase space of Fe-Co-Mo there is a composition near Fe$_{78}$Co$_{11}$Mo$_{11}$ with promising coercivity.

Table IV-6: Prediction of tetragonal Fe-Co-Mo of P4/m crystal structure type for the magnetically promising compound featured in Figure IV-38.

Lattice (Å)	Atom	x	y	z	M(μ_B)
a = 6.4295 c = 2.8840	Fe (4j)	0.68971	0.10091	0.00000	2.11
	Fe (4k)	0.20417	0.60188	0.50000	2.55
	Co (1c)	0.50000	0.50000	0.00000	1.67
	Mo (1b)	0.00000	0.00000	0.50000	-0.61

Conclusions and Future Directions

In our work within the Advanced RE Magnet Thrust Area, the single stage hot deformation (SSHD) method to fabricate fully dense anisotropic magnets from Zn-coated glassy MRE$_2$(Fe,Co)$_{14}$B flake appears promising as a manufacturing process for near-net shape fully dense sintered magnets with reduced Dy content. While successful as a relatively simple approach to generate aligned nano-metric grains, a major issue that needs additional work is the temperature tolerance, especially for extremely low Dy alloys. If sufficient funding was available, this approach would be developed further for high temperatures with additional alloy additions and other components added to the evaporated surface layer, particularly if industry demand was sufficient to continue this RE magnet work. However, a clear processing cost and performance advantage would need to be demonstrated to add assurance that industrial adoption can succeed. Also, a major barrier for substitution of a new RE magnet concept into traction drive motors depends on easing of demand growth for RE materials and/or stabilization of the market for RE supplies in the foreseeable future.

Since it is unlikely that the RE market uncertainty will be eliminated, a great sense of urgency drives our work in the BREM Thrust Area. On that pathway, we believe that the best near-term non-RE permanent magnet option is a modified version of today's alnico, based on the Al-Ni-Co-Fe system, where the magnetic properties need to be raised to the minimum level needed for advanced drive motor designs. Key questions remain to be addressed in further optimization of this class of alloys: To what extent has the spinodal decomposition been optimized? More specifically, how does the dimension, uniformity of shape and degree of chemical segregation affect H$_{ci}$? For example, doubling of the H$_{ci}$ of cast alnico 9 from 1500 to 3000 Oe while maintaining B$_r$ would result in an increase in (BH)$_{max}$ from 9 to ~18 MGOe, but would still require special directional solidification methods with limited up-scaling potential. Alternatively, if we synthesized alnico 8 by a powder processing method that could double the current 2000 Oe to 4000 Oe, while boosting the B$_r$ to the level of the cast versions, it might be possible to achieve 20 MGOe with a high production volume magnet processing approach. Determining how to achieve these advances in coercivity without a better understanding of the fundamental mechanisms (at the nano-scale and the micron scale) for suppressing reverse domain nucleation and enhancing domain wall pinning in these compounds would be difficult at best, which drives us to further alloying, processing, and characterization studies, along with continuing to use guidance from theory and simulation efforts.

For FY2014 alnico studies, in-depth analysis of annealing (with and without magnetic field) and calorimetric investigations (with constant external magnetic field) will be followed by detailed SEM and XRD studies (including in situ studies) of gas-atomized powders to determine the volume fraction and microstructural distribution of the possible phases, along with accurate transition temperatures. Based on understanding of the phases that are produced at different

temperatures, the magnet consolidation processing temperature and method can be developed in which we can avoid the formation of unwanted γ-phase, while promoting the phase separation reaction and maintaining a fine nanometric scale to enhance coercivity.

For long-term pursuit of alternative non-RE permanent magnet materials, we believe that the increasingly targeted efforts and initial results of our Theory Group add significant value to our team for this discovery process. A prime example of this growing value is revealed by the strong interaction of the experimental synthesis studies (at Maryland and Nebraska) and the structural characterization efforts (at Ames, Maryland, and Nebraska) with the theoretical investigations using both genetic algorithm and DFT tools (at Ames and ORNL) to approach specification of a promising metastable magnetic phase, Zr_2Co_{11}, that can be further alloyed with Fe, Mo, Si, B, and other elements. These complex alloying studies and the studies on alnico alloying (in near-term BREM work) will be facilitated greatly by the expanded supercomputer access afforded by our very recent INCITE award and by new experimental work that works in concert with the new theory findings. Certainly, our exploratory combinatorial synthesis work on such Fe-Co-X systems, where X=5d and 4d (e.g., W, Ta, Mo, Zr) and other dopants (e.g., Si, N, C) has also demonstrated its worth in providing a rapid survey tool that is useful for both theory and experiment. The recent upgrade of high rate structural and magnetic analysis capabilities have made this even more valuable. The alloy specific experimental synthesis capabilities of cluster deposition have provided new results that show potential for producing aligned nano-metric enhanced exchange coupled magnet samples, where it is likely that the cluster deposition method can reach far into the metastable phase region for these new PM compounds.

FY 2013 Publications/Presentations/Awards

1. Ames Lab proposal (Harmon, Ho, Wang) elected by the DOE (20 October 2012) to receive a 2013 Innovative and Novel Computational Impact on Theory and Experiment (INCITE) award.

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IV.4. Alternative High-Performance Motors with Non-Rare Earth Materials

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Start Date: Septemeber 2011
Projected End Date: January 2016

Objectives

- Design, build and test advanced traction mtoros that reduce or eliminate the use of rare-earth materials while meeting the DoE 2020 specifications
- Develop advanced materials to open up the design space for the new motors

Technical Barriers

- The specifications for hybrid vehicle motors are challenging in terms of power density, efficiency and cost. This requires a comprehensive approach to advance the state of the art, including novel concepts to push past barriers.
- High speed is key to high power density
- High speed leads to higher electrical frequency
- Higher stator core and rotor losses
- On top of all these challenges, eliminating rare-earth permanent magnets makes the problem an order of magnitude more challenging
- Scaling up materials processing to level needed for motor insertion

Technical Targets

The goal of the project is to develop traction motors that reduce or eliminate the use of rare-earth materials and meet the DoE specifications summarized in Table IV-7 and Figure IV-39.

Table IV-7: Motor Specifications.

Items	Specification
Max. Speed	14,000rpm
Peak Power	55kW @ 20% speed for 18sec
Maximum Current	400Arms
Cont. Power	30kW @ 20~100% speed @ Vdc=325
Efficiency	Refer to target efficiency map
Operating Voltage	200~450V (325V nominal)
Back EMF	<600Vpk line-to-line @ 100% speed
Torque Pulsation	<5% of Peak Torque @ any speed
Characteristic Current	< Maximum Current
Weight	≤35kg
Volume	≤9.7L
Cost @100k	≤$275
Ambient (outside housing) Operating Temperature	-40~140°C
Coolant inlet	105°C, <10LPM, 2psi drop, <20psi inlet
Minimum isolation impedance-phase terminal to GND	1Mohm
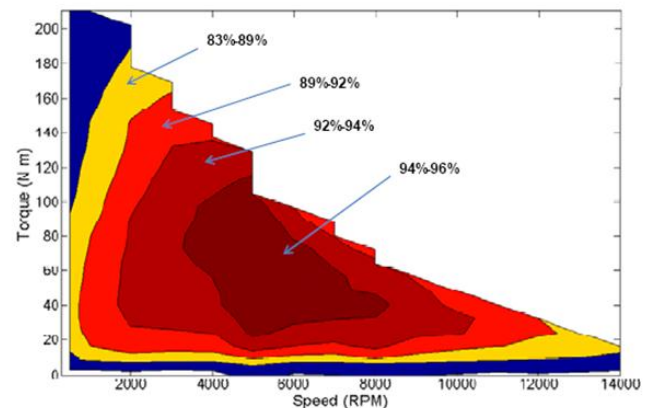
Figure IV-39: Motor Required Efficiency Map.

Accomplishments

(A) Motor accomplishments:

- Finalized the motor topologies that will be evaluated and done evaluating 9 of them
- Preliminary down-selection of 3 topologies that will be built and tested:
  - 1 has reduced rare-earth content; 1 has non-rare earth magnets; 1 has no magnets
- Identified the theoretical properties for the advanced materials to be developed and quantified their impact on some of the motor topologies

- First prototype is built and expected to be tested by end of 2013
- Second prototype is under construction and build is expected to conclude by end of 2013

(B) Materials accomplishments:

- Applied advanced manufacturing methods to non-rare earth permanent magnet materials and quantified processing factor dependence of key magnetic properties
- Completed first microstructural investigation GE-synthesized non-rare-earth Permanent magnets at Ames Laboratory
- Demonstrated higher tensile strength soft magnetic laminates with magnetic properties approaching those of Si-Steel
- Demonstrated stability of high temperature insulation materials at temperatures > 250°C
- Performed initial studies on scalability of new materials for sub-scale prototype motor builds

✧   ✧   ✧   ✧   ✧

Introduction

Electric drive systems, which include electric machines and power electronics, are a key enabling technology for advanced vehicle propulsion systems that reduce the petroleum dependence of the transportation sector. To have significant effect, electric drive technologies must be economical in terms of cost, weight, and size while meeting performance and reliability expectations.

The objective of the GE Global Research "Alternative High-Performance Motors with Non-Rare Earth Materials" program is to develop a higher power density traction motors at a lower cost while simultaneously eliminating or reducing the need for rare-earth materials. Successful completion of this program will accelerate the introduction of hybrid electric vehicles into the U.S. road vehicle fleet and bring the added benefits of reduced fuel consumption and environmental impacts.

(A) Motor Development

- Develop advanced motor concepts including electromagnetic, mechanical, and thermal concepts
- Build proof-of-principle machines to verify the design process as well retire the key risks
- Design and build 55 kW/30 kW machines that meet the DoE specifications
- Develop cost model to estimate the advanced motors cost based on 100,000 units/year
- Investigate the scalability of the developed concepts by evaluating 120 kW/65 kW machines

(B) Materials Development

The objective of the materials development tasks is to develop non-rare-earth containing component materials that enable non rare-earth containing motor designs that meet project performance goals. In the first phase of research, the

capability for improvement of four classes of materials are is being studied:

- Improving the coercivity of an existing non-rare-containing permanent magnet composition to enable operation at temperatures above 150°C
- Improving the tensile strength of electrical steel to enable high speed motor operation with low iron loss
- Improving the ability of motor laminates to control magnetic flux distribution
- Improving the ability of dielectrics to withstand operating temperatures in excess of 280°C

Approach

(A) Project uniqueness:

- The project proposes a very comprehensive approach in terms of identifying the technologies that will meet the required performance
- The project will explore various motor topologies; some include no magnets at all and some include non-rare earth magnets
- Some of the motor topologies use only conventional materials while others will be enabled by advanced materials that will be developed under the project
- Advanced materials including magnetic as well as electrical insulating materials will be developed to enable the motors to meet the required set of specifications
- Advanced motor controls and thermal management techniques will also be developed
- By evaluating the wide range of motor topologies and advanced materials, down-selected topologies/materials are expected to meet the required set of specifications

(B) Approach:

Motor Development:

- Perform tradeoff study of various motor topologies
- Identify promising scalable materials and produce coupons showing the expected properties
- Down-select promising topologies/materials
- Design/build/test 2-3 proof-of-principle motors
- Down-select final motor topology
- Design/build/test 3 identical motors as the key project deliverable(s)
- Develop cost model for the final motor

Materials Development:

The materials development approach for Phase I of the project is to develop the structure/ processing/properties relationships of four categories of motor components being made with novel materials. The Phase I materials tasks will produce and characterize samples of the new materials and will culminate in the selection of materials for scaled-up production in subsequent Phases.

- The microstructure of the non-rare-earth containing permanent magnet alloy is being refined through the application of modern casting and annealing technology. A series of designed experiments is being conducted to probe the capability of these technologies to increase

coercivity while maintaining energy product. Magnet post-processing and characterization is being performed at Arnold Magnetic Technologies. Atom-scale structural characterization is being performed in collaboration with Ames laboratory to produce in-depth structure/processing/properties relationships.

- A novel processing route is being applied to conventional silicon steel alloys to improve the tensile strength by while retaining comparable power loss. The approach relies on understanding and controlling the trade-off between coercivity (and hence power loss) and tensile strength. The processing technology is being developed to form the new material into sheets suitable for motor laminates.

- Novel processing technology is being developed to enable improved control of magnetic flux contained within motor laminates. This approach requires the development of new alloys that are operable with this processing method and the demonstration of scalable processing at dimensions specified by the motors teams.

- High temperature dielectrics are being developed that maintain high dielectric strength with resistance to degradation by oxidation. This requires the selection of suitable materials components, production of sample films, and verification of electrical and mechanical properties as a function of time at temperature.

Results

(A) Motor Development:

Several motor topologies have been evaluated. Most of them completely eliminate rare-earth materials while few eliminate the most critical rare-earth materials. The figures below show comparison between the various options vs. the baseline rare-earth IPM motor. "NRE" indicates complete elimination of rare-earth materials either by using non-rare earth magnets or not using magnets at all."RRE" indicates reduced rare-earth content. Some options are showing promising performance in terms of power density and/or efficiency. Two options have been downselected to build proof-of-concept machines. The first prototype has reduced rare-earth content. The stator and rotor of this prototype are shown in Figure IV-44 and Figure IV-45. The machine build is finalized and testing is expected to be completed by end of 2013. The second prototype has non-rare earth magnets and the build is expected to be completed by end of 2013 while the testing will take place in 2014. There are still few options under evaluation to choose the third proof-of-concept option that will have no magnets. The design, build, and testing of the third prototype will take place in 2014.
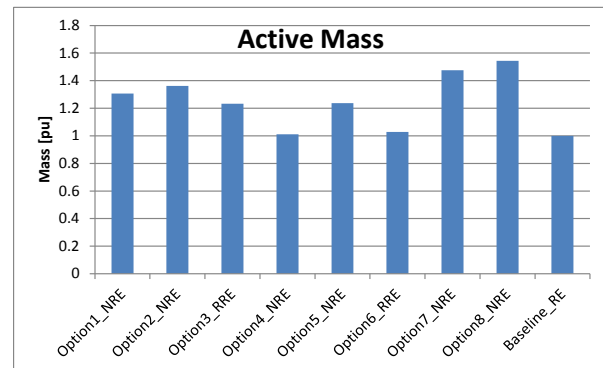
Figure IV-40: Comparison of motor topologies in terms of active mass.
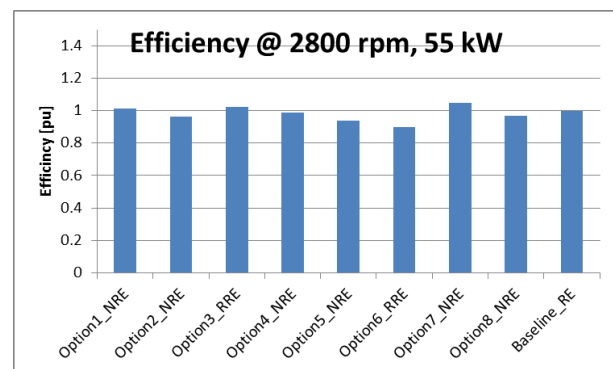
Figure IV-41: Comparison of motor topologies in terms efficiency @ 2800 rpm and 55 kW.
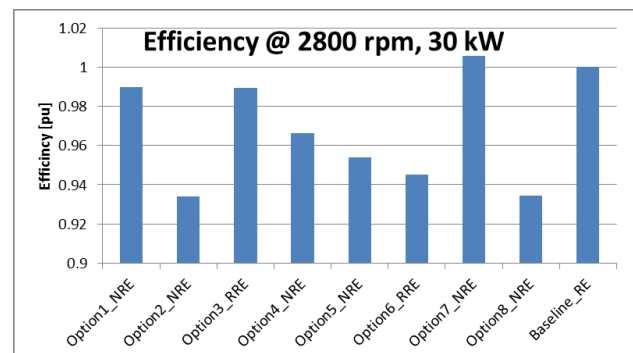
Figure IV-42: Comparison of motor topologies in terms of efficiency @ 2800 rpm and 30 kW.
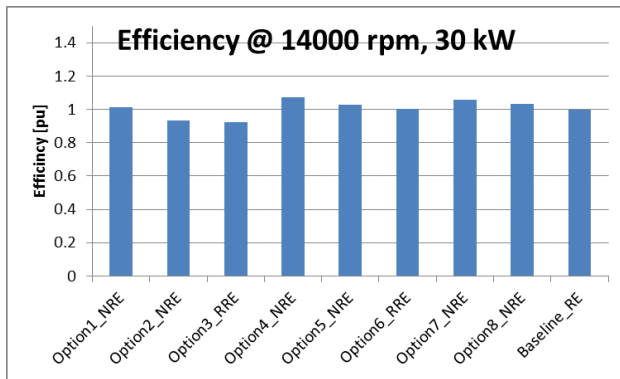
Figure IV-43: Comparison of motor topologies in terms of efficiency @ 14000 rpm and 55 kW.

Figure IV-44: Stator of first prototype.

Figure IV-45: Rotor of first prototype.

(B) Materials Development:

a. Non-rare earth containing permanent magnets

The advanced manufacturing method explored during this project has been found to have the most effective in controlling the remanence of the non-rare-earth magnet material. A variation in composition is being explored to increase the coercivity of the material while achieving the highest possible remanence enabled by the new manufacturing method. Table IV-8 and Figure IV-46 show that our best performing material made at the time of this report would nearly match the energy product of Alnico 9 with 25% higher intrinsic coercivity. Further experiments are underway to fully map the limits of coercivity and energy product enabled by this new manufacturing method.

Table IV-8: Comparison of magnet properties of commercial non-rare-earth permanent magnets with best performing sample produced by GE to date.

Composition	Hci (kOe)	Br (kG)	(BH)$_{max}$ (MGOe)
Alnico5DG	0.73	1.3	6.5
Alnico8H	2.2	7.2	5.0
Alnico9	1.53	10.8	10.0
Best GE to date	**2.1**	**9.5**	**9.8**
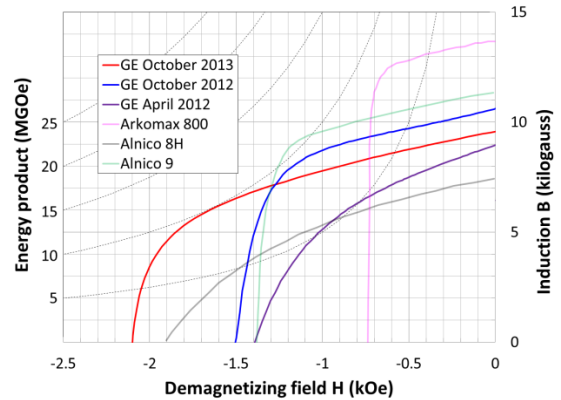
Figure IV-46: Improvement in magnetic properties for non-rare-earth permanent magnets cast via GE's advanced manufacturing method. Semi-transparent lines are commercially available Alnico type permanent magnets included for comparison.

b. High strength soft magnetic laminates

A single processing stream for producing high strength soft magnetic laminates has been developed. Efforts this year focused on quantifying the trade-offs between power loss and tensile strength in this material. A significant contribution to core loss was discovered to be oxide inclusions and porosity introduced into the microstructure during the manufacturing process. A modification to the process was found that avoided the introduction of these defects. Figure IV-47 shows the reduction in defects in the microstructure of samples produced before and after the process modifcation. The power loss and magnetic properties of these materials was still being determined at the time of this report.

Figure IV-48: Optical micrograph through the cross-section of lamination that has been processed to contain magnetic and non-magnetic regions. The interface between two regions is shown.

d. High temperature dielectrics

Two high heat resistant polymeric films identified last year have been further analyzed on their manufacturability. Most importantly, their compatibilities with other electrical insulation components in the motor such as varnish have been investigated. The mechanical properties of these films after thermal aging are tested in comparison of control samples; they show much slower thermal oxidative degradation, which is evidenced by minimal weight loss and high tensile strength retention after thermal aging at 320°C and 350°C as seen in Figure IV-49 and Figure IV-50. Those HT films were also subjected to 300°C thermal aging, there is slight change in tensile strength after more than 1000 hours continuous exposure in air at 300°C as shown in Figure IV-51.

Figure IV-47: Typical microstructures of high strength laminates (a) before and (b) after the process modification.

c. Improved magnetic flux control

One of two manufacturing methods was down-selected for further study. An alloy composition designed to be compatible with that microstructure was developed. The manufacturing method was determined to be capable of controlling magnetic properties in laminates as thick as 14 mils. The transition region between a locally magnetic and non-magnetic region was determined to be as small as four mils. Aging tests at 180°C showed this region to be stable for at least 2500 hours. Figure IV-48 shows a cross section of laminate that has been processed to have locally magnetic and non-magnetic regions. A full comparison between the magnetic and non-magnetic regions is underway at the time of this report and longer term-stability tests continue.

Figure IV-49: Retaining weight of high temperature films after aging in air at 320°C.
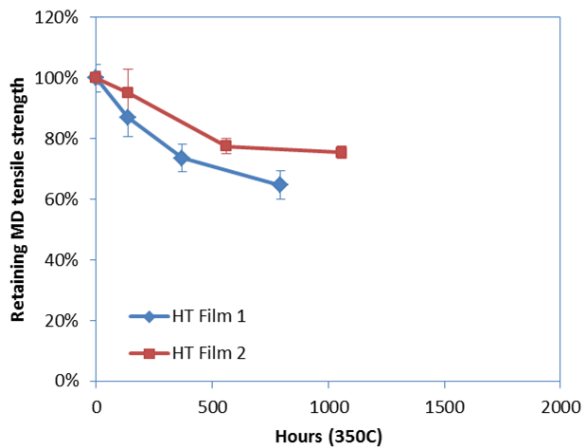
Figure IV-50: Retaining Mechanical Strength for high temperature films after aging in air at 350°C.
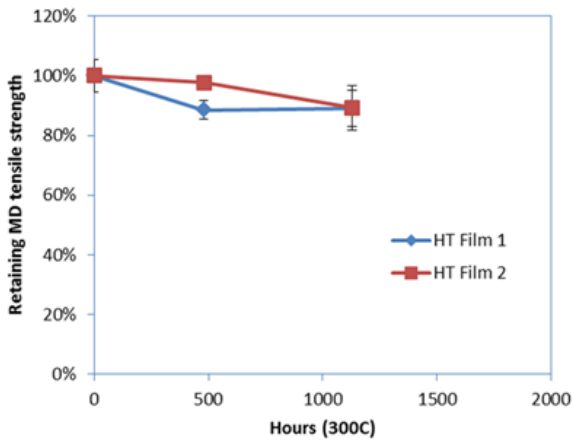
Figure IV-51: Retaining Mechanical Strength for high temperature films after aging in air at 300°C.

Since the HT films are developed for the slot liner in motor, the adhesion of varnish to the slot liner is critical to overall insulation quality. A pull-out test is devised to gauge the compatibility of HT films and high temperature varnish as shown in Figure IV-52. Pull force was measured until the film break as shown in Figure IV-53 and Figure IV-54. The adhesion of the HT film to the varnish proved to be very good.
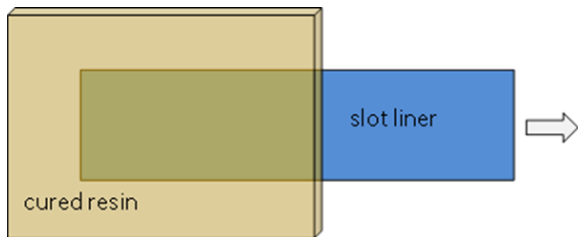
Figure IV-52: Pull-out adhesion test for slot liner to varnish.
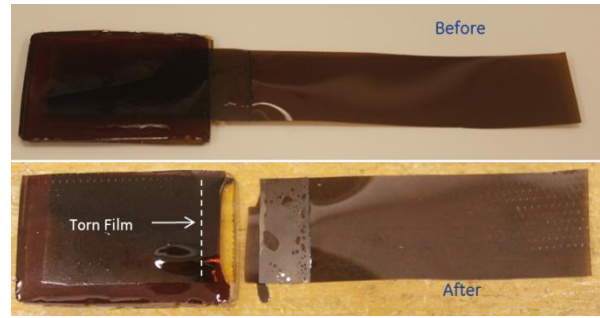
Figure IV-53: Pictures of samples before and after pull test.
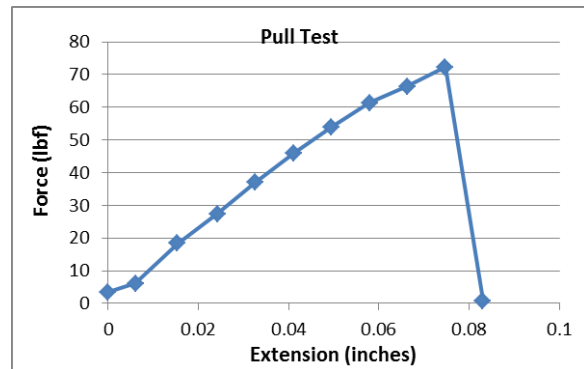
Figure IV-54: Pull force curve during pull test.

To retire the risk of using HT film as a slot liner in motor, statorettes were built with windings inserted in the slot with an HT film slot liner in place. A control statorette using Nomex as slot liner was also built for comparison, as shown in Figure IV-55 and Figure IV-56. Dielectric performances were measured after stator assembly and after thermal aging. The HT film has shown no sign of any degradation after thermal aging at 280°C for more than 2000 hours while stator with Nomex slot liner failed hipot test after 200 hours after 280°C thermal aging.
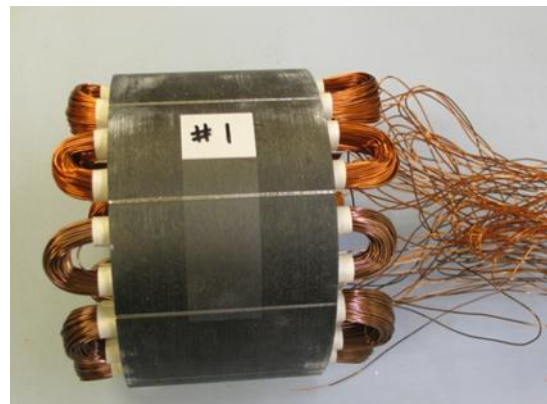
Figure IV-55: Statorette constructed with baseline Nomex as slot liner.

Figure IV-56: Statorette constructed with the HT film developed on this project as slot liner.

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Conclusions and Future Directions

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Conclusions

There is significant progress made in terms of evaluating the various motor topologies. Some of them show promising performance both in terms of power density and/or efficiency compared to rare-earth IPM motors. Two prototypes are under development. The first is already built and will be tested by end of 2013. The second will be built by end of 2013 and will be tested in 2014.

Also significant progress made in terms of developing the advanced materials. Coupons have been produced and tested and some are showing promising results.

Significant progress has been made in developing advanced magnetic and dielectric materials for use as motor

components. Structure/processing/properties relationships have been determined. Initial test coupons have been produced and characterized. All materials components have met their property milestones and work on all will continue into FY2013. In 2014 one or more of the material systems will be chosen for scaled-up processing to support a prototype motor build.

Future Direction

FY14

- Finish test proof-of-principle motors/materials
- Final selection of motor topology/materials based on test results of proof-of-principle motors
- Initiate design for final motor (s)

FY15

- Scaled manufacturing of selected materials
- Final motor build and test

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FY 2013 Publications/Presentations

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1. Presentation at the 2013 AMR, May 2013.
2. 12 disclosure to date many of which already filed as patent applications.
3. US08115434"High-Speed Self-Cascaded Electric Machine," Feb. 14, 2012.
4. US8,222,855B2"System and method for non-sinusoidal current waveform excitation of electrical machines", July 17, 2012.
5. US8274190,"Electric machine rotor bar and method of making same," September 25, 2012.

IV.5. Unique Lanthanide-Free Motor Construction

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Subcontractor: N/A

Start Date: October, 1, 2011
Projected End Date: October 31, 2015

Objectives

- This project pursues new motor construction that eliminates, or significantly reduces, the use of rare earth elements while maintaining the attractive size, weight and efficiency features of rare earth permanent magnet motors
- The primary drivers for this work include:
  - Lack of transparency in the rare earth magnet supply market and its pricing structures
  - Significant rare earth price escalation in calendar year 2011
  - Need for small, lightweight, high efficiency, low cost motors for electric traction drives
  - New architectures and/or materials that eliminate rare earth materials while maintaining performance that is attractive for electrified vehicles

Technical Barriers

The low coercivity of the AlNiCo magnets requires an unconventional rotor design for power density. This unconventional rotor design requires an innovative magnet retention system for high speed operation. The proof-of-concept (POC) rotor involves the use of retention bars, adhesive and fiber wrap to accomplish the retention.

A second item of concern is also related to the AlNiCo magnets and their characteristic of of de-magnetizing if not magnetically coupled with a conductive outer sleeve. This sleeve must be used anytime the rotor is not fully inserted in the stator. UQM has worked with the company that will be magnetizing the rotor to insure a sleeve can be designed to maintain the magnets.

Technical Targets

- The DOE motor specifications that are targeted for this work include:
  - 55 kW baseline design
  - Scalable to 120 kW or higher

Accomplishments

- Completed the full all analysis and design of the POC motor, including:
  - Final magnet select
  - Electromagnetic design, rotor geometry and magnet shape
  - 3D structural stress analysis of the magnet retention system
  - All other components of the POC motor
- Completed design of tooling and fixtures
  - Magnetizing fixture
  - De-magnetizing prevention sleeve
  - Assembly tooling and fixtures
- Procurement of hardware to construct two (2) full POC motors (1 for delivery in operational condition, 1 spare for risk reduction)
  - Numerous components have been received and inspected

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Introduction

Project Objective

This project pursues the development of a non-rare-earth permanent magnet motor architecture. It incorporates a novel rotor geometry that allows the use of lower energy Al-Ni-Co, Fe-Co-W, or other high flux, low coercivity magnet material. These materials are not currently adopted due to demagnetization within existing magnetic circuit designs, a problem that is overcome with this proposed design.

Project Description

Three unique design features of this motor architecture are proposed to enable the use of low coercivity magnet technology: magnet shape along with magnetization direction, a nonmagnetic support structure, and design features that reduce demagnetization fields. The project relies upon incremental improvement in the non-rare-earth magnet properties (collaboration with Ames Laboratory) and this is where the project starts. From there, UQM develops a motor design and integrates thermal technology in collaboration with the National Renewable Energy Laboratory. Finally, motors are built in years two and three (initial proof-of-concept motor followed by refined hardware). These will be tested at UQM and delivered to Oak Ridge National Laboratory for

independent confirmatory testing. The project concludes with designs scaled to higher power and detailed cost estimating activities. Cost is key to the adoption of electrified vehicles, so substantial focus is placed on the tasks related to the detailed costing of the technology.

Project Impact: Benefits and Outcomes

The outcome of the technology development and the resultant scalable hardware will be motor designs that apply to a full range of vehicle electrification, from mild hybrid to heavy hybrid to fully electric vehicles. This unique permanent magnet motor technology has an efficiency advantage over wound-field or induction machines (no energy consumed to create the magnetic field), and therefore, will decrease petroleum consumption relative to other non-rare-earth motor technologies. Economically, the magnet material used for this program is one-third the cost of NdFeB magnets on a per-pound basis, and therefore, supports lower cost if the material content can be maintained to be less than three times the amount of NdFeB for a given power level. UQM is confident that the total magnet cost of the proposed technology will be lower than the equivalent rare-earth motor. This will provide economic benefit to the end-use consumers (lower vehicle cost) and improve electrified transportation industry with products that compete more favorably with traditional petroleum engine driven vehicles.

Approach

- Pursue design that enables the use of low coercivity magnets
  - Unique magnet and supporting rotor geometry
  - Stator and rotor design features that reduce demagnetization fields
- Collaborate with FFRDC partners
  - Ames Laboratory for incremental improvements in high flux, low coercivity magnet materials
  - National Renewable Energy Laboratory for thermal management
  - Oak Ridge National Laboratory for testing
- Period 1 (10/2011 thru 4/2013) focused on the design of the electromagnetic circuit that will meet the DOE targets and be capable of manufacturing
  - UQM's focus was the electromagnetic design with existing AlNiCo technology
  - Ames Laboratory is pursuing increased performance of the AlNiCo material
  - NREL will provide assistance in the thermal management of the motor design
  - ORNL will provide testing of the motor
- Period 2: Build proof-of-concept motor and test with standard three-phase inverter
  - Test at UQM to confirm performance
  - Test at ORNL to validate results
- Period 3: Build and test proof-of-design motor
- Bill of materials with costs and higher power design at program completion

Results

N/A

Conclusions and Future Directions

Based on the analysis completed in the reporting period it was determined that the POC motor can be constructed and will demonstrate compliance with the DOE targets set at the onset of the program, including:

	Requirement	Value	Status
DOE Requirements	Efficiency	>90%	Analyzed, Comply
	Peak Power	55 kW	55 kW
	Maximum Speed	10,000 rpm	Analyzed, Comply
	Operating Voltage Range	200-450 VDC 325 VDC Nominal	Analyzed, Comply [1]
	Maximum phase current	400 A	Analyzed, small amount of demagnetization
	Torque	262 N-m	Analyzed, small amount of demagnetization
	Total Volume	≤ 9.7 L	9.59 L, based on preliminary design
UQM Internal Requirements	Max Stator Diameter	10 inches	Analyzed, Comply
	Magnet Weight Limit (For Cost)	4.5 kg	4.5 kg
	EMF THD	< 10%	2.86%
	EMF Harmonics	< 5% of Fundamental	2.27%
	Cogging Torque	< 4 N-m	3.85 N-m

The POC motors will be constructed in FY14 and tested to confirm compliance with the above list specifications. Upon completion of in-housing testing a motor will be delivered to ORNL for indepent testing and validation of performance.

Based on the POD analysis, design and testing a proof-of-concept (POC) design will be developed, constructed and tested.

FY 2013 Publications/Presentations

DOE Vehicle Technologies Office FY14 Kickoff Meeting (11/4-6/2013)

V.0 Thermal Management R&D

V.1. Advanced Liquid Cooling Research and Development

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Start Date: October, 2010
Projected End Date: December, 2013

Objectives

The goal of the project is to design, fabricate, and experimentally demonstrate a light-weight, low-cost, high-thermal-performance, single-phase, water-ethylene glycol (WEG) liquid-cooled heat exchanger. This demonstration is being done within the framework of a commercial inverter from UQM Technologies Inc. The bulk of the heat exchanger is made of plastic material because the cooling is provided by the jets impinging directly on the back side of the power module base plates. Micro-structured surfaces fabricated on the copper base plates will be employed as a simple, passive means of enhancing heat transfer. This cooling approach of impinging jets on the base plate is compared to the baseline channel flow cooling approach typical of automotive heat exchangers.

The objectives for FY2013 were:

- Comprehensive computational fluid dynamics (CFD) analyses will be performed to further optimize and improve heat transfer, reduce pressure drop, and design the second version of the light-weight heat exchanger. Additionally, the use of the MicroCool-enhanced surfaces will be incorporated into the new design to further improve thermal performance. The new, improved designs will be fabricate and their performance will be characterized.
- Additional experiments are initiated planned to evaluate the long-term reliability of enhanced surfaces and ceramic substrates (direct-bond copper [DBC] and direct-bond

aluminum [DBA]) subjected to WEG jets. Unlike the prior tests, these experiments will utilize automotive grade coolant (i.e., WEG with corrosion inhibitors) at coolant temperatures used in automotive power electronics applications (70°C). To minimize/eliminate oxidation and corrosion, the enhanced surfaces will be nickel plated. The effect of the impinging jets on the thermal performance of the enhanced surface and the integrity of the ceramic substrate will be evaluated over a one-year period.

Technical Barriers

Since it is a new technology or application for automotive power electronics, acceptance relies on proof of reliability of cooling technology performance and materials selected. The manufacturing processes of the heat exchanger must also be cost effective.

Technical Targets

This project is helping towards achieving 2015 and 2020 DOE Advanced Power Electronics and Electrical Motors (APEEM) Program goals (cost, power density, and specific power) for power electronics using high-temperature WEG coolant.

Accomplishments

- A jet impingement-based heat exchanger was fabricated out of high-temperature plastic and tested to characterize its thermal performance. Although the prototype was machined, it is possible to fabricate it with injection molding. CFD models were validated with the experimental data. Modeling at inverter-level power predicted full inverter thermal performance.
  - For the experiments, with 105 W heat dissipated, the thermal resistance was 5% lower for impingement on a plain surface and 13% lower for impingement on the microfinned-enhanced surface compared to the baseline, channel-flow-based heat exchanger.
  - Through modeling, with 2,520 W heat dissipated, the thermal resistance was 9% lower for impingement on a plain surface and 32% lower for impingement on the microfinned-enhanced surface.
  - Due to the reduction in weight and increased thermal performance, the specific power (kW/kg) increased up to 78% and the power density (kW/L) increased up to 47% (both values for the enhanced surface).
- Reliability testing indicated that the jet nozzle diameter does not change due to wear or clogging. Reliability testing for the enhanced surface thermal performance and DBC and DBA properties is ongoing.

✧   ✧   ✧   ✧   ✧

Introduction

Reducing cost and increasing power density and specific power are some of the key objectives of the DOE APEEM Program to meet the 2015 and 2020 Program targets and to help increase market penetration of electric-drive vehicles. Thermal management techniques can be used to help achieve the overarching goals of the program. The objective of this work is to design, develop, characterize, and demonstrate a light-weight, low-cost, inverter-scale (based on a commercially available inverter) single-phase liquid-cooled (with WEG, [50%–50% mixture by volume] coolant) heat exchanger/cold plate, which is a significant improvement over conventional channel-flow-based heat exchangers. Single-phase liquid jets have been studied extensively in the literature [1-4]. These studies include experiments, theoretical analyses, and numerical simulations. Different configurations of impinging jets have been studied, including single free-surface jets [5], multiple free-surface jets [6-8], single submerged jets [5, 9, 10], multiple submerged jets [6, 9], and confined single submerged jets [3, 11-13]. Both planar and circular jets have been studied. In the context of electronic cooling, a large number of experimental correlations have been developed for the local and average heat transfer coefficients on the surface of the simulated chip [1-3]. Most of the simulated chips are either 10 mm^2 x 10 mm^2 or 12.7 mm^2 x 12.7 mm^2. Air jets have also been studied extensively [9]. Some of the non-dimensional heat transfer correlations developed from studies on air jets [9] can be applied to liquid jets also. Researchers have explored the impact of a vast array of parameters—such as jet velocity, jet diameter, impact angle, nozzle-to-chip spacing, nozzle-to-nozzle spacing, turbulence levels, nozzle shapes, nozzle length, jet pulsations, jet confinement, chip-surface enhancement, and fluid properties—on the chip-surface heat transfer coefficients. All these are covered in detail in comprehensive reviews [1-3, 9].

Moreover, studies have demonstrated that jet impingement heat transfer can be further enhanced through the use of surface roughening techniques for both liquid and air jets [14-17]. Gabour and Lienhard [15] investigated the impact of surface roughness on jet impingement heat transfer. Their results demonstrated that stagnation-point heat transfer increases with increasing roughness with the roughest surface producing 50% greater heat transfer as compared to the baseline surface. Moreover, the roughness enhancement increased with increasing Reynolds numbers. The enhancement was associated with the roughness structures protruding through the thermal boundary layer within the stagnation zone. Sullivan et al. [16] also reported enhancement using roughened heat sources in the submerged jet configuration. In the study [16], the heat transfer enhancements of the roughened surfaces were associated with mechanisms occurring within the wall jet region. It was speculated that roughened surfaces increased heat transfer by advancing transition to turbulent flow and by disrupting the viscous sub-layer within the turbulent region. The heat transfer performance on a 12.7-mm-diameter copper

target surface of a number of enhanced surface configurations were presented in [17. The study [17] demonstrated the superior performance of the configuration of submerged/flooded jets impinging on a microfinned surface with respect to impingement on a plain surface as well as impingement on a number of other enhanced surfaces. These results were also noteworthy because of the feasibility of the submerged/flooded jet configuration for practical applications [18, 19].

In automotive power electronics, it is important to reduce cost and increase power density and specific power to help make electric-drive vehicles more cost effective and increase their market acceptance and penetration. Traditionally, channel flow-based cold plates using a WEG mixture (50%–50% by volume) are widely used in a majority of hybrid electric vehicles for cooling power electronics components [20].

Approach

Light-Weight Heat Exchanger
Design and Fabrication

Building on lessons learned from the first prototype fabrication and testing [21], a second prototype heat exchanger utilizing a submerged jet-impingement cooling approach and a light-weight plastic material was fabricated using a machining process. The two main differences of this prototype from the first prototype are the material and manufacturing process, and the flow path. The first prototype was a heat exchanger consisting of a fluid-manifold that was fabricated using a selective-laser-sintering rapid prototyping process using automotive-grade glass-fiber-reinforced nylon plastic. The second prototype was machined from Delrin, a high-temperature plastic, although this part could be injection molded from a variety of high-temperature plastics. The first prototype heat exchanger replaced the channel-flow with jets to impinge on the module surfaces. No other changes were made to the flow path from the baseline design. The second prototype removed unnecessary flow path to reduce the pressure drop, which increased with the introduction of the jets compared to the channel-flow technology.

The first prototype heat exchanger, shown in Figure V-1, was designed to cool a commercially available inverter from UQM Technologies Inc. The new heat exchanger design implements a light-weight manifold that incorporates liquid jets directly impinging on the power module base plates. The second prototype heat exchanger, shown in Figure V-2, shows the reduction in flow path with respect to the first prototype, as well as the jet nozzles. Parts of the manifold have been omitted from fabrication for ease of testing (for example, the platform for the capacitor bank). The jet impingement cooling approach eliminates the use of thermal interface material between the base plate and the heat sink/cold plate, and therefore is expected to improve thermal performance. Further details on the CFD modeling and design are given in [22].
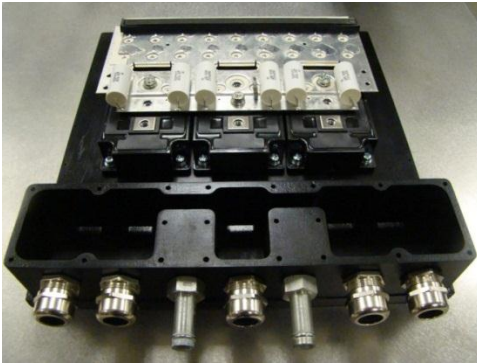
Figure V-1: First light-weight, inverter-scale plastic heat exchanger prototype (Photo credit: Mark Mihalic, NREL).
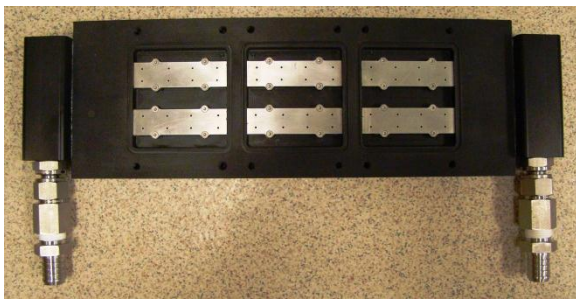
Figure V-2: Second light-weight, inverter-scale plastic heat exchanger prototype (Photo credit: Scot Waye, NREL).

Experimentation

Experiments were conducted to characterize the performance of the new heat exchanger, as seen in Figure V-3.

Previous experiments have characterized the first prototype as well as the baseline channel-flow-based aluminum heat exchanger. The tests were carried out using WEG (50%–50% mixture by volume) as the coolant at a temperature of 70°C. An industry-standard flow rate of 10 L/min (1.67×10^{-4} m³/s) as well as 2, 5, and 8 L/min were examined for the various heat exchangers. For these experiments, the diodes on one power module were powered, and their temperature was measured using a transient thermal tester. Based on the information of diode junction temperature as well as the total power dissipated in the diodes, the total thermal resistance was computed.
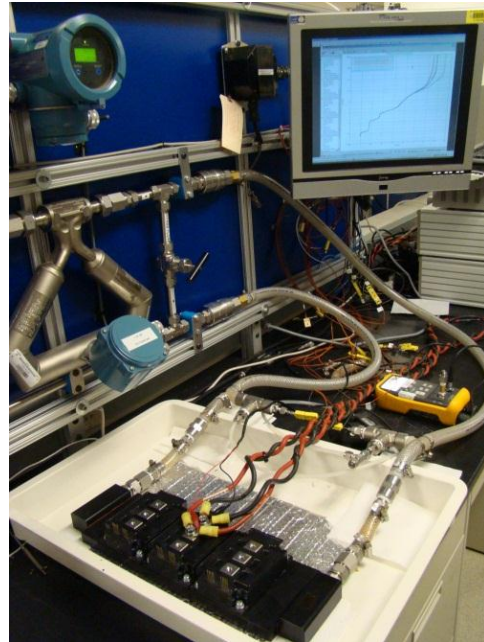
Figure V-3: Second prototype testing on the WEG loop (Photo credit: Scot Waye, NREL).

For the second prototype heat exchanger experiments, two sets of modules were used. The first set had plain copper base plates. The second set had microfinned surface enhancement located under each insulated gate bipolar transistor (IGBT)/diode pair, as seen in Figure V-4, with a close-up of the microfinned surface.

Full-scale inverter testing will be conducted using a dynamometer to simulate a real-world thermal load profile. The experimental results will be compared to full inverter power modeling results for the baseline and jet impingement-based heat exchangers.

Modeling

Through validated CFD modeling (via experiments), the improvement in thermal and overall performance of the impinging jet designs were analyzed at full power (2.5 kW) compared to the baseline channel-flow-based heat exchanger.

A CFD model was created using the same geometry and properties as the experimental setup. Using the experimental data obtained with four diodes powered to produce approximately 105 W of heat, the thermal resistance was matched in the model by adjusting the solder layer resistance for the jet-impingement cases and the thermal grease layer resistance for the channel flow cold plate case. The thickness and resistance of the solder and grease layers were unknown previously.

A k-ω turbulence model was used. The grid was adapted to yield a y+ (non-dimensional distance of grid centroids) of less than one on the impinging surface, and the average and maximum device temperatures were monitored. (All residuals were set to 10^{-3} except for energy, which was set to 10^{-6}).
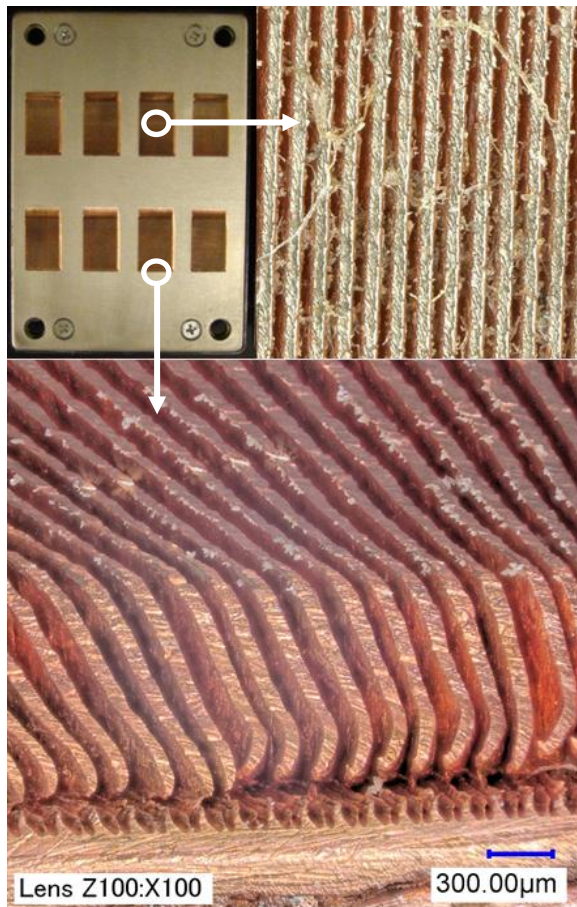
Figure V-4: Wolverine Tube MicroCool finned surface technology on module (top left) and close-up (top right and bottom) (Photo credits: Scot Waye, Mark Mihalic, Gilbert Moreno, NREL).

All of the 24 IGBTs and 24 diodes were powered at a two-to-one ratio, yielding a heat generation rate of 1.944×10^9 W/m^3 (70 W per device) for the IGBTs and 2.12×10^9 W/m^3 (35 W per device) for the diodes, yielding 2,520 W of total heat dissipation.

A flow rate of 10 L/min for WEG at 70°C was used for the simulations. To predict the thermal performance for the micro-finned enhanced surfaces, the flow rate was doubled to double the jet velocity. Previous research [22] found that for the microfinned surface enhancement used, the heat transfer coefficient at 10 L/min with the enhanced surface was approximately the same as the coefficient at 20 L/min for a plain surface.

Reliability

Experiments were conducted to evaluate the long-term reliability of Wolverine's MicroCool enhanced surfaces and DBA and DBC substrate samples.

Previous reliability testing run over a 12-month period used 35°C WEG free jets at 2, 5, and 12 m/s on unplated microfinned surfaces. Results showed no degradation in nozzle diameter and a decrease in thermal performance on the microfinned surfaces at high velocities due to oxidation.

Additional reliability tests are running using a 65°C automotive grade WEG on two nickel-plated microfinned surfaces, three DBA substrates, and three DBC substrates at 5 m/s. A schematic of the test apparatus is shown in Figure V-5. Near-continuous jet impingement testing has been performed for approximately four months.
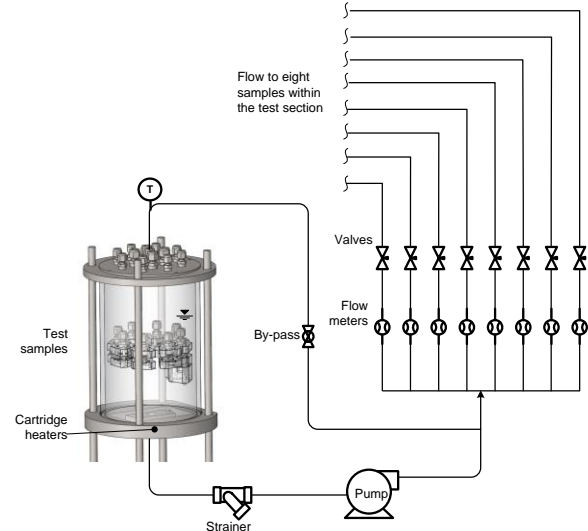
Figure V-5: Test setup for long term reliability tests.

The Delphi DBA and DBC substrate samples are examined with several testing metrics (see Figure V-6). Digital microscope images will examine surface characteristics and provide an overall qualitative comparison. A scanning acoustic microscope (CSAM) images layers below the surface, including the substrate interfaces. Laser profilometry examines the surface roughness and shape. Xenon flash is used to measure the thermal diffusivity.

The two Wolverine MicroCool nickel-plated samples are characterized using digital microscopy for surface images, and the heat transfer coefficient will be measured.
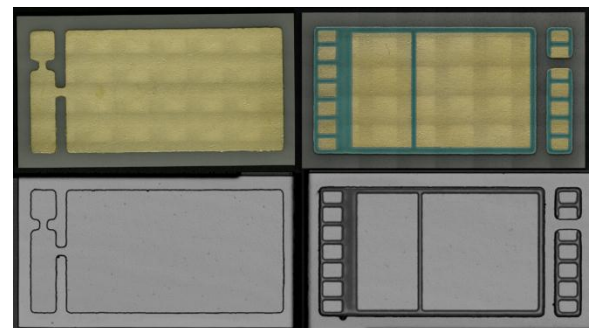
Figure V-6: Digital images of the DBA top (top left) and bottom (top right); C-SAM images of the DBA top (lower left) and bottom (lower right) (Photo credit: Jana Jeffers, NREL).

Collaborations

For this project, NREL established collaborations with UQM Technologies Inc., which provided the baseline heat exchanger and will be assisting in full invertor testing using a dynamometer; Wolverine Tube Inc., which manufactured the

microfinned enhanced surfaces; and Delphi, which provided DBC and DBA samples for reliability testing.

Results

Heat Exchanger Experimentation

Experimentation using a transient thermal tester yields structure functions which provide information on the thermal capacitance and the thermal resistance, which can ultimately be used to determine the thermal resistance of the passive stack and the cooling approach. By examining all the structure functions together regardless of flow rate or cooling strategy (channel flow cold plate, impingement on plain surfaces, impingement on enhanced surfaces), the point where the structure functions diverge indicates the boundary between the passive stack in the module and the convective cooling technology. For the PowerEx modules used in this testing, the thermal resistance of the passive stack was approximately 0.09 K/W.

For 8-L/min and 10-L/min flow rates, the junction to liquid thermal resistances ($R_{th,j-l}$ [K/W]) and percent reduction as compared to the baseline channel flow cold plate are provided in Table V-1. The structure functions for various heat exchanger configurations at 10 L/min are given in Figure V-7.
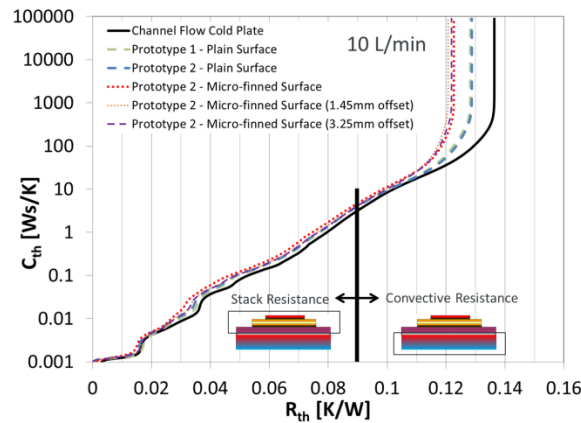
Figure V-7: Structure functions of heat exchangers showing thermal resistance (x-axis) of various cooling technologies.

The test cases included the channel flow, the first prototype jet-impingement heat exchanger with plain surfaces, and the second prototype jet-impingement heat exchanger

with plain and microfinned enhanced surfaces. For the jet-impingement heat exchangers, the nozzle-to-baseplate distance (target distance) was also examined. The nominal target distance was 0.5 mm. Offsets of 1.45 mm and 3.25 mm were introduced, yielding a 1.95 mm target distance for the plain surface. For the microfinned enhanced surface, the microfins extended approximately 200 µm into the flow, reducing the jet length to 1.75 mm and 3.475 mm with the two offsets, respectively.

For the plain surface, increasing the nozzle-to-target distance decreases the thermal performance. For the enhanced surface, the thermal performance slightly increases with increasing target distance, but as the target distance increases further, the thermal performance is reduced. The interaction of the jet with the surface to create a thin boundary layer and turbulence are important aspects to transfer the heat from the solid into the fluid. For very low velocities (flow rate and jet nozzle diameter) and large target distances, the momentum of the jet decreases and the jet core spreads, decreasing heat transfer on the surface. For enhanced surfaces, there is an optimal distance depending on the jet characteristics.

The thermal performance for the first and second prototypes with jets impinging on plain surfaces is nearly the same, which is expected due to keeping the jet design the same between iterations. For the jet-impingement on a plain surface heat exchanger, the thermal resistance was reduced by 5.1%. On the microfinned surface, the reduction was 12.5% at the best target distance and 10.3% at the nominally designed distance (0.5 mm).

The resistance of the passive stack was approximately 0.09 K/W. By subtracting this resistance from the total resistance, the convective resistance (the resistance from the solid to the fluid) ($R_{th,hx}$ [K/W]), or the part that is controlled by the heat exchanger design, is 15.2% lower for jet impingement on plain surfaces, and 37.0% lower for jet-impingement on microfinned enhanced surfaces. Additional reduction to the junction to liquid resistance can be achieved by more aggressive cooling strategies or reducing the resistance in the passive stack.

Table V-2 shows the experimental pressure drop across the various heat exchanger designs at 8 L/min and 10 L/min. As previously discussed, the first prototype had a large increase in pressure loss due to the introduction of the jets. By

Table V-1: Thermal resistance, $R_{th,j-l}$ [K/W] and improvement over channel flow heat exchanger for 8 L/min and 10 L/min: (1).

	Channel Flow	Jet/Plain (1)	Jet/Plain (2)		Jet/Microfinned (2)		
Target distance (mm)		0.5	0.5	1.95	0.3	1.75	3.475
Resistance, $R_{th,j-l}$ [K/W]							
8 L/min	0.139		0.136	0.143	0.126	0.126	0.128
10 L/min	0.136	0.128	0.129	0.136	0.122	0.119	0.122
Improvement over baseline							
8 L/min			2.2%	-2.9%	9.4%	9.4%	7.9%
10 L/min		5.9%	5.1%	0.0%	10.3%	12.5%	10.3%

removing unnecessary flow path in the second prototype, the pressure loss was closer to the baseline channel flow heat exchanger. Therefore, the improvement in the coefficient of performance, defined as the inverse product of the junction to liquid thermal resistance and the fluid power, was nearly the same for the jet impingement on the plain surface heat exchanger and 13% for the jet impingement on the microfinned surfaces heat exchanger.

Table V-2: Experimental pressure drop across heat exchanger [Pa]. (1) denotes first prototype, (2) denotes second prototype.

	Channel Flow	Jet/Plain (1)	Jet/Plain (2)	Jet/Microfinned (2)
8 L/min	12,686		13,221	12,755
10 L/min	19,598	24,407	20,581	19,995

Heat Exchanger Modeling

Flow rates, pressure drops, average and maximum temperatures and junction to liquid thermal resistances based on the respective temperatures are given in Table V-3.

The focus of the modeling was on a power ratio of two to one for the IGBTs and diodes for a total power of 2,520 W. Power ratios of one-to-one and three-to-one were also examined as well as total heat dissipation of 1,152 W and 3,456 W. In general, the overall resistance of the inverter remains the same at these three power levels.

The thermal resistance for the jet-impingement heat exchanger was reduced by 9% and 32% for the plain and microfinned surfaces, respectively. The average and maximum temperatures of the devices were reduced by approximately 5°C (Figure V-8) and 15°C for the plain and microfinned surfaces with jet impingement, respectively, as compared to the baseline heat exchanger.

The channel flow heat exchanger removes heat from the aluminum plate via the fluid. The locations of the modules and devices are not as critical for the channel flow heat exchanger compared to the jet impingement configuration, as the aluminum acts as a heat sink. For the jet impingement heat exchanger, the aluminum cold plate is removed and the jets impinge directly on the module copper baseplate. This localized and directed cooling creates high local heat transfer coefficients where the heat is the highest, under the devices, as shown in Figure V-9.

The reduction in thermal resistance from junction to liquid is greater for full inverter power than the partial power used in the experiments because the resistance is subject to not only the convective cooling resistance, which relies on the cooling strategy or technology, but also the heat flux magnitude and

distribution. As the heat seeks the path of least resistance, as illustrated in Figure V-10, either due to a low convective cooling resistance at the solid-fluid interface or the absence of multiple heat generating devices, it will manifest as a lower thermal resistance due to reduced heat spreading.
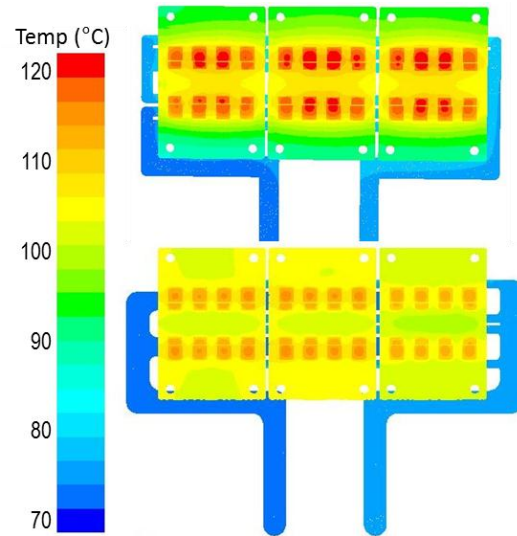
Figure V-8: Temperatures of modules for baseline (top) and jet impingement on the plain surface for the first prototype (bottom). The second prototype has similar thermal performance.
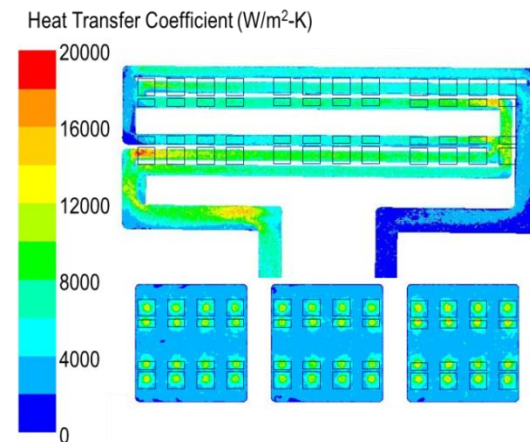
Figure V-9: Heat transfer coefficient at the solid-fluid interface for baseline (top) and jet impingement on the plain surface of the first prototype (bottom). The second prototype has similar thermal performance.

Table V-3: Thermal Resistance and Device Temperatures for Modeled Heat Exchangers. *Flow rate doubled to match heat transfer coefficient of microfinned enhanced surface.

	Flow rate [L/min]	ΔP [Pa]	$T_{avg,devices}$ [K]	$R_{th,j-l}$ [K/W]	$T_{max,devices}$ [K]	$R_{th,j-l}$ [K/W]
Channel Flow Cold Plate	10	17,891	391.6	0.0192	395.8	0.0209
Jet/Plain (1)	10	20,800	386.7	0.0173	390.6	0.0188
Jet/Microfinned (1)	20*		376.6	0.0132	380.1	0.0147
Jet/Plain (2)	10	18,732	387.2	0.0174	391.2	0.0190
Jet/Microfinned (2)	20*		376.2	0.0131	380.2	0.0147
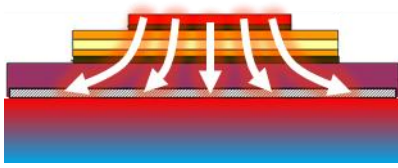
Figure V-10: Heat spreading from junction to liquid.

The coefficient of performance improves by up to 5% and 40%, specific power increases 29% and 55%, and power density increases 6% and 28% over the baseline for the plain and microfinned surfaces with jet impingement, respectively.

A 9% decrease in thermal resistance allows for 10% more heat to be dissipated. Using basic analytical equations for devices, this correlates to an approximate 6% increase in power per device area, or a 6% decrease in device area per power by varying only the current. Therefore, 6% of the device area (such as silicon) or number of devices could theoretically be removed, creating a cost savings. For example, a 32% decrease in thermal resistance translates to an approximate device area reduction of 22%.

Reliability

The reliability experiments have been running for almost four months. After 60 and 120 days, the samples were examined and potential defects were noted to observe closely as testing progresses. Because the entire substrate is submerged, there is a possibility of degradation from a reaction between the ceramic substrate and the WEG, which will be monitored (under normal operating conditions, one side may be exposed to WEG, but not completely submerged). Concerns of a reaction between the ceramic layers and WEG were realized. After 120 days, two DBA samples have severe degradation, possibly from a chemical reaction between the ceramic layers and the WEG. Reliability of jet impingement on the face of the substrate is the objective, so a completely submerged substrate may have caused unintended results. After 60 days, the thermal diffusivity of the substrate samples did not change outside of the uncertainty of the measurement. After 120 days, the thermal diffusivity is decreasing, especially for DBA1 and DBA3, which were the two samples that had degradation, as seen in Figure V-11.
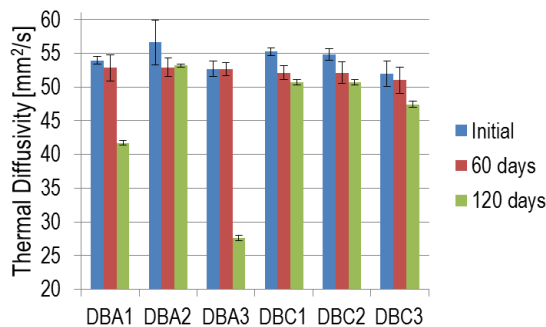
Figure V-11: Thermal diffusivity of DBA and DBC substrates. Error bars represent a standard deviation of five measurements.

Conclusions and Future Directions

- A new light-weight heat exchanger designed to cool a commercially available inverter was fabricated.
- Experiments at low power demonstrate that the new heat exchanger can reduce the thermal resistance by 5% to 13% with plain and microfinned-enhanced surfaces, respectively, with respect to a baseline channel flow-based heat exchanger.
- CFD modeling at inverter power projects thermal resistance reductions of 9% and 32% for plain and micro-finned-enhanced surfaces, respectively. Along with a weight reduction of approximately 3 kg, specific power is improved by up to 78%, and power density by 47% as compared with the baseline, channel-flow-based heat exchanger design.
- The fabrication of the new heat exchanger out of light-weight plastic may also provide additional cost savings associated with inexpensive materials and cost-effective manufacturing techniques.
- Experiments were conducted to evaluate the reliability of the Wolverine MicroCool enhanced surfaces and DBA and DBC substrates when subjected to near-continuous impinging WEG jets. Testing is ongoing.
- Inverter-level experiments using a dynamometer are planned to characterize the improvement in thermal performance for the jet impingement heat exchanger compared to the baseline.

FY 2013 Publications/Presentations

Narumanchi, S. "Advanced Liquid Cooling R&D." Presentation/Poster, DOE Annual Merit Review; May 13–15, 2013, Arlington VA.

Acknowledgments

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V.2. Air-Cooling Technology for Power Electronics

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Start Date: FY11
Projected End Date: FY15

Objectives

The overall project objective is to develop and apply air-cooling technology to improve power electronics thermal management design and influence industry, enhancing system performance to help meet the U.S. Department of Energy (DOE) Advanced Power Electronics and Electric Motors (APEEM) Program power electronics technical targets for weight, volume, cost, and reliability. This overall objective includes the following:

- Develop and demonstrate commercially viable, low-cost air-cooling solutions for a range of vehicle applications and assess their potential for reducing the cost and complexity of the power electronics cooling system.
- Enable heat rejection directly to ambient air, simplifying the system by eliminating liquid coolant loops, thereby improving weight, volume, cost, and reliability.
- Collaborate with Oak Ridge National Laboratory (ORNL) to demonstrate the feasibility of using a high-temperature air-cooled inverter to achieve DOE technical targets.
- FY 13 objectives included:
  - Determine the feasibility of high-temperature air-cooled inverter
  - Build a system-level test bench and begin investigation of balance-of-system components
  - Begin thermal design optimization to ensure that effective designs are being used to determine the bounds of air-cooled inverter design space.

Technical Barriers

The use of air as a coolant has several benefits, drawbacks, and challenges. Air is free, it does not need to be carried, it is benign (no safety or environmental concerns), and it is a dielectric. As a heat transfer fluid, however, it has a number of drawbacks. Air has a low specific heat, low density, and low conductivity. These make it a poor heat transfer fluid and cause a number of design challenges. To reject the high power densities required by electric drive power electronics using the heat transfer coefficients achievable with air, large increases in wetted area are needed. When increasing area, spreading resistance, fin efficiency, weight, volume, and cost need to be considered. Due to the low specific heat, larger mass flows of air are required to remove the heat. This can lead to parasitic power issues, especially coupled to the pressure loss of extended surfaces. This requires careful consideration of the system coefficient of performance. Depending on the location of the inverter, environmental loads and ducting to better air sources may need to be considered. Location can also affect the need for noise suppression for the prime mover (blower/fan). For example, the Honda system incorporated a silencer [1] because the inverter was located in the passenger compartment. In order to push heat transfer performance higher, small-channel heat exchangers can be used, but filtering must be addressed. If needed, filtering can add pressure drops and maintenance issues may need to be addressed.

Technical Targets

The DOE technical targets applicable to this research are the 2015 and 2020 APEEM Program targets for power electronics with 30-kW continuous and 55-kW peak power.

Accomplishments

- Revised heat generation analysis for updated device data from ORNL using conservative assumptions to yield 25 W per device heat load for a nine-module inverter approach and 45 W per device heat load for a six-module inverter approach.
- Through modeling, showed the heat transfer feasibility of a high-temperature, air-cooled inverter. Predicted 3.2 kW of heat rejection, surpassing the conservative target of 2.7 kW, using 0.054 m³/s (115 CFM) of air. This predicted flow rate and pressure drop could be provided by a 50-W fan. This flow rate is less than that used by a typical automotive climate control system.
- Using computational fluid dynamics (CFD), developed optimization driver combined with assumptions about remaining inverter components, conducted parametric study over design space to identify candidate heat exchanger designs that meet future DOE technical targets for weight and volume while limiting parasitic losses. Found designs exceeding 2015 targets with fan parasitic

power similar to automotive climate control system condensers or fans.

- Combined module-level optimization with balance-of-system components (ducting) to optimize heat exchanger design for system-level performance, which incorporated assumptions from experimentally obtained ducting pressure losses.

- Built test apparatus for sub-module testing for model validation.

✧   ✧   ✧   ✧   ✧

Introduction

All commercially available electric-drive vehicles, with the notable exception of the low-power Honda system, use liquid-cooled power electronic systems. All the heat from a vehicle, however, must ultimately be rejected to the air. For liquid-cooled systems, heat from the power electronics is transferred to a water-ethylene glycol coolant via a heat exchanger and then pumped to a separate, remote liquid-to-air radiator where the heat is rejected to the air. Air cooling has the potential to eliminate the intermediate liquid-cooling loop and transfer heat directly to the air.

Eliminating the intermediate liquid-cooling loop using direct air cooling of the power converter can reduce system complexity and cost by removing or reducing the pump, coolant lines, remote heat exchanger, remote heat exchanger fan, and coolant. In order to realize these gains, however, effective system-level design of the direct air-cooled system heat exchanger, fan, and ducting is needed. Decoupling the inverter/converter from the liquid cooling system also has the potential to provide increased flexibility in location. Honda took advantage of this benefit by placing its 12.4-kW power electronics system behind the rear seat of the vehicle cabin and integrating closely with the battery thermal management system [1].

As power electronic semiconductor and electronic packaging technology advances, higher allowable junction temperatures will further expand the feasible designs and benefits of direct air-cooled power electronics. Currently, silicon insulated gate bipolar transistors (IGBTs) have a maximum allowable junction temperature between 125°C and 150°C [2,3] that may be extended to 175°C in the future [3], while advanced semiconductor technologies such as silicon carbide (SiC) and gallium nitride (GaN) allow operation above 200°C [4–6] and may also improve the inverter efficiency at lower temperatures [5].

The Honda system is a mass-produced, commercially available solution. It is low power, however, with a peak power delivery of 12.4 kW [1]. The electric Mini-E uses an air-cooled AC Propulsion drive system. This has a 50-kW continuous, 150-kW peak power, but does not meet DOE technical targets and is low production volume [7]. Additional research adds to commercial solutions. Toshiba Corporation is researching and developing a new power module design for forced-air cooling systems for a power converter [8]. ETH Zurich University has published a number of studies on this topic recently and is

actively researching high-temperature, air-cooled power electronics for automotive and other applications. One of these papers found that, combined with a Peltier element, a high-temperature SiC automotive inverter could operate at a 120°C ambient [9]. Another reports the possibility of using extremely high-temperature SiC devices (234°C and higher) to create an air-cooled electric-drive vehicle inverter with a power density of 51 kW/L and operating at 120°C ambient [10]. For aggressive, high-flux cooling of electric-drive vehicle inverters, Aqwest is investigating circulating liquid metal flow loops to enable forced air cooling [11].

Approach

- Use a system-level approach that addresses the cooling technology, package mechanical design, balance-of-system, and vehicle application requirements.

- Research each of these areas in depth and apply findings to develop effective system-level designs.

- Develop experimental and analytical/numerical tools and processes that facilitate high-quality and rapid research results.

- Investigate the effect high-temperature power semiconductor devices have on air-cooled inverter design.

- Work closely with industry, university, and national laboratory partners to ensure relevant and viable solutions.

The objective of NREL's Air-Cooling Technology for Power Electronics Thermal Management project is to assess, develop, and apply air-cooling technology to improve power electronics thermal control design and influence industry's products, thereby enhancing system performance to meet DOE technical targets for weight, volume, cost, and reliability. This research effort seeks to develop the necessary heat transfer technology and system-level understanding to eliminate the intermediate liquid-cooling loop and transfer heat directly to the air. The relative merits of air-cooled, high-heat-flux automotive power electronic thermal management systems and the influence of high-temperature, wide bandgap semiconductors on this design space will be quantified, evaluated, and demonstrated under steady state and transient conditions.

Effectively and viably accomplishing these goals requires an air-cooled system thermal design understanding and approach. As shown in Figure V-12, this project will use modeling and experimentation to address each aspect of the system: heat transfer cooling technology, power electronics package thermal design, balance-of-system (prime movers, ducting, etc.), and their interconnected interactions. It is also critical to account for and understand the effects of constraints and inputs into the air-cooled thermal management system: thermal environment, device type, and vehicle context. The thermal environment constraints have a direct impact on the driving temperature difference available for air-cooled heat transfer and can vary depending on design targets and system location in a vehicle. Under-hood temperatures are approximately 100°C–140°C and are therefore unsuitable for cooling. External ambient air at 30°C–45°C is highly suitable

for cooling, and some additional benefit can be gained from using cabin air, but it must be balanced with the added parasitic load on the air conditioning system. The device type will determine both the maximum junction temperature and efficiency and thus influences the maximum allowable package surface temperature and heat load. Advanced power semiconductors, such as silicon carbide and gallium nitride, have the potential to greatly expand the air-cooling feasibility range by increasing the allowable junction temperature from 125°C to 200°C or higher while possibly improving efficiency. Vehicle context determines the power electronics duty cycle, affecting the total heat rejection needs and also imposing constraints on the system volume and weight. Understanding the in-vehicle demands on the power electronics systems will allow for modulated designs to meet cooling needs, reducing system overdesign and minimizing parasitic losses.
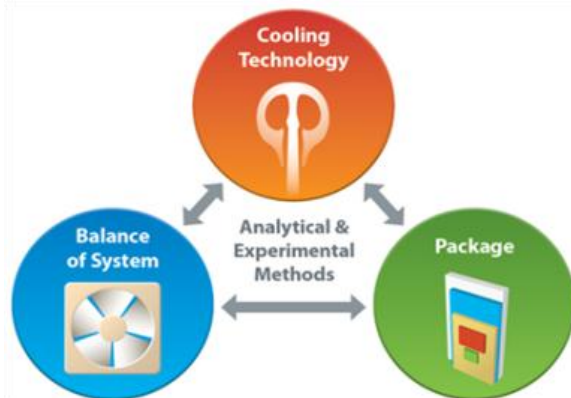
Figure V-12: Power electronics air-cooled thermal management system research and design approach.

To move ideas from concept to implementation, four levels of research, development, and demonstration will be used: novel cooling technology fundamental heat transfer, system-level heat transfer and balance-of-system, module-level application and demonstration, and inverter-level demonstration (Figure V-13). This process will both ensure that each level of complexity assists in achieving the overall objectives and serve to screen ideas so that only the best approaches pass to the next level.
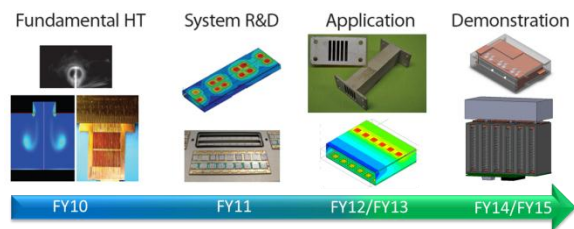
Figure V-13: Air-cooling system research, development, and demonstration approach.

Project Timeline

In FY11, NREL completed a proof-of-principle analysis using a system-level approach [12]. In this analysis, as expected, the baseline liquid-cooled system significantly outperformed the air-cooled system. The relative performance of the air-cooled system improved with increasing allowable

junction temperature and/or use of the improved concept spreader. At an allowable junction temperature of 200°C or 150°C plus the use of the advanced spreader, the air-cooled system was able to match the power density of the liquid-cooled approach. The air-cooled system using advanced technology could meet or exceed the power per total insulated-gate bipolar transistor (IGBT) area of the liquid-cooled system. This analysis indicated that a high-temperature air-cooled system held significant promise and should be pursued in more depth.

Based on these results, NREL established a high-temperature air-cooled inverter collaboration with ORNL. The goal of this project is to demonstrate the feasibility of meeting DOE's 2015 technical targets by using a high-temperature air-cooled inverter. ORNL is leading the advanced wide-bandgap-device evaluation and selection and electrical topology design. NREL is leading the thermal management design and evaluation at both the module- and system-level. The thermal system design approach for this collaboration is shown in Figure V-14. This is an iterative process between NREL and ORNL that involves other industry partners at various stages.
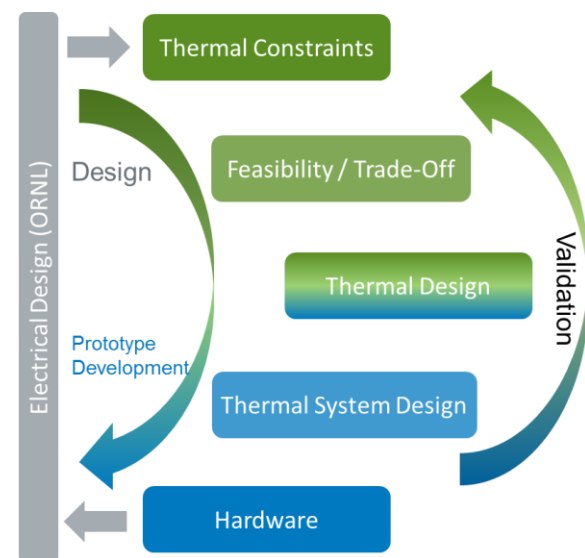
Figure V-14: High-temperature, air-cooled inverter thermal design approach.

In FY12, electrical design information was passed from ORNL to NREL, which then converted the information into thermal design targets. Based on this information, a feasibility/trade-off study was conducted using CFD modeling and experimental validation. After determining the feasibility, NREL applied modeling and experimental tools to begin a detailed thermal design to ensure an optimized prototype.

In FY13, the optimization continued and a sub-module section of the baseline design was fabricated to validate the models. Further optimization and exploration of the design space yielded viable solutions to meet targets without incurring excessive parasitic power.

In FY14, an optimized design will be chosen, prototyped, and tested. This will be combined with the module electronics from ORNL and tested as an operational unit. The thermal and

electrical performance will be tested in parallel, and lessons learned will be applied to further improve the design. A feasible ducting solution will be analyzed for flow characterization and pressure losses to size an appropriate fan for the system. The full system thermal feasibility will also be determined.

In FY15, the goal is to build and demonstrate an operational high-temperature, air-cooled inverter.

Experimental Methods

The Air Cooling Technology Characterization Platform, shown in Figure V-15, was updated in FY12. Compressed air is supplied to a desiccant dryer to remove moisture. The air is dried to a dew point of -20°C or lower. It is passed through a 5-μm particulate filter and regulated to a constant pressure of 68 to 137 kPa. This regulated pressure served as the source air for a mass flow controller, Sierra model C100L, which provided a range of flow from 3.3 cm^3/s to 166 cm^3/s. Next, a laminar flow element, CME model 10 (0–166 cm^3/s), is used for more accurate measurement of the actual air flow rate. This more accurate measurement is used to adjust the upstream mass flow controller set point. The air passes through a plate heat exchanger for optional temperature control. It then enters the fin test section. Ceramic resistance heaters provide the heat flux necessary, and power is adjusted to yield the desired junction temperature. Air flow exiting the fin section passes through porous aluminum foam to mix the air and get an accurate bulk air exit temperature. The test section was wrapped in insulation and placed in a Plexiglas enclosure to minimize the effect of ambient air motion in the laboratory. Heat transfer measurements were fully automated and controlled by a computer and a National Instruments data acquisition system.

The heater assembly had a copper base plate in contact with the fin section. Small grooves were machined to allow thermocouple placement. The assembly was fixed together with thermal epoxy. The channel flow experimental uncertainty was calculated in accordance with American Society of Mechanical Engineers (ASME) standard PTC 19.1-2005 [13].

In FY12, an air-cooling system-level test bench was completed (Figure V-16). This test bench is intended for fan performance characterization, duct and plenum measurement, inverter module-level testing, and system-level demonstration. The air flow measurement section of the test bench follows ANSI/AMCA Standard 210-07 [14]. By using a series of nozzles, the flow chamber can maintain high accuracy measurements over a 5–500 CFM range. In the current configuration, air enters the chamber at plane 1, passing through the device under test (fan currently), and through plane 2, entering the larger chamber. Using a combination of the variable exhaust fan and blast gate controls, the pressure at plane 7 is controlled for back pressure on the fan. The air passes through settling screens and across the nozzle plate. The pressure drop across the nozzles, plane 5 to plane 6, is used to determine flow rate. The air then passes through additional settling screens and exits through the blast gate and variable exhaust blower.
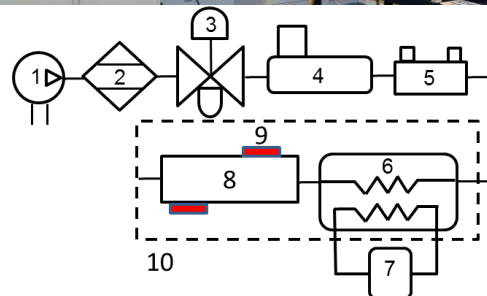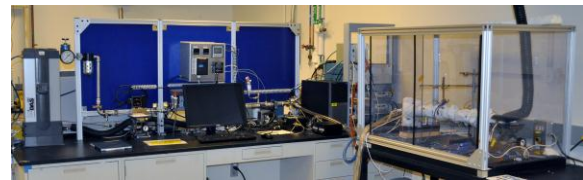
Figure V-15: Photograph (top) and schematic (bottom) of the channel flow experimental setup: (1) compressed air, (2) desiccant dryer, (3) filter/regulator, (4) mass flow controller, (5) laminar flow element, (6) plate heat exchanger, (7) temperature control bath, (8) fin test section, (9) ceramic resistance heaters, and (10) isolation box.
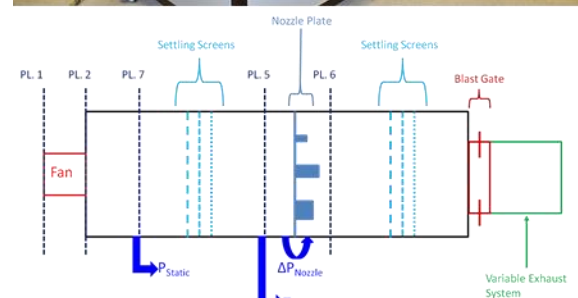
Figure V-16: System-level air-cooling test bench picture and schematic.

The test bench was checked for repeatability, transducer hysteresis, and instrument impedance effects, all of which had negligible errors. An optical fan speed sensor was used to measure fan speed. Uncertainty and propagation of error analysis, per ASME standard PTC 19.1-2005 [13], determined an average U_{95} uncertainty in flow of ±1.2% and an average uncertainty in pressure of ±0.94%.

Numerical Methods

CFD models were created in ANSYS Fluent software for several stages of this project. For most of these models, convergence criteria were 10^{-3} for all residuals except energy and continuity for which the convergence criteria were tighter. More stringent convergence criteria were tested with minimal impact on results. Velocity and pressure residuals were also monitored. When needed, a k-ε turbulence model with enhanced wall treatments was utilized. For each model, the results were confirmed to be mesh independent. To reduce computational expenses for the parametric optimization study, a full mesh sensitivity study was completed (Figure V-17). It can be seen that as the mesh size increases, the time to converge increases and the relative error decreases. The circled point was selected for the parametric simulations to balance run time and accuracy. Simulations were run on a high-performance computer, using up to 32 computational cores in parallel.
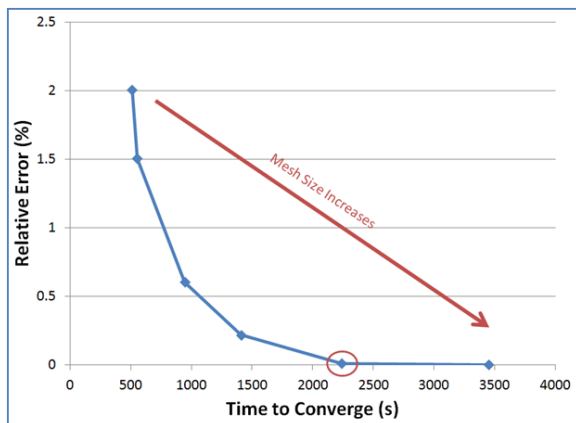
Figure V-17: Mesh sensitivity plot for parametric optimization study. The circled point was selected.

Results

Thermal Constraints

Previous thermal constraints were revisited with updated device data provided by ORNL. Analytical equations were used to estimate the heat generation loads. The analytical model followed methods found in the literature for calculating conduction and switching losses for pulse-width modulation (PWM) inverters [15,16].

ORNL provided experimental data for high-temperature semiconductor device parameters collected as part of its wide bandgap benchmarking efforts. Data included device voltage as a function of temperature and current, turn-on energy losses, turn-off energy losses, and reverse recovery losses. Using the data provided, the transistor conduction loss, diode conduction loss, transistor switching loss, and diode switching loss were calculated over a range of operating conditions. These results were checked for consistency and also compared with overall inverter efficiency estimations.

Although heat loads will vary depending on operating conditions, the current operation condition, power factor, and

junction temperature were all conservative. A safety factor of 1.5 was added to the metal-oxide-semiconductor field-effect transistor (MOSFET) heat loss, and that value was used for all devices, even though half of the devices are diodes with a lower heat generation rate under motoring conditions.

From this analysis, a design target for nine parallel modules (each module has 12 devices) of 2.7 kW of heat dissipation was determined, equating to a 95% efficient inverter (55 kW peak motoring power), as shown in Figure V-18. The heat generation rate of all the devices was set at 25 W per device. For six parallel modules, a design target of 3.26 kW (94% efficiency, 45 W per device) was established, seen in Figure V-19. Maximum junction temperatures ranging from 150°C to 200°C were selected to represent a range of near- to mid-term technologies, with 175ºC used for most analysis.
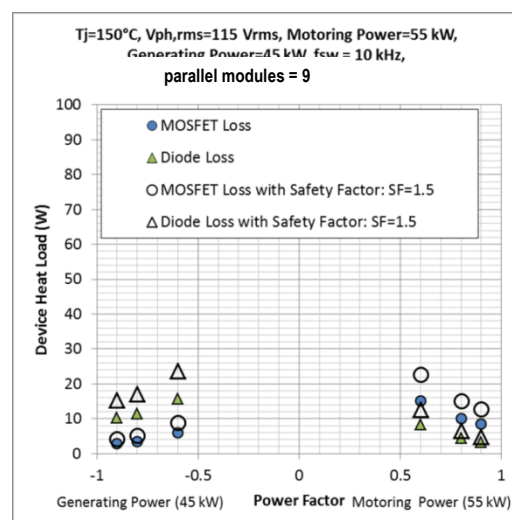
Figure V-18: Heat generation rates for MOSFET and diode power electronic devices for nine parallel modules.
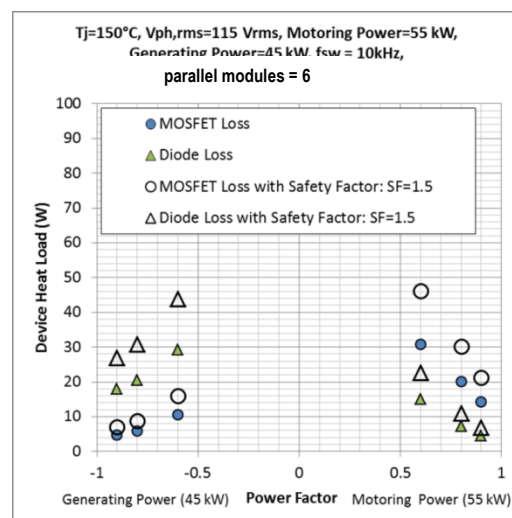
Figure V-19: Heat generation rates for MOSFET and diode power electronic devices for six parallel modules.

Heat Exchanger Optimization

With updated heat generation rates, optimization of the thermal design continued. The process is described in the previous year's annual report [17], but a short summary is provided here.

Using ANSYS Fluent and an NREL-developed "ANSYS Driver" tool, simulation parameters were selected and used in an iterative process, as described in [18]. Each device had a fixed heat generation rate and the air flow rate was updated using a Newton-Raphson method until the maximum device temperature (of either device) was 175°C±1°C. Therefore, designs were compared on an equal heat transfer performance basis and this ensured that they would all meet the thermal requirements if allowed sufficient air flow rate.

The optimization was to reduce weight, cost, and fluid power (the product of volumetric flow rate and pressure drop). Reducing fluid power (parasitic losses) and weight and volume can be competing goals.

The baseline geometry was a design from ORNL consisting of rectangular fins. A one-sixth portion of the module (with one device on the top and one on the bottom of this sub-module) (Figure V-20) was modeled simplify computational expense. Symmetry was used for full module extrapolation. Previous optimization showed the effect of various parameters, such as device location, fin thickness, and baseplate thickness. A constraint of 1 mm was also set for minimum thickness due to manufacturing concerns. Many of the parameters could be set at a near optimal level, while the length and height of the fins were the predominant parameters in meeting weight, volume, and acceptable fluid power targets.

In order to compare the design to the DOE targets for weight (specific power) and volume (power density), several assumptions must be made about the other components of the inverter in addition to the fin heat exchanger. The casing for the assembly was scaled with the fin block. ORNL provided several metrics for other components. The capacitor was assumed to be 1.62 kg and 1.13 L. The gate driver and control board were assumed to be 0.42 kg and 0.88 L. These values are typical or conservative. A 9x1 array of modules (Figure V-21) is examined with the substrate for this model being based on direct-bond copper (DBC).
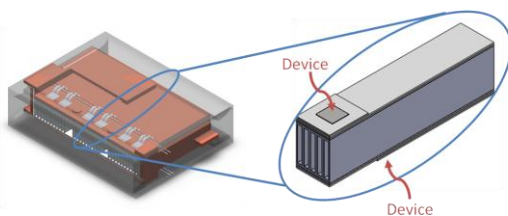
Figure V-20: CFD model domain for fin optimization.
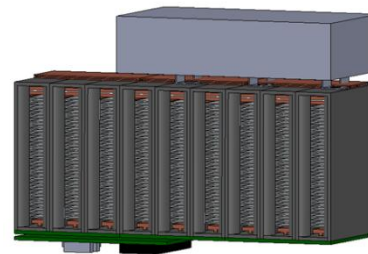
Figure V-21: Illustration of inverter assembly for 9x1 arrangement.

Using the same width as the baseline as well as fin thickness and channel width, the length and height of the fins were parametrically examined. Combining the weight and volume data with the other module components a map of designs can be shown. Figure V-22 shows the normalized fluid power (fluid power of the new design normalized by the fluid power of the baseline) versus the specific power for fin heights (h) from 15 to 24 mm and fin lengths (l) of 30 to 60 mm. The 2015 and 2020 targets are also illustrated. Figure V-23 shows the same map for power density.
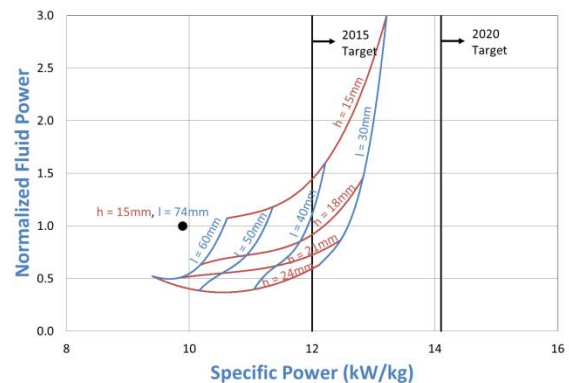
Figure V-22: Optimized geometries with varying fin heights and lengths compared to baseline (black circle) and DOE's specific power technical targets for power electronics, 175°C junction temperature, 9x1 array, DBC, 25 W per device.
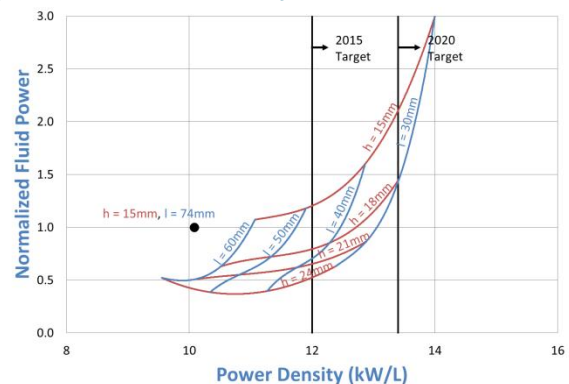
Figure V-23: Optimized geometries with varying fin heights and lengths compared to baseline (black circle) and DOE's power density technical targets for power electronics, 175°C junction temperature, 9x1 array, DBC, 25 W per device.

For both specific power and power density metrics, designs that were shorter in length (air flow direction) and taller in height were generally more favorable. Shorter fins reduced weight and volume, allowing the design to meet future targets. Increasing the height dropped the module fluid power.

In both cases, the contours become steeper, moving to the right. This indicates that there is a finite amount of material and volume that can be removed from the heat exchanger. To continue to improve the specific power and power density, improvements in other component weight and volumes must also be achieved. Figure V-24, for example, shows the breakdown of the component weights. 2015 targets are met with the reduced weight of the heat exchanger assembly, but it becomes increasingly difficult to attain 2020 targets by reducing heat exchanger weight only. The same holds true for volume as well.
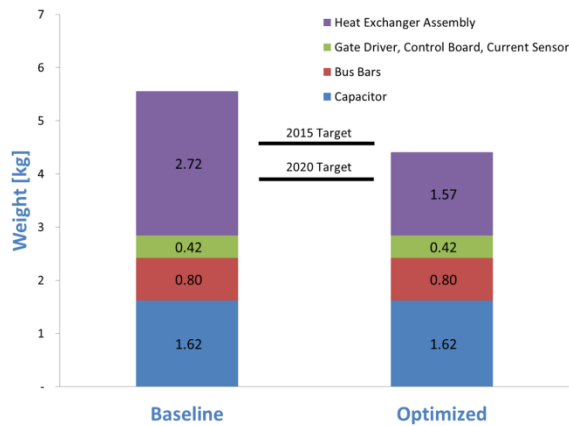
Figure V-24: Modeled inverter weight breakdown by major components.

Temperature contours of the sub-modules show the heat distribution of the devices to the aluminum fin block, as seen in Figure V-25. The optimized fin block has a more symmetrical temperature gradient, indicating that the fins are efficient and maximizing the conduction through the solid as the air convects the heat out of the fin block.

A full module model was created for the baseline design to compare to the sub-module with symmetry design. The agreement between the two is fairly close, with some slight end effect variations, as seen in Figure V-26. Note that Figure V-25 has a device heat generation of 25 W per device whereas Figure V-26 is for 30 W per device due to a different simulation being run.
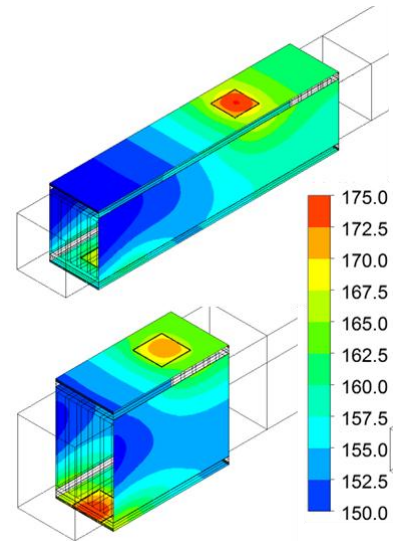
Figure V-25: Temperature contours of baseline (top) and optimized (bottom) geometries [°C] for junction temperature of 175°C, direct-bond aluminum (DBA) substrate, 25 W per device.
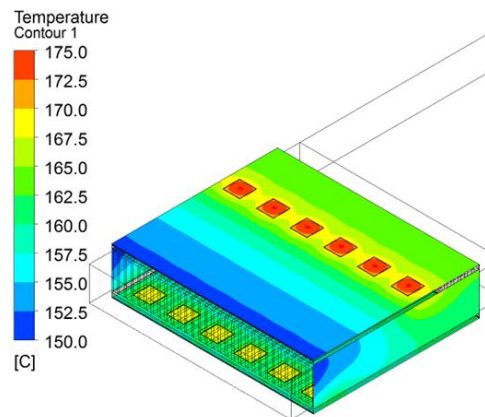
Figure V-26: Full module baseline model temperature contours, 175°C junction temperature, 9x1 array, DBA, 30 W per device.

Figure V-27 shows the predicted performance of a 9x1 arrangement with 175°C junction temperature in more detail for an optimized geometry with a fin height of 21 mm and fin length of 30 mm. The intersection of the fan curve and the predicted 9x1 inverter pressure loss results in a 0.054 m³/s (115 CFM) flow rate. The heat dissipation at this flow rate is approximately 3.2 kW, exceeding the conservative 2.7 kW target.

Although the module may be optimized for thermal performance compared to the baseline, which is somewhat arbitrary, it is more beneficial to examine the module thermal performance in the context of the entire system.
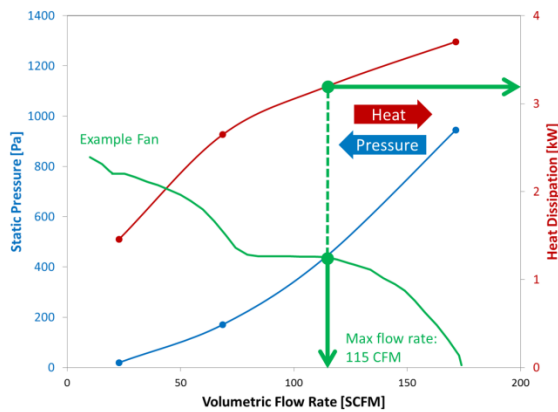
Figure V-27: Pressure loss and heat dissipation for optimized fin geometry operating at a 175°C junction temperature.

System Performance Optimization

Previous work measured the pressure loss of various production ducts using the system level test bench (Figure V-28). Two of the ducts are combined to estimate the inlet and outlet ducting from the inverter as a surrogate for the ducting system required.

The fluid power required for various flow rates is generally much higher for the ducting than it is for the air-cooling heat exchanger. Therefore, a system-level analysis is needed to draw conclusions about the optimized design. It may be that the heat exchanger is optimized to minimize fluid power on the inverter level due to a high flow rate and low pressure drop across the fins, but for the system level, this would cause a higher overall fluid power requirement. In general, for the system, a lower flow rate is desired because the pressure drop across the ducting rises as the square of the flow velocity.
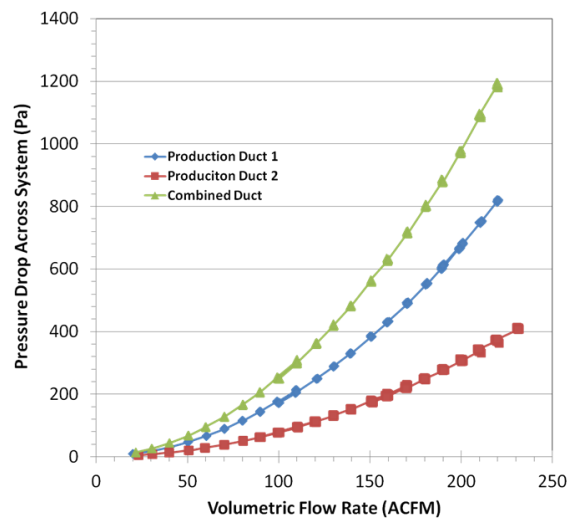
Figure V-28: Pressure loss of production ducts.

A similar parametric study using DBA substrates was conducted. The differences between using DBA and DBC substrates is small, and the overall conclusions based on geometry optimization are consistent.

Fin geometries with heights of 18 mm to 27 mm and fin lengths of 30 to 60 mm were examined with heat generation rates of 25 W per device (9x1 array of modules [see Figure 10]) and 45 W per device (6x1 array of modules) with DBA substrates and a maximum junction temperature of 175°C. The sub-module had a fixed width of 15 mm (same as the baseline design) and five channels (fin thickness of 1 mm, channel width of 2 mm).

Figure V-29 shows the map of results for the 9x1 array of modules. The scale is maintained for direct comparison with the 6x1 array, Figure V-30. For reference, the value for the baseline design is shown.
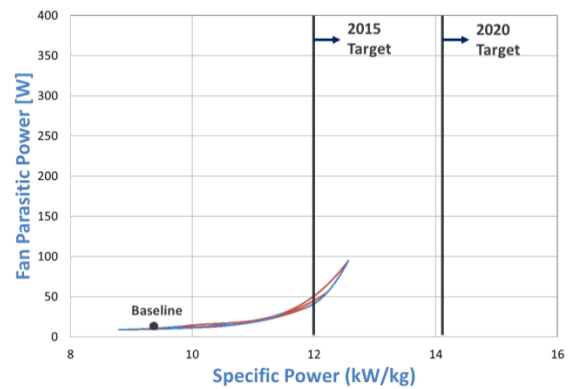
Figure V-29. Specific power and fan parasitic power for 9x1 array of modules, 175°C junction temperature, DBA, 25 W per device.
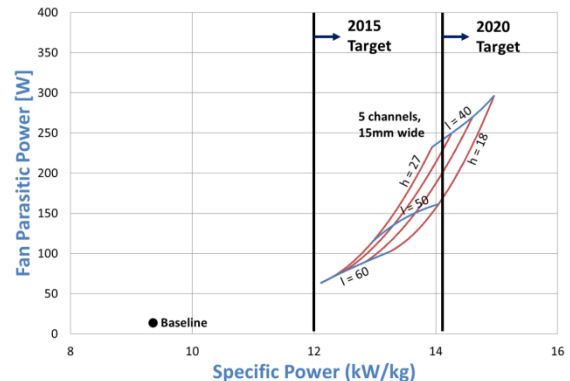
Figure V-30: Specific power and fan parasitic power for 6x1 array of modules, 175°C junction temperature, DBA, 45 W per device, five channels per device pair (top and bottom devices).

When using a system-level analysis to achieve weight and volume targets (Figure V-31), the fins tend to need to be shorter in height. By making the fin block shorter in length, the specific power and power density increase for the same fin height, but a penalty is paid with an increased fluid power requirement. For just the module, optimization indicated that the fin block should be taller in height and shorter in length. On this system level, it is more advantageous to allow for a higher pressure drop across the module while decreasing the flow rate so that the fluid power requirement of the ducting is limited as much as possible while still being able to dissipate the heat requirement.
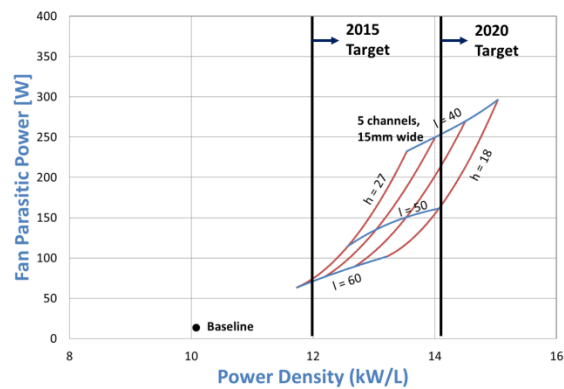
Figure V-31: Power density and fan parasitic power for 6x1 array of modules, 175°C junction temperature, DBA, 45 W per device, five channels per device pair (top and bottom devices).

Although there are no technical targets for the coefficient of performance or parasitic power, this metric should be examined for market acceptability. For comparison, a typical vehicle air-conditioning blower or condenser pulls about 50 W of power at steady-state conditions and 150 W of power under peak loads.

By expanding the design space but still using a simple rectangular channel design, further potential designs are found. Variations of channel width, fin thickness, number of channels per top and bottom devices (the sub-module modeled) while maintaining the 175°C junction temperature and 45 W per device heat generation were examined, with a few potential promising designs. For example, a sub-module design with 10 channels instead of 5, which also makes the whole module wider, yields parasitic power below 50–75 W, while attaining around 13 kW/kg specific power.

The thermal design must remove the amount of heat targeted within the constraints given, but the electrical design must also fit on the heat exchanger footprint. Additional constraints are being iterated on in discussions with ORNL, especially minimum footprint and spacing requirements for the devices. Although a thermal design may be optimal for heat removal, it must also work for the electrical topology. Conversely, the electrical design must be such that a heat exchanger can be designed to remove the heat while meeting the weight and volume targets.

The heat exchanger approach has been to keep the design relatively simple so that it may be easily manufactured. The current design of rectangular channels is conducive to extrusion techniques. Extruding aluminum is also advantageous over casting because aluminum with higher thermal conductivity may be used. In addition to meeting the thermal requirements, the design may be optimized for manufacturability to reduce costs.

Experimental design validation

The air cooling technology characterization platform test section was updated for a two heater-fin test section, as seen in Figure V-32. Figure V-33 shows the test section. The tabs on the side are for experimental assembly purposes. Results will be used to validate and update the models.

Figure V-32: Test section for testing baseline aluminum fins with two heaters for model validation; pressure calibration testing shown. (Photo Credit: Scot Waye, NREL).

Figure V-33: Baseline aluminum fin block sub-module test section.

Conclusions and Future Directions

- A heat exchanger design based on nine modules may attain 2015 targets, but the dimensions may be prohibitive for the electrical design. The six-module solution, even though the heat generated and dissipated is higher, appears to be more promising to reach 2015 as well as 2020 targets.
- A system-level analysis is critical to the thermal design so the heat exchanger design rejects the heat while maintaining a maximum junction temperature and meets weight and volume targets without requiring excessive parasitic power to drive the flow.
- The thermal design must also consider the electrical topology for allowance of all the required components and spacing as well as the ability to manufacture it at an acceptable cost.

Future work includes:

- Prototype and test optimized and advanced fin designs. Improve models based on test results. Down select best design for prototype module.
- Test balance-of-system components (fans and ducting). Incorporate results into system-level model. Develop initial high-temperature air-cooled inverter balance-of-system design. Demonstrate operation of thermal system design.

- Test optimized module design for thermal performance and in combination with high-temperature electronics from ORNL. Results will feed into improved design and future high-temperature air-cooled inverter demonstration with ORNL.

FY 2013 Patents/Publications/Presentations

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2. Bennion, K., Lustbader, J. U.S. Patent. "Integrated three-dimensional module heat exchanger for power electronics cooling." Number U.S. 8541875, September 24, 2013.

3. Lustbader, J. "Air Cooling Technology for Power Electronics Thermal Control." Presentation, DOE Annual Merit Review; May 13–15, 2013. Arlington VA.

Acknowledgments

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V.3.   Reliability of Bonded Interfaces

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Start Date: FY10
Projected End Date: FY13

Objectives

- Investigate and improve the thermal performance and reliability of emerging bonded interface materials for power electronics packaging applications.
- Identify failure modes in emerging bonded interface materials, experimentally characterize their lives under known conditions, and develop lifetime estimation models.

Technical Barriers

In automotive power electronics packages, conventional thermal interface materials such as greases, gels, and phase-change materials pose bottlenecks to heat removal and are also associated with reliability concerns. The industry trend is toward high thermal performance bonded interfaces. However, because of coefficient of thermal expansion mismatches between materials/layers and resultant thermomechanical stresses, adhesive and cohesive fractures could occur, posing a reliability problem. These defects manifest themselves in increased thermal resistance.

Technical Targets

Improved package reliability is an enabler to achieve the U.S. Department of Energy (DOE) Advanced Power Electronics and Electric Motors (APEEM) Program power electronics targets for improved efficiency, performance, and lifetime.

Accomplishments

We present results for thermal performance and reliability of bonded interfaces based on thermoplastic (polyamide)

adhesive, with embedded near-vertical aligned carbon fibers, as well as sintered silver material. The results for these two materials are compared to conventional lead-based ($Sn_{63}Pb_{37}$) bonded interfaces. These materials were bonded between 50.8-mm × 50.8-mm cross-sectional footprint silicon nitride substrates and Cu base plate samples. Samples of the substrate/base plate bonded assembly underwent thermal cycling from –40°C to 150°C according to Joint Electron Devices Engineering Council standard Number 22-A104D for up to 2,500 cycles. The dwell time of the cycle was 10 minutes, and the ramp rate was 5°C/minute. Damage was monitored every 100 cycles by acoustic microscopy as an indicator of an increase in thermal resistance of the interface layer. The acoustic microscopic images of the bonded interfaces after 2,500 thermal cycles showed that thermoplastics with embedded carbon fibers performed quite well with no defects, whereas interface delamination occurred in the case of the sintered silver material. Both these materials showed a superior bond quality compared to the $Sn_{63}Pb_{37}$ solder interface after 1,500 thermal cycles. The delamination percentage was calculated and compared between the three interface materials. Strain energy density values of $Sn_{63}Pb_{37}$ solder were obtained as an output from ANSYS simulations for lifetime estimation of the interface material.

✧   ✧   ✧   ✧   ✧

Introduction

In a power electronics module, a semiconductor chip/die is typically attached by a bonded interface material (BIM) such as solder to a metalized substrate. The substrate is composed of a ceramic bounded by Cu layers on either side and provides electrical isolation. This substrate is then mounted onto a base plate or directly to a heat exchanger, typically made of Cu or Al, via another BIM. A cross-section of a typical power electronics package is shown in Figure V-34.
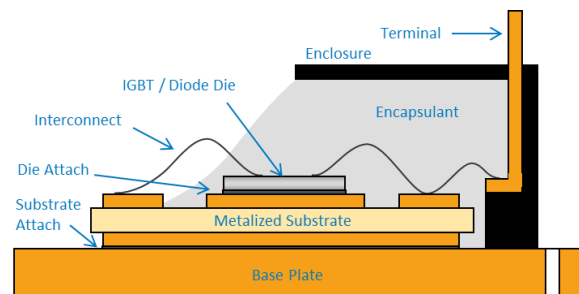
Figure V-34: Traditional power electronics package.

A coefficient of thermal expansion (CTE) mismatch between the ceramic substrate and the Cu base plate can cause defect initiation and propagation in the joining solder layer. Lead-based solders had predominantly been used in the electronics packaging industry; however, the Restriction of Hazardous Substances Directive [1] mandated lead-free solutions. Initially, the industry focused on various Sn, Ag, and

Cu (SAC) compositions as a suitable lead-free alternative, with Innolot ($SnAg_{3.8}Cu_{0.7}Bi_{3.0}Sb_{1.4}Ni_{0.2}$) proving to be a promising solution [2–3]. Research found that varying the composition of the Ag and Cu content in the SAC solders would help minimize creep strain. Overall, reliability under temperature cycling continues to be a concern with lead-free solders. To provide greater thermomechanical reliability under temperature cycling and to allow for higher temperature applications, sintered silver material has also emerged as a promising bonding solution in power electronics packages [4–5]. However, to reduce synthesis temperatures to below 300°C, up to 40 MPa of pressure must be applied to the package, causing a higher complexity in the production process and more stringent flatness specifications for the substrates. Hence, alternative bonding techniques are being developed to increase the thermomechanical reliability of this interface through the use of newer materials, such as thermoplastics with embedded micrometer-sized carbon fibers. Little information is available on the thermal performance and reliability of large-area attaches based on the more recently developed thermoplastic materials.

Prior work at the National Renewable Energy Laboratory (NREL) [6–7] focused on establishing a consistent and high-accuracy database, via the American Society for Testing and Materials steady-state approach [8], on the thermal performance of conventional as well as emerging thermal interface materials (TIMs). The conventional materials included greases, gels, phase-change materials, and filler pads. It was concluded that the tested conventional materials could not meet the thermal performance target of 5-mm^2K/W thermal resistance for a 100-μm bond line thickness. For a number of power electronics packaging stack-ups, the TIM stops being a bottleneck to heat removal when its resistance is on the order of 5 mm^2K/W; thus, it is a target. In addition, practical power electronics packaging configurations and manufacturing constraints dictate that the TIM has to fill gaps on the order of 100 μm.

Because BIMs are promising [9–13], work at NREL has focused on assessing their thermal performance and reliability. Conclusions on thermal performance and reliability from the present effort are intended to directly assist incorporation of these materials into automotive power electronics designs. This report focuses on thermoplastic (polyamide) adhesive with embedded near-vertical–aligned carbon fibers (8- to 10-μm diameter), sintered silver based on micrometer-sized Ag particles, and $Sn_{63}Pb_{37}$ solder as a baseline. The sample synthesis, characterization plan, and results are described below.

Approach

Materials and Sample Synthesis

The assembly consists of a 5-mm-thick Cu base plate attached to a 0.72-mm-thick active metal bonded substrate (0.32-mm-thick silicon nitride [Si_3N_4] with 0.2-mm-thick Cu foil on either side of Si_3N_4, 50.8 mm × 50.8 mm cross-sectional area footprint) via the bonding material. Before assembly, the Cu metallization layers in the substrate were plated with 4 μm

of electroless Ni-P, 1 μm of Pd, and 0.3 μm of Ag to improve adhesion with the bonding material. The Cu base plate was electroplated with 5 μm of Ag. An assembled sample is shown in Figure V-35.
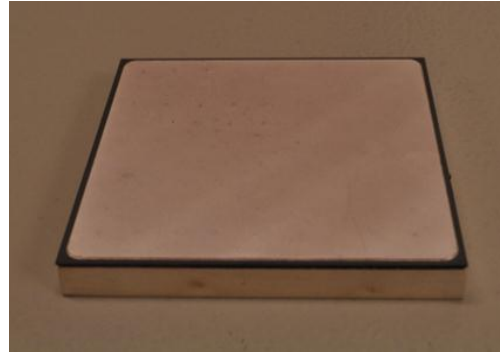
Figure V-35: Representative metalized substrate/base plate assembly.

A tabletop hot press was developed for synthesizing test samples requiring both temperature and pressure bonding parameters. Two hot plates were positioned, one on either side of the sample to be bonded, and were embedded with five 250-W cartridge heaters. Three heaters were inserted in the top hot plate and two in the bottom hot plate. A temperature controller adjusted the power of the heaters based on the temperature measurement by a thermocouple located in the bottom hot plate. The test sample and hot plates were placed between layers of mica and cold plates, and then inserted into an arbor press [14]. Glycol-water (50%–50% mixture by volume) coolant was circulated within the cold plates to isolate the high bonding temperatures from the hydraulic piston and the fluid. A screw jack was also placed between the hydraulic piston and top cold plate to provide fine adjustment to the applied bonding pressure. The pressure of the hydraulic fluid was electronically monitored to determine the force applied to the sample under bonding.

The HM-2 material, manufactured by Btech Corporation, is a composite structure consisting of 8- to 10-μm-diameter carbon fibers embedded in a polyamide/thermoplastic adhesive at approximately 40% fill factor by volume. The HM-2 was placed between the substrate/base plate assembly and subjected to a pressure of 689.5 kPa and a temperature of 190°C. Once the temperature was reached, the assembly was allowed to cool to room temperature while the pressure was maintained.

Bonded interfaces based on sintered silver particles were synthesized by Semikron. Corners of the Si_3N_4 substrate were rounded off to match the 2-mm radius of the Cu layers. The sample assembly was placed in a hot press and raised to its processing temperature, after which pressure was applied.

As a baseline, a $Sn_{63}Pb_{37}$ bond was also synthesized between the substrate/base plate assembly. A 127-μm-thick stainless steel stencil with 9-mm × 9-mm square openings and 1-mm separation was used to apply solder evenly to the substrate and base plate surfaces. After the solder was applied, the assembled sample was placed in a vacuum solder reflow oven. The reflow profile ensured that

flux was removed from the bond and that voiding remained less than 2%.

Initial BIM Characterization

Degradation (e.g., cracks, voids, and delaminations) of the bonded interface can be non-destructively detected by acoustic microscopy. After defect initiation, the thermal and electrical performance of the sample assembly degrades. A C-mode acoustic microscope (C-SAM) emits ultrasound waves with frequencies ranging from 5 MHz to 400 MHz into a sample suspended in water. The strength of the signal reflected back to the microscope's transducer from an interface within a sample depends on the relationship between the acoustic impedances of the two materials forming the interface. A crack, void, or delamination will create a solid-to-air interface, which will cause a strong reflection to be detected by the microscope's transducer. Samples were measured for their initial bonding condition and then subsequently tested every 100 thermal cycles. Images showing the bonded interface within samples before accelerated thermal testing are shown in Figure V-36. The circular bands visible in each sample are artifacts of the C-SAM representing top surface curvatures as 2-D images and are not indicators of bond quality. The $Sn_{63}Pb_{37}$ solder, Btech HM-2, and sintered silver all exhibited uniform bonds between the base plate and substrate samples.
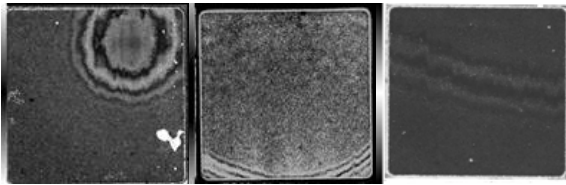
Figure V-36: C-SAM images showing initial bond quality in $Sn_{63}Pb_{37}$ solder (left), sintered silver (center), and Btech HM-2 (right) (Photo credit: Doug DeVoto, NREL).

In addition to acoustic microscopy, the electrical resistance of the Si_3N_4 insulation layer was measured. In a high potential (hipot) test, a high voltage is applied to an electronic device's current-carrying components. The quality of the insulation in the device is determined by measuring the presence of a leakage current. Leakage current indicates that dielectric breakdown in the insulation layer has occurred [15]. A dielectric resistance tester was previously constructed based on the hipot testing process to detect when a crack in the Si_3N_4 has developed. A custom fixture contacts the top and bottom sides of a test sample, and a test voltage of 2.0 kV is applied for 20 seconds, which is sufficient voltage to cause an arc in the air through a defect or crack in the 0.32-mm-thick Si_3N_4 layer. Measurement of the leakage current from an arc indicates that damage occurred within the Si_3N_4 layer in the sample. The sample successfully passes the test if no current was measured over the analysis period. The results correlated with acoustic microscopy images, indicating that all initial samples exhibited no defects within the Si_3N_4 layer.

CTE mismatches within the samples cause package deformation and stresses to build up in the Si_3N_4 layer during the cooldown from the synthesis temperature to room temperature. These stresses can be sufficient to cause crack

initiation and propagation within the Si_3N_4, leading to failure of the layer's electrical insulating properties. Representative CTE parameters for materials common within a power electronics package and examples of package deformation conditions are shown in Figure V-37. As a package cools from a stress-free temperature, the Cu base plate's higher CTE relative to the substrate and silicon die causes it to contract more and induce a bow into the package. Heating will conversely cause the base plate to expand more quickly than the rest of the package and create a bow in the opposite direction.
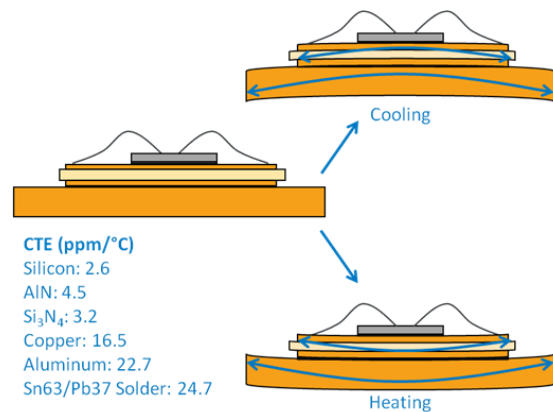
Figure V-37: Power electronics package deformation caused by CTE mismatch under cooling and heating conditions.

The high pressure and temperature synthesis requirements for sintered silver did not cause crack initiation within the Si_3N_4 substrate; however, package deformation was evident when samples were at room temperature. A laser profilometer was used to scan the top and bottom surfaces of sintered silver samples for accurate measurements of these deformations. Figure V-38 shows the top surface profile of one sintered silver sample as well as a cross-section profile between two of the sample's corners. The height variation across the sample was measured to be 166 µm. Surface profile measurements were also taken for $Sn_{63}Pb_{37}$ solder and thermoplastic samples, but no significant package deformations were found.
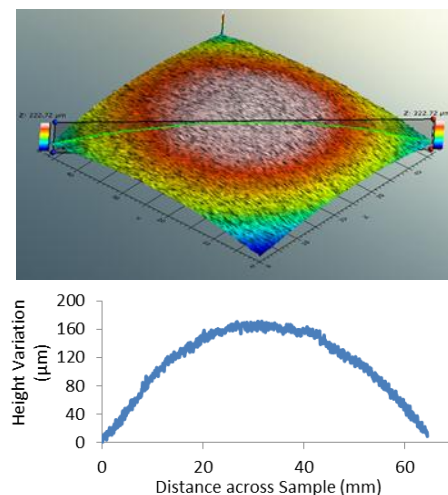
Figure V-38: Surface profile of sintered silver sample at room temperature.

Modeling of Strain Energy Density in $Sn_{63}Pb_{37}$ Solder

The BIM reliability modeling approach involves first calculating the accumulated viscoplastic strain energy density per cycle using finite element analysis. Results are then implemented into a fatigue model to obtain a correlation of the strain energy density with experimentally determined number of thermal cycles to BIM failure. ANSYS Mechanical was selected for the finite element analysis because of its established accuracy in this field [16–20].

An ANSYS Parametric Design Language (APDL) code was developed that included model pre-processing, solver, and post-processing stages. The model geometry matched the experimental test sample geometry and consisted of a stackup of 50.8-mm × 50.8-mm cross-sectional area footprint composed of a Cu base plate, $Sn_{63}Pb_{37}$ solder BIM, and a Si_3N_4 substrate. A quarter symmetry of the package was utilized in the modeling to save computational space and time, shown in Figure V-39.
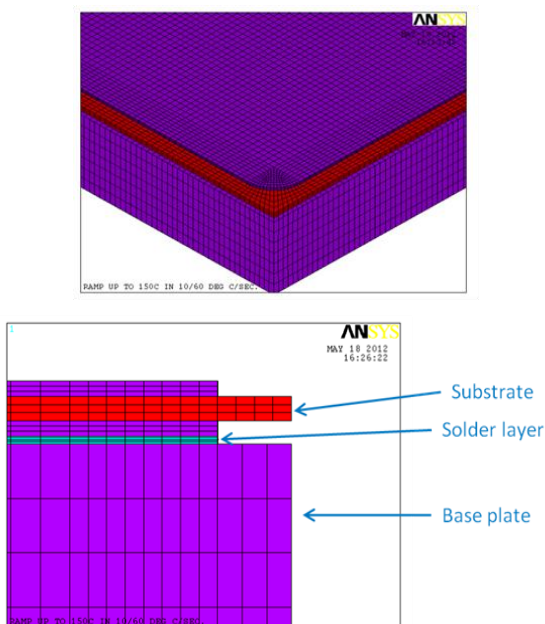
Figure V-39: Quarter symmetry model (top) and layers in the bonded assembly (bottom).

After the geometry was constructed, material properties were assigned to the various layers within the package. The Anand constitutive model was used to define the viscoplastic nature of the solder interface while temperature-dependent, elastic properties were applied to the base plate and substrate layers [21–22]. Nine parameters in the Anand model were obtained from published literature. Various mesh controls, including element sizing, edge sizing, and meshing technique, were then used to create a structured mesh that increased in density at the bonded interface layer. Furthermore, these controls ensured that no mesh mismatch occurred between the model layers. The model was then subjected to a cyclic temperature load with maximum and minimum temperatures of 150°C and –40°C, respectively, a ramp rate of 5°C/min, and a dwell time of 10 minutes. Four such cycles were simulated to study the plastic behavior of the solder interface.

The package design was modified to create a fillet at the corner region to reduce the maximum strain energy distribution. The fillet was created both for the solder layer and for the Cu metallization layers in the substrate. The geometry construction and the meshing sections of the APDL code were significantly modified to incorporate the fillet at the corner region. Separate control over the mesh in the fillet region was achieved in the modified code. This was important for minimizing computational time and mesh size, as mesh density could then be increased in the solder fillet region independently of the solder inner region. An appropriate element size was chosen after conducting a mesh independence study to achieve a balance between computational time and accuracy of the results. Model variations with a fillet radius of 1.5 mm and 2 mm were analyzed as the application of a fillet onto a substrate's metalized layers is a common technique to increase the reliability of the solder layer in the corner region.

Results

BIM Condition after Thermal Cycling

After initial characterization of the test samples, conditions must be applied to create thermally induced stresses, leading to cracking, voiding, or delamination failures. Generally, three types of thermal duty cycles can be used to create thermally induced stresses: a temperature cycle, a thermal shock cycle, and a power cycle. A temperature cycle specifies the temperatures to which a sample under test will be exposed, the durations of exposure, and the rate of temperature change when the sample under test is brought to a new temperature set point. A thermal shock cycle is similar to a temperature cycle, but consists of rapid changes in the ambient temperature. Finally, a power cycle is created by heat dissipation in an actual electronic device to create realistic heat flow patterns and temperature distributions in a sample under test. Because the lifetimes of samples are too long to be tested in real time, an accelerated temperature cycling test procedure is employed to bring testing times down to a reasonable duration.

Samples were cycled between –40°C and 150°C, a common temperature range for electronics testing, to evaluate the quality of the bonded interfaces [23–26]. A soak, or dwell, time of 10 minutes at the maximum and minimum temperatures was chosen to promote solder fatigue and creep [23]. Ramp rates for thermal cycling must be sufficiently low to avoid transient thermal gradients in the test samples; therefore, ramp rates were in the 5°C/min range. Each sample was cycled up to 2,500 thermal cycles, or until degradation propagated to sufficient levels to separate the substrate from the base plate. A failure is defined as a crack in the Si_3N_4 substrate, a cohesive fracture within the BIM, or an adhesive/interfacial fracture between the BIM and either the substrate or base plate surface. A crack in the Si_3N_4 substrate would indicate loss of electrical insulation capabilities and the sample would immediately be considered failed. Cohesive or adhesive/interfacial fractures in the BIM would increase the thermal resistance of the power electronics package,

eventually creating a thermal bottleneck that would elevate the operating temperature of a die above its maximum limit. For testing purposes, a fracture leading to 15% area delamination of the BIM is defined as a failure.

Thermoplastic HM-2 samples have undergone 2,500 temperature cycles and have shown no initiation of defects in the Si_3N_4 substrate or the BIM. Figure V-40 shows C-SAM images highlighting the corner regions of the Btech HM-2 interfaces after 1,000 temperature cycles, 1,500 cycles, and 2,500 cycles.
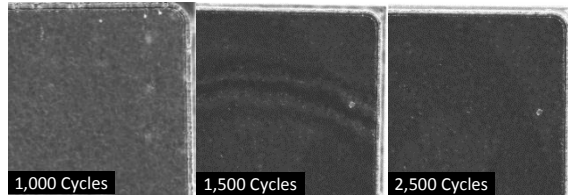
Figure V-40: C-SAM images of Btech HM-2 thermoplastic material after select number of thermal cycles. (Photo credit: Doug DeVoto and Paul Paret, NREL)

Sintered silver samples have also undergone 2,500 temperature cycles but have shown progressively increasing delamination of the BIM. This is observed in acoustic images of a corner region of the sintered silver material after 1,000 temperature cycles, 1,500 cycles, and 2,500 cycles, as shown in Figure V-41.
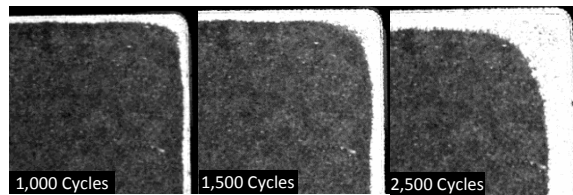
Figure V-41: C-SAM images of sintered silver material after select number of thermal cycles. (Photo credit: Doug DeVoto and Paul Paret, NREL)

Measurements of the delamination percentage within the sintered silver BIM were taken every 100 cycles from C-SAM imaging. Depending on the sample, this perimeter fracturing increased to 19%–32% of initial bonded area after undergoing 2,500 temperature cycles, as shown in Figure V-42. Under these specific bonding and temperature cycling conditions, the sintered silver samples remained defect free until approximately 300 cycles. A period of transient rate delamination occurred after defect initiation until approximately 1,000 cycles, after which a constant rate delamination was observed to the conclusion of temperature cycling at 2,500 cycles.
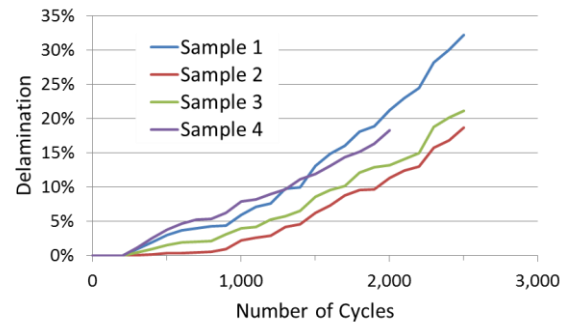
Figure V-42: Perimeter delamination of sintered silver BIM as a function of number of thermal cycles.

The fourth sample was cross-sectioned and the bonded interface layer was imaged after 2,000 temperature cycles. It was determined that the delamination observed in acoustic microscope images was the result of cohesive fracturing within the sintered silver material. The cohesive fracturing is shown in Figure V-43. After 2,500 cycles, additional cross-sectioning and imaging confirmed that cohesive fracturing occurred in the remaining three sintered silver samples.
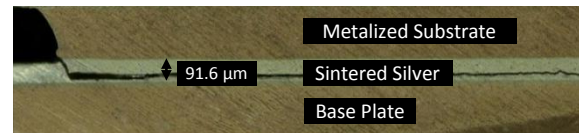
Figure V-43: Cohesive fracture within sintered silver BIM after 2,000 temperature cycles.

$Sn_{63}Pb_{37}$ solder samples have been subjected to 1,500 thermal cycles. C-SAM images show a higher amount of delamination, indicating a relatively poor performance of the BIM (Figure V-44).
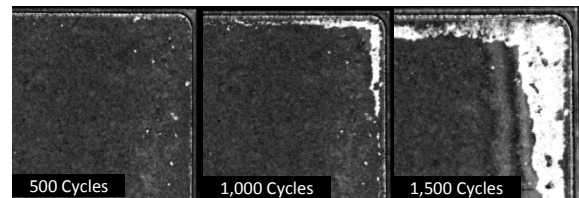
Figure V-44: C-SAM images of $Sn_{63}Pb_{37}$ solder material after select number of thermal cycles. (Photo credit: Doug DeVoto and Paul Paret, NREL)

The delamination percentage was calculated for the $Sn_{63}Pb_{37}$ solder material and compared with the other two interface materials. After 1,500 cycles, cohesive fracturing within the solder material reached 21%–24% delamination, and observed delamination rates were higher in the solder samples than in sintered silver or thermoplastic HM-2 samples. Delamination rates of all three interface materials are shown in Figure V-45.
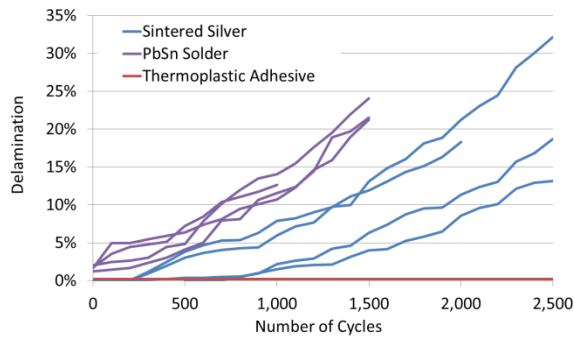
Figure V-45: Perimeter delamination of sintered silver, $Sn_{63}Pb_{37}$ solder, and thermoplastic adhesive as a function of number of thermal cycles.

Modeling Results

Figure V-46 shows the temperature profile and development of shear strain and shear stress within the solder interface's corner region as a function of time. Calculations of strain levels within the solder interface are critical to develop relationships with fatigue failures within the interface material. As the temperature ramps up from room temperature to 150°C, strain within the solder develops and reaches a maximum value at the end of the elevated dwell period. During the subsequent ramp down, the strain decreases and reaches the lowest level at the end of the low-dwell period. A similar pattern is also seen for shear stress, where the stress level first increases with temperature during the ramping up period. Stress relaxation is then observed during the last portion of ramping up and continues to relax through the elevated dwell period. Negative shear stress levels develop during ramp down and reach a minimum at the low dwell, where some stress relaxation is then observed. This model confirms that for $Sn_{63}Pb_{37}$ solder, creep effects accelerate at elevated temperatures.

Analysis of stress-strain hysteresis loops helps to understand the inelastic behavior exhibited by the interface and combines the effect of stress and strain into a single parameter: the strain energy density. On completion of a simulation, the node with the maximum equivalent strain was selected and its stress and strain values as a function of time were obtained through post-processing. Results indicated that the maximum strain energy distribution occurred at the solder's corner region, at the interfacial joint with the Cu base plate. The inelastic behavior of the solder joint under varying thermomechanical loads during a temperature cycle is illustrated in Figure V-47. The temperature cycle is segmented into four different cases, a high dwell at 150°C, a ramp down to –40°C, a low dwell at –40°C, and then a ramp up back to 150°C. Beginning at the 150°C high dwell, shear stress slightly decreases as shear strain increases, with creep strain playing a predominant role. The ramp down segment causes both stress and strain values to decrease until the low dwell at –40°C, at which point stress levels increase slightly while strain values continue to decrease. As the temperature increases during ramp up to 150°C, stress levels increase until approximately room temperature, at which point stress decreases and strain values begin to increase from temperature-dependent creep. At room temperature, the

homologous temperature of solder is more than 0.5 and hence stress relaxation begins to occur with the rise in temperature.
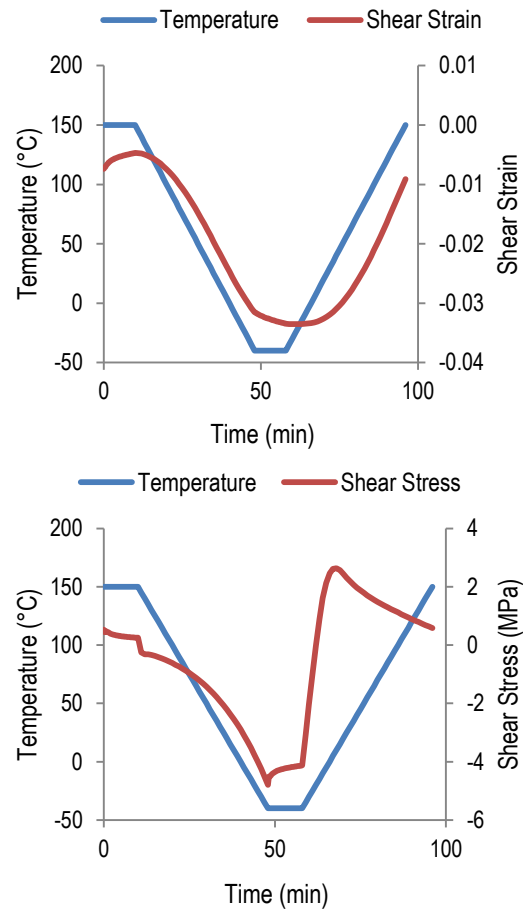
Figure V-46: Temperature and shear strain versus time (top) and temperature and shear stress versus time (bottom).
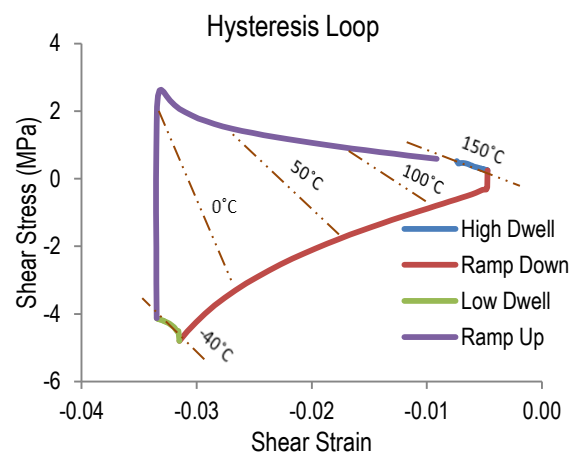
Figure V-47: Hysteresis loop from a solder interface's 2-mm fillet maximum equivalent strain node.

Figure V-48 shows a comparison of stress-strain values between solder interfaces with 1.5-mm and 2-mm fillet corners. Separate simulations were run to obtain the results. The figure shows that under the same temperature loading conditions, an equivalent amount of stress was induced but

the maximum shear strain values were reduced in the 2-mm fillet geometry.
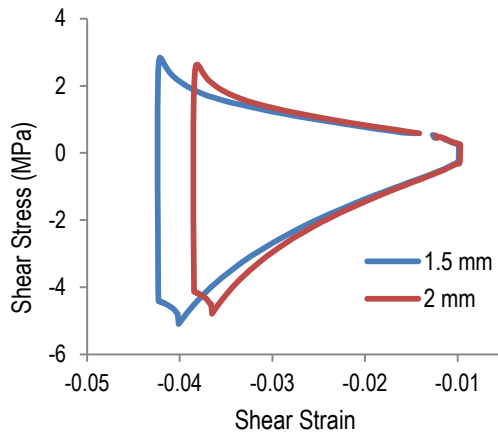
Figure V-48: Stress-strain comparison.

Energy stored in the solder interface region from deformation during the temperature loading conditions is referred to as the strain energy. The strain energy density is the strain energy per unit volume and is determined by calculating the area within the stress-strain hysteresis loop for a given temperature cycle. The strain energy density values calculated over the entire fillet regions for 1.5-mm and 2-mm fillet corners were 9.04 MPa and 8.91 MPa, respectively.
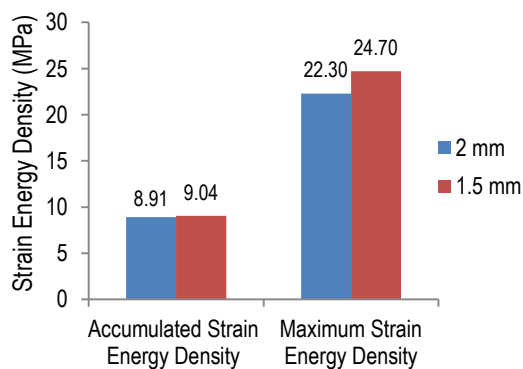
Figure V-49: Strain energy density values.

These strain energy density values will be correlated with an experimentally determined number of thermal cycles to failure for the $Sn_{63}Pb_{37}$ solder BIM.

Conclusions and Future Directions

A consistent framework has been implemented to establish the thermal performance and reliability of large-area bonded interfaces based on novel/emerging materials such as thermoplastics with embedded carbon fibers and sintered silver materials as compared to $Sn_{63}Pb_{37}$ solder. These large-area attachments are currently being considered in state-of-the-art power electronics packages for electric-drive vehicle applications. Results for bond quality after thermal cycling suggest that thermoplastics with embedded fibers could be a promising alternative to solders. Future work with sintered

silver material will focus on minimizing the occurrence of cohesive fracturing by optimizing processing conditions.

Modeling of strain energy density for the $Sn_{63}Pb_{37}$ solder BIM bonded between the metalized substrate and Cu base plate was performed using the Anand model parameters for the solder BIM from the literature. The results will be leveraged in the efforts to generate experimental cycles-to-failure versus strain energy density models for BIMs of interest.

FY 2013 Publications/Presentations

1. DeVoto, D., Paret, P., Narumanchi, S., and Mihalic, M., "Reliability of Bonded Interfaces for Automotive Power Electronics," InterPACK2013-73143, *Proceedings of the 2013 InterPACK Conference,* July 2013, Burlingame, CA (Outstanding Paper Award–Second Place, Mechanics).

2. DeVoto, D., Paret, P., and Mihalic, M., "Reliability of Bonded Interfaces," *2013 DOE Vehicle Technologies Office (VTO) Annual Merit Review,* Crystal City, VA, May 2013.

3. DeVoto, D., Paret, P., and Mihalic, M., "Reliability of Bonded Interfaces," *Presentation to the DOE Vehicle Technologies Office Electrical and Electronics Team,* Southfield, MI, April 2013.

4. DeVoto, D., Paret, P., and Mihalic, M., "Reliability of Bonded Interfaces," *Advanced Power Electronics and Electric Motors FY13 Kickoff Meeting, DOE VTO,* Oak Ridge, TN, November 2012.

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V.4. Reliability of Electrical Interconnects

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Start Date: FY11
Projected End Date: FY14

Objectives

- Investigate and improve the reliability of the ribbon bonds using Al and Cu/Al-clad ribbon materials.
- Develop predictive lifetime models for ribbon bonds that can be used to design components and packages.

Technical Barriers

In automotive power electronics modules, standard packaging technologies have limited the advancement of insulated gate bipolar transistor (IGBT)-based power modules toward designs that promise higher performance and reliability. Increased power densities and larger temperature swings reduce lifetimes for traditional wire bond interconnects. Wire bonds can be replaced with a transition to ribbon bonding technology. The ribbon bond process promises a reduction in bonding time, lower loop heights (and corresponding less heel fatigue), and higher current densities than wire bonds. However, as a newer technology, ribbon bond failure mechanisms are not well understood and thus do not have an accurate lifetime estimate.

Technical Targets

Improved package reliability is an enabler to achieve the U.S. Department of Energy (DOE) Advanced Power Electronics and Electric Motors (APEEM) power electronics targets for improved efficiency, performance, and lifetime.

Accomplishments

- Evaluated the initial strength of bonded wire and ribbon interconnects of various configurations.

- Completed temperature cycling and corrosion testing on wire and ribbon interconnects.
- Performed strength evaluation on wire and ribbon interconnects after accelerated testing.

✧   ✧   ✧   ✧   ✧

Introduction

The drive toward reduced cost, weight, and volume of components in electric drive vehicles has led to increased performance demands on power electronics modules. The trend toward higher power densities, current levels, and operating temperatures has shown that traditional packaging designs cannot meet the industry's reliability needs. Figure V-50 shows an example of a power electronics package with electrical interconnects (wire or ribbon bonds), die (IGBT or diode), metalized substrate, and base plate components.
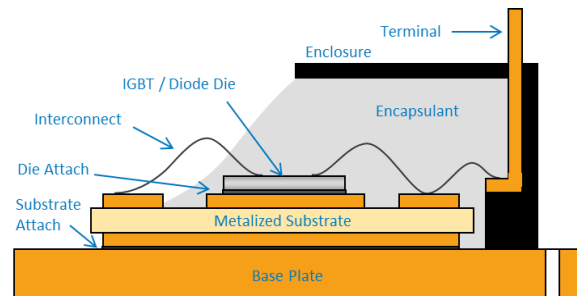
Figure V-50: Traditional power electronics package.

Wire bonding technology is used to electrically connect dies to each other, to the top metallization layer within the substrate, or to lead frames for connections outside of the power electronics package. Au, Cu, or Al has traditionally been used as the wire material, with each having tradeoffs in cost, current carrying capability, and mechanical strength [1]. For most common applications, Al has replaced Au and Cu because of its lower cost, but Cu is still selected for power module designs with high current requirements. In addition to material selection, the maximum current a wire can carry is dependent on its length and diameter; wire sizes are typically between 300 and 500 µm in diameter. If the maximum current level is exceeded, ohmic self-heating will cause the wire to fuse [2]. Heating from within the wire as well as from the silicon dies creates large temperature fluctuations during operation. These temperature variations and coefficient of thermal expansion (CTE) mismatches between the wire material and silicon dies or metalized substrates cause failures in the heel of the wire through flexure fatigue as well as bond pad lift-off. Analytical models have been developed for both failure modes to estimate the mean number of cycles to failure. Failure modes for wire and ribbon interconnects are shown in Figure V-51.
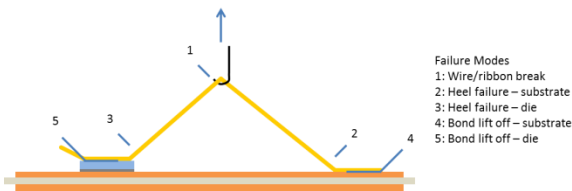
Figure V-51: Wire and ribbon interconnect failure modes.

For high-current power modules, mechanical limitations to bonding a wire with a diameter larger than 500 μm has required multiple wires to be bonded in parallel. Adding more parallel wires is limited by a substrate's bond pad area and increases the time and cost of bonding. These limitations have generated interest in replacing wire bonds with ribbon bonding technology. Three Al wire bonds with diameters of 400 μm can be replaced on an equivalent electrical current basis by one ribbon bond with a cross section of 2,000 μm × 200 μm [3]. The single ribbon requires a bond width of 2 mm; the three wire bonds require a width of 2.5 mm. Bonding times for both technologies remain the same (300 ms per bond); therefore, the ribbon bonding time for a package can be reduced. For the same span distance, a ribbon bond allows for a lower loop height than a wire bond. This helps to reduce heel stress and ultimately flexure fatigue. Minimizing heel stress is necessary as desired IGBT operating junction temperatures continue to rise to 175°C or higher [4]. However, because of the ribbon's larger geometry, higher bonding energies and forces are required and bond pad contact areas become larger. Damage initiated during the bonding process could be more likely under ribbon bonding, and CTE mismatches between the interconnect material and silicon devices or metalized substrate could cause failure under thermal cycling conditions.

The performance and reliability of conventional wire bonding are well understood; however, lifetime uncertainties of newer interconnect technologies remain barriers for those novel processes to be utilized by industry. The work at NREL focuses on providing a comprehensive reliability assessment of alternative interconnect technologies to wire bonds, beginning with ribbon bonding. Ribbon bonds are attached to a substrate under a variety of materials and geometries, and then subjected to accelerated test conditions that highlight the same failure mechanisms found under normal operating conditions. Ideas unique to ribbon bonding will be evaluated, first with the selection of a Cu/Al-clad ribbon that allows the Al to be easily bonded to silicon die surfaces while providing the improved electrical performance of Cu [5]. The ribbon's rectangular cross-section geometry makes twisting to create forced angles more difficult than with wire bonding; therefore, bonds with several forced angles will be attached to substrate samples [6]. The proposal to attach multiple ribbons over the same bond pad location will be explored as a stacked bonding technique [7]. In conjunction with accelerated testing, physics-of-failure models based on wire bond geometry will be validated for ribbon bonds.

Approach

Materials and Sample Synthesis

NREL has chosen several ribbon materials under various geometries for accelerated testing. The variations are as follows:

- Material–Al ribbon and a 2:1 ratio Cu/Al-clad ribbon.
- Ribbon cross-section–Two cross-sections suitable for current levels within a power module were chosen to be 2,000 μm × 200 μm and 1,000 μm × 100 μm.
- Ribbon span–10-mm and 20-mm spans were selected. Corresponding loop heights were set at a ratio of 1:2.2 to ribbon span.
- Number of stitches–Single and double stitches were bonded for 20-mm ribbon spans.
- Ribbon stacking–Stacking one ribbon pad above a second pad can minimize the bonding area on the top of a die but may create a weaker bond.
- Forced angle–Forcing a ribbon at various angles from its bond pad orientation would allow for offset pad locations, but may also create a weaker bond.
- Bond pad interfaces–One end of each ribbon will be bonded to a silicon die and the other end to a substrate's top Cu metalized surface.
- Bonding power–Two bonding powers were selected to evaluate the relationship between bond pad strength and long-term reliability.

The ribbon material and geometry variations cover a design space likely used within a power electronics unit if wire bonds were to be replaced with ribbon bonds. The ribbon bond variations are shown in Figure V-52.
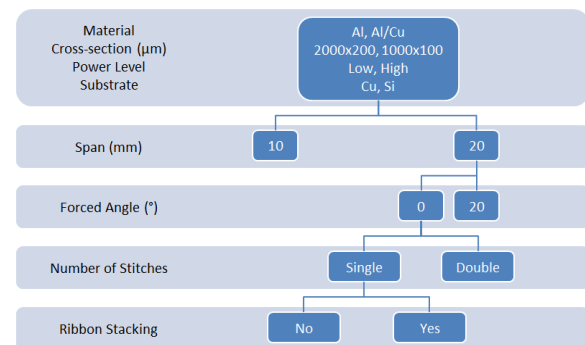
Figure V-52: Ribbon bond variations.

Three instances of each ribbon configuration were arranged on a 140-mm × 190-mm test substrate. The substrate was obtained from Curamik and is constructed of a 0.635-mm-thick alumina layer sandwiched between two 0.203-mm-thick Cu metallization layers. The design of the etch mask for the top Cu layer configures four ribbon bonds electrically in series with multiple parallel paths. This layout was chosen for power cycling samples, but remains the same for all samples. Before the ribbon material was attached to the test substrate, Vishay 5-mm × 5-mm Schottky diodes were soldered in place. The selected diodes have a breakdown voltage of 100 V and can reach a maximum junction temperature of 175°C. The diode backside has a Cr/Ni/Ag coating for good solderability;

the top side includes a 3-µm layer of Al (1% Si) to be compatible with the ultrasonic bonding process. Each test substrate was imaged by acoustic microscopy to ensure that the solder attachment for each diode contained minimal voiding. The first end of each ribbon interconnect was bonded to the top Cu metallization layer of the test substrate; the second was bonded to the top surface of the diode. Both Al- and Cu/Al-clad ribbon materials were obtained from Materion Technical Materials and were attached using an Orthodyne 3600 wedge bonder at Kulicke & Soffa. Dow Corning 3-4150 gel kits were used to protect the interconnects in silicone encapsulant. An example of a test substrate with a completed design layout is shown in Figure V-53.
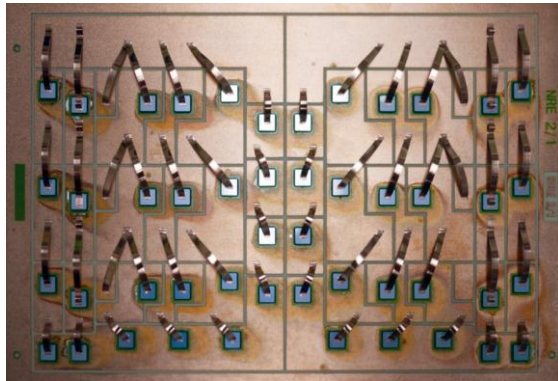
Figure V-53: Test substrate showing ribbon layout. (Photo credit: Doug DeVoto, NREL)

The four geometry variations (span, forced angle, number of stitches, and ribbon stacking) require eight ribbon interconnects; repeating each variation three times brings the total number of interconnects to 24, or one half of a test substrate. Including the additional ribbon selection variations (material, cross-section, and power level) requires a total of eight test substrate halves, or four test substrates. An additional half test substrate is added to include 500-µm-diameter Al wire bonds as a reference to the ribbon bonds. Thus, four and a half test substrates are required for each accelerated test condition.

Ribbon Bonding Mechanical Characterization

An XYZTEC Condor 100-3 mechanical bond tester was used to measure the pull strength of the ribbon and wire bonds. As this was a destructive evaluation, one set of test sample substrates without any prior accelerated testing was selected to measure initial bond strength through pull tests. Silicone encapsulant was removed prior to pull testing with Digesil NCX de-polymerization compound. For the pull test, a hook was first positioned under the ribbon bond. At the initiation of the test, a constant velocity of 250 µm/s was applied to the hook and maintained for a travel distance of approximately 4 mm. Sufficient force was used to maintain this velocity against the tensile strength of the ribbon material and strength of the bond pads. A test was completed when one of the five failure modes previously listed occurred, and the maximum force required for failure was recorded. This force was compared to minimum acceptable bond strengths as outlined in Method 2011.8 of the Department of Defense Test Method Standard 883H. The minimum acceptable pull force is

a function of the interconnect's cross-section, as shown in Figure V-54.
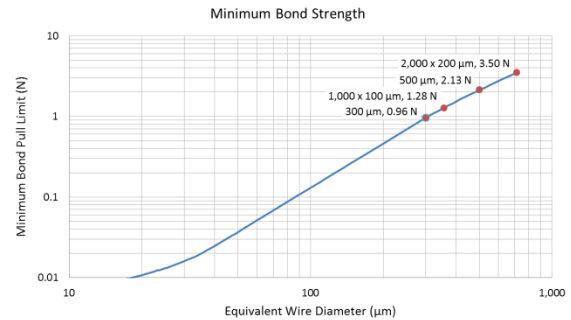
Figure V-54: Minimum wire and ribbon bond pull strength limits.

In addition to recording the maximum tensile force, the failure mode was documented. Images showing the most common modes are shown in Figure V-55.

Figure V-55: Failure modes from the left: wire break (left), heel failure from substrate (center), and bond lift-off from substrate (right). (Photo credit: Doug DeVoto, NREL)

Accelerated Testing

Subjecting a component to accelerated test conditions identifies its failure mechanisms in a shorter time relative to normal operating stress conditions. Various accelerated tests were selected to evaluate likely failure mechanisms within ribbon interconnects and are shown in Table V-4. These test procedures are based on standards for the microelectronics industry [8].

Table V-4: Accelerated Testing Procedures.

Accelerated Test	Testing Condition	Duration
Temperature Elevation	150°C	1,000 hours
	200°C	96 hours
	250°C	96 hours
Temperature Cycling	–40°C to 150°C, less than 20 s transition time	3,000 cycles
	–40°C to 200°C, less than 20 s transition time	3,000 cycles
Corrosion Testing	85°C, 85% relative humidity, cycled DC bias	1,000 hours
	121°C, 100% relative humidity	96 hour s
Power Cycling	–40°C to 125°C, 10 minute dwell, 10°C/min ramp rates, cycled DC bias	1,500 temperature cycles
Vibration Testing	Highly accelerated life test	Until interconnect fails

Accelerated test methods—humidity, thermal, power, vibration, or a combination of the four—are designed to highlight a particular interconnect's failure mode.

- Samples subjected to high-temperature storage testing will highlight thermally activated failure mechanisms. Ribbon bonds will be stored under three separate test conditions, at 175°C for 1,000 hours and at 200°C and 250°C for 96 hours.
- Alternating temperature extremes will test the ability of interconnects to withstand thermally induced mechanical stresses. Samples will be cycled either from –40°C to 150°C or –40°C to 200°C for 3,000 cycles. Transition times between temperature extremes will be completed in less than 20 seconds and no dwell/soak times will be held.
- Two humidity-based tests will evaluate the corrosion resistance of the ribbons and their bond pads. Under a humidity bias test, ribbon interconnects will be placed in an 85°C, 85% relative humidity environment for 1,000 hours. A DC bias will be applied during the test. Under a second humidity test, samples will be subjected to a 121°C, 100% relative humidity environment for 96 hours with no electrical bias. This is considered a destructive test.
- Under combined power and thermal cycling, interconnects will be subjected to a periodically applied operating bias while they experience high and low temperature extremes. Samples will be cycled from –40°C to 125°C for 1,500 cycles, with ramp rates of 5°C/minute and dwell/soak times of 10 minutes.
- Random six-degree-of-freedom vibration and rapid thermal cycling will stress the ribbon bonds beyond their design specifications to quickly highlight predominant failure mechanisms.

Two accelerated tests were completed for 500-µm-diameter Al wire and 1,000 µm × 100 µm ribbon. Their testing conditions and durations are outlined in Table V-5.

Table V-5: Completed Accelerated Tests.

Accelerated Test	Testing Condition	Duration
Temperature Elevation	200°C	144 hours
Corrosion	121°C, 100% relative humidity	144 hours

Results

Initial Results

Initial results from pull test data are shown in the following figures for Al wire, Cu/Al ribbon, and Al ribbon. The Al wire used has a cross-section of 500 µm; the ribbon interconnects have 1,000 µm × 100 µm cross-sections. The bonding power for ribbon interconnects is specified as either low or high. Three test bonds were completed for each bonding method, which includes defined interconnect material, geometry, and bonding parameters. The averages of these pull strength tests between Al wire, Cu/Al ribbon, and Al ribbon are shown in Figure V-56; error bars indicate the standard deviations between tests.
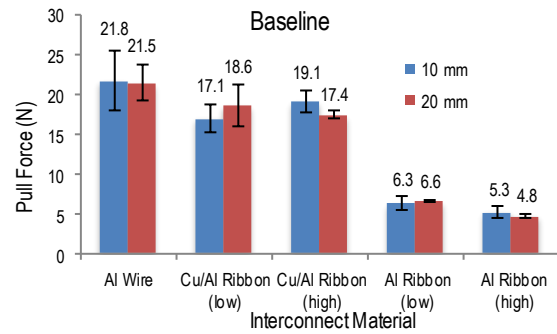
Figure V-56: Pull force versus interconnect material.

Al wire interconnects exhibited the greatest strength from the pull tests, closely followed by Cu/Al ribbons. The strength of Al ribbon bonds was noticeably lower, but still strong enough to be considered successful. The key aspect to monitor is if the bond strength for each respective interconnect material significantly decreases after accelerated tests. The failure modes associated with the above pull test measurements are shown in Figure V-57. The three interconnects tested for each bonding method typically failed by a similar method. Although bond strength remained approximately the same between low and high power bonds for Cu/Al ribbons, the failure method shifted from bond pad lift-offs to heel failures. This indicates that the lower power setting for Cu/Al ribbons may not be sufficient to adequately bond the Al side of the ribbon to the metalized substrate, but accelerated testing will highlight if the lower power setting ultimately ends in a bond with longer lifetime.
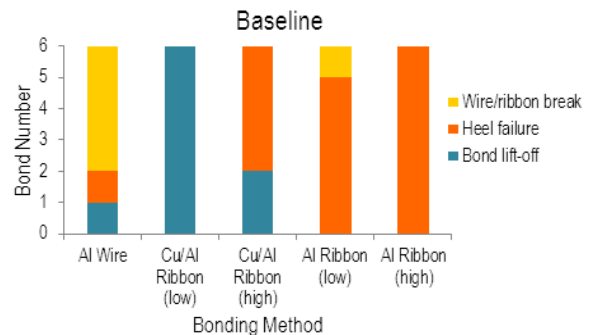
Figure V-57: Failure modes for interconnect materials.

A similar analysis of bond strength for Cu/Al ribbon interconnects at various forced angles was also completed. Results indicated that bond strength was reduced as a consequence of imparting a forced angle onto the ribbon bonds. The averages of these pull strength tests are shown in Figure V-58; error bars indicate the standard deviations between tests.
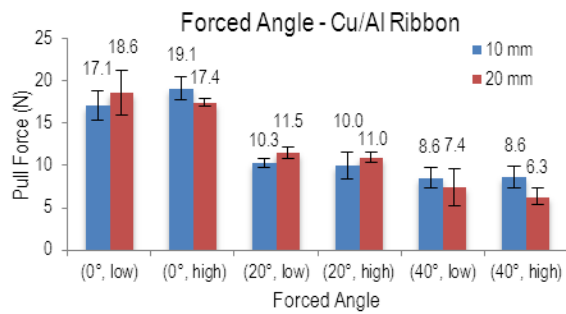
Figure V-58: Pull force versus forced angle of Cu/Al ribbon.

A forced angle analysis was also completed for Al ribbon bonds, as shown in Figure V-59. The bond strength is slightly reduced when incorporating forced angle geometries.
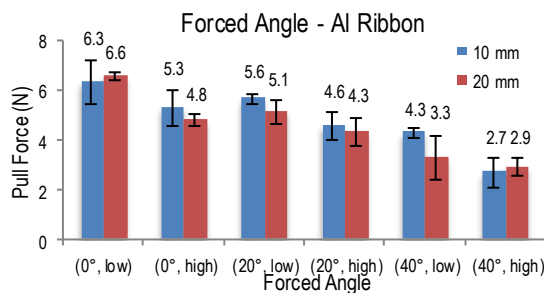
Figure V-59: Pull force versus forced angle of Al ribbon.

As previously apparent with Cu/Al ribbon bonds with no forced angle, increasing bonding forces shifted the failure methods from bond pad lift-offs to heel failures, as shown in Figure V-60.
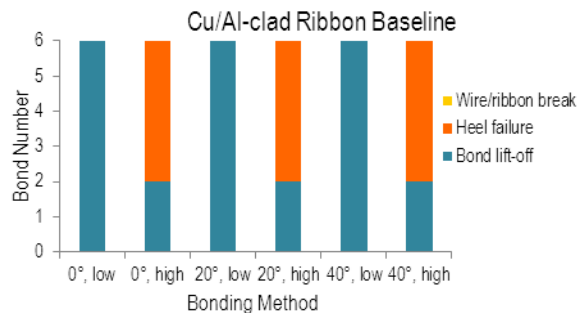
Figure V-60: Failure modes for Cu/Al ribbon at forced angles.

The failure modes for Al ribbon under forced angles were consistently heel failures on either the die or substrate side of the ribbon, shown in Figure V-61.
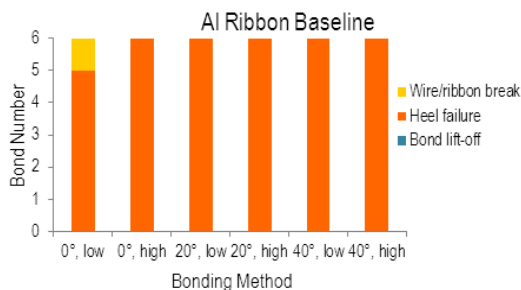
Figure V-61: Failure modes for Al ribbon at forced angles.

Mechanical tests are conducted on samples after they complete their designated accelerated testing procedure. In addition to mechanical evaluation, cross-sections of ribbon bond pads will provide a qualitative way to determine if the grain structure has changed after accelerated testing. Bonding of dissimilar metals between the ribbon and pad causes intermetallic formation and Kirkendall voiding under high-temperature storage tests. Visual analysis will also monitor signs of corrosion development.

Accelerated Test Results

Pull testing of the wire and ribbon interconnects after accelerated testing indicated various reductions in bond strength. The effects of temperature elevation and humidity testing reduced the bond strength of Al wire and Cu/Al ribbon interconnects, but strength levels were still above minimum acceptable values. Humidity testing of Al ribbon caused pull strength failures below acceptable strength levels outlined by MIL-STD-883H Method 2011.8. Results for 10-mm span and 20-mm span interconnects are shown in Figure V-62 and Figure V-63.
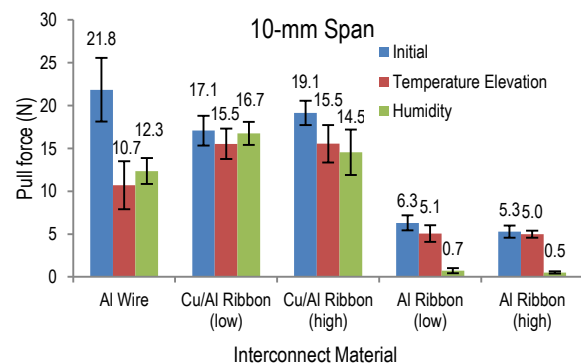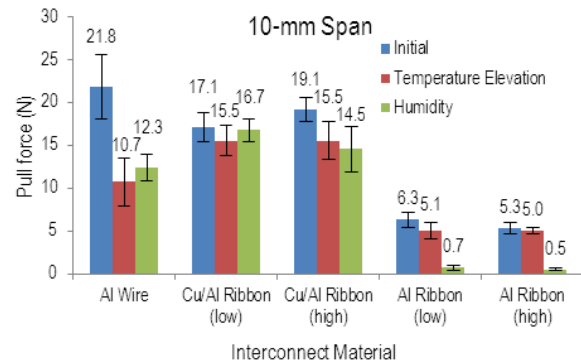
Figure V-62: Pull force versus 10-mm span interconnect material after accelerated tests.
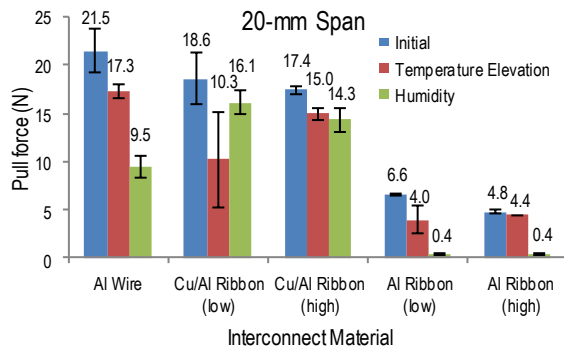
Figure V-63: Pull force versus 20-mm span interconnect material after accelerated tests.

Failure modes were recorded for each interconnect after accelerated testing. Temperature elevation testing resulted in Al wire breaks from the initial pull testing evaluation to shift to bond pad lift-off failures. Al and Cu/Al-clad ribbon failure modes remained the same. Temperature elevation testing failure mode results are shown in Figure V-64.
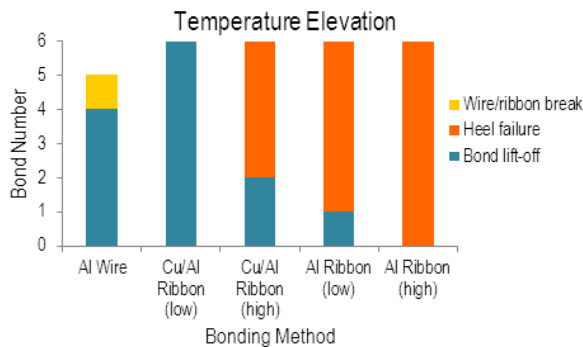
Figure V-64: Failure modes for interconnect materials after accelerated tests.

Corrosion testing resulted in Al wire breaks from the initial pull testing evaluation to shift to bond pad lift-off failures. Al ribbon heel failures from initial pull testing shifted to ribbon breaks, indicating that the low pull force results were caused by a decrease in the strength of the interconnect material itself. Cu/Al-clad ribbon failure modes remained the same. Corrosion testing failure mode results are shown in Figure V-65.
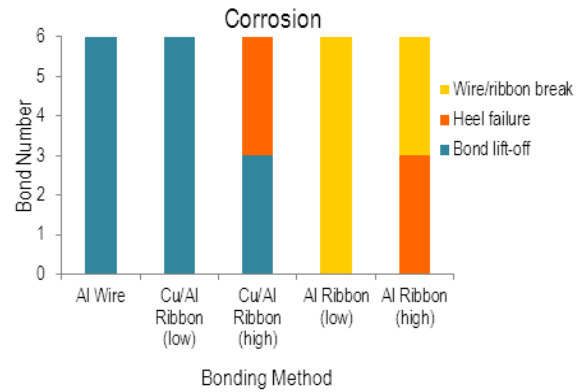
Figure V-65: Failure modes for interconnect materials after accelerated tests.

Physics of Failure Models

Under temperature cyclic loads, the CTE mismatch between the ribbon material and the silicon die or metalized substrate results in stress/strain reversals in the heel of the ribbon interconnect, gradually leading to its failure. Physics of failure models identify the root cause of this failure and then provide lifetime estimation based on material properties, geometry, and environmental conditions [9]. Using the theory of curved beams, the strain prediction on the upper side of the ribbon bond can be approximated using equation 1:

$$\varepsilon = \frac{r(\rho_f - \rho_i)}{\rho_i \rho_f} = r(k_i - k_f) \qquad (1)$$

where

ε is strain induced

r is half the thickness of the ribbon

ρ_f is the radius of curvature of the ribbon heel after heating

ρ_i is the radius of curvature of the ribbon heel before heating

k_f is the curvature at the heel of the ribbon after heating

k_i is the curvature at the heel of the ribbon before heating

This equation shows that the strain induced in the lower side ($[\rho_i / \rho_f]$+2r) will be lower compared to the strain in the upper side of the ribbon. Once the strain is calculated, the number of cycles to failure, N_f, can be determined using the Coffin-Manson equation:

$$N_f = C_\gamma \varepsilon^{-m_\gamma} \qquad (2)$$

where C_γ and m_γ are fatigue properties found through material tensile tests.

As the loop geometry plays a significant role in the prediction of strain values, the ribbon should be in a state of minimum potential energy. An energy-based cubic spline model is used to determine the geometry of the loop that achieves a minimum potential energy [9]. For a given span,

the loop height is varied to find the least energy state, by equation 3:

$$d = \frac{Dh}{H}\left[1 - \sqrt{1 - \frac{H}{h}}\right] \qquad (3)$$

where

d is half the span

h is loop height

D is the total span of the ribbon

H is the height offset between bond pads

This calculation was used to determine the least energy state for a ribbon interconnect to have a ratio of 1:2.2 loop height-to-span length.

A finite element analysis (FEA) model was developed to find the stress and strain values induced in an Al ribbon bond with a 10-mm span. The model geometry of a sample ribbon interconnect was created in SolidWorks and imported into ANSYS Workbench. A cross-section image of the sample ribbon was experimentally measured using a microscope to create a spline fit profile that could be imported into the FEA model. The plasticity model was specified as a multilinear kinematic hardening model to properly define the plastic behavior of the Al material, with stress-strain values at room temperature obtained from corresponding curves from literature [10]. A test case was run with a temperature cycle profile from 20°C to 160°C at a ramp rate of 5°C/min. A maximum deflection of 33.8 μm was observed at the center of the profile at the highest region. Maximum von Mises stress values of 193.9 MPa and 183.1 MPa were found to be at the heel for the first and second bond pads, respectively. The maximum deflection result from the model will be compared against experimentally obtained deflection results to validate the FEA model. The SolidWorks geometry and maximum von Mises stress are shown in Figure V-66.
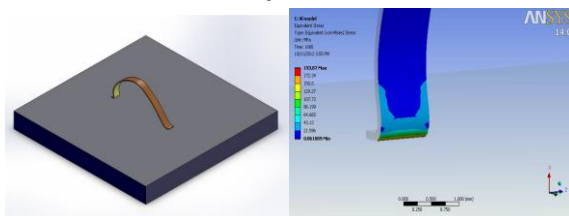
Figure V-66: FEA model of 1,000 μm × 100 μm Al ribbon with 10-mm span (left) and maximum stress shown at heel location near second bond pad (right).

Future modeling results will be improved by including temperature-dependent material properties for Cu and Al, and will be expanded to include Cu/Al-clad ribbon geometries. Deflection, von Mises stress, and strain results will be compared to the failure modes observed in the experimental accelerated tests. Analytical and FEA results will be incorporated into the Coffin-Manson relation to predict the number of cycles to failure, and validated with experimental test results for cycles to failure.

Conclusions and Future Directions

The work establishes the foundation for a comprehensive evaluation of the reliability of ribbon bond interconnects. To date, the impact of temperature elevation and humidity on the interconnects have been investigated. Some key findings were that temperature elevation and humidity testing reduced the bond strength of Al wire, Al ribbon, and Cu/Al ribbon, but the strength levels were still above minimum acceptable levels. Humidity testing of the Al ribbon caused pull strength failures below acceptable strength levels. When the interconnects were pull tested after accelerated testing, some interesting changes in the pattern of the failure modes were observed with respect to the modes of failure observed in pull testing prior to accelerated testing. A variety of materials and geometries will continue to be tested under various accelerated testing conditions to highlight failure mechanisms. Combining experimental results with time-to-failure models will enable reliability predictions for ribbon interconnects.

FY 2013 Publications/Presentations

1. DeVoto, D., Paret, P., and Mihalic, M., "Reliability of Electrical Interconnects–June 2013 Milestone Report," *FY2013 DOE milestone report,* June 2013.

2. DeVoto, D., Paret, P., and Mihalic, M., "Reliability of Electrical Interconnects," *Presentation to the DOE Vehicle Technologies Office (VTO) Electrical and Electronics Technical Team,* Southfield, MI, May 2013.

3. DeVoto, D., Paret, P., and Mihalic, M., "Reliability of Electrical Interconnects," *2013 DOE VTO Annual Merit Review,* Crystal City, VA, May 2013.

4. DeVoto, D., Paret, P., and Mihalic, M., "Reliability of Interconnects," *Advanced Power Electronics and Electric Motors FY13 Kickoff Meeting, DOE VTO,* Oak Ridge, TN, November 2012.

Acknowledgments

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V.5. Electric Motor Thermal Management

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Start Date: October 2009
End Date: September 2013

Objectives

With the push to reduce component volumes, lower costs, and reduce weight without sacrificing performance or reliability, the challenges associated with thermal management increase for power electronics and electric motors. Thermal management for electric motors will become more important as the automotive industry continues the transition to more electrically dominant vehicle propulsion systems. The transition to more electrically dominant propulsion systems leads to higher-power duty cycles for electric drive systems. Thermal constraints place significant limitations on how electric motors ultimately perform, and as thermal management improves, there will be a direct trade-off between motor performance, efficiency, cost, and the sizing of electric motors to operate within the thermal constraints (Figure V-67).
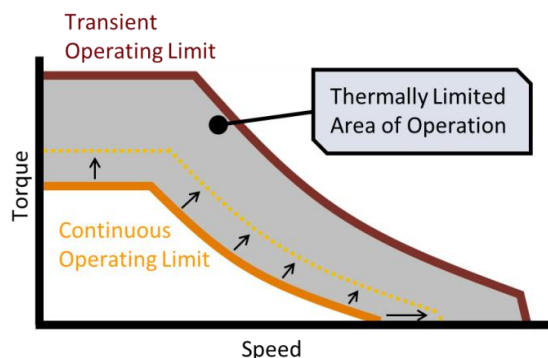
Figure V-67: Illustration of thermal management impact on motor performance as continuous power demands increase with higher electrical duty cycles.

The goal of this research project is to characterize the current state of thermal management technologies for electric traction-drive motors and quantify the impact of thermal management on the performance of electric motors. The ultimate goal is to identify areas for improvement and knowledge gaps that would benefit from additional research, leading to focused efforts within the identified areas. The research objectives are summarized as follows:

- Establish a foundation on which to evaluate potential improvements to electric motor thermal management
- Quantify opportunities for improving cooling technologies for electric motors
- Link thermal improvements to their impact on advanced power electronics and electric motor (APEEM) targets to prioritize future research
- Increase available information to support thermal management of electric motors in the public domain.

The focus for FY13 emphasized the final objective to increase the available information to support thermal management of electric motors. Past work highlighted potential areas where improvements in motor thermal management could impact motor performance [1], and during FY13, NREL's core thermal analysis and experimental capabilities were developed and applied to increase available data to improve the thermal design of electric motors. The work is on the path towards commercialization because the data and results have been used by industry and are necessary to improve motor designs.

Technical Barriers

The technical challenge of motor thermal management is summarized by Hendershot as "[h]eat transfer is as important as electromagnetic and mechanical design. The analysis of heat transfer and fluid flow in motors is actually more complex, more nonlinear, and more difficult than the electromagnetic behavior." [2]. A significant barrier to research in motor thermal management is the wide variation in motor types and designs. The analysis, data collection, and thermal management technologies should be applicable to as many motor configurations as possible. For this reason we collaborated with industry, university and research partners with expertise in alternative electric motor designs. The variation in thermal loads in terms of location and magnitude for different operating conditions presents another significant challenge. The variation in heat generation magnitude and location based on the operating conditions of the motor require the ability to evaluate the impact of thermal management technologies under multiple operating conditions.

Technical Targets

The DOE technical targets applicable to this research are the goals outlined in the Electrical and Electronics Technical Team Roadmap [3]. Specifically, the 2015 motor technical

targets are $7/kW, 1.3 kW/kg, and 5 kW/L. Thermal management of electric motors supports improvements in each of the technical targets because of impacts on current density, material costs, and magnet costs (dysprosium). In addition, thermal management of the electric motor impacts efficiency and reliability.

Accomplishments

- Designed and fabricated an experimental apparatus to test the forced convection heat transfer performance of automatic transmission fluid (ATF)
- Evaluated the effects of temperature and jet velocity on ATF heat transfer coefficients
- Estimated the thermal performance of ATF jet impingement cooling of electric motors by testing samples with surface features simulating wire bundles
- Increased publically available information on ATF jet impingement cooling performance
- Expanded lamination tests to measure the thermal contact resistance between laminations, which is critical for modeling the axial flow of heat through the electric motor.

✧   ✧   ✧   ✧   ✧

Introduction

The ability to remove heat from the electric motor depends on the passive stack thermal resistances within the motor and the convective cooling performance of the selected cooling technology. The passive thermal design refers to the geometrical layout, material selection, and thermal interfaces that affect the heat spreading capabilities within the motor. The ability for heat to spread through the motor affects the thermal temperature gradients within the motor. The convective cooling technology is the cooling mechanism that ultimately removes the heat from the motor and transfers the heat to another location to reject the heat to the ambient environment. Without the ability to remove heat, the motor cannot operate without sacrificing performance, efficiency, and reliability.

During FY13, work continued from past efforts to characterize the passive thermal stack of the motor. Past work generated preliminary thermal data for materials and key thermal interfaces within the electric motor. The thermal data were incorporated into parametric thermal models for electric motors. The interest from industry into the passive thermal stack measurement results led to expanded tests to characterize the thermal contact resistance between motor laminations. During FY13, the test procedure was developed, and tests were performed for one sample lamination material. This work will continue as part of a new project in FY14, and a publication is scheduled for FY14 to outline the procedure and results.

The primary focus during FY13 involved characterizing the convective cooling technologies incorporating ATF. Figure V-68 provides a cut cross section view illustrating general convective cooling approaches for automotive traction drive applications. One approach to

cooling the motor includes a cooling water jacket incorporated into the motor housing that surrounds the motor stator. The water jacket is typically cooled with a mixture of water and ethylene glycol. When the motor is packaged within the transmission it is also possible to use ATF or other oils to cool the motor. While ATF does not perform as well as the water/ethylene glycol mixture as a coolant, the ability to use ATF to directly cool the rotor or motor end windings has significant advantages for removing heat. However, the flow of the ATF oil as it impinges onto the end winding is a complicated heat transfer and fluid dynamics problem. An understanding of the heat transfer of the ATF as it impinges onto the end windings is critical for motor designers in industry in order to maximize the performance of the motor while providing the required reliability and efficiency. The lack of available data for the convective cooling performance of ATF impinging jets is an important gap in the ability to model and design electric motors for automotive traction drive systems. During FY13, we focused on addressing this gap.
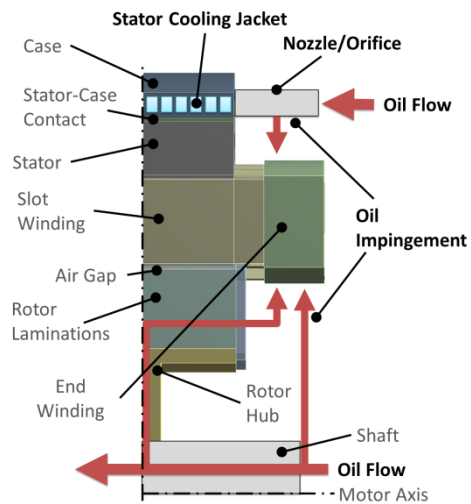
Figure V-68: Illustration of typical thermal management approaches incorporating a stator cooling jacket and oil cooling with ATF within the rotor and end windings.

ATF Convective Cooling Performance

Cooling of the electric motors in some hybrid vehicles is accomplished by impinging ATF jets onto the motor's copper windings [4]. This cooling method is practical because ATF fluid is a dielectric and because, in some cases, the electric motors are housed within the vehicle's transmission or transaxle where ATF fluid is readily available. Although this cooling method is common, currently there is minimal publicly available information regarding the jet impingement performance of ATF fluids.

In this study, we provide the results of recent experiments characterizing the thermal performance of ATF jets. Ford's Mercon LV was the ATF evaluated in this study. Experiments were carried out at various ATF temperatures and jet velocities to quantify the influence of these parameters on heat transfer coefficients. Fluid temperatures were varied from 50°C to 90°C to encompass potential operating temperatures within an automotive transaxle environment. The jet nozzle velocities were varied from 0.5 to 10 m/s. The lower jet
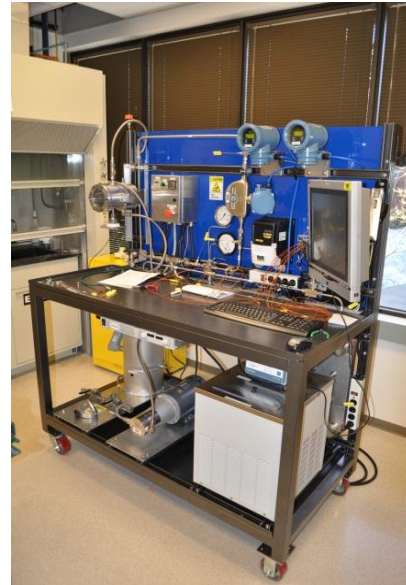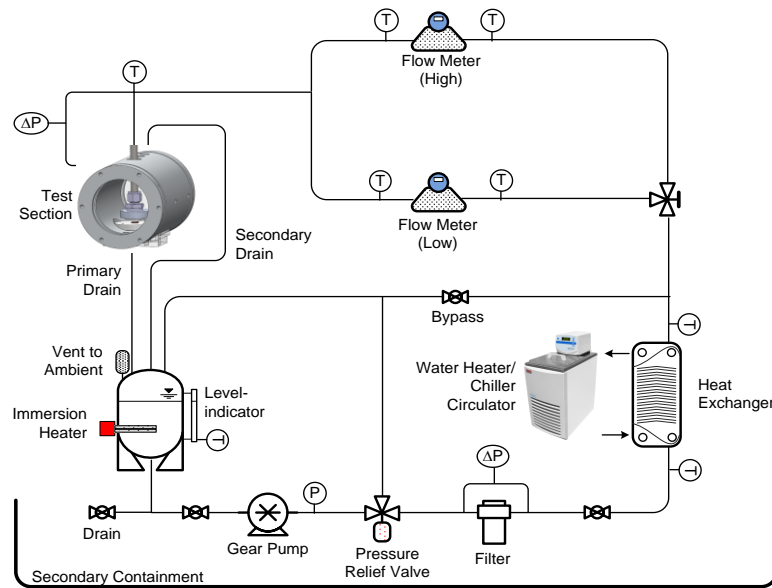
Figure V-69: Test flow loop schematic (left) and picture (right).

velocities are typical of ATF jet impingement velocities within current automotive motor cooling systems. Higher jet velocities up to 10 m/s were included to investigate the impact of more aggressive jet impingement.

The experimental ATF heat transfer coefficient results provided in this report are a useful resource for engineers designing ATF-based motor cooling systems. Moreover, results from this study may also be applicable to potential ATF cooling strategies for automotive power electronics components to support situations where the power electronics are integrated with the electric motor.

Approach

A schematic of the experimental test loop is provided in Figure V-69. The test loop was designed and fabricated to characterize the forced convection thermal performance of ATF. The loop can be configured to conduct jet impingement or channel flow tests and can accommodate a variety of test articles (e.g., small test heaters or larger electric motors). Fluid flow rates of up to 20 liters per minute (Lpm) and fluid temperatures of up to 110°C can be produced by the system.

Approximately 15 liters of Mercon LV ATF are contained within the loop. The fluid is circulated through the loop via a variable-frequency-drive-controlled gear pump. Two Coriolis mass flow meters are provided to measure fluid flow rates. The low-flow-rate flow meter has a range of 0–2 Lpm and provides accurate measurements at lower flow rates. The high-flow-rate flow meter has a range of 2–20 Lpm and allows for accurate measurements at higher flow rates. System fluid temperatures are controlled and maintained constant using a heater/chiller bath circulator and flat-plate heat exchanger system as well as an immersion heater located within the reservoir tank. Temperature (K-type thermocouples) and pressure sensors are located throughout the loop as shown in Figure V-69.
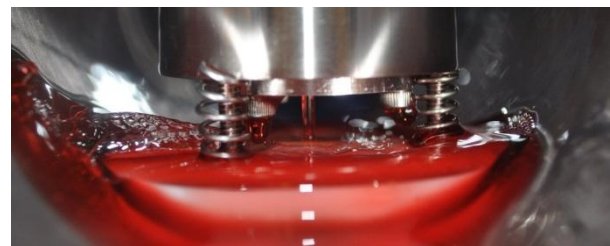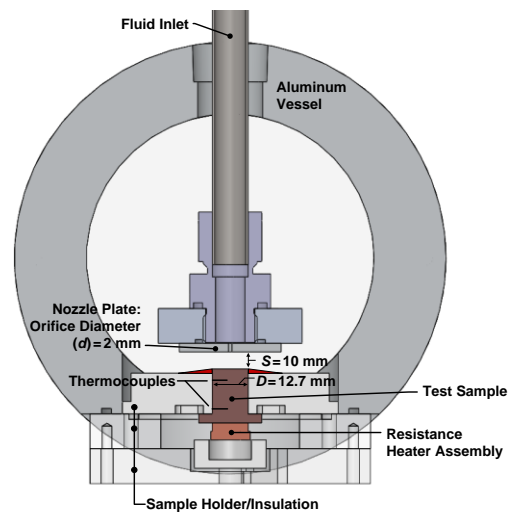
Figure V-70: Schematic (top) and picture (bottom) of the test section showing the nozzle and test sample.

ATF jet impingement experiments were conducted within the test section shown in Figure V-70. Fluid entered the test section through a tube at the top of the chamber. Fluid then flowed through a nozzle plate to generate an impinging jet onto the test sample. The nozzle was a simple orifice type with a 2-mm orifice diameter (d). Drain ports at the front and back of the vessel allowed the fluid to gravity drain and create a free-jet condition (i.e., non-flooded). A thermocouple located just upstream of the test section measured the fluid inlet

temperature. A differential pressure transducer measured the pressure drop across the nozzle. Viewports on the front and back of the test section enabled visualization of the experiments as shown in Figure V-70.

The test samples, fabricated from oxygen-free copper, had an impingement or cooled surface diameter (D) of 12.7 mm. The copper test samples were inserted into Teflon disks ("sample holder/insulation" part in Figure V-70) for support and thermal insulation. A combination of high-temperature silicone sealant and epoxy was applied around the test samples and between the samples and Teflon to prevent fluid leaks. Two calibrated K-type thermocouples were embedded within the sample to measure heat fluxes and to calculate surface/wall temperature. The sample was heated using a computer-controlled power supply that powered a resistance heater assembly attached to the lower side of the sample. Thermal interface material (grease) applied between the resistance heater assembly and the test sample reduced the contact resistance between the resistance heater assembly and the test sample.

The thermal performance of four test samples with different surface features were evaluated under jet impingement (free-jet) cooling conditions. The baseline sample was sandpaper-polished (600 grit) to create a smooth/plain impingement surface. The other three samples were fabricated (via wire electrical discharge machining) with surface features that were intended to simulate wire bundles found in electric motors. The features on these samples consisted of a series of parallel circular ridges running straight across the impingement surface (Figure V-71 and Figure V-72). The radius of these ridges corresponds to the radius of the American wire gauge (AWG) (i.e., 18 AWG, 22 AWG, or 26 AWG) plus the thickness of the wire insulation based on Polyurethane-180 heavy build insulation from MWS Wire Industries. Relevant dimensions of these test samples along with impingement surface area measurements are provided in Table V-6.
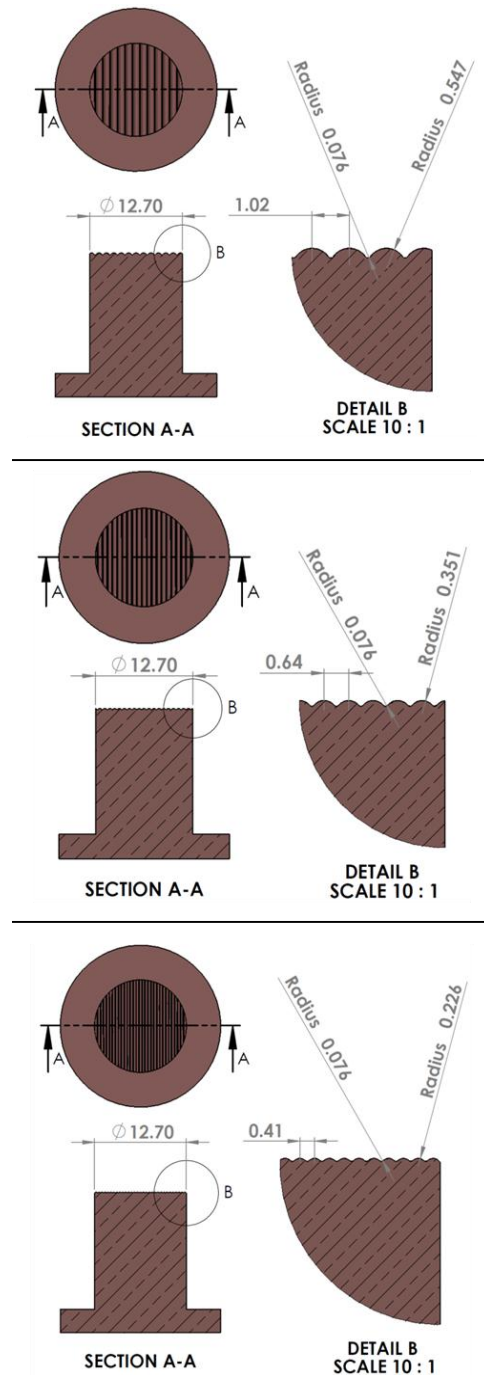
Figure V-71: Computer-aided design models of the 18 AWG (top), 22 AWG (middle), and 26 AWG (bottom) samples. Dimensions shown are in millimeters. The top 12.7-mm-diameter surface was the jet impingement surface.
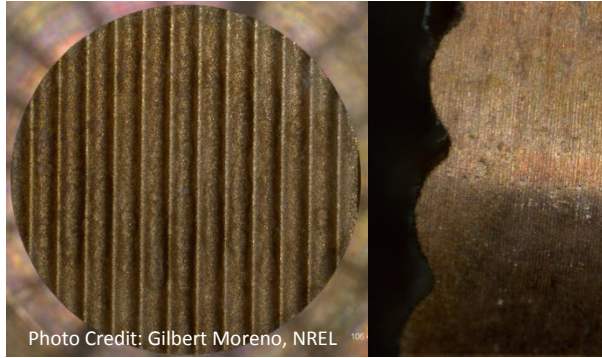
Figure V-72: 18 AWG surface target: Top view (left), side view (right).

Table V-6: Test Sample Feature Dimensions and Surface Area Measurements.

	Baseline	18 AWG	22 AWG	26 AWG
Radius, mm (wire and Insulation)	N/A	0.547	0.351	0.226
Total wetted surface area, mm²	126.7	148.2	143.3	139.2

The nozzle and test sample assembly were aligned vertically and the nozzle-to-impingement-surface distance (S) was set to 10 mm (S/d = 5). The test sample and nozzle assembly were then installed within the test section. The gear pump was activated, and the fluid was circulated through the loop. The bath circulator and the immersion heater were then turned on to achieve the desired test section fluid inlet temperature. Once the system reached the set point temperature, the pump speed was adjusted and the bypass valve was throttled to achieve the desired flow rate. Upon achieving the desired fluid conditions, the experiments were initiated.

A LabVIEW program controlled and monitored experiments via a data acquisition system and direct current power supply. For these experiments, the power supply powered the resistance heater that heated the test sample. Power was adjusted to achieve a test sample impingement surface temperature of approximately 110°C. Once temperature equilibrium was reached, the program recorded temperature, pressure, and flow rate data and calculated the heat transfer coefficient values. For every case, the heat transfer coefficients ($\bar{h}$) were defined according to Equation 1.

$$\bar{h} = \frac{Q}{A_p(T_w - T_l)} \qquad (1)$$

Q is the heat dissipated through the top 12.7-mm-diameter surface, and Tw is the sample's average impingement surface temperature. Both values (Q and Tw) were calculated via the two thermocouples embedded within the test sample, assuming one-dimensional, steady-state heat transfer. Due to the highly conductive properties of the oxygen-free copper samples, the calculated surface temperature (Tw) is taken to be an average of the surface temperatures. In other words, Tw is the average temperature of the stagnation and wall-jet regions on the test sample. For the baseline sample, Tw is the average impingement surface temperature. For the other

samples, Tw is calculated at a plane of constant cross-sectional area just below the surface protrusions/features. Ap is the surface area of the 12.7-mm-diameter impingement area (the increased surface area from the features in the 18 AWG, 22 AWG, and 26 AWG samples is not included), and Tl is the temperature of the liquid jet, as measured by the thermocouple probe immediately upstream of the nozzle. System parameters relevant to this study are summarized in Table V-7. Every test condition was repeated a minimum of three times.

Table V-7: Test Sample Feature Dimensions and Surface Area Measurements.

D (mm)	d (mm)	S (mm)	S/d	D/d
12.7	2.06	10	5	6.2

Results

Experiments were conducted to characterize the thermal performance of Mercon LV ATF impinging jets (free jets). The effect of fluid jet velocity and temperature on heat transfer coefficients was measured. Jet velocities of approximately 0.5 m/s, 2.8 m/s, 5 m/s, 7.5 m/s, and 10 m/s and fluid temperatures of 50°C, 70°C, and 90°C were studied. A significant amount of fluid heat was lost to the ambient environment at the highest fluid temperature tested. This prevented us from conducting experiments at lower fluid velocities with a fluid temperature of 90°C. Therefore, 90°C fluid temperature experiments were only conducted at velocities equal to or greater than 5 m/s.

Figure V-73 displays the average heat transfer coefficient results for the baseline sample at inlet fluid temperatures of 50°C, 70°C, and 90°C. The heat transfer coefficient results provided are an average of all test runs completed. As expected, the heat transfer coefficients increased with increasing impinging jet velocity. Varying the inlet temperature had minimal influence on heat transfer coefficients for the flat target surface.
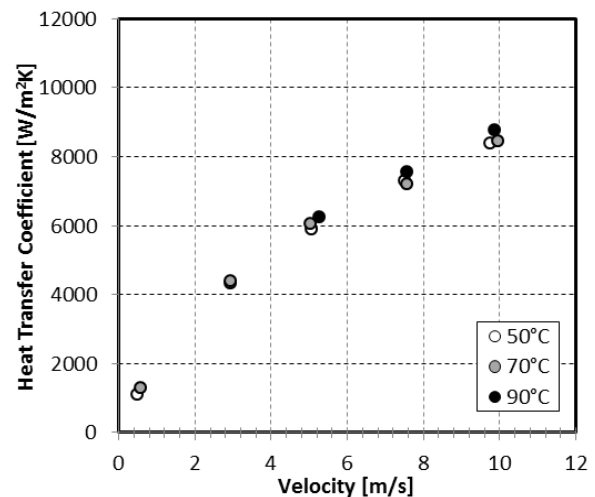
Figure V-73: Baseline sample heat transfer coefficient results.

Figure V-74, Figure V-75, and Figure V-76 compare data from all samples tested at inlet temperatures of 50°C, 70°C, and 90°C, respectively. All the heat transfer coefficient values are averaged values computed from multiple test runs for each sample. At the lowest jet velocity tested (0.5 m/s), all four samples provided about the same performance (Figure V-73 and Figure V-74). This suggests that the wire bundle features of the 18 AWG, 22 AWG, and 26 AWG samples had minimal effect on performance at this low jet velocity (i.e., a jet velocity consistent with automotive ATF motor cooling applications). Variations in the performance of the samples are more apparent at higher jet velocities. At more elevated jet velocities, the 18 AWG and 22 AWG test samples did provide some heat transfer coefficient enhancement as compared to the baseline sample. In all cases, the 26 AWG sample and the baseline sample produced almost identical results, indicating that the surface features on this sample had minimal effect on performance.
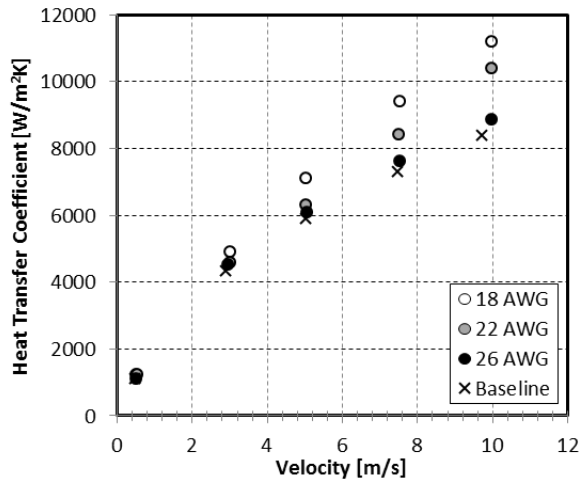
Figure V-74: Heat transfer coefficients of all target surfaces at 50°C inlet temperature.
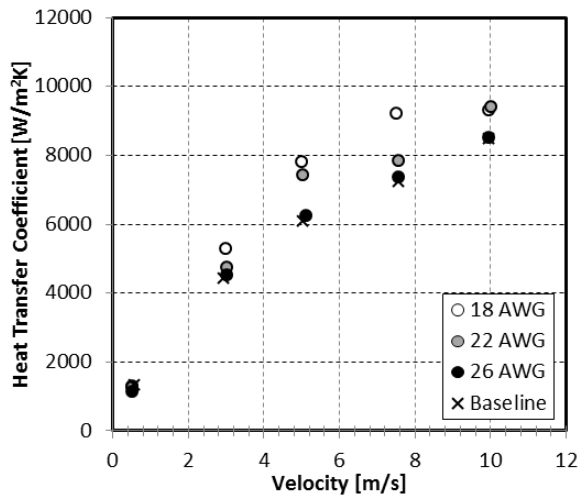
Figure V-75: Heat transfer coefficients of all target surfaces at 70°C inlet temperature.
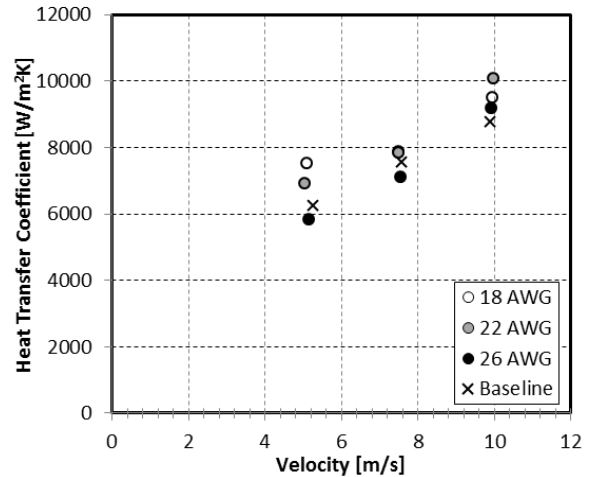
Figure V-76: Heat transfer coefficients of all target surfaces at 90°C inlet temperature.

For the 50°C temperature case (Figure V-74), the heat transfer coefficient results for the various samples are in line with the surface area measurements provided in Table V-6—the greater the surface area, the higher the heat transfer coefficients. At 50°C, the 18 AWG sample with the highest surface area outperformed all samples. At lower jet velocities, the test samples with the wire features perform similar to the baseline flat surface.

The performance trends at higher fluid temperatures are less clear. At 70°C and 90°C (Figure V-75 and Figure V-76), fluid splatter was observed for the 18 AWG, 22 AWG, and 26 AWG samples at higher jet velocities. This phenomenon is associated with fluid being deflected off the surface by the samples' round, protruding features. This deflection reduced the amount of fluid supplied to the outer sections of the samples, leading to reduced performance. This effect was a random, uncontrolled event leading to variation in the results and was more pronounced with the 18 AWG and 22 AWG samples. Evidence of this splattering effect is indicated by a plateau in the heat transfer coefficient curves at the higher jet velocities as seen in Figure V-75. The effect is less clear at 90°C in Figure V-76, but the 18 AWG sample shows the largest effects due to fluid splattering. Figure V-77 shows images of the ATF jet impingement with and without the fluid splatter.
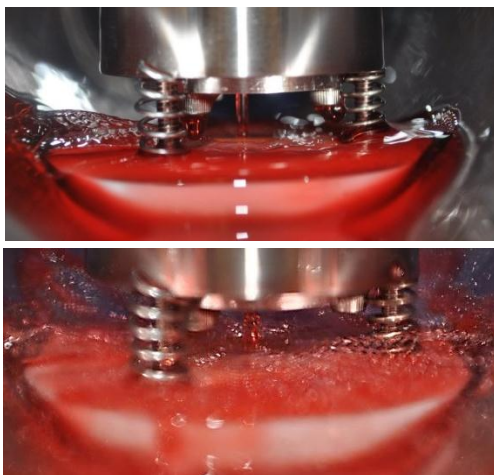
Figure V-77: ATF flowing over surface (top), ATF deflecting off surface (bottom).

Figure V-78 represents only data from the 18 AWG sample and focuses on the trends in the heat transfer coefficient with increasing jet velocity and inlet temperature. For the 50°C inlet temperature, the heat transfer coefficient increases almost linearly with nozzle velocity. At this temperature, the surface splattering described above did not occur. At a 70°C inlet temperature and at approximately 7.5 m/s, the fluid impinged on the center of the sample surface and moved outward over the entire surface. Conversely, at 10 m/s, some of the fluid deflected off the surface immediately after impingement, and this effect is manifested as a plateau in the 70°C heat transfer coefficient curve at the higher velocities. In the 90°C data, fluid splatter was observed to occur at lower velocities. Because the fluid splatter was more prevalent at higher temperatures, we speculate that the lower ATF viscosities at higher temperatures are more conducive to this splattering effect. The higher jet velocities examined in this project are not currently used within automotive ATF motor cooling applications because of potential wire insulation reliability issues. These elevated velocities were evaluated here to characterize the thermal performance of ATF fluids over a wide jet velocity range.
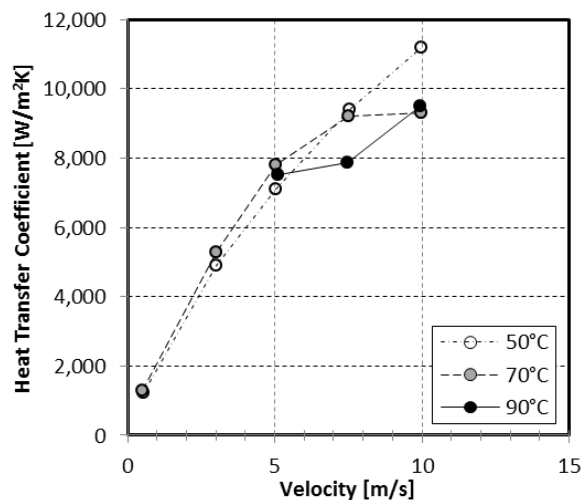
Figure V-78: Heat transfer coefficients of 18 AWG sample for all inlet temperatures.

Figure V-79 plots the pressure drop across the nozzle versus the jet velocity at the three fluid temperatures tested. This nozzle was utilized for all experiments presented in this study. The trend seen in Figure V-79 illustrates that the pressure drop increases as the velocity/flow rate increases. This result aligns with accepted theories in fundamental fluid dynamics. The pressure drop is also seen to decrease for increasing inlet temperatures at the same nozzle velocity. This effect is associated with lower ATF viscosities at higher temperatures, which results in the observed decrease in pressure drop.
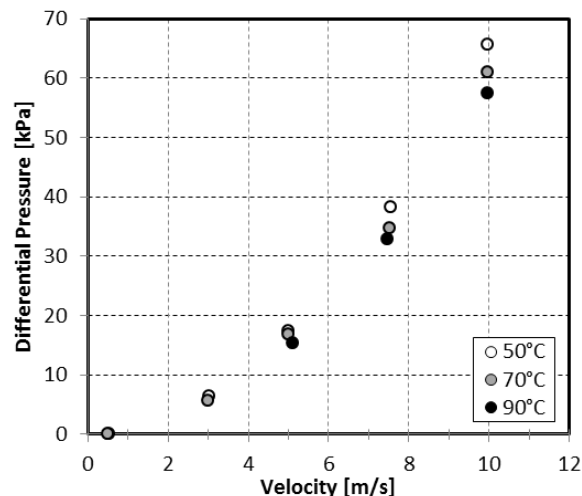
Figure V-79: Differential pressure drop across the nozzle plotted versus the jet velocity.

Conclusions and Future Directions

Experiments were conducted to measure the heat transfer coefficients of impinging ATF (Mercon LV) jets. Jet impingement cooling of motor windings was simulated by fabricating various test samples with wire-bundle features on the impingement surface. The effects of fluid jet velocity and temperature on thermal performance were evaluated. The major conclusions for this study are summarized below.

- For the baseline/smooth test sample, increasing the jet velocity increased heat transfer coefficients. Fluid temperature was found to have negligible effect on heat transfer coefficients for the baseline flat target surface.
- The wire-bundle features on test samples (18 AWG, 22 AWG, and 26 AWG) had minimal effect on heat transfer coefficients at the lowest jet velocity tested (0.5 m/s). At this low velocity, all three test samples yielded nearly identical results that were similar to the results for the baseline sample. At higher jet velocities, the 18 AWG and 22 AWG samples, for the most part, provided heat transfer values greater than those of the baseline sample. The performance of the 26 AWG sample mirrored that of the baseline sample at all temperatures and jet velocities.
- Fluid splattering/deflecting off the impingement surface was observed to occur on the 18 AWG, 22 AWG, and 26 AWG samples at higher jet velocities (≥ 7.5 m/s). This

effect reduced the fluid available for heat removal and thus reduced heat transfer coefficients. This phenomenon was more pronounced with the two samples that had the larger surface features (i.e., 18 AWG and 22 AWG).

- The pressure drop across the nozzle was found to decrease with increasing fluid temperatures. This effect is associated with lower ATF viscosities at higher temperatures. Lower pressure drop implies lower parasitic power losses.
- The results presented in this study are intended to increase the amount of publicly available information on the thermal performance of ATF jet impingement cooling. The data may be used in designing ATF-jet-impingement-based motor cooling systems.

Future work is planned to further evaluate the forced convection heat transfer of automatic transmission fluids. A new project for FY14 is planned to focus on expanding this work in relation to convective cooling of electric motors with ATF. Future work is summarized below.

- Measure or obtain the ATF properties at various temperatures and utilize this information along with the current experimental results to generate correlations for ATF jet impingement cooling. The correlations can be used as a means to estimate the performance of ATF at various operating conditions (i.e., jet velocity and temperature).
- Utilize thermochromic liquid crystal technology and potentially infrared imaging to measure the spatial temperature variations on surfaces cooled by ATF impinging jets. Localized heat transfer coefficient information will allow us to map the heat transfer variation from the stagnation zone through the wall-jet region.
- Design and fabricate a larger test article that better simulates cooling of an electric motor. The test article may incorporate rotation to simulate the rotor. This is an effort to move toward more system-level research.
- Develop computational fluid dynamics models for the ATF impinging jet experiments and validate the model results with the available experimental data. This work will build confidence in modeling capabilities relative to ATF impinging jets, which will serve as a valuable guide for expanding confidence in larger-scale simulations with impinging jets on motor end windings.

FY 2013 Publications/Presentations

1. K. Bennion, J. Cousineau, J. Jeffers, C. King, M. Mihalic, and, G. Moreno, "Oil Cooling of Electric Motors–July 2013 Milestone Report," FY2013 DOE milestone report, July 2013.

2. K. Bennion, J. Cousineau, D. DeVoto, T. Jahns, S. McElhinney, M. Mihalic, and G. Moreno, "Electric Motor Thermal Management," 2013 DOE Vehicle Technologies Office (VTO) Annual Merit Review, Crystal City, VA, May 2013.

3. K. Bennion, J. Jeffers, and G. Moreno, "Electric Motor Thermal Management," Presentation to the DOE VTO Electrical and Electronics Technical Team, Southfield, MI, August 2013.

4. K. Bennion, J. Cousineau, D. DeVoto, T. Jahns, S. McElhinney, M. Mihalic, and G. Moreno, "Electric Motor Thermal Management," Advanced Power Electronics and Electric Motors FY13 Kickoff Meeting, DOE Vehicle Technologies Program, Oak Ridge, TN, November 2012.

Acknowledgments

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1. K. Bennion and J. Cousineau, "Sensitivity Analysis of Traction Drive Motor Cooling," in IEEE Transportation Electrification Conference and Expo (ITEC), 2012, pp. 1–6.

2. J. R. Hendershot and T. J. E. Miller, *Design of Brushless Permanent-Magnet Motors*. Magna Physics Pub., 1994.

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Start Date: October 2011
Projected End Date: September 2013

Objectives

A cost-effective, compact, efficient, and reliable electric traction drive is a key enabling technology for the electrification of vehicle propulsion systems. Heat dissipation has a significant impact on the power capability of power electronics, which leads to increased device cost and package volume or size. The optimal thermal performance is a function of the power electronics packaging and the heat exchanger design. To reach the desired cost and performance objectives, a solution that integrates commercially available packages with low-cost cooling technologies is needed. As seen in Figure V-80, approximately 46% of the inverter cost is attributed to the power silicon, thermal management, and housing [1]. The National Renewable Energy Laboratory (NREL) team has developed a concept for an integrated power electronics module heat exchanger to reduce cost and improve the power per die area.
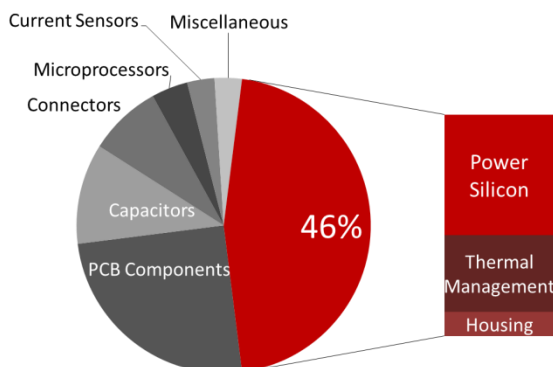
Figure V-80: Inverter cost drivers [1].

The primary objectives are to:

- Improve power per die area by 100% over existing commercial power electronics thermal management systems
- Maintain best-in-class power density capabilities as compared to existing systems
- Enable a modular or scalable thermal approach to reduce the need for custom heat exchanger redesigns as applications scale in power
- Eliminate internal fluid seals commonly found on existing integrated cooling concepts to reduce leakage-induced failure modes
- Reduce parasitic power requirements for the cooling system.

Technical Barriers

The intent of the project is to demonstrate the concept and potential application of the thermal management approach. The pathway towards commercialization requires addressing the following potential barriers.

- Scaling the research and development prototype to address high-volume manufacturing processes for reduced cost.
  - We collaborated with an industry partner with experience in heat exchanger manufacturing methods to get input and guidance to reduce fabrication cost.
- The integration of the electronics package with the heat exchanger requires robust and low thermal resistance interfaces.
  - Past and current work performed within the Advanced Power Electronics and Electric Motor (APEEM) activity in regards to thermal interface materials and bonded interface materials is seen as a critical enabler for this this project.
- The cooling design should support multiple power semiconductor packaging methods.
  - The project considered the application of the design to multiple packaging and interconnect methods.
  - The design addressed in the project is compatible with single- and double-sided cooling configurations for power semiconductor thermal management.

Technical Targets

The U.S. Department of Energy (DOE) technical targets applicable to this research are the goals outlined in the Electrical and Electronics Technical Team Roadmap [2]. Specifically, the project helps in meeting 2015 and 2020 power electronics technical targets. Because this project focuses on the thermal management of the power electronics and not the development of a full inverter, the APEEM technical targets were cascaded down into project goals specific to the thermal management research. The

approach of cascading the APEEM system-level targets to thermal management goals specific to the project is shown in Figure V-81. The specific project goals are summarized as follows:

- Cost
  - Improve power per die area with comparable or better power density
  - Low cost, scalable, and low-waste manufacturing methods
- Volume
  - Maintain equivalent or better power density
- Weight
  - Eliminate large cast heat exchangers
- Reliability
  - Remove internal fluid seals to reduce leak-induced failure modes
  - Increase passive stack thermal capacitance for transient heat loads
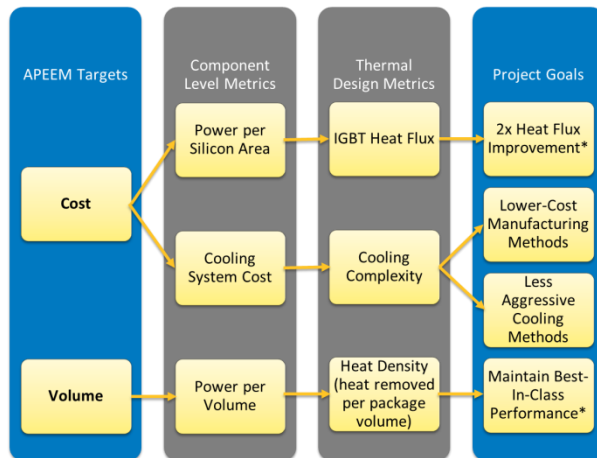
*As compared to Lexus LS 600h benchmarked through APEEM activity

Figure V-81: Project goals.

Accomplishments

The project concluded in FY13 because the project goals were achieved and the next path towards commercialization would involve a collaborative industry project to further develop the concepts for a specific inverter application. During FY13, the following project goals were achieved:

- Demonstrated the potential to double the heat removal capability of the power semiconductor devices, leading to increased power per semiconductor die area
- Demonstrated a greater than 30% increase in the package heat density, which exceeded the original project goal, which leads to improved power density
- Showed one approach to using extruded cold rails for power electronics cooling, potentially reducing weight and eliminating the need for large cast metal heat exchangers
- Illustrated a concept that removes internal seals to reduce potential failure modes from internal fluid leaks
- Demonstrated an approach to improve semiconductor thermal management without negatively impacting the

thermal capacitance within the module, which impacts the temperature cycling behavior of the module and reliability

- Developed a modular and scalable thermal approach, which can reduce the need for custom heat exchanger redesigns as applications scale in power
- Reduced cost and increased reliability by using larger channel dimensions that are more economical to manufacture and less likely to clog
- Maintained compatibility to alternative power semiconductor packaging technologies such as wire bonds, ribbon bonds, or planar interconnect technologies for single and double sided cooling
- Built three prototype designs and validated model results against experimental results
- Established a collaboration with a heat exchanger development partner (Sapa Extrusions North America)
- Received patent incorporating proposed cooling approaches [3].

✧   ✧   ✧   ✧   ✧

Introduction

Improving the ability to remove heat from power electronics semiconductor packages is significant in reducing the cost and size of semiconductor devices [4]. For this reason, new and improved thermal management approaches are needed for power electronics systems. The overall thermal performance of the power electronics system depends on both the thermal packaging of the semiconductor devices and the design of the cooling interface. As shown in previous work, the cooling performance must be matched to the package design to get the optimal integrated solution [5]–[7].

Existing State of the Art

The heat dissipation limitations of a conventional power electronics package, as shown in Figure V-82, are well known and described in the literature. The thermal limitations of the thermal interface material between the heat spreader and the heat exchanger have led to efforts to improve the thermal interface [8] or remove interface materials through direct cooling.
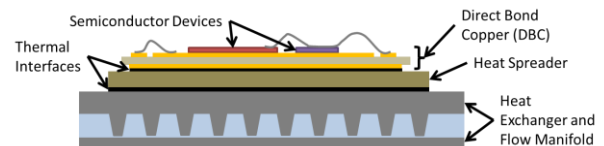
Figure V-82: Conventional power electronics semiconductor thermal stack with heat spreader and thermal interface material between the heat spreader and the heat exchanger surface.

Direct cooling of the power semiconductor package can take multiple forms, but generally involves removing intermediate layers between the semiconductor device and the cooling fluid. Two common approaches involve direct cooling of the heat spreader, as shown in Figure V-83, or direct cooling of the substrate metallization layer (Figure V-84). Examples include direct bond copper (DBC) or direct bond aluminum, as shown in Figure V-84. Direct cooling

reduces available cooling surface area and requires more aggressive cooling mechanisms [6]. Examples include fluid jets that impinge on the heat spreader or DBC directly [9]–[11], microchannels [12], pin fins [13]–[16], or other fin structures such as folded fins attached to the heat spreader [17].

Figure V-83: Example package with a direct-cooled heat spreader
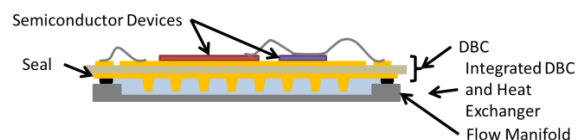
Figure V-84: Example package with direct-cooled metallization layer such as DBC.

In addition to improving the thermal performance through reducing the thermal stack resistance and more aggressive cooling, others have proposed methods to remove heat from both sides of the power semiconductor device (also known as double-sided-cooling) [4, 18, 19]. A commercial example is the 2008 Lexus LS 600H hybrid electric vehicle, which is summarized in a report by Burress et al. [20] and which achieved the highest power density of the commercial devices benchmarked through the DOE's Vehicle Technologies Office. A schematic of the cooling and thermal package structure is provided in Figure V-85.
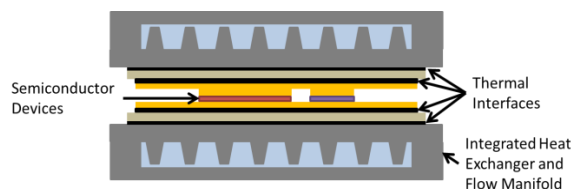
Figure V-85: Example package enabling cooling on both sides of the power semiconductor device (double-sided cooling).

While the approaches discussed previously are effective at improving the ability to remove heat from the semiconductor devices, they face challenges regarding implementation. All of the cooling approaches highlighted above are dominated by planar heat removal structures that focus on one-dimensional heat transfer out of the power semiconductor package through the top or bottom of the package. The heat spreader does allow for some thermal spreading, but the cooling is applied to a single surface of the package. When the heat spreader is removed and the coolant fluid is directly applied to the DBC, the reduced heat spreading requires more aggressive cooling to maintain the same performance as illustrated by Bennion and Moreno [6]. The drive to more aggressive cooling leads to concerns related to fluid channel size, parasitic power, reliability, construction, and cost. To enable less aggressive convective cooling technologies, the heat spreading characteristics of the package passive thermal stack must be

matched or optimized to the convective cooling performance. The removal of layers within the semiconductor package also reduces the thermal capacitance of the structure, making the semiconductor more susceptible to transient loading effects, which impacts reliability. Also, the direct-cooling approaches illustrated inFigure V-83 and Figure V-84 often require seals to prevent coolant from leaking into the electronics, which can lead to issues related to performance and reliability [13].

Proposed Concept

NREL's proposed cooling approach [3] attempts to emphasize the use of the heat spreader to enable high cooling performance with less aggressive convective cooling methods. The approach integrates the heat spreader with the heat exchanger to provide multiple heat transfer paths within th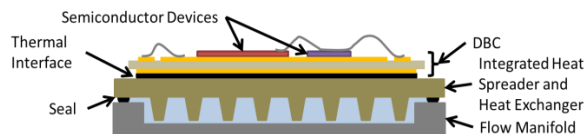e heat spreader. Improving the heat spreading characteristics of the package provides an opportunity to increase the available surface area in contact with the coolant and does not rely on aggressive convective cooling methods or small fluid channel passages. Instead of relying on a planar thermal stack dominated by one-dimensional heat transfer (Figure V-86), the concept design uses the available space around the package to spread and remove heat along multiple paths, as illustrated in Figure V-87.
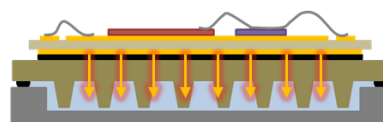
Figure V-86: Conventional system with one-dimensional dominated heat flow path.
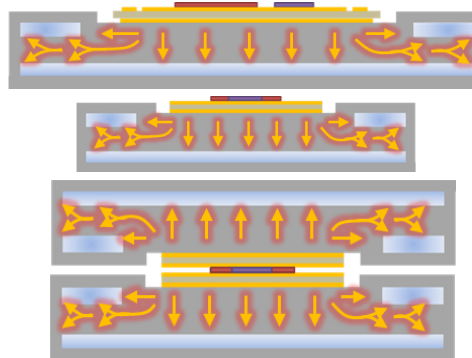
Figure V-87: Conceptual drawings of integrated heat spreader and heat exchanger system to enhance heat spreading and cooling performance.

In addition to improving the thermal performance, the concept features other important characteristics not directly related to heat transfer. The design enables a modular, or scalable, approach to the cooling of power semiconductor devices that builds upon high-volume manufacturing methods already accepted by the automotive industry. Examples include thin-film folded fins used in brazed automotive heat exchangers and extruded aluminum materials used in a wide range of applications. The concept also eliminates the internal seals shown in Figure V-83 and Figure V-84. The seals are moved to external locations to reduce the risk of coolant interfering with the electrical components. Additionally, the parasitic power requirements for the cooling system are reduced by increasing the fluid channel dimensions.

Approach

The goal of the project was to prove the potential of the cooling concept and refine the design that would lead to a hardware prototype for validation of the model results. Our work during FY13 focused on the process highlighted in Figure V-88, which involves the following steps:

- Performing thermal finite element analysis (FEA) design optimization of the heat spreader structure to investigate the thermal structure design, select heat spreader materials, and identify convective cooling performance targets
- Evaluating cooling surface enhancement designs using computational fluid dynamics (CFD) modeling tools and confirming the ability to develop a heat exchanger surface that meets the minimum convective cooling performance requirements
- Building and testing hardware prototypes
- Simulating the full system to iterate on the heat spreader design and the convective cooling heat exchanger surface to enable lower cost manufacturing.
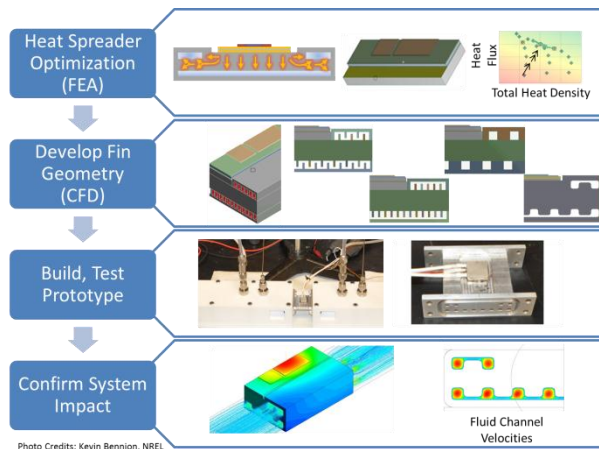
Figure V-88: Thermal management design strategy.

Analytical Design Approach

The heat spreader was optimized through a series of iterations involving FEA and CFD. Thermal FEA has an advantage over CFD simulation in speed, allowing more design iterations within a set period of time. CFD has the advantage of providing detailed fluid dynamics and heat transfer results for specific heat exchanger geometries. For this reason, we developed a method to decouple the fluid dynamics and heat transfer results within CFD simulations from the passive stack thermal model within CFD or FEA framework. The first step in the process is estimating the appropriate convective boundary conditions for the thermal FEA model.

The effective convection coefficient (h) is calculated following the Effectivness-Number of Transfer Units (NTU) heat exchanger analysis method following equations 1–5 [21]. The first step in the analysis estimates the convection coefficient and area product (UA) for the reference surface. Knowing the mass flow ($\dot{m}$) and fluid specific heat (c_p) it is possible to calculate the heat exchanger NTU and

effectiveness (ε), which can be used to calculate heat exchanger thermal resistance ($R_{th,NTU}$), area weighted thermal resistance ($R_{th,NTU}^{"}$), and h. The final result is an appropriate convection coefficient that can be applied to the thermal FEA model, such as within ANSYS that accounts for the impact of fluid properties and fluid flow rate.

$$NTU = \frac{UA}{\dot{m}c_p} \tag{1}$$

$$\varepsilon = 1 - e^{-NTU} \tag{2}$$

$$R_{th,NTU} = \frac{1}{\varepsilon \dot{m}c_p} \tag{3}$$

$$R_{th,NTU}^{"} = \frac{A}{\varepsilon \dot{m}c_p} \tag{4}$$

$$h = \frac{1}{R_{th,NTU}^{"}} \tag{5}$$

Two approaches were develedoped to calculate the convection coefficient and area product (UA) in equation 1. Figure V-87 illlustrates the two approaches. The first approach estimates a UA over the channel wetted area, while the second approach estimates a UA over a flat base surface.
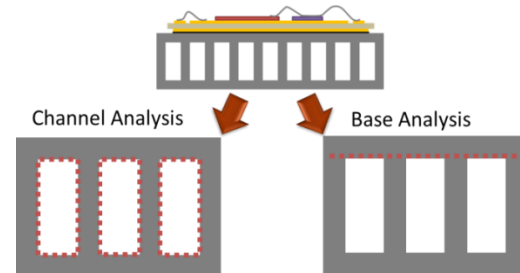
Figure V-89: The convective heat transfer boundary conditions were evaluated along the channel (left) and a cut plan along the base of the heat exchanger (right).

In the first approach, the effective convection coefficient along the channel wetted area is calculated from CFD simulation results. The effective convection coefficient is then applied within the thermal FEA model. Applying the convection coefficient within the thermal FEA model provides a secondary check on the passive stack thermal model within the CFD and FEA models. Performing the analysis within a thermal FEA also allows for quicker sensitivity studies associated with the convection coefficient and passive thermal stack of the package. The procedure for calculating the channel UA product follows equations 6–9, where the symbols are defined in Table V-8. This approach assumes a uniform convection coefficient is applied to the FEA thermal model at the fluid inlet temperature.

$$\Delta T_1 = T_{surf,av,ch} - T_{c,o} \quad (6)$$

$$\Delta T_2 = T_{surf,av,ch} - T_{c,i} \quad (7)$$

$$\Delta T_{lm,ch} = \frac{(\Delta T_1 - \Delta T_2)}{ln\left(\Delta T_1 / \Delta T_2\right)} \quad (8)$$

$$(UA)_{ch} = \frac{Q}{\Delta T_{lm,ch}} \quad (9)$$

Table V-8: Nomenclature for channel calculations.

Symbol	Description
$T_{c,o}$	Outlet coolant temperature
$T_{c,i}$	Inlet coolant temperature
$T_{surf,av,ch}$	Average temperature of channel walls
$\Delta T_{lm,ch}$	Channel log mean temperature difference
$(UA)_{ch}$	Channel convection coefficient and area product
Q	Heat into channels

The second approach simplifies the analysis by cutting the heat exchanger along the base, removing the geometry complexities of the fins. This analysis is useful for comparing the interactions between the passive stack thermal resistance and an effective heat exchanger convective cooling thermal resistance. Instead of calculating a UA along the wetted channels, a UA across an arbitrary plane is defined. The process is listed in equations 10–13, where the symbols are defined in Table V-9.

$$\Delta T_1 = T_{surf,av,base} - T_{c,o} \quad (10)$$

$$\Delta T_2 = T_{surf,av,base} - T_{c,i} \quad (11)$$

$$\Delta T_{lm,base} = \frac{(\Delta T_1 - \Delta T_2)}{ln\left(\Delta T_1 / \Delta T_2\right)} \quad (12)$$

$$(UA)_{base} = \frac{Q}{\Delta T_{lm,base}} \quad (13)$$

Table V-9: Nomenclature for base calculations.

Symbol	Description
$T_{surf,av,base}$	Average temperature along base
$\Delta T_{lm,base}$	Base log mean temperature difference
$(UA)_{base}$	Base convection coefficient and area product

Breaking up the heat exchanger analysis as outlined above provides a method for evaluating the combined thermal performance incorporating the passive thermal stack and the convecting cooling performance. The process allows quick design studies and optimization with thermal FEA models and selective CFD analysis at periodic intervals. Also, prior to having prototype hardware for testing, the ability to compare CFD and FEA model results provides a valuable check for

modeling errors. Full conjugate heat transfer simulations within CFD were compared to simplified FEA models with boundary conditions calculated from the full model.

Adjustments for Manufacturing Cost

The heat exchanger was designed with a focus on cost. The goal was not to maximize the heat transfer convection coefficient for the heat exchanger. Instead, design iterations focused on making the heat exchanger more economical while still meeting the targeted cooling performance. The initial focus for the design focused on designing an extruded aluminum heat sink. An extruded aluminum process was selected because of its lower tooling cost as compared to aluminum castings and the ability to use higher thermal conductivity alloys (36% improvement in thermal conductivity) with lower material cost.

The adjustments to the design followed guidelines consistent with input obtained through an extrusion design manual provided by Sapa Extrusions North America [22]. Some of the key features to reduce the manufacturing cost are highlighted in Figure V-90, and they include rounded corners, reducing the number of internal voids, and maintaining a minimum recommended thickness that is dependent on the size of the part. One key factor in reducing tooling cost is the open "E-fin" design in Figure V-90. The "E-fin" reduces the number of voids in the extruded part as compared to closed channels, which results in 12 voids. Based on industry input, the reduction from 12 to three voids results in an approximate 25% cost reduction. The final design prototype is shown in Figure V-91 with a heater bonded to the surface. The flanges are included to attach the prototype to the inlet and outlet manifolds for testing.
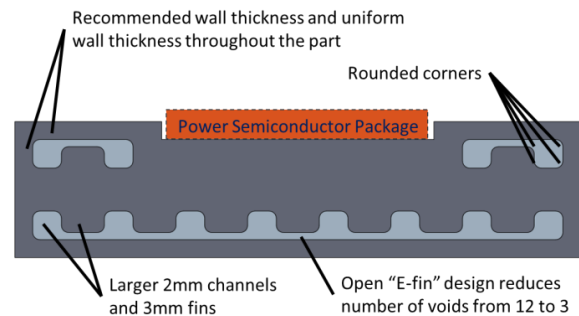
Figure V-90: Sample parameters from design guidelines to reduce fabrication cost.
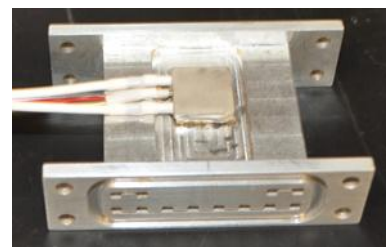
Figure V-91: Prototype heat exchanger with heater.

Experimental Approach

Once the design was selected, three heat exchangers were built. Two heat exchangers representing the design were

built with Al6061 and Al6063. The third heat exchanger represented a baseline with a single cooling zone beneath the package, which was made with Al6061. The baseline and design heat exchanger geometries are shown in Figure V-92. The materials used to fabricate the heat exchangers are listed in Table V-10. The Al6063 material was provided by Sapa Extrusions North America.
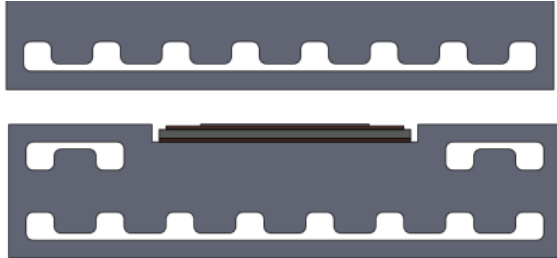
Figure V-92: Fabricated heat exchanger geometries showing baseline (top) and design (bottom).

Table V-10: Tested heat exchangers and materials.

Geometry	Material
Baseline	Al 6061
Design	Al 6061
Design	Al 6063

Each of the heat exchangers listed in Table V-10 was tested experimentally to verify the simulated thermal and fluid characteristics of the heat exchanger from the CFD simulation results. The model validation experiments were performed with a water-ethylene glycol (WEG) mixture of 50%/50% by volume. The heat exchangers were tested at 2.0 kg/min, 4.0 kg/min, and 6.0 kg/min (1.9 L/min, 3.8 L/min, and 5.7 L/min). The tests on the baseline heat exchanger included five repetitions, and tests on the design heat exchanger included six repetitions for each test condition. The inlet coolant temperature was set to 30°C for each test, and the specific gravity of the fluid was checked prior to starting tests to ensure the fluid properties remained constant.

The test setup is shown in Figure V-93and Figure V-94. Figure V-93 is a drawing of the inlet manifold that attaches to the heat exchanger flange, while Figure V-94 shows the hardware with temperature and pressure measurement apparatuses within the inlet and outlet manifolds.
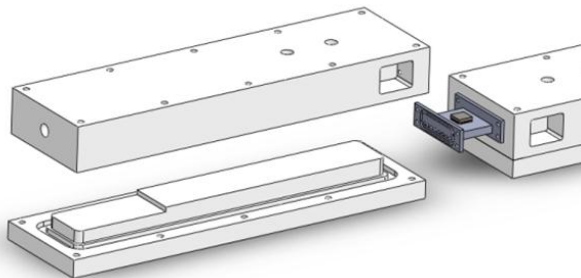
Figure V-93: Test section showing inlet manifold for CFD model validation.

Figure V-94: Heat exchanger installed in test fixture with inlet and outlet temperature and pressure measurements

As shown in Figure V-91, a heater representing a power semiconductor device heat load was mounted to a copper spreader with epoxy (Figure V-95). The copper spreader was bonded to the heat exchanger with Btech thermoplastic material (referred to as Btech - Figure V-95). The copper spreader was instrumented with thermocouples in two locations (Figure V-96), and the thermocouples were soldered into the copper spreader to ensure good thermal contact.
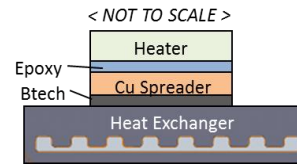
Figure V-95: Heater assembly layers.
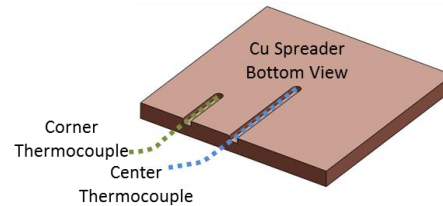
Figure V-96: Thermocouple locations in the copper spreader.

The measurement uncertainties of temperature and pressure were estimated to include systematic and random errors. The thermocouples were calibrated, and the total 95% confidence interval (U95) was within ±0.13°C (~0.4%). The heater also included a temperature measurement, but it was not calibrated with the thermocouples installed into the copper spreader. The inlet and outlet pressures were monitored with a U-tube manometer with a U95 of ±14 Pa (~1%).

The epoxy layer and the Btech layer represented unknown thermal resistance within the stack. The values for these thermal resistances were estimated by matching the temperature measurements at the lowest flow rate to the model results. The process for determining the effective thermal conductivity of the epoxy and Btech layers followed the listed steps and is illustrated in Figure V-97.

- The convection coefficients were mapped from a single flow rate CFD model to the FEA model channels.
- The effective resistance and thermal conductivity of the epoxy and Btech layers were solved iteratively for a single test by matching the temperature change between the heater to copper spreader and the temperature change between the copper spreader to the inlet coolant temperature.

- The effective thermal resistance values for the epoxy and Btech layers were applied to the CFD model and validated against experimental results for other flow rates.

Tc,i: Coolant inlet temperature
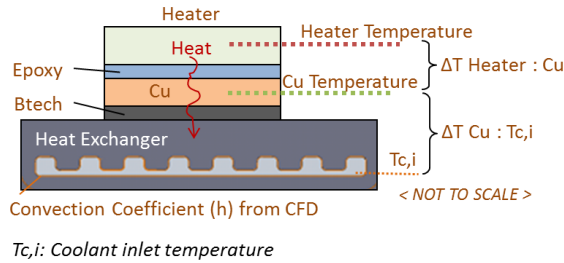
Figure V-97: Interface thermal resistance estimation for epoxy and Btech bonding layers.

System Level impacts

Once the CFD model results for the heat exchanger design were validated against the experimental results, the next step involved evaluating the cooling impacts for an insulated gate bipolar transistor (IGBT)/diode package. The heat exchanger was designed to operate in the flow configuration shown in Figure V-98 in which each IGBT/diode package is cooled in parallel. In addition to the assumed flow arrangement, other assumptions were applied related to the heat distribution and maximum component temperatures. The ratio of heat in the IGBT to the heat in the diode was set to 3:1, and the maximum device temperature was limited to 150°C. The bond between the package and the heat exchanger was also assumed to provide equivalent thermal performance as solder. The inlet WEG coolant temperature was fixed at 70°C.
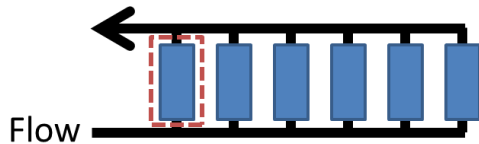
Figure V-98: Assumed parallel flow arrangement for system-level analysis.

Results

The key results from the work performed during FY13 are summarized below. The results are broken into sections covering the modeling results, experimental results, and system-level impacts.

Design Modeling Results

Heat spreader performance as compared to alternative package arrangements is shown in Figure V-99 and Figure V-100. The primary goal of the research was to enable high thermal performance (IGBT heat flux) with less aggressive cooling (higher heat exchanger side thermal resistance). Early in the design process, a targeted cooling performance range was identified as highlighted in Figure V-99, which was selected from past experience related to power electronics cooling with WEG.
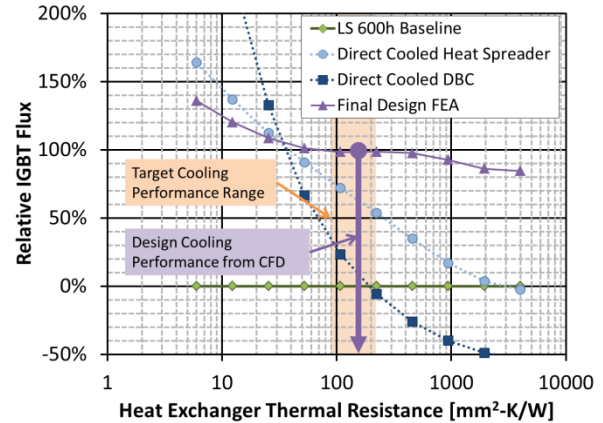
Figure V-99: Thermal FEA comparing IGBT heat flux of heat spreader design showing the original target cooling performance range and the final design.

The final design was compared against three potential baseline package configurations with the LS 600h package representing the reference. The direct-cooled DBC approach shows significant potential to increase IGBT heat flux, but the improved heat flux is only available with more aggressive cooling that exceeded our targets for the cooling performance range. The direct-cooled heat spreader configuration shows a performance increase over the LS 600h reference within the targeted cooling performance region, but it does not meet the target of doubling the IGBT heat flux within the target cooling performance range. Through thermal FEA analysis, the final design shows the potential to meet the target to double the heat flux relative to the LS 600h module configuration over the targeted cooling performance region. The heat exchanger cooling performance of the final design obtained from CFD is also shown in Figure V-99, showing that it falls within the targeted cooling performance range.
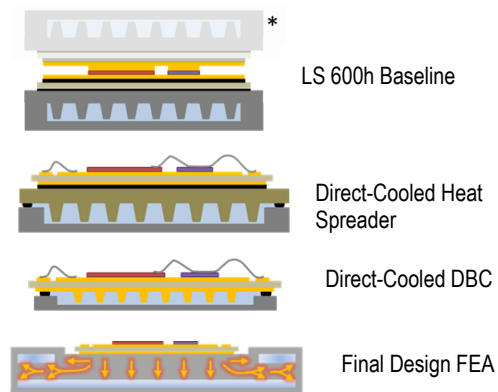
* All packages are compared based on single-sided cooling for consistency.

Figure V-100: Package illustrations of configurations highlighted in Figure V-99.

CFD analysis of the heat exchanger fin geometry was used to design the shape of the flow channels. As mentioned previously, the goal was not to maximize the heat transfer coefficient, but rather to design a heat exchanger within manufacturing constraints to minimize cost while achieving the

targeted cooling performance. Figure V-101 highlights some of the CFD analyses. Figure V-101 shows the fluid flow velocities within the channels. The key result to highlight is the uniform flow velocities within the channels.
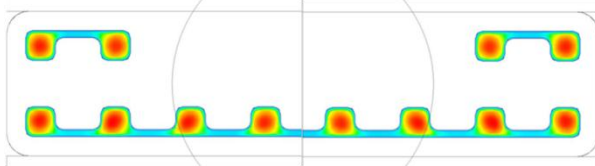
Figure V-101: Channel inlet fluid velocity.

Experimental Testing

The procedure for validating the simulation results with experimental data was described previously. The results are highlighted below. The experimental validation focused on the heat exchanger flow and temperatures results. Figure V-102 compares the difference between the experimental temperature and CFD model temperature within the copper spreader block. The difference between the model and the experimental results was found to be within about 2% over all of the flow rates and heat exchangers tested.
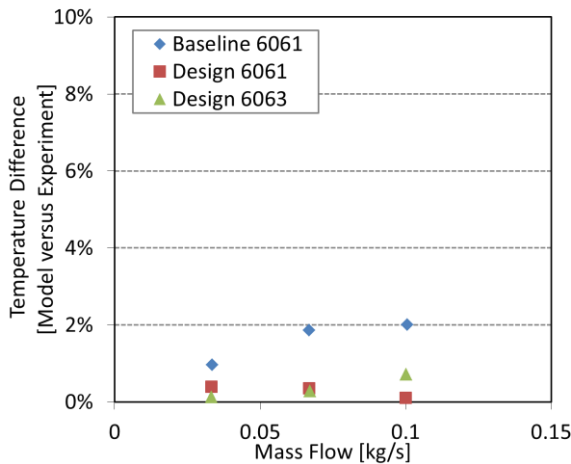
Figure V-102: Temperature validation.

Figure V-103 compares the experimentally measured pressure drop with the CFD model results. The difference between the model and the experimental results was within about 9% across all flow rates and heat exchangers that were tested. With the analysis, it was found that the pressure drop is affected by small variations in the channel geometry. We used a high-resolution digital microscope to measure the manufactured channel dimensions for each heat exchanger and applied the results to the CFD model.
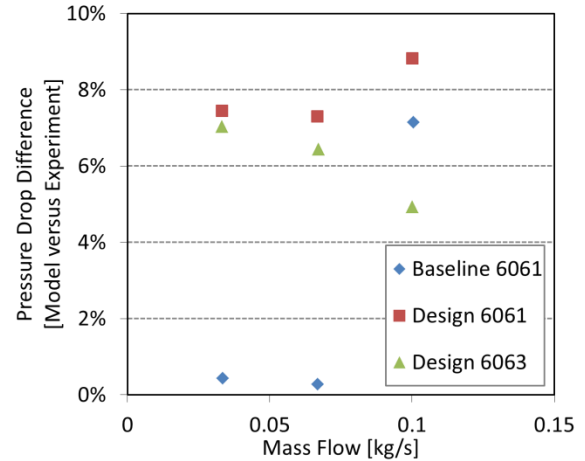
Figure V-103: Pressure Drop validation.

System-level impacts

The system-level impacts of the heat exchanger design were determined through simulation using the validated heat exchanger CFD model. Figure V-104 compares the design against the LS 600h reference package and the baseline aluminum heat exchanger described in Figure V-92. The comparison in Figure V-104 is at the equivalent flow rate for the LS 600h package (0.0086 kg/s per side of package), which is based on past modeling and analysis efforts. At equivalent flow rate, the design improves the IGBT heat flux by a factor of 1.6 with a slight improvement in package heat density. When the flow rate is held constant, the pressure drop across the design heat exchanger is significantly lower than the LS 600h reference or the baseline. With the improved heat transfer and reduced pressure drop, the coefficient of performance for the design improves by a factor of 7.9 as compared to the reference LS 600h.
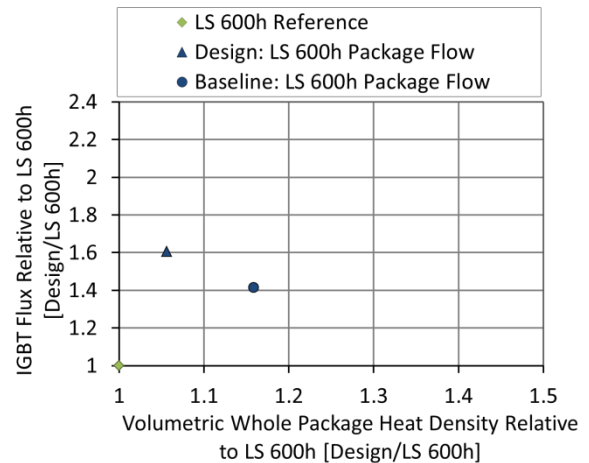
Figure V-104: Model results for design and baseline comparison at LS 600h package flow rate.

When evaluated at the target system flow rate of 10 L/min in the parallel configuration shown in Figure V-98, the design meets the performance targets defined at the beginning of the project. Figure V-105 shows the results with 1/6 of the system flow going to each package. The IGBT heat flux improved by

about a factor of two, and the package heat density improves over 30%. The design heat exchanger also exceeds the performance of the baseline at the same fluid parasitic power.
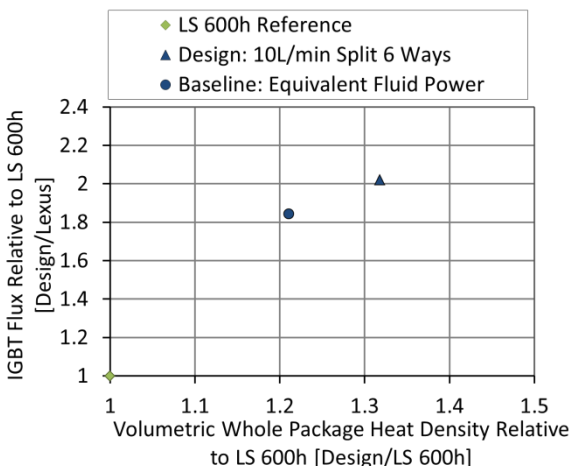
Figure V-105: Model results for design at target flow and baseline at equivalent parasitic fluid power.

As mentioned previously, the design was based on a parallel arrangement of the heat exchangers as shown in Figure V-96 with one package or module per cooling branch. Preliminary investigations were also performed to investigate the impact of series connections on the effective convection coefficient within the channels. Figure V-106 compares the average convection coefficient within the channels for three separate heat exchangers connected in series. As seen in Figure V-106, the convection coefficient does drop as the flow passes through the first heat exchanger. The convection coefficient appears to stabilize as the flow passes through the second and third heat exchangers. The drop in the convection coefficient would need to be investigated as part of future work depending on the intended application.
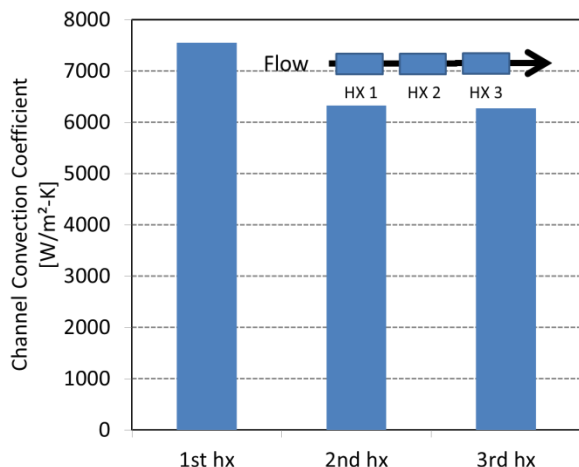
Figure V-106: Effective channel convection coefficient in each section.

Conclusions and Future Directions

This research project focused on the development and demonstration of a general design concept to enable less aggressive cooling while improving the system-level semiconductor package thermal performance to improve the capability of power semiconductor devices. The improved power capability directly relates to improving the cost per power of the power electronics

The performance of the design was compared against two baseline packages of power semiconductor devices. The design doubled the IGBT heat flux capability of the LS 600h reference with significant improvements in the coefficient of performance. The LS 600h package was selected as the reference because of its best-in-class performance of the modules benchmarked through the APEEM activity. The design also outperformed the baseline direct cooled base plate configuration with similar extruded fin geometry.

The design approach built upon a recently issued patent to enable high performance with less aggressive cooling. Future work could extend the concept to enable other cooling technologies with less effective coolants such as air or automatic transmission fluid. Directly cooling the power electronics with air or automatic transmission fluid could eliminate the dedicated WEG loop for cooling the power electronics and lead to potential cost reductions and elimination of cooling system components. The specific design can go through additional refinement for specific power electronics applications and this work will be included on future industry collaborations related to cooling power electronics.

FY 2013 Publications/Presentations

1. K. Bennion and J. Lustbader, "Integrated Three-Dimensional Module Heat Exchanger for Power Electronics Cooling," U.S. Patent 20130082377 A10 4-Apr-2013.

2. K. Bennion, J. Cousineau, J. Lustbader, "Integrated Power Module Cooling," Presentation at the VTO Annual Merit Review, Crystal City, VA, May 2013.

3. K. Bennion, J. Cousineau, J. Lustbader, "Integrated Module Heat Exchanger," Presentation to the DOE Vehicle Technologies Office Electrical and Electronics Technical Team, Southfield, MI, April 2013.

4. K. Bennion, J. Cousineau, J. Lustbader, "Integrated Module Heat Exchanger," Advanced Power Electronics and Electric Motors FY13 Kickoff Meeting, DOE Vehicle Technologies Office, Oak Ridge, TN, November 2012.

Acknowledgments

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3. K. Bennion and J. Lustbader, "Integrated three-dimensional module heat exchanger for power electronics cooling," US20130082377 A104-Apr-2013.

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5. M. O'Keefe and K. Bennion, "A Comparison of Hybrid Electric Vehicle Power Electronics Cooling Options," in IEEE Vehicle Power and Propulsion Conference (VPPC), 2007, pp. 116–123.

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V.7. Combining Fluid Loops on Electric-Drive Vehicles

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Start Date: FY 2011
Projected End Date: FY 2014

Objectives

- Improve vehicle range and reduce cost from combining thermal management systems
- Collaborate with industry partners to research the synergistic benefits of combining thermal management systems in vehicles with electric powertrains

Technical Barriers

Electric-drive vehicles (EDVs) have increased vehicle thermal management complexity. They introduce new requirements for thermal management of the energy storage system (ESS) as well as power electronics and electric motor (PEEM), including increased costs for separate cooling loops and increased energy consumption to meet thermal demands. The energy consumption increase is particularly critical for battery electric vehicles (BEVs), where it leads to decreased vehicle range and therefore user "range anxiety," which decreases market acceptance.

Technical Targets

- PEEM coolant loop with temperatures less than 105°C without requiring a dedicated system
- Maximize the usage of waste heat from the PEEM and ESS components and enable heat pump operation
- Reduce aerodynamic drag by minimizing the area and number of heat exchangers in the front end of the vehicle
- Reduce overall energy consumption for vehicle thermal systems and improve range

Accomplishments

- An experimental combined fluid loop (CFL) system was constructed
  - Prototype heat exchangers provided by partner Delphi
  - A prototype automotive electric compressor was provided by partner Halla Visteon Climate Control
- A test apparatus was constructed to simulate load, control, and measure the performance of the CFL system
  - The experiment can be operated in a variety of different test configurations over a range of vehicle operating conditions from very cold to very hot

✦   ✦   ✦   ✦   ✦

Introduction

Plug-in hybrid electric vehicles and BEVs have increased vehicle thermal management complexity (e.g., PEEM, ESS, and vehicle cabin). Multiple cooling loops may lead to reduced effectiveness of fuel-saving control strategies. The additional cooling loops increase weight, volume, aerodynamic drag, and fan/pump power, thus reducing electric range. This reduces customer acceptance of BEVs by increasing range anxiety and presents a barrier for the penetration of BEVs into the national vehicle fleet. Our goal is to improve vehicle performance (fuel use or BEV range) and reduce cost by capturing the synergistic benefits of combining thermal management systems. The overall goal is to solve vehicle-level heat transfer problems, which will enable acceptance of vehicles with electric powertrains.

The objective of this project is to research the synergistic benefits of combining thermal management systems in vehicles with electric powertrains. Currently, EDVs typically have a separate cooling loop for the PEEM components. It would be beneficial to have a PEEM coolant loop with temperatures less than 105°C without requiring a dedicated system. Range would be increased in the winter by minimizing electrical resistance heating through a combined thermal management system that maximizes the usage of waste heat from the PEEM and ESS components and enables heat pump operation. With increased focus on aerodynamics, minimizing the area and number of heat exchangers in the front end of the vehicle has the potential to reduce drag. An additional benefit of combining cooling loops is that the ESS, passenger compartment, and thermal management fluid loops can be preconditioned.

In the first year of the project (FY 2011), Halla Visteon Climate Control, a Tier 1 automotive heating, ventilation and air conditioning (HVAC) component supplier, supplied detailed thermal component and system information. This included drawings, thermal and flow component data, and system performance data. The NREL researchers built component

models in KULI [1] using the geometry, heat transfer, and pressure drop information. The individual component models were verified to function as expected. Cabin thermal, air conditioner (A/C), and PEEM cooling loop models were then developed by combining the individual component models into systems, which were then compared to test data.

In the second year of the project (FY 2012), the individual thermal models of the cabin A/C, cabin heater, PEEM, and ESS fluid loops were improved based on the results from comparisons to test data. A baseline electric vehicle thermal system model was created from these sub-system models, and its performance was evaluated. The A/C system and ESS cooling loop controls were updated with more sophisticated models, and several CFL strategies were investigated. The CFL system modeling demonstrated that the design properly conditioned the ESS during heating and cooling, maintained cabin air comfort temperatures, lowered PEEM temperatures to enable higher power, and reduced heating energy through heat recovery [2].

Approach

The overall approach of the project is to demonstrate the feasibility and energy savings benefits of an integrated vehicle thermal management (IVTM) system through modeling with KULI software and experimental validation using a bench testing apparatus. Previously conducted KULI modeling work demonstrated that the IVTM system decreased energy consumption while reducing the number of system components and satisfying the thermal management requirements of the ESS, PEEM, and cabin. An experimental test system was designed and constructed to validate the KULI modeling results previously obtained, as well as further investigate both heating and cooling performance.

To perform the experimental study, a test apparatus capable of evaluating the steady-state and transient performance of an electric vehicle thermal system was constructed. The ultimate goal of the test apparatus is to measure the impact of the IVTM technology on EDV range. In order to demonstrate the effect on vehicle range, a variety of drive cycles will be simulated on the IVTM experimental hardware over a range of ambient air temperatures from -30°C to 43°C.

In addition to measuring the energy efficiency enhancement, the experiment will also investigate control strategies and system configurations. This information will then provide feedback and insight for manufacturers when selecting system designs for vehicle implementation. The expectation is that the results will lead to a future project in which a prototype system is installed into a test vehicle with a design based on the KULI modeling and experimental test bench findings.

Combined Fluid Loop Concept

The CFL concept is an experimental system design that is one possible configuration for an IVTM system. The goal of the CFL design is to provide a platform through which a variety of IVTM operation modes can be tested. Choosing the best IVTM system configuration for a given vehicle will involve making tradeoffs between cost and capability or, in other words, complexity and energy savings. The CFL concept is designed to investigate a number of the possible system configurations in order to quantify their performance. As such, the experimental CFL design is more complex than would be expected for most vehicle applications.

The CFL concept that was developed for bench testing is intended to allow operation of the system with a variety of control strategies under a wide range of operating conditions. The system loads will be representative of a typical passenger BEV. In addition to cooling the cabin in A/C mode, it also enables waste heat recovery from the PEEM and ESS when beneficial, ambient cooling of the PEEM and ESS when possible, active cooling of the ESS as required, and heat pump operation.

In this CFL design, a "secondary loop" configuration is used, in which the vapor compression cycle transfers heat between the R134a refrigerant and the 50%/50% by mass water/ethylene glycol (WEG) liquid coolant mixture. This is accomplished through the use of aluminum brazed plate-type heat exchangers as the condenser and evaporator/chiller. One of the biggest advantages of this design is that it is more compact than the typical automotive design, which uses refrigerant-to-air heat exchangers at the front of the vehicle and within the vehicle console HVAC unit. This also eliminates the necessity for long lengths of permeable hose, reducing refrigerant leakage.

A basic component-level schematic of the CFL system is shown in Figure V-107. The five three-way valves with "S" controllers represent solenoid valves capable of switching the flow between two ports. The two two-way valves with "S" controllers represent simple on/off solenoid valves. The three three-way valves with "Var." controllers represent variable proportioning valves that can modulate the degree of heat exchanger flow bypass. The "PTC Heater" represents a supplementary positive temperature coefficient (PTC) electrical resistance heater.
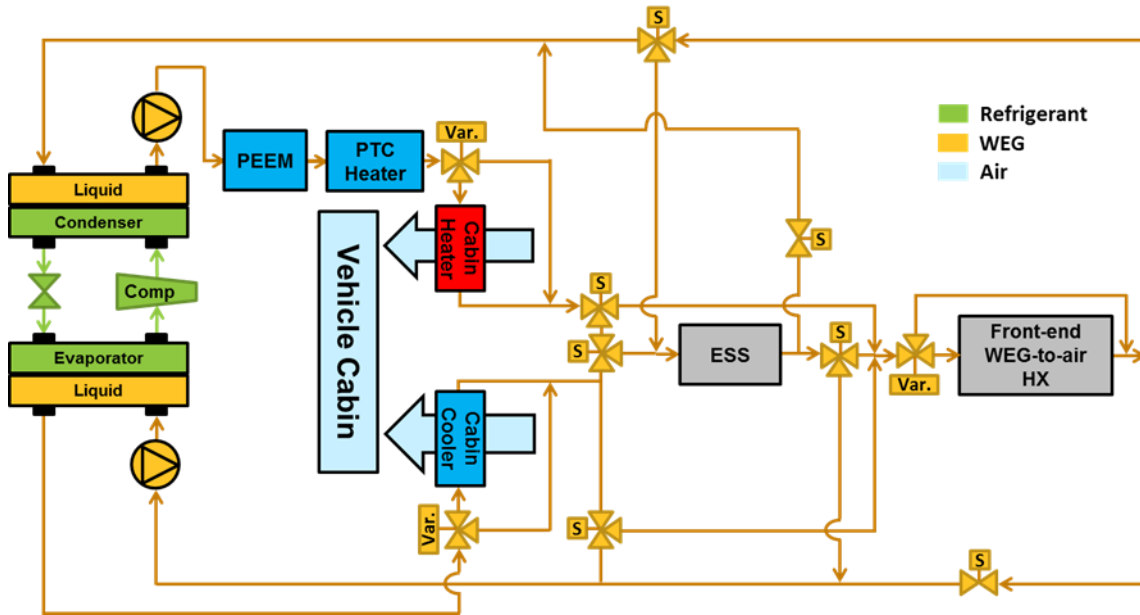
Figure V-107: Combined fluid loop concept schematic.

For the experimental system being tested, Delphi has provided prototype heat exchangers from its "Unitary Heat Pump-A/C" system, as shown in Figure V-108. In addition to the condenser and chiller heat exchangers shown, they have also supplied WEG-to-air heat exchangers for the low-temperature front-end heat exchanger (FEHX), cabin heater core, and cabin cooler core, as represented in

. These heat exchangers are designed to deliver the heating and cooling capacities necessary for a small to mid-size BEV.

Figure V-108: Prototype Delphi "Unitary HPAC" system.

To complete the vapor compression cycle system, a compressor is needed. To most accurately reflect the performance in a passenger BEV, an automotive electric compressor is used instead of the more traditional automotive belt-driven compressor. The compressor was provided by Halla Visteon Climate Control and is shown in Figure V-109. The compressor is a prototype unit that is designed to operate over a wider range of conditions than a typical automotive A/C compressor. The ability to handle extended conditions is necessary for the lower suction pressures and higher pressure ratios inherent to heat pump operation.

Figure V-109: Halla Visteon Climate Control "E-comp" electric compressor.

Test Apparatus

A test apparatus was constructed in order to subject the experimental CFL system to realistic loads and measure the resulting performance. The test apparatus consists of two air loops that are designed to condition and measure the air temperatures and flow rates to the air-side heat exchangers of

the experimental CFL system. A basic schematic of the test apparatus is shown in Figure V-110, and a picture of the completed assembly is shown in Figure V-111.

Figure V-110: Basic overview of bench test apparatus design.

The larger air duct delivers a constant air temperature and variable air flow rate to the FEHX to simulate the outdoor ambient air passing over the front of the vehicle. The smaller air duct delivers a variable air temperature and air flow rate to the cooler core and heater core heat exchangers to simulate the cabin recirculation temperature. The test apparatus also employs two electrical resistance heaters to simulate the PEEM/PTC and ESS heat loads on the experimental CFL WEG system.

Figure V-111: Constructed bench test apparatus.

All of the controlled parameters of the test apparatus are designed to simulate steady-state and transient vehicle

operation. Without an environmental chamber housing the test apparatus, it is capable of operating at test conditions from the ambient room temperature, up to a 43°C outdoor temperature and a 63°C cabin soak temperature. The test apparatus is built on wheels so that it can be moved into an environmental control chamber for low temperature testing. When housed in a low-temperature environmental chamber, the range is extended down to -30°C for both the outdoor and cabin soak temperatures. The intention is that the experimental testing will simulate conditions of operating a vehicle in ambient outdoor conditions from -30°C to 43°C for both city and highway driving.

The instrumented measurement equipment of the test apparatus and CFL system include relative humidity sensors, air flow venturis, barometric air pressure sensors, air-side thermocouples, WEG flow rate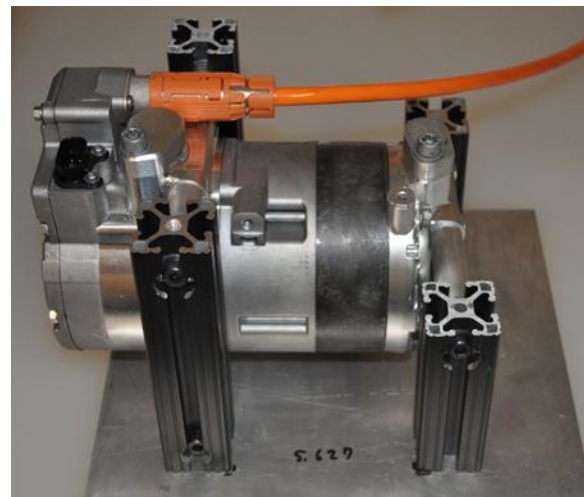 Coriolis meters, WEG thermocouples, refrigerant turbine flow meter, refrigerant thermocouples, and refrigerant pressure transducers. The accuracies of the selected sensors were chosen to maintain propagated uncertainties for the key experimental parameters under 5%. This includes measurements such as flow rates, cooling and heating capacities, and coefficient of performance (COP). The thermocouples were calibrated to obtain accuracies better than 0.3°C.

To put realistic loads on the CFL system, LabVIEW [3] data acquisition and control code was written to simulate the loads and thermal responses of a BEV. Controls integrated into the LabVIEW code will modify the test apparatus

hardware outputs as necessary to maintain the operational conditions specified by the software models. The mathematical models from NREL's Future Automotive Systems Technology Simulator (FASTSim) [4] vehicle simulation software were written into the LabVIEW code to calculate the simulated vehicle's propulsion loads based on the selected drive cycle profile. The FASTSim models provide the waste heat outputs from the PEEM and ESS.

To calculate the expected thermal response of the PEEM and ESS components and their interaction with the CFL WEG system, the heat transfer models created for the KULI model [2] were written into the LabVIEW software. These models interact with the measured performance of the experimental CFL WEG system, i.e., inlet WEG temperatures, such that the temperatures of the simulated components can be calculated. Additionally, a heat transfer model was created for the vehicle cabin to predict the air and interior mass temperatures, including the temperature of the recirculation air of the HVAC unit. The cabin model is a transient, physics-based model developed by Gado [5]. The temperatures calculated by the ESS, PEEM, and cabin thermal models are particularly important as performance metrics because the CFL system must be able to maintain the ESS and PEEM temperatures within specific ranges to maximize performance and reliability, and the cabin temperatures can be used to predict passenger comfort.

Results

Initial testing of the CFL concept in the test apparatus is in progress.

Conclusions and Future Directions

An experimental CFL system was constructed using prototype heat exchangers from Delphi and a prototype automotive electric compressor from Halla Visteon Climate Control. The system is designed to be operated in a variety of different test configurations over a range of operating conditions from very cold to very hot. The CFL system enables cabin A/C, PEEM and ESS waste heat recovery, ambient cooling of the PEEM and ESS, active cooling of the ESS, and heat pump operation.

A mobile test apparatus was constructed to load, control, and measure the performance of the CFL system for a BEV. Mathematical models were integrated into the data acquisition and control system to simulate ESS, PEEM, and cabin loads

due to propulsion and ambient conditions, as well as their thermal responses. The test apparatus imposes these transient loads on the CFL system via hardware in order to measure the energy consumption of the IVTM system. The measured energy consumption will then be used to estimate the improvement in vehicle range.

FY 2013 Publications/Presentations

Rugh, J. P., and Bennion, K., (2012) "Electric Vehicle Thermal Modeling to Assess Combined Cooling Loop Concepts," Proceedings of the SAE Thermal Management Systems Symposium, October 31–November 1, 2012, Scottsdale, AZ.

Acknowledgments

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V.8. Two-Phase Cooling of Power Electronics

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Start Date: October 2010
End Date: September 2014

Objectives

The overall project goal is to enable the U.S. Department of Energy (DOE) Advanced Power Electronics and Electric Motors (APEEM) Program's power electronics specific power, power density, and cost targets to be achieved through the use of two-phase cooling technology. Specific project objectives are listed below.

- Characterize and compare the performance of new candidate refrigerants for use in the two-phase–based cooling systems.
- Explore techniques to enhance two-phase heat transfer coefficients and critical heat flux (i.e., dry out).
- Demonstrate a compact, inverter-scale passive two-phase cooling system capable of dissipating automotive power electronic heat loads. Quantify the system's metrics including thermal performance, coefficient-of-performance, mass, and volume and compare them those of conventional automotive power electronics cooling systems.

Technical Barriers

Two-phase cooling is well known to provide very high heat transfer capacity as compared to other forms of cooling [1]; however, concerns regarding reliability and cost of two-phase–based cooling systems hinder their implementation within automotive-based applications. In this project, we attempt to demonstrate a two-phase cooling solution for automotive power modules based on a passive and indirect cooling strategy. The indirect cooling strategy eliminates direct contact of the refrigerant with the electronics and thus eliminates

material compatibility issues. Moreover, this approach also eliminates electrical feed-through penetrations that may pose a refrigerant leakage potential. The passive approach (i.e., no compressor or pump) simplifies the system, which has implications for reduced cost and increased efficiency. Although not the conventional method of cooling automotive power electronics, passive two-phase cooling solutions have been used to cool power electronic components (Gate-Turn-Off thyristors) in mining haul truck and high-speed train systems [2-5].

Technical Targets

This project aims to enable achieving the DOE APEEM targets listed below by significantly improving thermal management:

- Power Density
- Specific Power
- Efficiency
- Cost.

Accomplishments

- We fabricated a proof-of-concept passive two-phase cooling system (evaporator and condenser) designed to cool six Delphi discrete power modules. We experimentally demonstrated that the cooling system could dissipate at least 2.7 kW of heat with 250 mL (330 grams) of the refrigerant hydrofluorocarbon (HFC)-245fa.
- We identified techniques to improve the thermal performance and reduce the weight and size of the evaporator. A Record of Invention describing these innovations was submitted. The new evaporator design combined with an improved condenser will constitute the second-generation power electronics two-phase cooling system. Tests are planned to fully characterize the performance of this system.
- We initiated experiments to evaluate the long-term reliability of enhanced surface coatings.

Introduction

An efficient thermal management strategy can be an effective means of reducing the size and cost of electronics as well as improving performance and reliability. In this project, we are evaluating two-phase heat transfer as a means of cooling automotive power electronics. The high heat transfer rates and isothermal characteristics of two-phase heat transfer allow for increased power density and specific power, which may enable achieving the DOE APEEM Program technical targets. The intent is to demonstrate superior thermal performance, increased efficiency, reduced weight and

volume with the two-phase cooling system(s) developed. Passive (pump-less) two-phase systems with an air-cooled condenser will be developed due to their inherent efficiency and simplicity.

Approach

In this project, we performed both fundamental and system-level research to evaluate two-phase (boiling/evaporation) heat transfer as a potential power electronics cooling solution. Figure V-112 depicts the strategy for this project. As shown, initial research efforts were focused on characterizing the pool boiling performance of novel coolants/refrigerants as well as investigating promising boiling enhancement techniques. These fundamental research results then fed into the design of the system-level components. The system-level study is focused on developing a prototype passive two-phase cooling system capable of dissipating automotive power electronic heat loads. Small-scale experiments were first conducted to understand and improve the performance of a passive two-phase cooling system (i.e., evaporator and condenser). Current efforts are now focused on demonstrating an inverter-scale passive two-phase system for automotive power modules (Delphi's discrete power switches).

Results

Comparing the Performance of Candidate Refrigerants

Two refrigerants are being evaluated for use in the two-phase–based cooling systems developed in this project: hydrofluoroolefin (HFO)-1234yf and HFC-245fa. HFO-1234yf's nearly identical thermophysical properties to HFC-134a [6] and low global warming potential (GWP = 4) [7, 8] make it the leading candidate as the next generation refrigerant in automotive air-conditioning systems. The use of automotive air-conditioning refrigerants for two-phase cooling of automotive power electronics is an attractive option because these refrigerants are already qualified for automotive use [9], and because it may allow for potential consolidation of cooling systems as proposed by Campbell et al. [10]. In the first year of this project, the boiling heat transfer performance of HFO-1234yf was characterized on both plain and microporous-enhanced surfaces. The results from these tests have been published in Ref. [11]. More recently, we characterized the pool boiling performance of HFC-245fa [12]. HFC-245fa's higher critical temperature, non-flammable nature, and lower operating pressure make it a good candidate for two-phase cooling of electronics. The higher critical temperature ($T_{critical}$ = 154°C) allows for higher operating temperatures, which has implications for reducing the system condenser size.

Characterize Performance of New, Candidate Refrigerants

Define System Requirements and Performance with a Small-Scale System

Demonstrate an Inverter-Scale Passive Two-Phase Cooling System
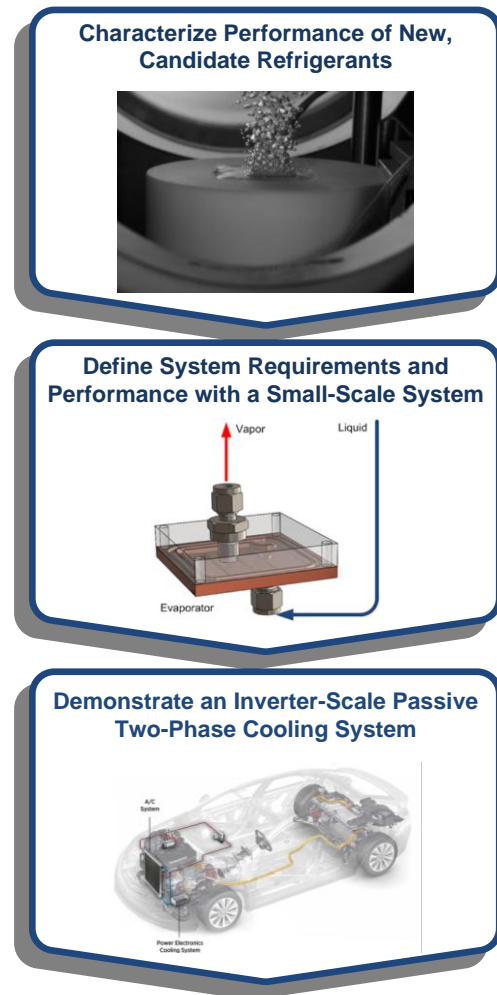
Figure V-112: Flow chart depicting the project approach.

In Figure V-113, the boiling heat transfer coefficients for HFO-1234yf, HFC-245fa, and HFC-134a are plotted versus the saturation temperature. The temperature range evaluated pertains to potential operating temperatures for a two-phase–based cooling system for automotive power electronics. The performance of HFC-134a is provided as a comparison because this refrigerant is currently utilized in automotive cabin cooling systems. The performance for the refrigerants on plain surfaces (sandpaper polished with a surface roughness R_a = 0.3 μm) and microporous-coated surfaces are shown in Figure V-113a and Figure V-113b, respectively. The microporous coating used in these experiments was developed by 3M [13]. The coating, shown in Figure V-114, is composed of copper micrometer-sized particles bonded to the surface to form an approximately 150-μm-thick microporous coating with an estimated 40%–50% porosity.

In boiling heat transfer, heat transfer coefficients are dependent on the imposed heat flux. In this case, the heat transfer values provided in Figure V-113 are taken at a heat flux of 20 W/cm². For the plain surface case, HFC-245fa was found to provide heat transfer values that were approximately 44% and 49% lower than the heat transfer coefficients of HFO-1234yf and HFC-134a, respectively. At the same saturated

temperature, HFC-245fa operates at a lower reduced pressure P_r (P_r = vapor pressure / critical pressure) as compared with the other two refrigerants resulting in its lower performance. The reduced pressure is well known to play a critical role in boiling heat transfer, with boiling heat transfer coefficients increasing with increasing reduced pressure [14, 15].

As shown in Figure V-113b, the use of the 3M microporous coating greatly enhanced heat transfer coefficients for all three refrigerants. Less variation in heat transfer rates between the various refrigerants was observed for the microporous-coated surfaces. With the coatings, all refrigerants produced high transfer coefficients that can exceed 100,000 W/m^2-K. These high heat transfer values enable higher device power densities that may translate to more compact and efficient cooling systems. Increased evaporation within the coating's porous structure, combined with increased nucleation site density, increased wetted area, and capillary wicking within the coating, are believed to be the mechanisms responsible for the microporous-coating heat transfer enhancements.
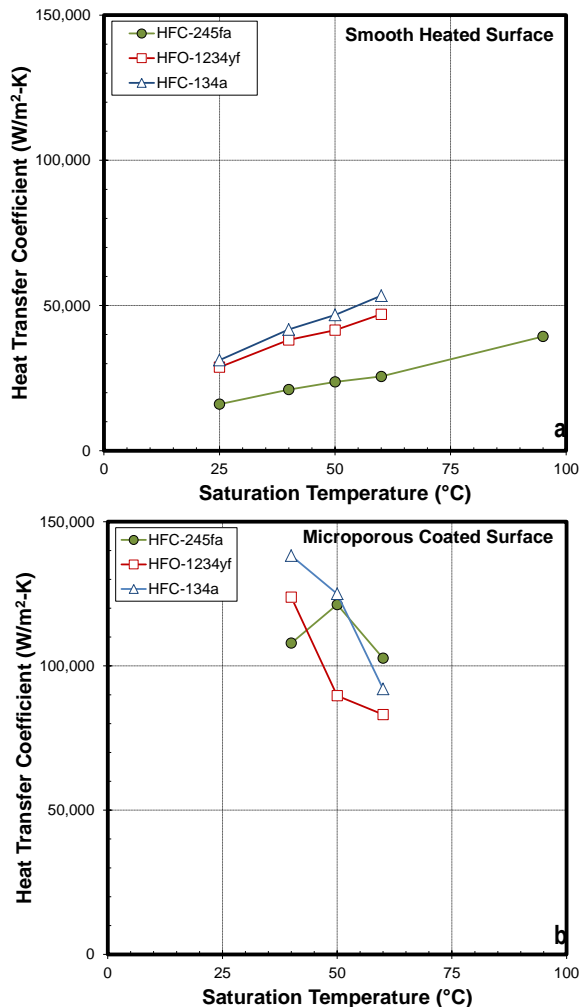

Figure V-113: Heat transfer coefficient values plotted versus the saturation temperature for a sandpaper-polished (a) and microporous coated (b) surfaces. The coefficient values are taken at a heat flux of 20 W/cm^2.

Passive Two-Phase Cooling System

Research has also been conducted to design a complete (evaporator and condenser) passive two-phase cooling system for automotive power electronics. An initial proof-of-concept passive two-phase cooling system has been designed and fabricated. The cooling system was designed to cool six Delphi discrete power modules and has a maximum operating pressure of 1.03 MPa. Structural finite element analysis was used to design the system components for the elevated pressure requirements. Once fabricated, the system was hydrostatically pressure-tested to verify the system's pressure rating. The system's pressure rating allowed it to be charged with refrigerants HFO-1234yf or HFC-245fa.
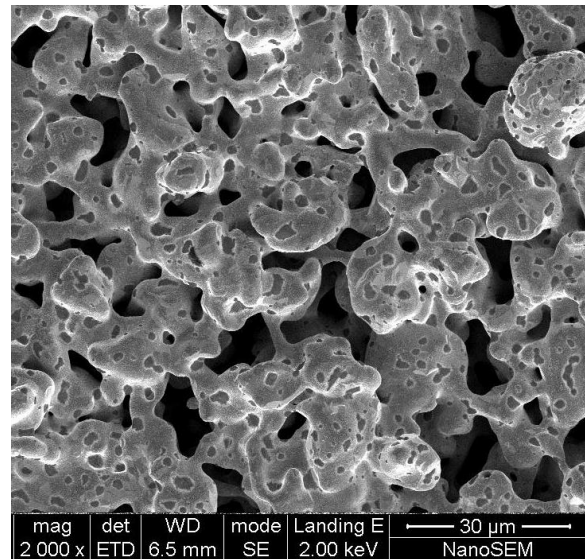

Figure V-114: Scanning microscope image of the 3M boiling enhancement, microporous coating.

The main objective of these tests was to determine if the evaporator could dissipate 3.5 kW of heat with only 250 mL of refrigerant without reaching dry-out. Dry-out occurs at elevated heat fluxes when vapor restricts liquid access to the cooled surface, causing temperatures to significantly increase. The 3.5-kW target is based on the estimated maximum steady-state heat dissipation requirements of automotive power electronics components rated for 55 kW peak power requirements. Prior tests with a smaller-scale cooling system were used to size the volume of the evaporator. Based on those results, it is estimated that it requires ≤ 250 mL of refrigerant to dissipate about 3.5 kW of heat using a passive two-phase cooling configuration.

Equipment and Procedures

The condenser for this proof-of-concept system consisted of ten finned tubes that were connected together at the top and bottom. The total air- and condensate-side surface areas for the condenser were 1 m^2 and 0.05 m^2, respectively. The finned structures on the exterior of the tubes allowed for a larger surface area on the air-side. Calibrated K-type thermocouples were used to measure the inlet-air, liquid, vapor, and heater temperatures. System vapor pressure was

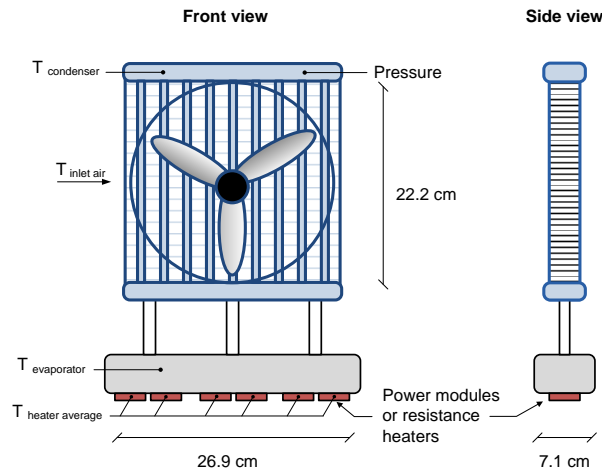measured using an absolute pressure transducer. A schematic of the cooling system is shown in Figure V-115.

Figure V-115: Schematic of the two-phase cooling system.

Existing thermal transient power supplies do not have the capacity to heat the Delphi power modules above about 150 W. Therefore, the initial experiments were conducted using six ceramic resistance heaters in place of the six Delphi power modules. The dimensions of the ceramic heaters (25 mm × 15 mm × 2.5 mm) were similar to those of the Delphi modules. Each heater can generate about 580 W of heat (total power for six heaters: 3.5 kW). The ceramic heaters were externally attached to the evaporator using thermally conductive grease as the thermal interface material. The temperatures of the heaters were measured via thermocouples embedded within the ceramic heaters.

Once the heaters were attached to the evaporator, the air in the system was evacuated using a vacuum pump. Pressure within the system was allowed to decrease to about 10 Pa to indicate that most of the air was removed from the system. The system was then charged with refrigerant via a transfer tube connected above the cooling system. A valve between the transfer tube and the system was opened, allowing the 330 grams (250 mL of liquid) of HFC-245fa to enter the system. Once the refrigerant was transferred, the valve between the transfer tube and the system was closed, and the transfer tube was disconnected from the system. Measurements of the vapor temperature and pressure confirmed saturated conditions verifying that no air was present within the system.

Experimental Results and Discussion

The unit (area-weighted) thermal resistance of the cooling system is plotted versus the heat dissipated in Figure V-116. These results are for an evaporator without any boiling enhancement coating. Because ceramic heaters attached via thermal interface material were used as a substitute for actual power modules attached via bonded interface materials (e.g., thermoplastics, solder), the thermal resistance values are not necessarily indicative of the thermal performance of the cooling system. However, the main objective of these initial

tests was to measure the maximum heat dissipation of the system (i.e., dry-out heat flux).

The heater-to-evaporator resistance is defined per Equation 1:

$$R''_{th,\ evaporator} = \frac{(\overline{T_{htr}} - T_l)}{Total\ power} \times Heater\ area \tag{1}$$

The condenser-to-air resistance is defined per Equation 2:

$$R''_{th,\ condenser} = \frac{(T_v - T_a)}{Total\ power} \times Heater\ area \tag{2}$$

$\overline{T_{htr}}$ is the average temperature of the six heaters. T_l, T_v, and T_a are the liquid, vapor, and inlet-air temperatures. The *total power* is the total heat dissipated by the system, and *heater area* is the total surface area of the six heaters.
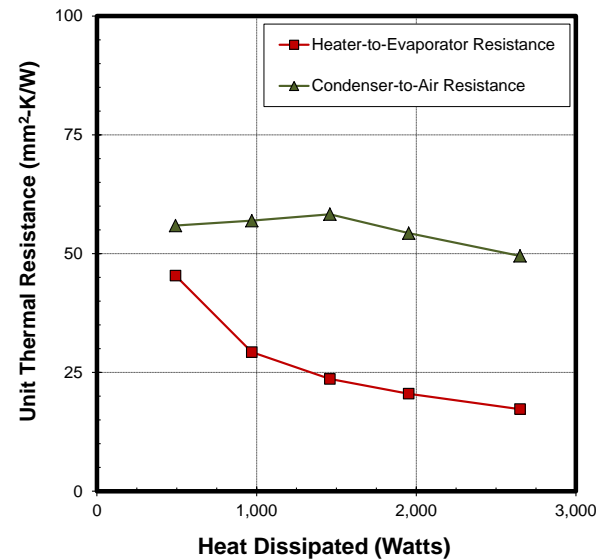

Figure V-116: Area-weighted thermal resistance versus the heat dissipated.

As shown in Figure V-116, the heater-to-evaporator resistance decreases with increasing heat dissipation. This effect is associated with an increased contribution from two-phase heat transfer (i.e., boiling/evaporation) at higher power levels, which improves thermal performance. The system's temperature and pressure increased with increasing heat dissipation. Boiling heat transfer rates will increase with increasing pressure; thus, this effect also contributes to the observed heater-to-evaporator decreasing resistance trend. The thermal resistance of the condenser is less affected by the increasing heat dissipation (i.e., increasing system temperature and pressure).

The maximum heat dissipated by the passive two-phase cooling system was approximately 2.7 kW. This limit on the total heat dissipated was not a thermal limitation, but instead a pressure limitation of the system. Increasing the amount of heat imposed into the system increased the system's temperature and pressure. At the maximum heat dissipated (2.7 kW), the vapor pressure reached the maximum operating

pressure of the system, causing the system to shut down, and prevented testing to higher power levels.

Increasing the condensing capacity of the system will decrease the condenser resistance and allow for operation at lower temperatures and pressures. A new condenser has been designed and is currently being fabricated by a heat exchanger coil manufacturer. The new condenser will be fabricated using common fabrication techniques (i.e., inexpensive) and will have higher fin densities (i.e., increased air-side surface area) as compared to the existing condenser. It has been designed to dissipate 3.5 kW at a maximum inlet-air temperature of 50°C while maintaining device junction temperatures just below 150°C. Computational fluid dynamic simulations were performed to size the condenser (Figure V-117). Compared to the existing condenser, the new condenser's overall dimensions/footprint will be slightly smaller, but its air-side and condensation-side surface areas will be increased by 180% and 130%, respectively. Two new condensers will be fabricated, one with condensation-enhanced surfaces and one with plain/smooth surfaces. Comparing the performance of the two condensers will allow us to evaluate the effect of condensation enhancement techniques on a passive two-phase cooling system. Condensation-side enhancements have the potential to improve performance and reduce the size and weight of the condenser.
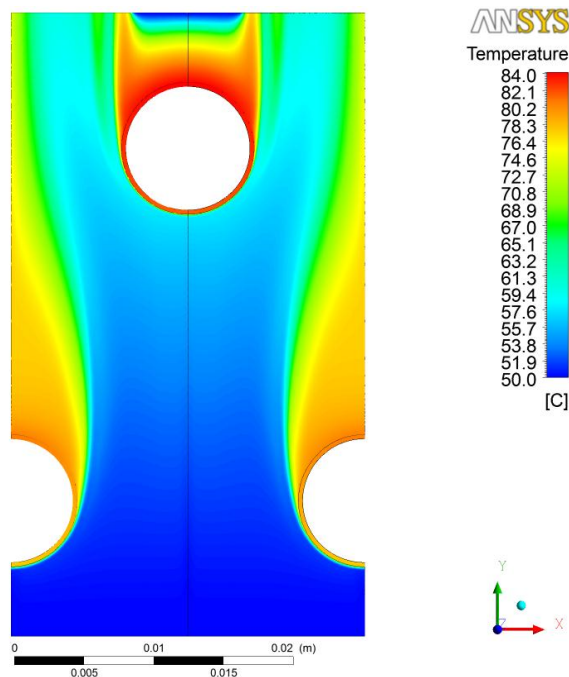

Figure V-117: Computational fluid dynamics air temperature contours.

Techniques to improve the evaporator performance and reduce its size have been identified, and a Record of Invention has been submitted. The techniques incorporate features to reduce the evaporator resistance while utilizing low-cost fabrication techniques and materials (e.g., aluminum). A computer-aided-design model of the Delphi power modules mounted on the improved evaporator design was generated

and incorporated all the thermal resistance interfaces (i.e., solder layer and bonded interfaces). The model was then imported into ANSYS Workbench for thermal analysis. Finite element simulations combined with experimentally measured heat transfer coefficient values taken from the fundamental research were used to evaluate the performance of this advanced evaporator design.

The unit/area-weighted thermal resistance results (junction-to-liquid) as predicted by finite element analysis are provided in Table V-11. The Delphi module insulated gate bipolar transistor's area and temperature (i.e., junction temperature) were used to calculate the thermal resistance values. Two evaporator designs were analyzed: aluminum based and copper based. For comparison, the thermal resistance values (junction-to-liquid) of state-of-the-art automotive power modules are also shown in Table V-11. The thermal resistance values of the aluminum (i.e., 23 mm^2-K/W) and copper (i.e., 17 mm^2-K/W) evaporators are about 33% and 48% lower, respectively, than that of the dual-side cooled 2008 Lexus power module. These reductions in the thermal resistance have the potential to increase power densities by 44%–80%. Moreover, the passive cooling approach also has implications for increasing the system efficiency.

Table V-11: Unit thermal resistance (junction-to-liquid) values for the advanced evaporator design per finite element simulations. Automotive power module thermal resistance values are provided for reference.

	Nissan Leaf [1]	Toyota Prius (2010) [1]	Lexus Hybrid (2008) [2]	**Passive Two-Phase Advanced Design**
Unit Thermal Resistance R"$_{th}$ (mm^2-K/W)	52	47	33	**17-23**
	Single-side cooled	Dual-side cooled		

[1] Liang [16]

[2] Sakai et al. [17]

Enhanced Surface Reliability Studies

An experimental system has been fabricated and procedures have been established to experimentally evaluate the long-term reliability of boiling enhancement coatings. The objective for these experiments is to evaluate for coating delamination and its effect on thermal performance. The coating evaluated for these tests is the 3M microporous coating shown in Figure V-114.

For these experiments, three coated samples are housed within a pressure vessel charged with refrigerant HFC-245fa. An image of the samples submerged in refrigerant within the vessel is provided in Figure V-118. A schematic of a sample is provided in Figure V-119. As shown, a cartridge heater is inserted into each copper sample to provide the heating capacity. Two calibrated (36 average wire gauge) K-type thermocouples are embedded within the 10-mm-diameter length of the samples to allow for calculation of the total heat and surface temperature, assuming one dimensional and

steady-state heat transfer. The total heat and the surface temperature combined with the refrigerant liquid temperature are then used to calculate an average two-phase heat transfer coefficient for the coated surface.
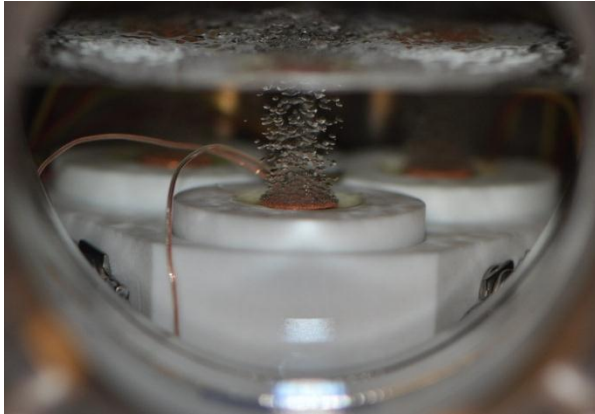

Figure V-118: Picture of boiling occurring on one of the coated samples.
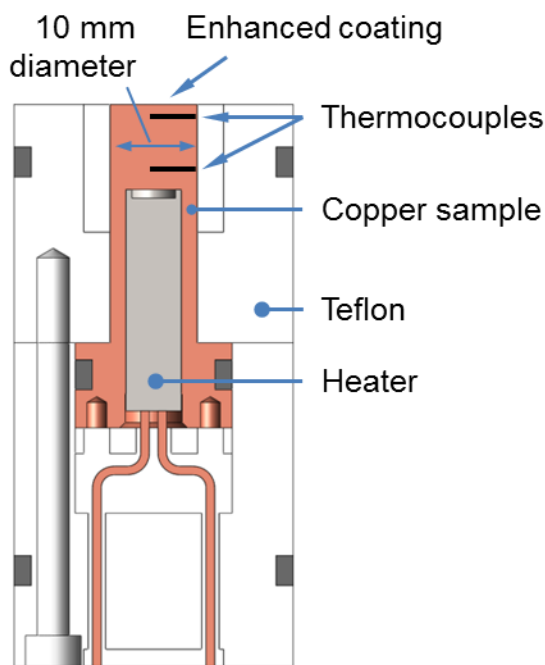

Figure V-119: Schematic of the enhanced surface sample.

The testing procedures involve heating one sample at a time for a total of five minutes. Approximately 15 W/cm^2 are dissipated from the coated surface—enough heat to generate full nucleate boiling. Due to the small size of the samples, steady-state temperatures are typically achieved within a minute, but heat is maintained for a total of five minutes. The entire testing process is automated and operates unattended. The process is controlled via a LabVIEW program and dedicated computer, data acquisition system, and power supply.

To date, the samples have been subjected to approximately 8,000 on/off heating cycles. Thus far, results indicate some degradation in performance; however, the

degradation is believed to be associated with contaminants collecting on the porous sample surface and not coating delamination. Evidence of some fouling on the surfaces was visually observed when samples were removed from the vessel. The source of the contaminants could be either from residual solder flux on the various thermocouple connections or contaminants within the sample that were not removed in the initial cleaning process. As stated before, the objective for these experiments is to evaluate for coating delamination. The samples and system are currently being cleaned. Once this process is complete, the reliability experiments will be restarted.

A parameter monitored during these tests is boiling incipient behavior. In boiling heat transfer, some amount of superheat (i.e., temperature of the heated surface minus the saturated/boiling temperature of the fluid) is required to initiate boiling on a heated surface. Ideally, the superheat required to initiate boiling should be low to prevent wide temperature cycling of the sample (e.g., electronic device being cooled). Microporous-coated surfaces are effective at reducing the superheat required to initiate boiling; however, their ability to maintain this performance under long-term use conditions is unknown. Although the temperature sampling rate used for these tests (measurement every ½ second) cannot measure every temperature (i.e., cannot sample at a continuous rate) during the heating process, based on the data collected we can conclude the following. The results suggest that for all three samples the superheat essentially remained unchanged for the entire 8,000 cycles. Moreover, the maximum temperature overshoot (sample's maximum temperature just prior to boiling incipience minus the sample's steady-state temperature) was observed for sample one and was approximately 3.5°C. In other cases (samples two and three), there was negligible temperature overshoot.

Conclusions and Future Directions

Future Directions

Work is currently underway to fabricate the advanced two-phase power electronics cooling system that consists of the new condenser and improved evaporator. Tests are planned to thoroughly characterize the thermal performance of the advanced design. The next steps for this project are summarized below.

1. Characterize the performance of the cooling system using refrigerants HFC-245fa and HFO-1234yf.

2. Understand the effect of inclination on performance by varying the inclination of the cooling system and measuring its thermal performance. These tests will evaluate the effect of vehicle inclination (e.g., climbing a hill) on the cooling system's performance.

3. Quantify the system's performance metrics (thermal performance, coefficient of performance, volume, weight) and compare with the performance metrics of a typical water/ethylene-glycol–cooled automotive system.

Conclusions

Research has been conducted to design, fabricate, and characterize the performance of a passive two-phase system. The major conclusions for this study are summarized below.

1. A proof-of-concept indirect, passive, two-phase cooling system (evaporator and air-cooled condenser) was fabricated. Experiments demonstrated that the system can dissipate at least 2.7 kW of heat with only 250 mL (330 grams) of HFC-245fa.

2. An advanced two-phase cooling system has been designed and is currently being fabricated. The new system consists of a custom-fabricated condenser and an improved evaporator. The evaporator incorporates features to reduce its thermal resistance and size while utilizing low-cost fabrication techniques and materials (e.g., aluminum). A Record of Invention detailing these enhancement techniques has been submitted. The new system is designed to dissipate 3.5 kW of heat at a maximum air-inlet temperature of 50°C while maintaining junction temperatures below 150°C. Finite element analysis of this advanced design indicates that the system can reduce the thermal resistance by as much as 48% as compared with the state-of-the-art automotive systems. The thermal resistance reductions have the potential to increase power density by as much as 80%.

3. Experiments to evaluate the reliability of boiling enhancement coatings have been initiated. To date, samples have been exposed to about 8,000 on/off cycles. Results indicate no delamination of the coated surfaces and no change to the boiling incipient superheat behavior.

Nomenclature

P	pressure
R''_{th}	area-weighed/unit thermal resistance, mm^2-K/W
T	temperature, °C
Subscripts	
a	air
htr	heater
l	liquid
r	reduced (e.g., reduced pressure)
v	vapor

FY 2013 Publications/Presentations

1. Moreno, G., Narumanchi, S., and King, C., 2013, "Pool Boiling Heat Transfer Characteristics of HFO-1234yf on Plain and Microporous-Enhanced Surfaces," *ASME Journal of Heat Transfer*, 135(11), pp. 111014.

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4. Moreno, G., Jeffers, J., Narumanchi, S., and King, C., "Passive Two-Phase Cooling of Automotive Power Electronics using Refrigerant HFO-1234yf," *Proc. SAE Thermal Management Systems Symposium*, Scottsdale, AZ, USA, October 2012.

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