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Acronyms and Abbreviations

2D	two dimensional	DOE	U.S. Department of Energy
3D	three dimensional	DPT	double pulse tester/testing
ac	alternating current	DSC	differential scanning calorimeter
Adc	amps direct current	DUT	device under test
AFM	atomic force microscopy	ECI	Electronic Concepts, Inc.
ANSYS	modeling and simulation workbench	EDS	energy dispersive spectroscopy
APEEM	Advanced Power Electronics and Electric Motors (program, DOE)	EDV	electric drive vehicle
ASTM	American Society for Testing and Materials	EDX	energy dispersive x-ray spectroscopy
AT	automatic transmission	EETT	Electrical and Electronics Technical Team (U.S. Drive)
bcc	body centered cubic	EM	electric motor
BHT	3,5-di- <i>t</i> -butyl-4-hydroxytoluene	emf	electromotive force
BIC	best-in-class	EMI	electromagnetic interference
BIM	bonded interface material	ESC	electro-slag casting
BNC	Bayonet-Neill-Concelman (connector)	ESL	equivalent series inductance
BNC	Birk Nanotechnology Center	ESR	equivalent series resistance
BOPP	baseline biaxially-oriented polypropylene	ESS	energy storage system
BREM	beyond rare earth magnets	ETS	electric traction system
C-SAM	C-mode scanning acoustic microscope	EV	electric vehicle
CAN	controller area network	EWG	ethylene water glycol
Cdg	drain-to-gate capacitance	FE	finite element
Cds	drain-to-source capacitance	FEA	finite element analysis
CF-trans-qZSI	current-fed trans-quasi-ZSI	GA	genetic algorithm
CF-trans-ZSI	current-fed trans-ZSI	GE	General Electric
CFD	computational fluid dynamics	GOSS	grain oriented silicon steel
CHF	critical heat flux	GUI	graphical user interface
COP	coefficient of performance	GWP	global warming potential
CSD	chemical solution deposition	HALT	highly accelerated lifetime tests
CSI	current source inverter	HD	hydrogen decrepitation
CTE	coefficient of thermal expansion	HEV	hybrid electric vehicle
CVD	chemical vapor deposition	HSG	hybrid starter-generator
DBA	direct bonded aluminum	HVAC	heating, ventilation and air conditioning
DBC	direct bonded copper	ICE	internal combustion engine
dc	direct current	ID	inner diameter
DFT	density functional theory	IGBT	insulated gate bipolar transistor
		IMFP	isolated multiple flux path
		IMMD	integrated modular motor drive

INV/CONV	inverter/converter	PWM	pulse width modulated/modulation
IPM	interior permanent magnet	PoF	physics of failure
JBS	junction barrier Schottky	PoP	Proof-of-principle
JEDEC	Joint Electron Device Engineering Council	PWB	printed wire board
KULI	thermal management system for automotive applications	R&D	research and development
LCR	inductance, capacitance and resistance	R-L	inductor-resistor
LFE	laminar flow element	RB	reverse-blocking
LNO	LaNiO ₃	RE	rare earth
Lp	parasitic inductance	regen	regenerative braking
MEC	magnetic equivalent circuit	rms	root mean square
M/G	motor/generator	Rp	parasitic resistance
mmf	magnetomotive force	SEM	scanning electron microscopy
MOSFET	metal-oxide semiconductor field-effect transistor	SF	specific force
MRE	mixed rare earth	SOA	state of the art
NREL	National Renewable Energy Laboratory	SJT	super junction transistor
NFC	novel flux coupling	SP	specific power (peak)
NIH	number-in-hand	SPICE	Simulation Program with Integrated Circuit Emphasis
Nm	Newton meter	SPM	surface permanent magnet
OD	outer diameter	SSRL	Stanford Synchrotron Research Laboratory
ORNL	Oak Ridge National Laboratory	SR	switched reluctance
OVT	Office of Vehicle Technologies	SRM	switched reluctance motor
PCU	power control unit	T3Ster	Transient Thermal Tester
PD	power density (peak)	TC	thermal conductivity
PE	power electronics	TEM	transmission electron spectroscopy
PEEM	Power Electronics and Electric Machines (subprogram, ORNL)	THD	total harmonic distortion
PEI	polyetherimide	TIM	thermal interface material
PEM	power electronics module	Tj	junction temperature
PEPL	Power Electronics Packaging Laboratory (ORNL)	Tjmax	maximum junction temperature
PEV	plug-in electric vehicle	TMC	Toyota Motor Company
PF	power factor	TSDPSR	total switching device power stress ratio
PFC	power factor correction	TSI	Thermal Anemometry Systems
PHEV	plug-in hybrid electric vehicles	TXV	thermal expansion valve
PID	proportional-integral-derivative	U.S. DRIVE	Driving Research and Innovation for Vehicle efficiency and Energy sustainability (cooperative research effort between DOE and industry partners)
PLZT	(Pb,La)(Zr,Ti)O ₃	UW	University of Wisconsin
PM	permanent magnet	V2G	vehicle-to-grid
PMSM	permanent magnet synchronous motor		

Vac	volts of alternating current	VSI	voltage source inverter
Vdc	volts of direct current (operating voltage)	VTP	Vehicle Technologies Program (DOE)
Vds	drain-to-source voltage	WBG	wide bandgap
Vgs	gate-to-source voltage	WEG	water-ethylene glycol
VSA	vehicle systems analysis	XRD	x-ray diffraction
VSATT	Vehicle Systems Analysis Technical Team (U.S. Drive)	ZCSI	Z-source current source inverter
		ZSI	Z-source inverter

I. Introduction

The U.S. Department of Energy (DOE) announced in May 2011 a new cooperative research effort comprising DOE, the U.S. Council for Automotive Research (composed of automakers Ford Motor Company, General Motors Company, and Chrysler Group), Tesla Motors, and representatives of the electric utility and petroleum industries. Known as U.S. DRIVE (Driving Research and Innovation for Vehicle efficiency and Energy sustainability), it represents DOE's commitment to developing public-private partnerships to fund high risk–high reward research into advanced automotive technologies. The new partnership replaces and builds upon the partnership known as FreedomCAR (derived from “Freedom” and “Cooperative Automotive Research”) that ran from 2002 through 2010 and the Partnership for a New Generation of Vehicles initiative that ran from 1993 through 2001.

The Advanced Power Electronics and Electric Motors (APEEM) program within the DOE Vehicle Technologies Program (VTP) provides support and guidance for many cutting-edge automotive technologies now under development. Research is focused on developing revolutionary new power electronics (PE), electric motor (EM), thermal management, and traction drive system technologies that will leapfrog current on-the-road technologies. The research and development (R&D) is also aimed at achieving a greater understanding of and improvements in the way the various new components of tomorrow's automobiles will function as a unified system to improve fuel efficiency.

In supporting the development of advanced vehicle propulsion systems, the APEEM program has enabled the development of technologies that will significantly improve efficiency, costs, and fuel economy.

The APEEM program supports the efforts of the U.S. DRIVE partnership through a three phase approach intended to

- identify overall propulsion and vehicle related needs by analyzing programmatic goals and reviewing industry's recommendations and requirements and then develop the appropriate technical targets for systems, subsystems, and component R&D activities;
- develop and validate individual subsystems and components, including EMs and PE; and
- determine how well the components and subsystems work together in a vehicle environment or as a complete propulsion system and whether the efficiency and performance targets at the vehicle level have been achieved.

The research performed under this program will help remove technical and cost barriers to enable the development of technology for use in such advanced vehicles as hybrid electric vehicles (HEVs), plug-in HEVs (PHEVs), battery electric vehicles, and fuel-cell-powered automobiles that meet the goals of the VTP.

A key element in making these advanced vehicles practical is providing an affordable electric traction drive system. This will require attaining weight, volume, efficiency, and cost targets for the PE and EM subsystems of the traction drive system. Areas of development include

- novel traction motor designs that result in increased power density and lower cost;
- inverter technologies involving new topologies to achieve higher efficiency with the ability to accommodate higher temperature environments while achieving high reliability;
- converter concepts that use methods of reducing the component count and integrating functionality to decrease size, weight, and cost;
- new onboard battery charging concepts that result in decreased cost and size;
- more effective thermal control through innovative packaging technologies; and
- integrated motor-inverter traction drive system concepts.

Thermal management of electronics and electronic systems represents a major technical barrier to achieving specific APEEM technical targets. Excessive temperature, temperature cycling, and power cycling can degrade the performance, life, and reliability of power electronic components. Advanced thermal management technologies can enable higher power density and higher specific power as well as lowering system costs by facilitating the use of lower-cost package configurations and lower-cost materials with minimal impact on performance and reliability.

The Thermal Management of Advanced Power Electronics and Electric Motors research activity is focused on developing thermal management technologies that enable advanced power electronics and electric motor technologies that are efficient, small, lightweight, low cost, and reliable. Specifically, we are concerned with addressing and overcoming any and all thermal barriers to these systems within the systems context of the entire vehicle—ultimately working towards a total vehicle electric traction drive system that is low-cost, small, lightweight, reliable, effective, and efficient.

These thermal management and reliability enhancements will permit U.S. industry to improve the range and reduce the purchase, operating and maintenance costs of electric vehicles leading to a widening of their acceptance by the public. The larger volume of advanced fuel saving vehicles manufactured in the United States will result in higher domestic employment, while significantly reducing the trade deficit by reducing the amount of imported oil.

DOE's continuing R&D into advanced vehicle technologies for transportation offers the possibility of reducing the nation's dependence on foreign oil and the negative economic impacts of crude oil price fluctuations. It also supports the Administration's goal of deploying 1 million PHEVs by 2015.

II. Power Electronics Research and Technology Development

II.1 Wide Bandgap Materials

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- Perform an assessment of WBG technology to determine when the viable market introduction for automotive use will occur.
- Perform inverter simulations with selected device models: The inverter simulations will be performed to evaluate the impact of the device performance at system level.

Major Accomplishments

- Acquired, tested, and characterized SiC metal-oxide semiconductor field-effect transistors (MOSFETs), SiC super junction transistors (SJT), and SiC junction barrier Schottky (JBS) diodes.
- Completed the WBG technology assessment for market viability.
- Simulated the performance of the SiC MOSFET and diode over the US06 drive cycle.

Objectives

- Overall objectives
 - Test and evaluate new technology devices as they become available to maintain a library of wide bandgap (WBG) device performance characteristics.
 - Assess the system level impacts of WBG semiconductor devices on hybrid electric vehicles.
- FY 2012 objectives
 - Evaluate device performance by testing and characterizing devices and assessing their performance through simulations.
 - Perform an assessment of WBG technology to understand the performance trends, the cost time line, the system level benefits, and how this technology will help to meet U.S. DRIVE targets.

Approach

- Evaluate device performance: Acquire, test, and characterize newer technology WBG power devices including the following:
 - static characteristic tests,
 - dynamic characteristic tests, and
 - behavioral modeling.

Future Direction

- State-of-the-art and new technology WBG power devices will be acquired, tested, and characterized.
- SPICE models of the devices will be developed.

◇ ◇ ◇ ◇ ◇

Technical Discussion

I. Device Testing

The new WBG devices acquired this year were SiC MOSFETs, SiC JBS diodes, and SiC SJTs. On-state characteristics and switching energy losses of the devices were obtained over a wide temperature range. The test results for these devices are presented in the following sections. All the devices obtained were experimental samples.

1. 1,200 V, 30 A SiC MOSFET

Both static and switching characteristics of a 1,200 V, 30 A SiC MOSFET have been tested. Figure II - 1 shows the forward characteristic at different temperatures. The on-state resistance has also been calculated and is shown in Figure II - 2. One point to note is that the SiC MOSFET does not have the negative temperature coefficient around 50°C that was noticed in samples from previous years.

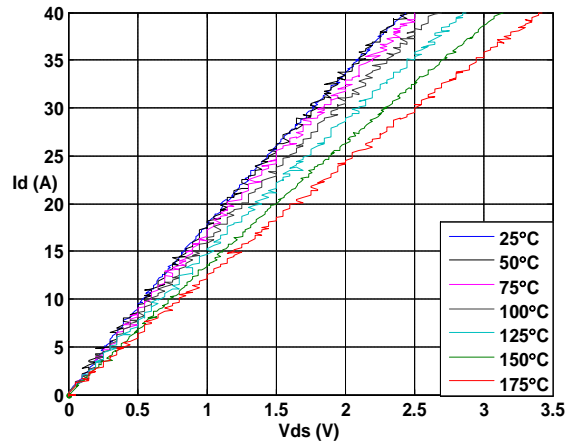


Figure II - 1: Forward characteristic of 1,200 V, 30 A MOSFET.

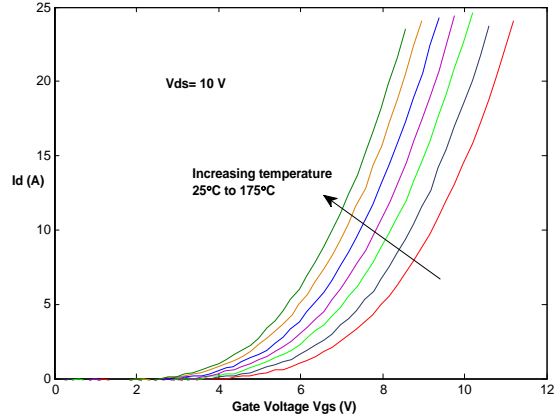


Figure II - 3: Transfer characteristic of 1,200 V, 30 A MOSFET.

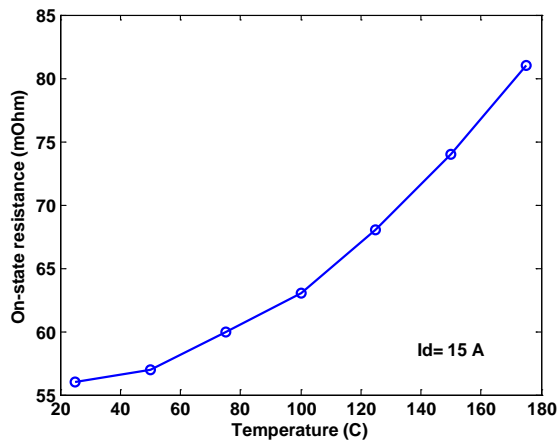


Figure II - 2: On-state resistance of 1,200 V, 30 A MOSFET.

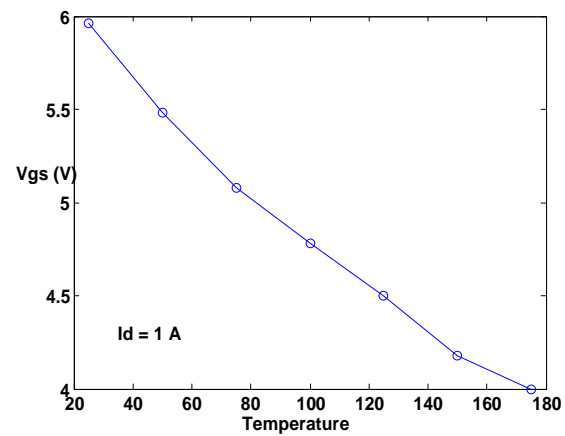


Figure II - 4: Threshold voltage of 1,200 V, 30 A MOSFET.

Figure II - 3 shows the transfer characteristics of the device over a wide temperature range at $V_{ds} = 10$ V. Figure II - 4 shows the threshold voltage obtained from the transfer curves. The threshold voltage decreases as temperature increases.

The turn-on and turn-off energy losses were obtained with a load inductance of $140 \mu\text{H}$, and a 1,200 V, 30 A SiC JBS diode was used as the clamping diode in the circuit. The gate driver used for this testing was a commercial gate driver, IXDD414. The gate voltage was varied from +15 V to -5 V. The data were obtained at $325 V_{dc}$ for various currents at temperatures from 25°C to 175°C. The total energy losses increase with increase in current; however, losses do not change much with increases in temperature (Figure II - 5).

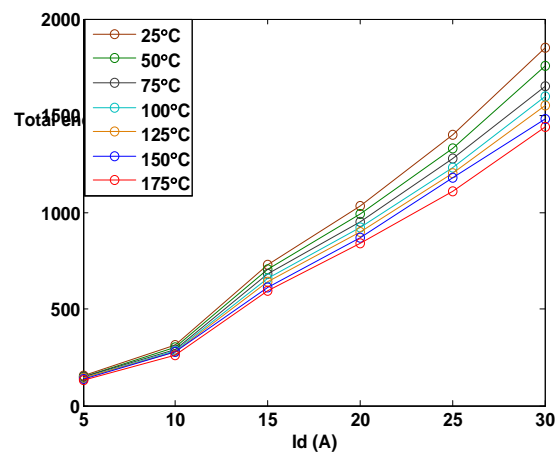


Figure II - 5: Switching losses of 1,200 V, 30 A MOSFET at 325 V.

2. 1,200 V, 100 A SiC MOSFET

Both static and switching characteristics of a 1,200 V, 100 A SiC MOSFET were obtained over a wide temperature range. Figure II - 6 shows the forward characteristic at different temperatures. The on-state resistance has also been calculated and is shown in

Figure II - 7. Again it should be noted that this SiC MOSFET does not have a negative temperature coefficient around 50°C, which was noticed in low current samples from previous years. Figure II - 8 shows the transfer characteristics of the device over a wide temperature range at $V_{ds} = 10$ V. Figure II - 9 shows the threshold voltage obtained from the transfer curves. The threshold voltage decreases as temperature increases. The switching loss data were obtained at 600 V_{dc} for various currents at temperatures ranging from 25°C to 175°C using a double pulse testing circuit. The gate voltage was varied from +15 V to -5 V. The total energy losses increase with increases in current; however, the losses do not change much with increases in temperature (Figure II - 10).

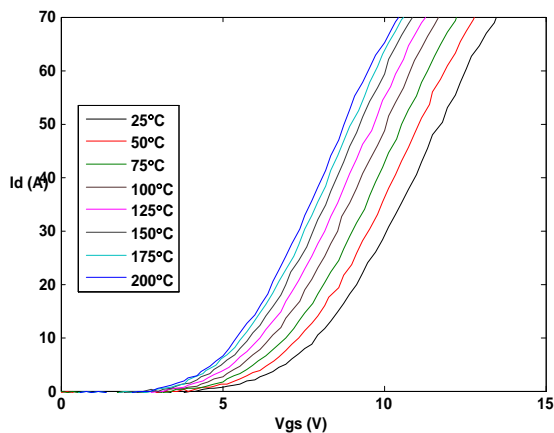


Figure II - 8: Transfer characteristics of 1,200 V, 100 A MOSFET.

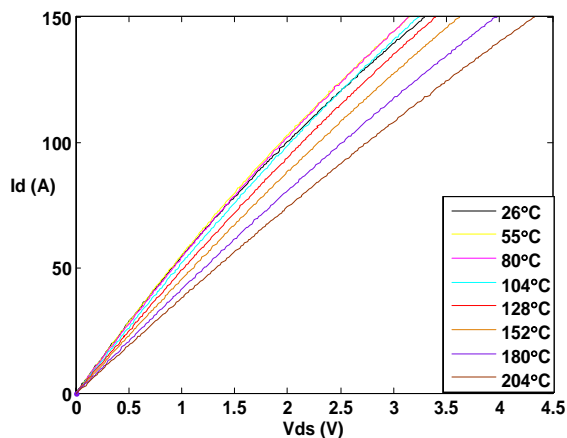


Figure II - 6: Forward characteristic of 1,200 V, 100 A MOSFET.

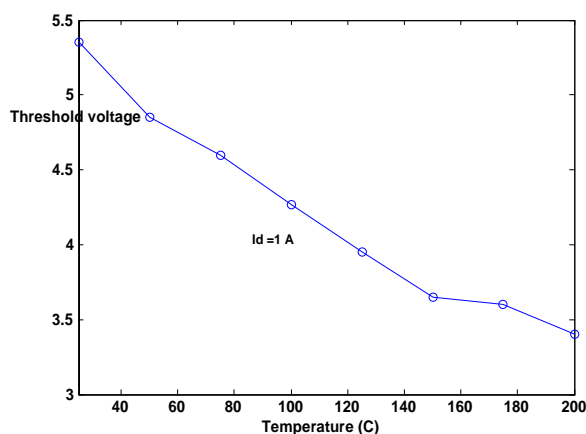


Figure II - 9: Threshold voltage of 1,200 V, 100 A MOSFET.

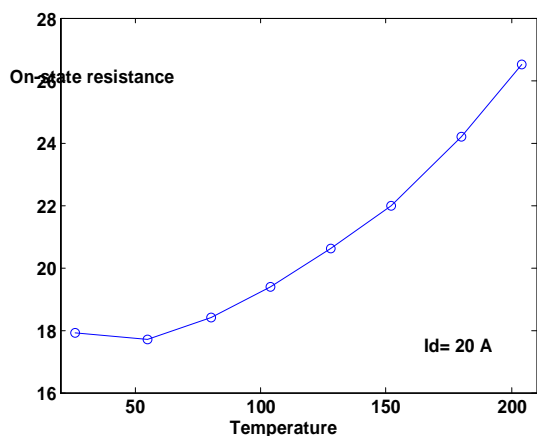


Figure II - 7: On-state resistance of 1,200 V, 100 A MOSFET.

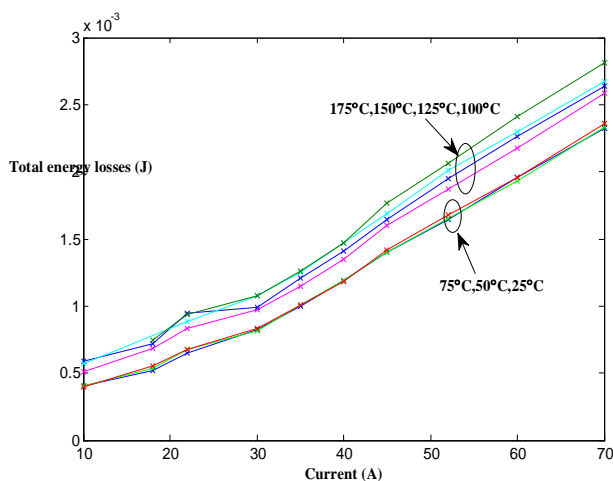


Figure II - 10: Switching losses of 1,200 V, 100 A SiC MOSFET at 600 V and temperatures ranging from 25°C to 175°C.

3. Comparison of 1,200 V, 100 A SiC MOSFET with 1,200 V, 100 A Si IGBT

SiC MOSFET modules in a half bridge configuration with 100 A output current were also tested; however, those

modules had devices paralleled for higher ratings. The 1,200 V, 100 A SiC MOSFET is the first single discrete device with higher current rating that has been tested under this project. This allows for a comparison with the single discrete 1,200 V, 100 A Si insulated gate bipolar transistor (IGBT) to assess the loss difference. The forward characteristics of the Si IGBT and SiC MOSFET are shown in Figure II - 11. The forward voltage drop of the SiC MOSFET is lower than that of the Si IGBT over a temperature range of 25°C to 150°C and for all currents up to 100 A.

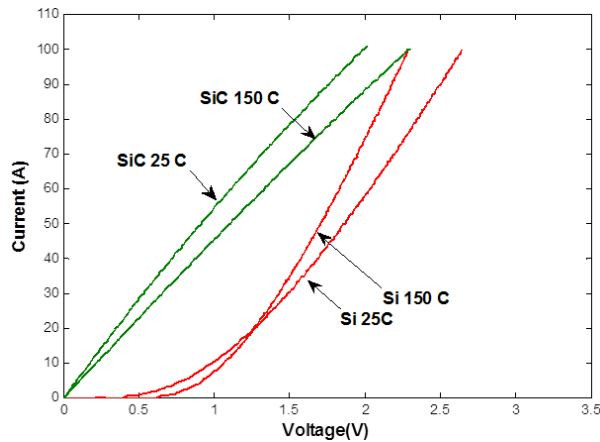


Figure II - 11: Comparison of switching energy losses of a 1,200 V, 100 A SiC MOSFET and a 1,200 V, 100 A Si IGBT at 600 V over a temperature range of 25°C to 150°C.

Switching loss comparisons at 25°C and 150°C are shown in Figure II - 12 and Figure II - 13. The switching losses were obtained with similar gate voltages (+15 V to -5 V). The SiC MOSFET has up to a 50% reduction in losses at 25°C and up to 70% at 150°C. However, it should be noted that the Si IGBT losses include reverse recovery losses of the Si pn diode, which was used as the clamping diode in the test circuit. The SiC MOSFET was tested using a SiC JBS diode.

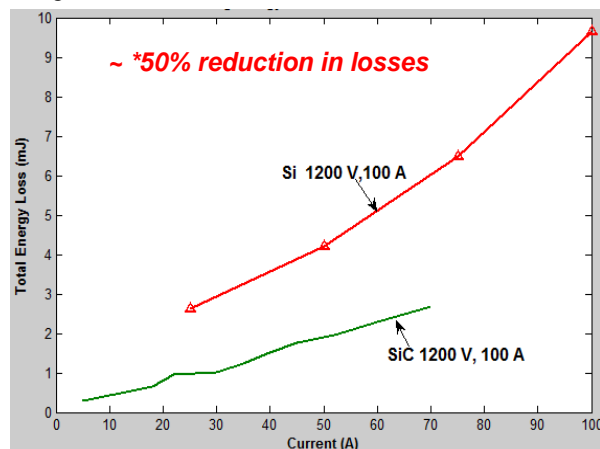


Figure II - 12: Comparison of switching energy losses of a 1,200 V, 100 A SiC MOSFET and a 1,200 V, 100 A Si IGBT at 25°C and 600 V.

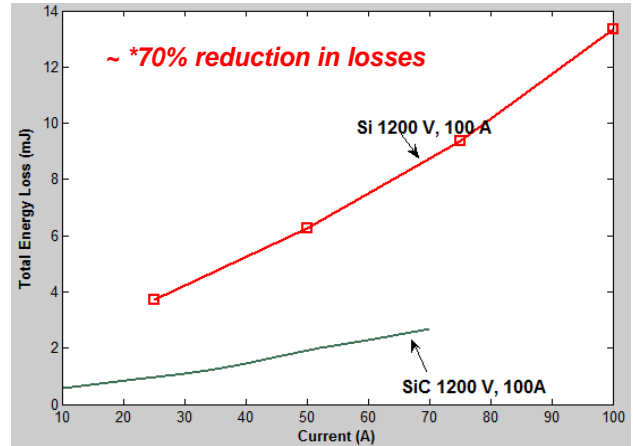


Figure II - 13: Comparison of switching energy losses of a 1,200 V, 100 A SiC MOSFET and a 1,200 V, 100 A Si IGBT at 150°C and 600 V.

4. 1,200 V, 7 A SiC SJT

The SiC SJT is a current-controlled normally off device. Figure II - 14 shows the forward characteristics of the SJT at different temperatures for a 350 mA base current. The gain was calculated for different base currents in the saturation region (shown in Figure II - 14). It can be seen that the gain is decreasing with both temperature and collector current. Figure II - 15 is the on-state resistance of the SJT, which increases with temperature.

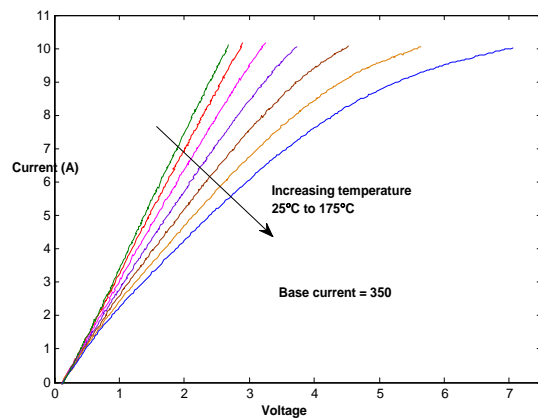


Figure II - 14: Forward characteristic of 1,200 V, 7A SiC SJT.

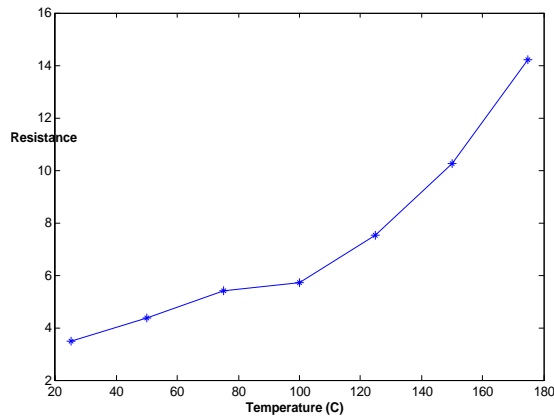


Figure II - 15: On-state resistance of 1,200 V, 7 A SiC SJT.

The turn-on and turn-off energy losses were obtained with a load inductance of 140 μ H, a SiC JBS diode was used as the clamping diode in the circuit. The gate drive requirements for this device are very similar to a bipolar junction transistor. It needs current to stay on and an initial current for charging the capacitor. The data were obtained at 600 V_{dc} for various temperatures from 25°C to 175°C. The total energy losses increase with increases in current; however, the losses do not change much with increases in temperature, similar to other SiC devices (Figure II - 16).

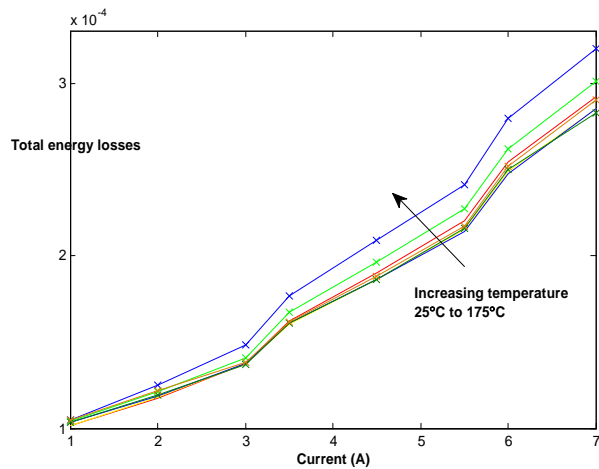


Figure II - 16: Switching losses of 1,200 V, 7 A SiC SJT at 600 V and various temperatures from 25°C to 175°C.

5. 1,200 V, 50A SiC JBS Diode—High temperature test coupon

ORNL obtained a 1,200 V, 50 A bare die JBS diode from a vendor and packaged it to demonstrate the high temperature performance of the die. A test coupon capable of operating up to 250°C and 1,500 V was built and tested (Figure II - 17). This coupon enables static and dynamic measurements of diodes and switches in a single co-pack configuration or in a half bridge configuration and can accommodate die sizes up to 15 mm². Using the test

coupon, static characteristics of a 1,200 V, 50 A SiC JBS diode were obtained over a wide temperature range (25°C–200°C) (Figure II - 18).

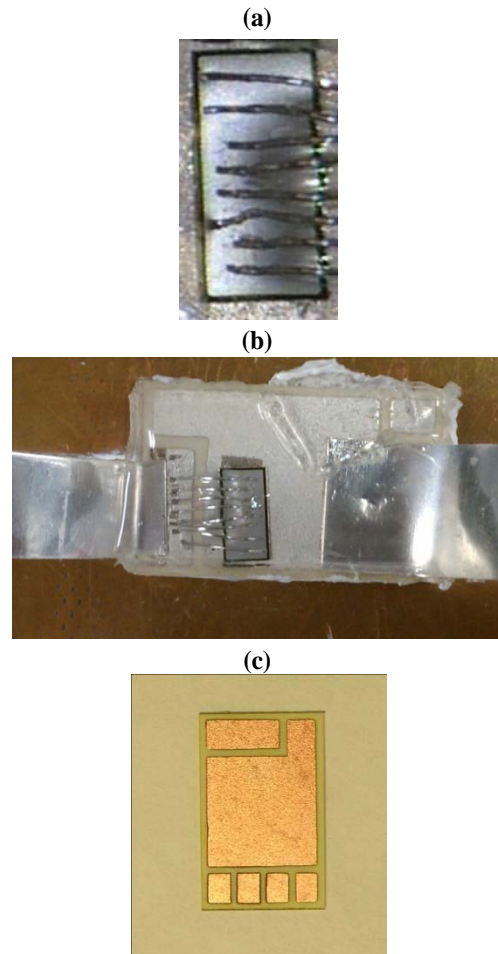


Figure II - 17: Test setup for the 1,200 V, 50 A SiC JBS diode test: (a) the bare JBS diode, (b) the JBS diode packaged in a package developed at ORNL through the VTP packaging project, and (c) the test coupon developed for the co-pack configuration.

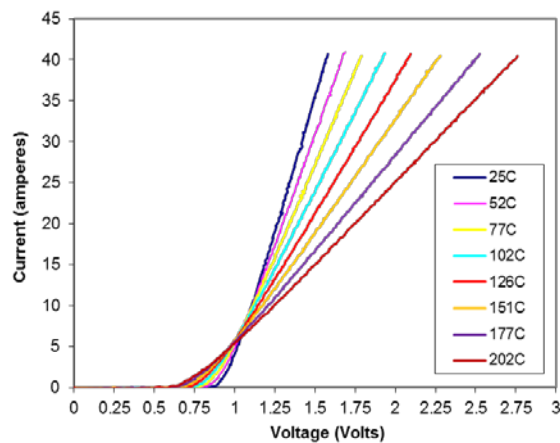


Figure II - 18: Forward characteristic of 1,200 V, 50 A SiC JBS diode.

II. Traction Drive Model

The traction drive model consists of two parts: (1) an electric motor/generator model that computes the current, voltage, and phase angle that will optimally produce 100% of the torque required at each time step and (2) an inverter loss model that computes the temperature dependent device losses associated with the voltages, currents, and frequencies demanded by the motor. The details of the motor model were presented in the FY 2010 annual report.

1. Inverter Loss Model

The temperature dependent conduction loss parameters, on-state resistance and voltage drop, and switching losses were obtained from testing the 1,200 V, 100 A SiC MOSFET and 1,200 V, 100 A SiC JBS diode discrete devices. The details of the inverter model were also presented in the FY 2010 annual report.

2. Simulation Results

The drive model was simulated for the US06 drive cycle with SiC MOSFET and JBS diode models at switching frequencies of 10 kHz and 20 kHz and two different coolant temperatures, 70°C and 105°C. The drive model outputs time dependent, cycle average, and cumulative values of interest for all pertinent parameters. The average inverter efficiency and inverter losses over the drive cycle for 10 and 20 kHz with 70°C and 105°C cooling are shown in Table II - 1.

Table II - 1: Simulation results of traction drive for the US06 drive cycle.

10 kHz		20 kHz	
<i>Inverter efficiency (%)</i>			
70°C	105°C	70°C	105°C
96.74	96.69	94.83	94.8
<i>Inverter energy loss (kJ)</i>			
70°C	105°C	70°C	105°C
117.2	118.7	190.1	195.7

The inverter efficiency corresponds to the losses of devices in the inverter only, and the losses in the boost converter are not included. For 10 kHz operation, the efficiency of the inverter decreased by only 0.05% for the change in coolant temperature from 70°C to 105°C. For 20 kHz operation, the efficiency of the inverter decreased by only 0.03% for the change in coolant temperature from 70°C to 105°C. However, when the switching frequency was increased from 10 kHz to 20 kHz, the efficiency of the all-SiC inverter decreased by 1.96% and 1.89% at 70°C and 105°C coolant temperature, respectively.

Conclusion

Several new SiC MOSFETs, JBS diodes and SJTs were acquired, tested, and modeled. The traction drive was successfully completed, and the simulation results of the all-SiC inverter, developed based on 1,200 V, 100 A SiC MOSFET and JBS diode testing, were presented. The results of the WBG assessment will be presented in a separate report.

Patents

None.

Publications

None.

References

None.

II.2 Power Device Packaging

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Objectives

- Overall objectives
 - Identify the limitations and shortcomings with existing device packaging approaches.
 - Develop new packaging concepts for improved electrical and thermal performance, manufacturability, and reliability.
 - Complement other power electronics research efforts within the DOE Vehicle Technologies Program.
- FY 2012 objectives
 - Evaluate industry state-of-the-art (SOA) power modules, including packaging performance, materials, processing, and structure analysis.
 - Continue Planar_Bond_All (PBA) power module development, including the following.
 - Packaging process optimization: Material/structure; cost-effective manufacturing.
 - Prototype module fabrication: Integration of advanced processing techniques.
 - Module testing and analysis: Electrical and thermal properties measurement and analysis.
 - Provide packaging support for other DOE Vehicle Technologies Program (VTP) Advanced Power Electronics and Electric Motors (APEEM) projects, including fabrication of customer-specific power modules.

Approach

- Benchmark existing power device packaging technologies, including package configuration, materials characterization, processing, and thermal and electrical performance evaluations.
 - Determine the “weak links.”
- Develop new packaging approaches through simulation and experiments to improve power module electrical, thermal, and thermomechanical performance and manufacturing cost-effectiveness.
- Apply packaging expertise to provide customer-specific power modules for VTP projects.

Major Accomplishments

- Benchmarked SOA automotive power modules.
 - Nissan LEAF module: electrical and thermal tests; insulator sheet analysis.
 - Toyota Prius 2010 module: thermal and microstructure tests.
 - Infineon HybridPack1: thermal and microstructure tests.
 - Mitsubishi TPM_II: semiconductor and package microstructure tests.
- Developed PBA power module packaging technologies and fabricated power modules that achieved the following.
 - Decreased package thermal resistance by 30%.
 - Decreased package parasitic electrical inductance by 3/4th and electric resistance by 90%.
 - Reduced the major packaging manufacturing steps from five to two.
 - Achieved greater than 30% volume and weight reductions.
- Delivered the following customer-specific power modules:
 - segmented drive inverter modules and
 - high power SiC diode modules.

Future Direction

- Enhance reliability of PBA concept.
 - Perform thermomechanical design and simulation of advanced planar bond module packages.
 - Implement cost-effective materials and structures into PBA power modules.

- Conduct simulations and preliminary reliability tests of packages.
- Continue high temperature module packaging development.
 - Incorporate advanced bonding material/processing techniques.
 - Investigate new encapsulate and thermal materials.
 - Evaluate the implications of high temperature packaging on cost, efficiency, and reliability using Si, SiC, and GaN power semiconductors.
- Continue to benchmark SOA technologies as needed (module performance, materials evaluation, and processing).
- Continue to provide packaging support for other projects.



Technical Discussion

Introduction

Advanced vehicles such as hybrid electric vehicles (HEVs), plug-in HEVs, fuel cell electric vehicles, and pure electric vehicles (EVs) require that power electronics control the electric energy from the battery to assist in the propulsion of the vehicle, either from the battery alone or in combination with an engine. The proliferation of HEVs and EVs in the past decade has created a huge opportunity for the power electronics and power semiconductor industry. Power modules represent about 40% of the inverter and converter costs in automotive electric drive systems. A \$2 billion to \$5 billion market for automotive power modules is predicted to emerge in the next 5 to 10 years as more electrified vehicles are developed and manufactured.

Power modules in electric drive systems contain multiple power semiconductor switches such as insulated gate bipolar transistors (IGBTs) and diodes in a three-phase-leg topology for dc-ac inverters and in a one-phase-leg configuration for dc-dc converters. The module packaging provides electrical interconnections, thermal management, and mechanical support. Modules for automotive applications are required to meet high reliability standards in harsh operating environments that include high ambient temperature range, high operation temperature, temperature excursion and thermal shock, mechanical vibration and shock, and frequent power surges. To ensure reliable operation of such power modules, packaging needs to be modified in terms of materials and processing [1, 2].

As cost remains a major barrier to broad customer acceptance of electric drive vehicles, pressure to decrease the cost of the power module has resulted in many changes

to the packaging form factor and thermal management through improved cooling efficiency and implementation of system-level integration schemes.

The electric conversion efficiency of a power module depends to a large degree on the performance of the power semiconductor switches. However, interconnectors within the package add extra power losses through their parasitic electric inductance, resistance, and capacitance. To reduce these parasitic parameters, new interconnection techniques have been developed.

Unlike power modules in the standard electric drive industry, automotive power modules are designed and manufactured by tier 1 (inverter/converter level) suppliers and even automakers who want to differentiate their products from those of competitors. Thus, many proprietary innovations applicable only to certain cars have been incorporated in power module packaging. Combining such diversity with design considerations and integration strategies makes power module packaging technology far from standardized.

The main criteria used to evaluate an automotive power module are its cost, reliability, size, weight, power density, and efficiency, which are generally determined by the power semiconductors, packaging, and manufacturing technology used. These metrics are dependent upon the power module's electrical, thermal, thermomechanical, and mechanical properties, as well as packaging materials and processing techniques.

The focus of this project was on the development of advanced automotive power module packaging technology through benchmarking existing commercial power modules and applying that knowledge to develop new innovative packaging materials, structures, and processes. The technical parameters of automotive power modules are good indicators of their performance. Examining technical parameters and their relationships aids the evaluation of power module technologies to identify the salient features of existing technology and develop new power module concepts.

Automotive Power Module Evaluation

First generation automotive power modules were manufactured with standard wire bond packaging technology [3], including soldered die attach, wire bond interconnect, silicone gel encapsulate, and multiple/hybrid manufacturing processes. The modules were mounted onto a cold plate with a thermal interface material (TIM) such as thermal grease. Second generation modules use a variety of advanced packaging technologies such as integrated cooling [4], direct copper lead top interconnection [5], and double sided copper bonding [6]. In [7], we summarized the packaging technologies of SOA automotive power modules. All these technologies contribute unique improvements in power module performance.

As an example, the power module in the Nissan LEAF all-electric vehicle is shown in Figure II - 19 [8]. Power semiconductor dies are attached to a copper bar on one side and have wire bonds to other copper interconnections to form a single phase inverter in which each switch unit comprises three silicon IGBT and diode dies. Then the whole module, with transfer molded power block, and silicone gel encapsulation, is mounted onto a cold plate with a separated high thermal conductivity electrical insulator sheet (HTCI). This arrangement also eliminates the direct bonded copper (DBC) substrate and baseplate (cf. baseline package).

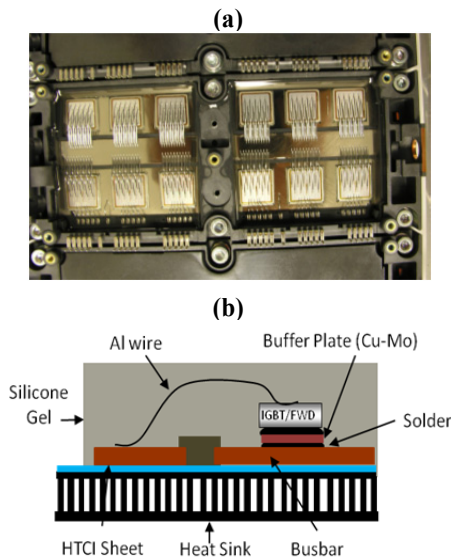


Figure II - 19: Nissan LEAF power module with copper-thermal sheet structure for power substrate. (a) Top view of module without cover and (b) schematic of cross-sectional view of packaging components stack.

A measurement method described in last year's report [9] was used to examine its thermal performance. Figure II - 20 shows the measured temperature rise of one IGBT die versus its power loss. Here, in addition to the temperature value obtained from the IGBT voltage drop, V_{ce} , it is measured from a diode temperature sensor manufactured on the IGBT die, located in the middle of the die surface. This curve is depicted as TS_{diode} in the figure. From these curves, the thermal resistance of the power module assembly was determined to be $0.32^{\circ}\text{C}/\text{W}$ and $0.24\text{ cm}^{\circ}\text{C}$ for the two measurement methods discussed. The difference between the two measurement results is because the TS_{diode} sensing method gets the maximum temperature (in the middle of the die), while the V_{ce} sensing method measures the average temperature over the whole die. (It is well-known that the temperature in the IGBT die is largely not uniform due to the spreading effect.) These test results also indicate that attention must be paid to die size effects when thermal performance is characterized.

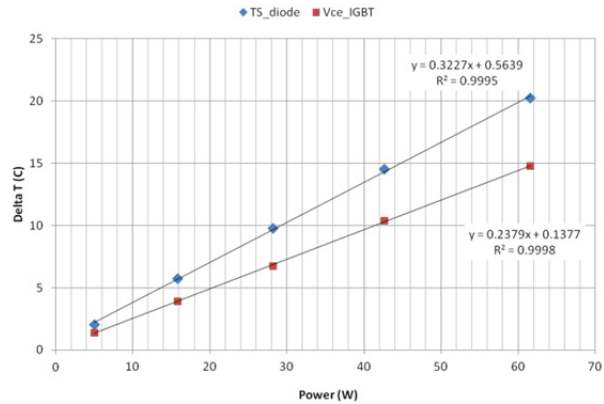


Figure II - 20: The IGBT junction temperature rise vs. power loss in the Nissan LEAF power module measured through on chip sensor, TS_{diode} , and voltage drop, V_{ce} .

To evaluate the electrical performance of SOA modules and their packaging, we have developed a set of experimental measurement systems for obtaining their electrical parameters. Figure II - 21(a) shows the Nissan LEAF power module in a double pulse test measurement circuit. Double pulse testing is a widely used approach to characterize the parasitic inductance of power module packaging. It is performed by operating the phase leg (or half bridge) module in a standard switching process including turn-on, conduction, turn-off, and blocking modes with an inductive load, which can control the current going through the switches and voltage applied. To accurately gauge the parasitic inductance, the voltage drop across the lower IGBT was tested at two test points simultaneously during Ice turn-off: between power terminals and between signal pins. Figure II - 21(b) shows the voltage waveforms of the lower IGBT measured on the pin and power terminal sides. The large overshoot is associated with the V_{ce} (terminals), which indicates that the parasitic inductance outside the power module is significant. The ΔV_{ce} can be obtained by deducting V_{ce} (terminals) from V_{ce} (pins). The inductance related to the interconnection path (loop) can then be easily obtained by accounting for the (dI_{ce}/dt) during this switching transition.

Parasitic electrical parameters in a module have direct effects on the dynamic behavior of power switches in the module. They cause voltage spikes affecting blocking voltage requirements, electromagnetic interference containment and susceptibility, and direct and indirect power dissipation. These phenomena are exacerbated as the power density of modules increases. To ensure high efficiency and high performance operation of a power module, optimization of electrical interconnections is required in multichip module packaging structures. Using a wire bond packaging platform, these efforts are concentrated on reduction of the interconnection wire's length and electric topology. However, the two-

dimensional layout configuration limits further improvement.

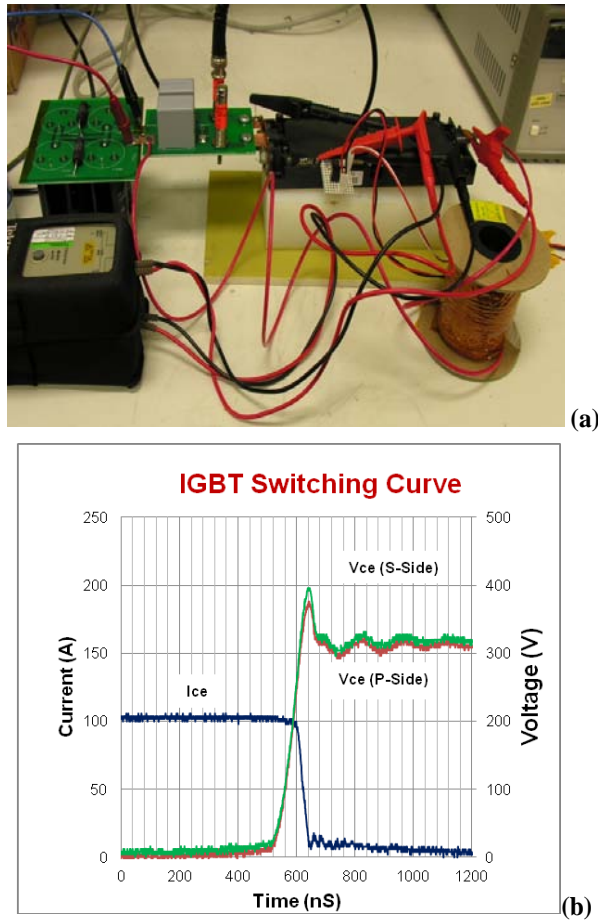


Figure II - 21: Double pulse testing of the Nissan LEAF power module: (a) test setup; (b) waveforms associated with specific test points in the power module package.

New Automotive Power Module Packaging

To meet the challenges of automotive power electronics modules in cost, efficiency, reliability, etc., a new planar interconnection configuration has been proposed, featuring a symmetric sandwiched substrate-switches-substrate structure. It provides a large bond area, thick electrical traces, a special orientation of switch pairs in a phase leg, and double sided cooling capability, resulting in comprehensive improvement in all aspects of power module technical performance. Technical details such as packaging structure and associated packaging process technology are demonstrated with a new 200 A, 1,200 V phase leg power module prototype. The improvements in performance and manufacturability have resulted in considerable strides toward achieving targets for power electronics systems in modern electric drive vehicles.

The graph in Figure II - 22(a) is an electric schematic of a typical phase leg configuration, which consists of two

switch units, upper IGBT/diode pair and lower IGBT/diode pair. It is a building block for various electric power converters and inverters in automotive power electronics systems. A schematic of the packaging structure for this phase leg power module is shown in Figure II - 22(b). The IGBT and diode dies are mounted between two insulated substrates. The electrical interconnection is achieved by bonding semiconductor dies to the copper on two direct bonded copper (DBC) substrates, which are patterned to form a circuit that matches with the electrode pad layout on the dies. The DBC substrate offers electrical insulation via the inner layer of ceramic material sandwiched between the copper layers. As shown in Figure II - 22(b), the upper switch pair and lower switch pair in the phase leg are oriented physically in a face-up-face-down configuration. This makes use of the dies' vertical semiconductor (electrode) structure (i.e., electrodes are arranged on both top and bottom surfaces of the dies). This layout change, compared to a wire bond packaging layout, results in the change of the main power flow loop from the X-Y plane to the X-Z plane. Due to the thickness of the die (in the 0.1 mm range) compared to the length/width (10 mm), the enclosed area of the loop is reduced dramatically, leading to an enormous reduction in electrically parasitic inductance in addition to reduction of electric resistance due to larger bond areas and large copper electric conduction traces.

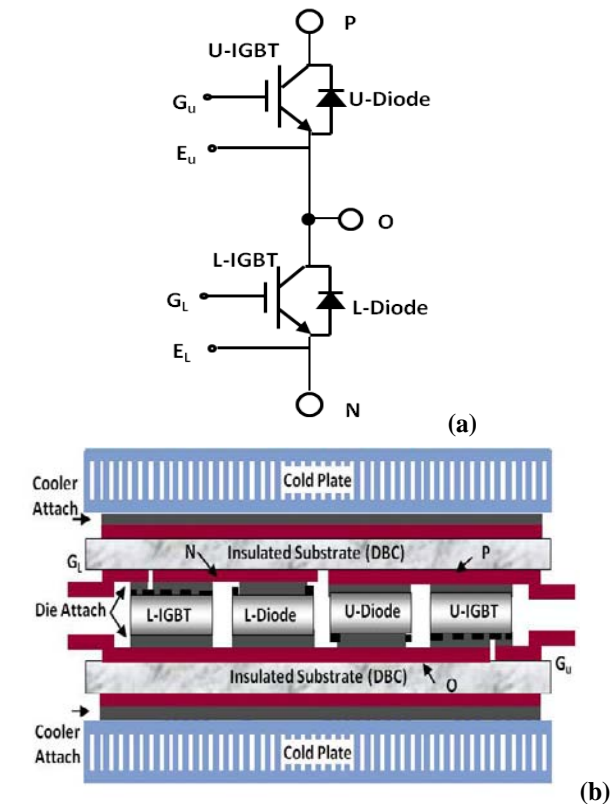


Figure II - 22: Schematic of planar bond integrated power module: (a) electrical diagram and (b) planar bond packaging structure.

This planar bond structure also exposes the top surfaces as extra thermal paths for the power switches. The heat removal from hot power switch dies is greatly improved by applying double sided cooling (here focused on the forced liquid). In addition, special mini-coolers for this application are designed to be directly attached to the power stage by planar bond layers, as depicted in Figure II - 22(b). The direct cooler bonding, instead of stacking through a TiM layer, leads to further reduction of the thermal resistance in the thermal paths.

The mismatch of thermomechanical parameters, including the coefficient of thermal expansion, between multiple hybrid materials and structure asymmetry are major failure mechanisms of conventional power modules. The sandwiched die configuration offers symmetrical mechanical support, while the replacement of bond wires by planar bonds reduces the complexity of material combinations, all of which is advantageous to containing the deformation due to mismatched thermal expansion of power semiconductors operating with large amounts of generated heat.

Planar_Bond_All Packaging Technology

This structural design alters the multiple hybrid bonding forms in the conventional packaging structure into a few identical planar bonds. To accomplish this paradigm shift in the packaging scheme, a special packaging process technology was developed. As described in [9], all packaging components are first assembled into a fixture. The components include patterned substrates, bare dies, shims, bonding material (premade such as solder foil), power terminals and signal pins, mini-coolers, etc. The second step involves heating up the assemblies to form the bonds and create the final packages. This manufacturing process not only reduces the conventional multiple hybrid packaging processes to two steps, but also makes batch processing possible. The simplicity of the process helps reduce costs and greatly improves the manufacturability of the modules. The technology is called Planar_Bond_All.

Figure II - 23(a) is a photograph of the prototype power module fabricated with this packaging technology. It is a one-phase-leg (half bridge) electrical configuration comprising two pairs of single silicon IGBT and diode dies, both rated at 200 A, 1,200 V. The module body measures 52 mm × 30 mm × 2mm, excluding the terminals and pins. The soldering process is used to form these planar bonds because of its good electrical conductivity and processing feasibility. The special front metallization of the power semiconductor dies, instead of conventional aluminum (designed for wire bonding), was created at the wafer level. The power terminals [positive, neutral, and negative (P, O, and N)] and signal pins (G_U , E_U , and G_L , E_L) are also mounted between the two substrates to form compact input/output connections.

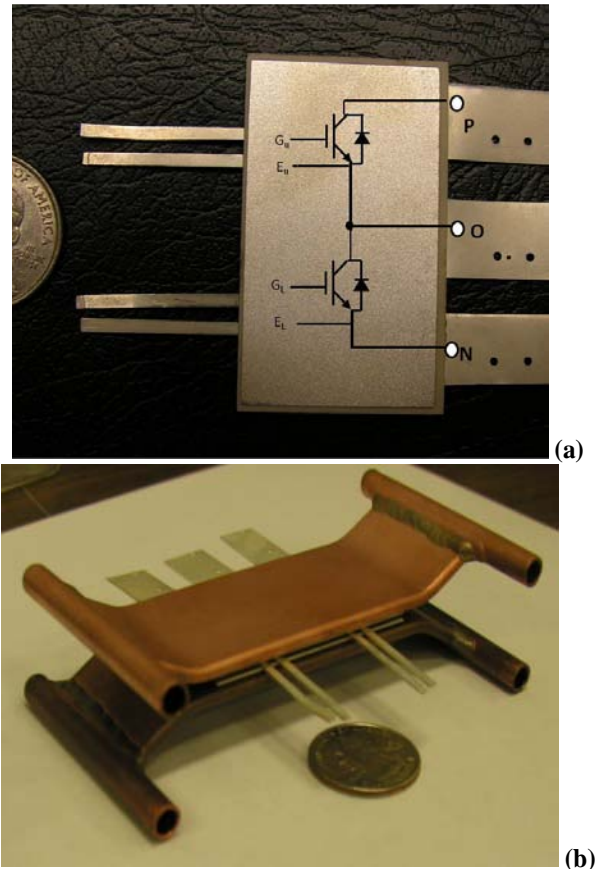


Figure II - 23: Prototype PBA module: (a) photo of the prototype; (b) photo of the power module integrated with two mini-coolers mounted from both top and bottom.

This module was designed to be cooled from both sides, as depicted in Figure II - 23(b). Various configurations can be used for double sided cooling. Figure II - 23(b) is an example of two copper flat tube cold plates (mini-coolers) integrated with the power module. The effective cooling area is 58 mm by 30 mm, and the tube thickness is 3 mm. Made of all copper and having a unique internal crisscross fin structure, this mini cold plate offers thermal resistivity of $0.33 \text{ cm}^2 \cdot \text{C}/\text{W}$ at a water coolant flow rate of 1 GPM, which is superior to conventional cold plates.

1. Electrical Characterization

The electrical parameters attributable to the module packaging (resistance, inductance, and capacitance) are additive to those from the semiconductor components. The parasitic electric resistance and inductance are attributed to the electrical interconnection path in the planar bond power module. A lumped element model was developed using an electromagnetic simulation tool, MAXWELL Q3D Extractor, in which the effective electric components (lumped elements) were calculated physically based on the electric and electromagnetic fields with current going through the conduction path sections. The sum of the

lumped elements along the path from the positive terminal through the upper IGBT and then through the lower diode to the negative terminal represents the parameters of a packaging structure. In this planar bond power module, the total inductance L is 12.08 nH, while the total resistance R equals 0.22 m Ω . For comparison, the parasitic electrical parameters in a conventional wire bond packaged power module, shown in Figure II - 24, with the same power semiconductor dies, were also extracted. The analogous values for the major parameters defined above are $L=50.3$ nH, and $R=2.35$ m Ω .

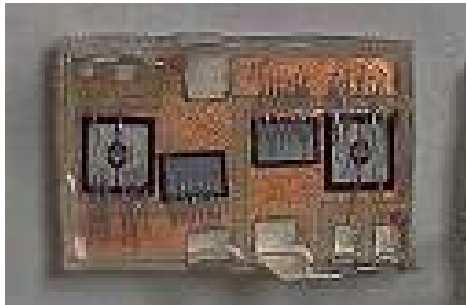


Figure II - 24: A wire bond packaging prototype.

The parasitic electrical inductance was also measured with a double pulse test, as described previously. The parasitic inductance involved in the current loop can be obtained from the voltage overshoot. Figure II - 25 shows the voltage waveforms during turn-off of an IGBT in both power modules. It can be seen that the voltage overshoot is 156 V and 72 V, respectively, for the wire bond and planar bond modules (the turn-off rate of current is different). Table II - 2 gives the experimental results for parasitic inductance for both modules and the simulated (calculated) values associated with the section of the power flow path. The experimental value for the planar module inductance is only one-third that of the baseline wire bond module, consistent with simulation results.

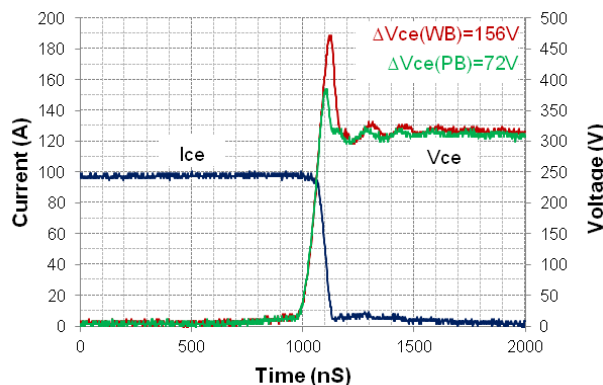


Figure II - 25: Comparison of measured voltage waveforms of wire bond (WB) and planar bond (PB) modules.

Table II - 2: Parasitic inductance with packaging interconnection.

Inductance (nH)	Experimental Value	Calculated Value
Planar Bond– Lower IGBT	10.5	6.3
Wire Bond– Lower IGBT	31.9	23.5

Figure II - 26 presents the simulated voltage V_{ce} variation with different parasitic inductances from 5 nH to 45 nH. It can be seen that the overshoot voltage is in the range from 30 V to 150 V over the 300 V bus voltage. Because of its smaller parasitic inductance compared to the conventional module (12.08 nH vs. 50.3 nH), the planar module can use devices with much lower voltage breakdown ratings, which offers greater flexibility for device optimization and the potential for cost reduction and other benefits.

The power module package parasitic inductance not only causes voltage overshoot but also increases the power loss of switches during switching. Figure II - 27 shows the variation in turn-off energy loss of an IGBT versus the inductance of its package. It is assumed the semiconductor itself has a turn-off energy of 15 mJ without accounting for parasitic inductances. The blue “X” represents the additional parasitic inductance due to the 10.5 nH from a PBA package, while the red “X” shows the additional parasitic inductance (31.9 nH) from a traditional wire bonded module. Some commercial wire bonded modules have up to 50 nH inductance; this can cause significant increases in energy loss.

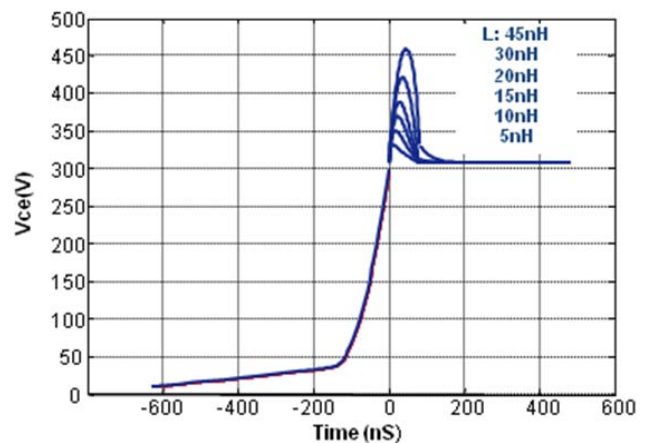


Figure II - 26: Simulated voltage overshoot vs parasitic inductance with an IGBT in phase leg module.

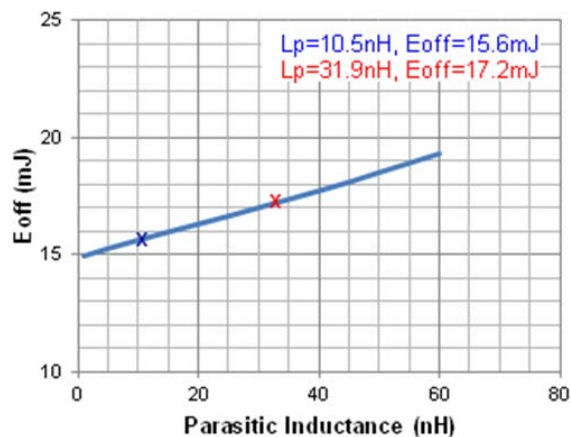


Figure II - 27: Simulated turn-off switching power loss of an IGBT vs parasitic inductance.

Unlike inductance, parasitic resistance will directly dissipate electric power as heat when current is flowing through it. To evaluate this power loss, a typical automotive application was taken as an example. Figure II - 28 presents the root mean square current profile of an inverter phase leg operating during a standard driving cycle (US06) over a 10-minute period with 1-second steps. The power loss profiles for parasitic electric resistance associated with the wire bond module and the planar bond module under this driving cycle are shown in red and blue, respectively. To clearly compare them, the average power loss for each of them during the whole period is also depicted in the figure: 11.08 W for the wire bond module and 1.03 W for the planar module. Total losses for the planar module are less than 10% of those for the wire bond module. These power losses from bond wires makes them hot spots during module operation. The smaller power loss in the planar module prevents this possible cause of failure.

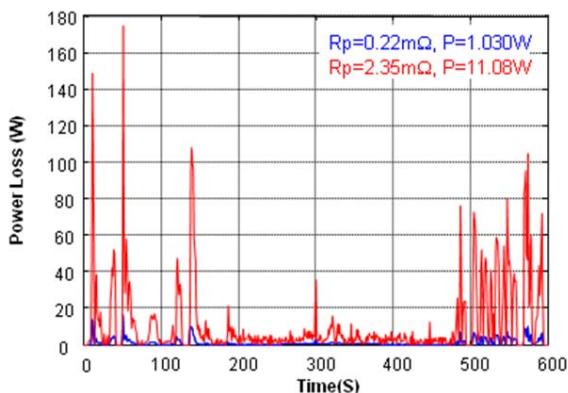


Figure II - 28: Simulated power loss profiles associated with package electric resistance under the US06 driving cycle. (Red = standard wire bond module; blue = planar bond module.)

Combining conduction and switching power losses, the planar power module reduces the total power dissipation dramatically. This in turn leads to significantly

improved power conversion efficiency in the entire power electronics system.

2. Thermal Characterization

The thermal performance of a power module can be modeled as a network of thermal resistance and capacitance in series. The thermal capacitance largely determines the transient response of the power module to power dissipation in switches, while the thermal resistance mainly determines the cooling efficiency. The characterization of the thermal parameters has been performed through both simulation and experimental methods. In [9] the temperature distribution in the planar power module under the following conditions is presented: the power loss of the IGBT is 100 W, the diode's loss is 70 W; the coolant flow rate is 2.5 GPM; the coolant temperature at the inlet is 65°C. The thermal parameter network has been analyzed based on these criteria.

The same parameters were obtained by experimental thermal tests through emulating real-world operation of power modules. Figure II - 29(a) shows the thermal performance test setup with the planar bond module sandwiched between two mini-coolers, as depicted in Figure II - 23(b). Typically V_{ce} in an IGBT can be used to measure junction temperature due to its sensitivity to temperature. Once a power pulse heats up the IGBT, its temperature will increase and stabilize at a certain temperature. When the power is cut off, the IGBT will cool down from this high temperature. By processing the cooldown temperature curves and input power data, the thermal parameters (resistance and capacitance) within the module can be obtained [9]. In evaluating the thermal performance of a packaging assembly, the specific thermal resistance was taken as a figure of merit, which is a normalized parameter by die size (i.e., specific thermal resistance equals die size \times thermal resistance). Figure II - 29(b) gives the specific thermal resistance of the planar bond module and two other SOA modules. One is the Nissan LEAF module, which is wire bond and mounted on a cold plate with thermal grease. Its specific thermal resistivity is 0.52 $\text{cm}^2 \cdot ^\circ\text{C}/\text{W}$. The other, the 2010 Prius module, representing integrated single side cooling, has a rigid bond between the module and cold plate. Its specific thermal resistance is 0.47 $\text{cm}^2 \cdot ^\circ\text{C}/\text{W}$. The double sided cooling of the planar module assembly reduces the specific thermal resistivity to 0.33 $\text{cm}^2 \cdot ^\circ\text{C}/\text{W}$, which is 30% to 37% lower than either of these SOA modules and 38% lower than that of most first generation module assemblies.

The die size used in a power module is proportional to the specific thermal resistance of the module assembly. With smaller thermal resistance, the semiconductor die size can be tailored to be smaller for a certain power rating, which is an effective way to reduce the cost of power modules.

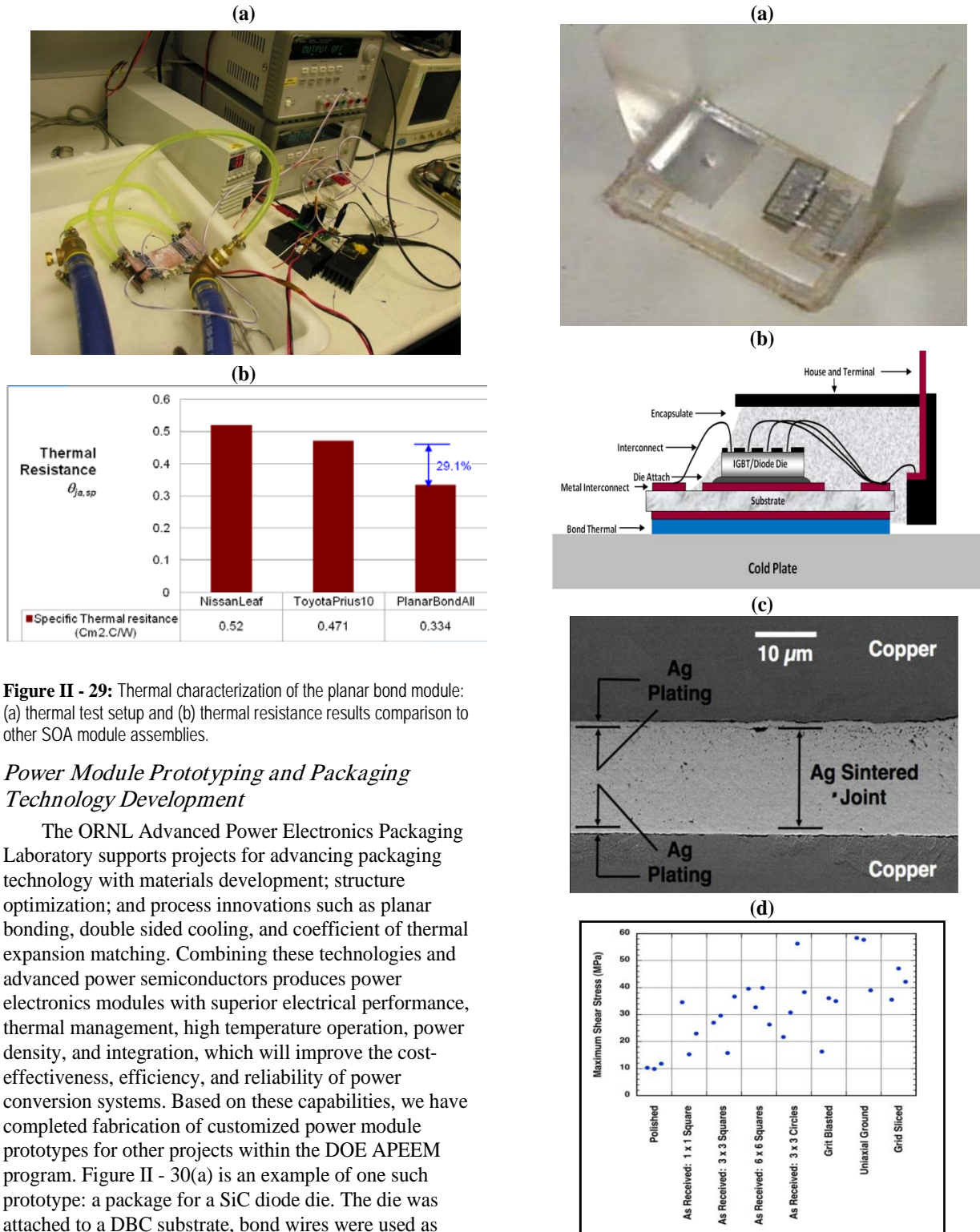


Figure II - 29: Thermal characterization of the planar bond module: (a) thermal test setup and (b) thermal resistance results comparison to other SOA module assemblies.

Power Module Prototyping and Packaging Technology Development

The ORNL Advanced Power Electronics Packaging Laboratory supports projects for advancing packaging technology with materials development; structure optimization; and process innovations such as planar bonding, double sided cooling, and coefficient of thermal expansion matching. Combining these technologies and advanced power semiconductors produces power electronics modules with superior electrical performance, thermal management, high temperature operation, power density, and integration, which will improve the cost-effectiveness, efficiency, and reliability of power conversion systems. Based on these capabilities, we have completed fabrication of customized power module prototypes for other projects within the DOE APEEM program. Figure II - 30(a) is an example of one such prototype: a package for a SiC diode die. The die was attached to a DBC substrate, bond wires were used as interconnections, and then the module was encapsulated by silicone gel. The package was delivered for further performance measurement and analysis.

Figure II - 30: Examples of power module prototypes and packaging technology development: (a) a SiC prototype for another APEEM project, (b) an integrated cooling assembly for a power module, (c) sintered silver bonding layer in package, and (d) shear strength of bonding layer vs. substrate topography and attachment pad geometry.

The prototypes built had no baseplates, resulting in lower thermal resistance compared to standard modules. To affix the substrate to the cold plate an epoxy with high thermal conductivity was used as a TiM between the module and cold plate, which provides strong mechanical bonding. This assembly configuration is schematically illustrated in Figure II - 30(b). Figure II - 30(c) is a cross-sectional view of a sample in which two copper plates are bonded together with sintered silver. This is an emulation of the bonding for die attach to DBC and DBC to copper baseplate. The sintered silver bonding layer offers high reliability, high temperature capability, and lower thermal and electric resistivity. It has been intensively studied in the past year. For example, the dependence of the initial shear strength on the substrate topography and attachment pad geometry was measured as shown in Figure II - 30(d). The use of smaller square pads or circle pads for the joint, compared to a single large square pad of the same bonding area, produced higher average shear strengths. Because topographical modifications and the use of proper pad geometry can increase shear strength, it is reasonable to combine and hybridize their effects to further increase overall shear strength. This is an important observation as more attention in the future will be devoted to joining constituents with different areas in electronic packages.

Conclusion

Progress in packaging technologies has been examined in commercial modules by evaluating technical parameters such as module electrical, thermal, and thermomechanical properties, leading to conclusions as to cost-effectiveness, reliability, efficiency, and power density. Efforts have continued to develop experimental methods to identify technical features and advances in SOA power modules and packaging technologies.

A power module packaging technology, the so-called Planar_Bond_All, has been developed and applied in fabrication of a 200 A, 1,200 V phase leg power module. It features all planar bonds, three-dimensional power interconnection of power semiconductors, and integrated double sided cooling. The electrical and thermal performance parameters have been characterized with simulation and experimental measurement tools. The improved performance and anticipated cost reduction of the packaging process, a unique automatic manufacturing technology, will result in considerable strides toward achieving power density and cost targets for automotive power electronics systems.

Patents

1. Zhenxian Liang, Laura D. Marlino, Puqi Ning, and Fei Wang, "Power Module Packaging with Double Sided Planar Interconnection and Heat Exchangers,"

US Patent Application 61/509312, filed July 19, 2011.

Publications

1. Puqi Ning, Zhenxian Liang, Fred Wang, Laura Marlino, "Power module and cooling system thermal performance evaluation for HEV application," in Proceedings of the 27th IEEE Annual Applied Power Electronics Conference and Exposition (APEC 2012), February 6–9, 2012, Orlando, Florida, pp. 2134–2139.
2. Zhenxian Liang, Puqi Ning, Fred Wang, Laura Marlino, "Reducing Parasitic Electrical Parameters with a Planar Interconnection Packaging Structure," in Proceedings of the 7th International Conference on Integrated Power Electronics Systems, March 6–9, 2012, Nuremberg, Germany.
3. Andrew A. Wereszczak, Daniel J. Vuono, Zhenxian Liang, Ethan E. Fox, Sintered silver joint strength dependence on substrate topography and attachment pad geometry, in Proceedings of the 7th International Conference on Integrated Power Electronics Systems, March 6–9, 2012, Nuremberg, Germany.
4. Zhenxian Liang, "Status and Trend of Automotive Power Packaging," in Proceedings of the 24th IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD2012), 3–7 June, 2012 Bruges, Belgium (invited).
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6. Andrew A. Wereszczak, Daniel J. Vuono, Hsin Wang, Mattison K. Ferber, and Zhenxian Liang, *Properties of Bulk Sintered Silver As a Function of Porosity*, ORNL/TM-2012/130, Oak Ridge National Laboratory, 2012.

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 6. Yasuyuki Sakai, Hiroshi Ishiyama, and Takaji Kikuchi, “Power control unit for high power hybrid system,” in Proc. 2007 SAE International Conference, p. 2007-01-0271.
 7. Zhenxian Liang, “Status and trend of automotive power module packaging,” in Proc. of the 24th International Symposium on Power Semiconductor Devices & ICs, 3–7 June, 2012, Bruges, Belgium, pp. 325–331.
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 9. US Department of Energy, *Oak Ridge National Laboratory Annual Progress Report for the Power Electronics and Electric Machinery Program*, ORNL/TM-2011/263, Oak Ridge National Laboratory, October 2011.

II.3 A Segmented Drive Inverter Topology with a Small dc Bus Capacitor

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Objectives

- Overall objectives
 - Design, develop, build, and test a 55 kW integrated segmented traction drive system that can reduce the inverter dc bus ripple current and thus the capacitance by at least 60%.
 - Address the 2015 inverter target of 12 kW/kg and the 2020 inverter target of 13.4 kW/L.
 - Eliminate the capacitor-related hurdle for high temperature operations.
- FY 2012 objective
 - Design, build, and test a 55 kW segmented inverter that is suitable for integrating with a motor.

Approach

- Use a segmented drive system topology that does not need additional switches or passive components but can significantly reduce the dc link ripple current and the amount of capacitance.
- Integrate the segmented inverter and motor into a single package drive system to eliminate cable connections and reduce the drive system cost.
- Perform simulation study of various pulse width modulation (PWM) schemes using commercial circuit simulation software to assess their impact on the capacitor ripple current.

- Design, build, and test a 55 kW inverter prototype to experimentally validate the simulation study.
- Design, build, test, and characterize a 55 kW prototype segmented inverter that is packaged for integrating with a motor.

Major Accomplishments

- Demonstrated a 55 kW segmented inverter prototype with a 60% reduction of dc bus capacitance compared to a standard voltage source inverter (VSI) with test results showing reductions of
 - capacitor ripple current by 55% to 75%,
 - battery ripple current by 70% to 90%, and
 - motor ripple current by 60% to 80%.
- Completed design, fabrication, and testing of two ring-shaped 55 kW segmented inverters that are suitable for integration with a motor.
 - Finite element analysis (FEA) results indicated satisfactory thermal performance of the toroidal heat exchanger designs: maximum junction temperature of 111°C for the four-channel design and 85°C for the six-channel design at an inlet coolant [water ethylene glycol (WEG)] temperature of 70°C.
 - FEA results also revealed the six-channel design can keep junction temperatures below 125°C with 105°C coolant temperature.
 - Use of heavy copper printed circuit board technology for interconnecting the power modules eliminated the need for bus bars and greatly simplified the inverter assembly steps.
 - The first inverter prototype using the four-channel toroidal heat exchanger yielded a power density of 17.1 kW/L and specific power of 15.6 kW/kg, while the second inverter design using the six-channel toroidal heat exchanger increased the power density to 17.8 kW/L.
 - Test results with both a resistive load bank and an induction motor showed significant reductions of ripple current in the battery and motor currents.

Future Direction

- Project is completed and no future work is planned.

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Technical Discussion

Background

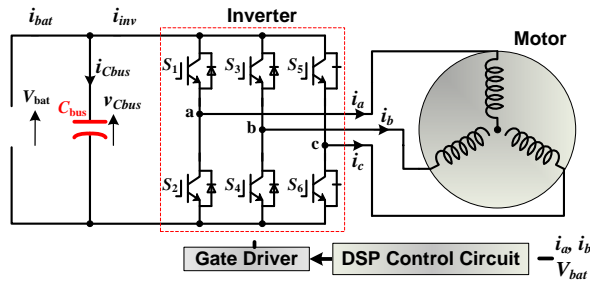


Figure II - 31: Standard VSI-based drive system in HEVs.

The dc bus capacitor is an indispensable component for maintaining a stable dc bus voltage and smooth battery current for the VSI-based traction drive systems in electric vehicles (EVs), hybrid EVs (HEVs), and plug-in HEVs. Figure II - 31 is a schematic drawing of the standard VSI-based drive system. The VSI, mainly comprising six power semiconductor switches—typically insulated gate bipolar transistors (IGBTs)—and a dc bus filter capacitor, switches the battery dc voltage to produce a desired set of three-phase ac voltages according to a chosen PWM scheme. The ac voltages in turn regulate the motor current to control the motor torque and speed. In doing the switching operations, the inverter generates large ripple components in the dc link current, i_{inv} , thus necessitating the use of the dc bus filter capacitor to absorb the ripple currents and suppress voltage transients. These occur on the dc bus at every instant of inverter switching and, if not sufficiently constrained, are detrimental to the battery life and reliability of the semiconductor switches in the inverter.

Figure II - 32 shows calculated capacitor ripple current as a percentage of motor current vs. inverter modulation index for a given power factor in the standard VSI-based drive system [1]. The maximum ripple current occurs at around a modulation index of 0.65 and is more than 60% of the motor current. In a typical 55 kW HEV inverter, the capacitor ripple current can exceed 110 Arms. As a result, a bulky and costly dc bus capacitor of about 1,000 μ F is required to prevent this large ripple current from flowing into the battery and to maintain a smooth dc bus voltage. Even with the large bus capacitor, there can still be a relatively large ripple component in the battery current.

Concerns about the reliability of electrolytic capacitors have forced HEV makers to use self-healing film capacitors, and currently available film capacitors that can meet the demanding requirements are costly and bulky, taking up one-third of the inverter volume and making up one-fifth of the cost. The dc bus capacitor, therefore, presents significant barriers to meeting the requirements of the U.S. DRIVE program goals for

inverter volume, lifetime, and cost established by DOE and its industrial partners [2].

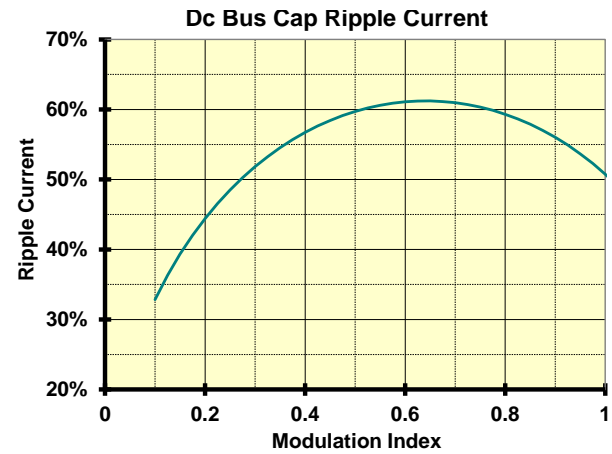


Figure II - 32: Calculated capacitor ripple current as percentage of motor current vs. inverter modulation index for a given power factor in the standard VSI-based drive system.

The large ripple currents become even more problematic for the film capacitors in high temperature environments as their ripple current handling capability decreases rapidly with rising temperatures. Figure II - 33 shows this effect for one of the best 150 μ F film capacitors available on the market: as the ambient temperature rises from 85°C to 105°C, ripple current handling capability decreases from 50 A to 11 A. To compensate for this loss in ripple current handling capability, the weight, volume, and cost of capacitors would need to increase by a factor of 5.

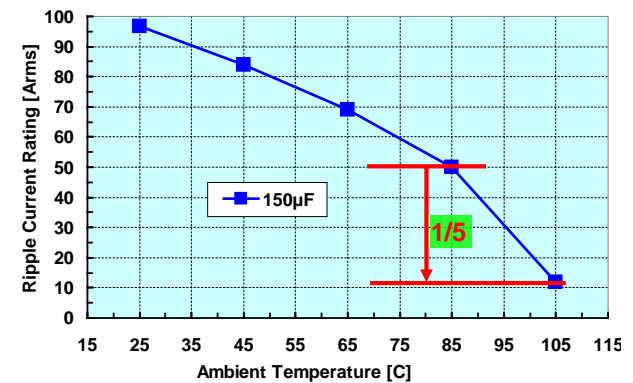


Figure II - 33: Film capacitor ripple current capability vs. ambient temperature (Electronic Concepts UL31 Series) [3].

To help achieve the U.S. DRIVE targets, there is an urgent need to minimize this bulky component by significantly reducing the inverter ripple current. The following factors, however, make this a difficult task: (1) increasing the switching frequency, which is one of the anticipated benefits with future wide-bandgap-based switches, has little impact on the bus capacitor ripple currents because the capacitor ripple currents

depend on the motor peak current, although increasing switching frequency does reduce the dc bus voltage and motor current ripples, and (2) the major components of the capacitor ripple currents have frequencies of multiples of the switching frequency (nf_{sw}) or their side bands ($nf_{sw} \pm f_m, nf_{sw} \pm 2f_m, \dots$), as given by Eq. (1) and illustrated in Figure II - 34.

$$i_{inv} = I_{dc} + \sum_{k=0}^{\infty} \sum_{n=1}^{\infty} I_{n,k} \sin[2\pi(nf_{sw} \pm kf_m)t + \alpha_{n,k}] \quad (1)$$

where $I_{n,k}$ and $\alpha_{n,k}$ represent respectively the amplitude and phase angle of the harmonic component identified by the integers n and k .

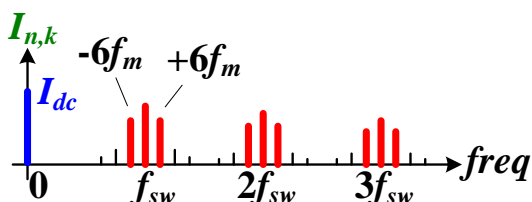


Figure II - 34: Ripple components in the dc link current in the standard VSI-based drive system.

The high frequency harmonics are impractical to filter out with an active filter. The harmonics should be absorbed by the dc bus capacitor, and the sum of them is the capacitor ripple current, i_{Cbus} . The root mean square (rms) value of the capacitor ripple current, $I_{Cbus(rms)}$, can be calculated by [2]

$$I_{Cbus(rms)} = \sqrt{\frac{M}{4\pi} [2\sqrt{3} + (8\sqrt{3} - 4.5\pi M) \cos^2 \varphi] \cdot I_{m1(rms)}} \quad (2)$$

Description of the Segmented Drive System

Figure II - 35 illustrates the proposed segmented traction drive system that includes a battery, a dc bus filter capacitor, a three-phase inverter, and a three-phase electrical motor/generator. The inverter switches in the power module (S_1 – S_6) and stator windings in the motor are separated into two sets of switches (indicated in red and blue in the figure) and windings $a_1, b_1,$ and c_1 and $a_2, b_2,$ and c_2 . Further, each phase group of the stator windings (a_1, a_2), (b_1, b_2), and (c_1, c_2) can be colocated in the same stator slots or displaced in different regions for a multipole motor. Each group of switches (red or blue) is connected as an inverter bridge and connects to one set of the motor stator windings, forming an independent drive unit as shown in Figure II - 36. Because switches in most high power inverter modules comprise multiple IGBT and diodes connected in parallel, only minor modifications to the switch configuration and three additional terminals with

half the current rating of the original ones are needed to form the segmented arrangement.

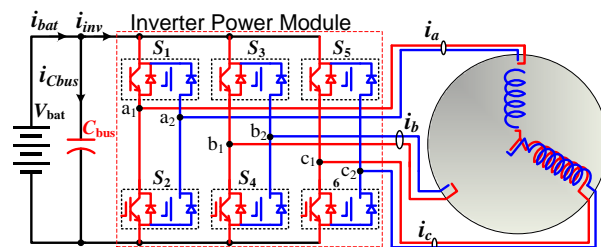


Figure II - 35: Proposed segmented traction drive system.

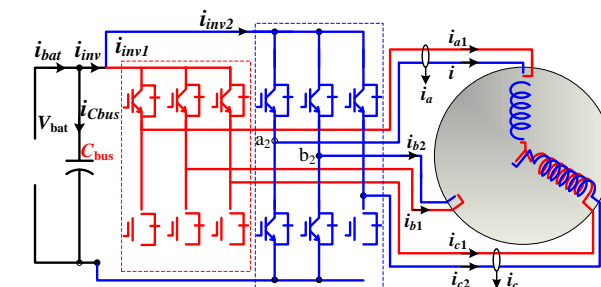


Figure II - 36: An equivalent arrangement of the segmented traction drive system.

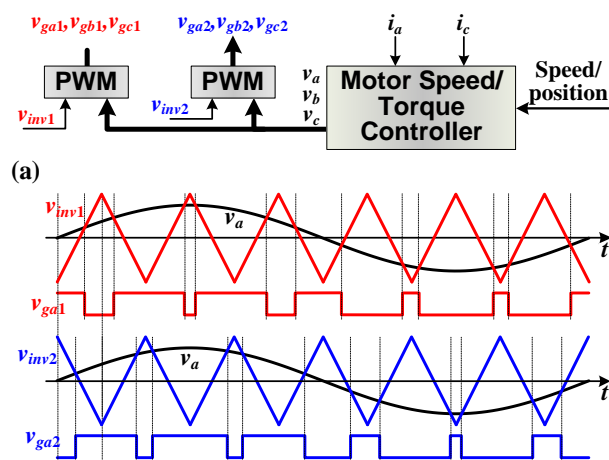


Figure II - 37: Control of the segmented drive with interleaved PWM switching to minimize the capacitor ripple current: (a) control block diagram; (b) interleaved PWM switching control based on two identical carriers with a phase angle displacement between them.

The timing of the turn-on and turn-off of the corresponding switches in the two independent drive units is controlled in a way that minimizes the dc bus ripple currents. No changes are needed in the implementation of the motor control except modifications in the PWM control of the switches in the inverter. Figure II - 37 shows a block diagram for control of the segmented drive with interleaved PWM switching to minimize the capacitor

ripple current and a carrier-based interleaved PWM switching scheme. To control the motor speed or torque, two of the combined three-phase motor currents, $i_a (= i_{a1} + i_{a2})$, $i_b (= i_{b1} + i_{b2})$, and $i_c (= i_{c1} + i_{c2})$ and the motor speed or rotor position are sensed and fed to a chosen motor control scheme, which is typically based on the field orientation control. Therefore, no additional current sensors are required, compared to the nonsegmented drive. The motor controller produces a set of three-phase voltage modulation signals, v_a , v_b , and v_c , which are then compared with two identical carriers with a phase angle displacement, v_{inv1} and v_{inv2} , to generate interleaved PWM switching control signals for the two inverter units, v_{ga1} , v_{gb1} , v_{gc1} , and v_{ga2} , v_{gb2} , v_{gc2} . Alternatively, space-vector-based PWM methods can be used to generate interleaved PWM switching control signals.

The two inverter dc link currents, i_{inv1} , and i_{inv2} , and the combined current, i_{inv} , in the segmented inverter in Figure II - 36 can be expressed by

$$i_{inv1} = 0.5 \left\{ I_{dc} + \sum_{k=0}^{\infty} \sum_{n=1}^{\infty} I_{n,k} \sin[2\pi(nf_{sw} \pm kf_m)t + \alpha_{n,k}] \right\}, \quad (3)$$

$$i_{inv2} = 0.5 \left\{ I_{dc} + \sum_{k=0}^{\infty} \sum_{n=1}^{\infty} I_{n,k} \sin[2\pi(nf_{sw} \pm kf_m)t + \beta_{n,k}] \right\} \quad \text{and} \quad (4)$$

$$i_{inv} = I_{dc} + \sum_{k=0}^{\infty} \sum_{n=1}^{\infty} \sqrt{\frac{1 + \cos(\beta_{n,k} - \alpha_{n,k})}{2}} I_{n,k} \times \sin[2\pi(nf_{sw} \pm kf_m)t + \frac{\alpha_{n,k} + \beta_{n,k}}{2}] \quad (5)$$

where $\alpha_{n,k}$ and $\beta_{n,k}$ represent the phase angles of the harmonic components of the two inverters identified by the integers, n and k . As shown in the equations above, the amplitude of each combined ripple component can be reduced by introducing a phase shift into the corresponding ripple components of the two drive units to make $\alpha_{n,k} \neq \beta_{n,k}$. Moreover, the combined ripple current components can be reduced to zero by introducing a 180 electrical degree phase shift into the corresponding ripple components of the two drive units. Shifting the relative phase angle of the carrier signals as shown in Figure II - 37 can lead to cancellation of some of the ripple current components while reducing others. The net effect is a significantly reduced dc bus ripple current to be filtered out by the dc bus capacitor. As a result of the reduced dc ripple current, the size of the dc bus capacitors can be reduced by 55%–75%, and less costly and less bulky capacitors can be used.

A simulation study using PSIM carried out in FY 2009 has validated the segmented drive concept. Various interleaved carrier-based and space vector PWM methods were studied in simulation and tested with both a resistive load bank and an induction motor to quantify their impacts

on the dc bus ripple current. Test results were given in previous annual reports and show significant reductions of 55% to about 75% in capacitor ripple current, 70% to about 90% in battery ripple current, and 60% to about 80% in motor ripple current.

Integrated Segmented Drive System

The segmented drive system can significantly reduce the ripple current and thus the requirement on bus capacitance. To further reduce the drive system cost, integrated inverter/motor packaging techniques are being explored to eliminate inverter/motor connection cables. Figure II - 38 illustrates such a design concept, in which the heat sink, IGBT power module board, gate driver board, and capacitor board are all made in cylindrical shapes so that they can be tightly packaged into the motor housing.

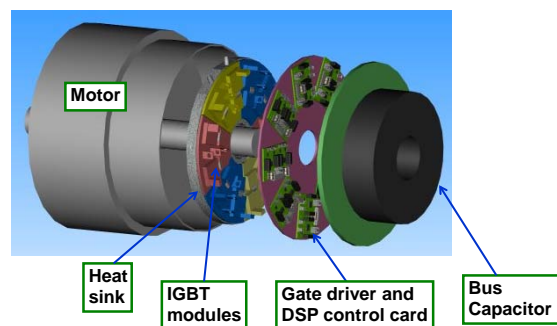


Figure II - 38: Design concept for an integrated segmented inverter-motor drive system.

Design and Fabrication of 55 kW Inverter Prototypes for Integrating with a Motor

Two ring-shaped segmented inverters that are suited to be integrated into typical cylindrical motors were designed, fabricated, and tested. Figure II - 39 shows three-dimensional drawings of the hardware design for the first 55 kW prototype. The design comprises a toroidal heat exchanger with four circular water channels, IGBT modules, a dc bus capacitor attached to a printed circuit board that is constructed using heavy copper printed circuit technology which also functions as bus bars to interconnect the IGBT power modules, and a gate drive and control logic board. The toroidal heat exchanger has an outer diameter of 9 in., inner diameter of 4 in., and thickness of 0.75 in. Although the required capacitance was fulfilled using multiple discrete block capacitors for this prototype design, a custom-built ring-shaped capacitor would fully use the spaces and thus reduce the inverter volume. Also, the gate drive board is divided into six identical arc sections to save design time and cost. Future designs could put all the gate drive and control circuits on a single ring-shaped board.

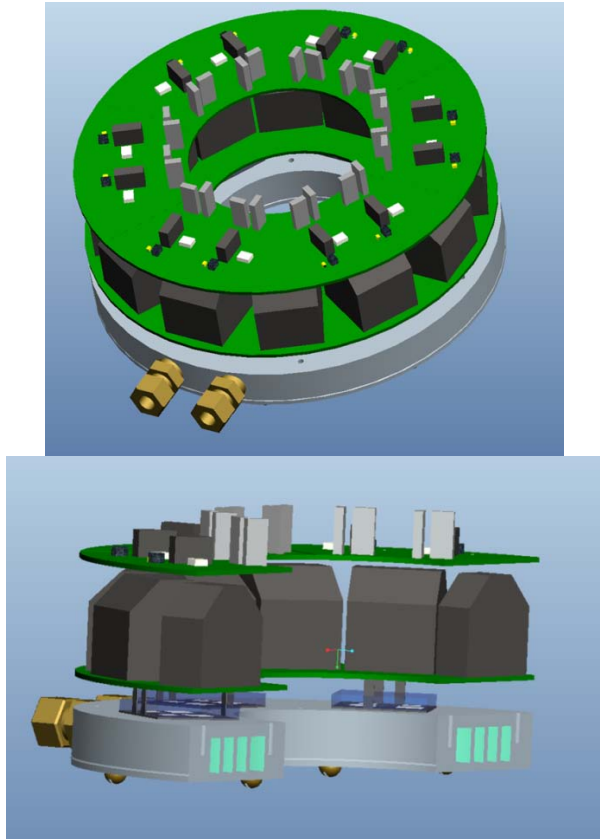


Figure II - 39: First hardware design for a 55 kW ring-shaped segmented inverter that is suited to be integrated with typical cylindrical motor prototypes.

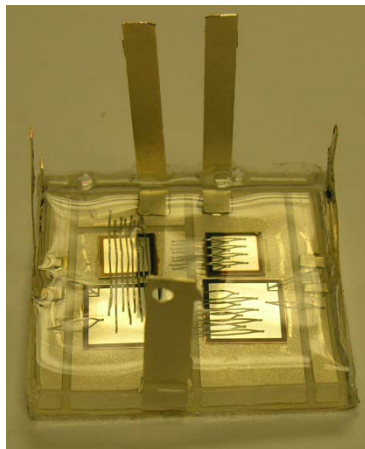


Figure II - 40: ORNL packaged IGBT module.

The IGBT modules (Figure II - 40) for the first prototype were designed and packaged at the ORNL packaging laboratory using ABB IGBT and diode dies rated at 1,200 V and 75 A. The dies are soldered on a rectangular aluminum oxide direct bonded copper substrate with a footprint of 1.5 in. by 1.38 in. The modules use wire bonds for interconnections and are potted with a type of relatively high temperature silicone

gel. A “wirebondless,” planar IGBT module featuring double-sided cooling is under development at ORNL and could be used in future prototype designs. Features of the new ORNL planar module could substantially improve thermal performance and decrease parasitic resistance and inductance in the package.

The IGBT modules were characterized using the well-known double pulse test method. Figure II - 41 shows the double pulse test circuits for the bottom and top IGBTs and the hardware setup. Figure II - 42 gives typical double pulse test waveforms of collector-emitter voltage, V_{ce} , collector current, i_c , and gate-emitter voltage, v_{ge} . IGBT conduction and switching losses at various collector currents were measured from these test waveforms.

FEAs were carried out to evaluate the thermal performance of the four-channel toroidal heat exchanger. Inlet water flow was set to 3 L/min. Water properties were consistent with that of a 66°C WEG mixture. The cooling chamber material was aluminum, with a thermal conductivity (TC) of 160 W/(m K). The silicon chip, with a TC of 163 W/(m K), was mated to a copper plate with a copper TC of 400 W/(m K). The chip-copper set was mated to Duralco thermally conductive adhesive with a TC of 5.8 W/(m K). The chip was set to produce a total of 165 W of waste heat. This waste heat was applied as a volumetric heat load. The WEG was set to an inlet temperature of 70°C. The FEA (Figure II - 43) gave a maximum junction temperature of 110.7°C, well below the typical safe operation limit of 125°C. FEA results indicated that the toroidal heat exchanger design presents a relatively low pressure drop of 0.2 psi, with the bulk of it occurring at the narrow inlet and outlet fixtures. This provides an opportunity for further optimization of the cooling channels in terms of the number and width of the channels for higher coolant temperature operations.

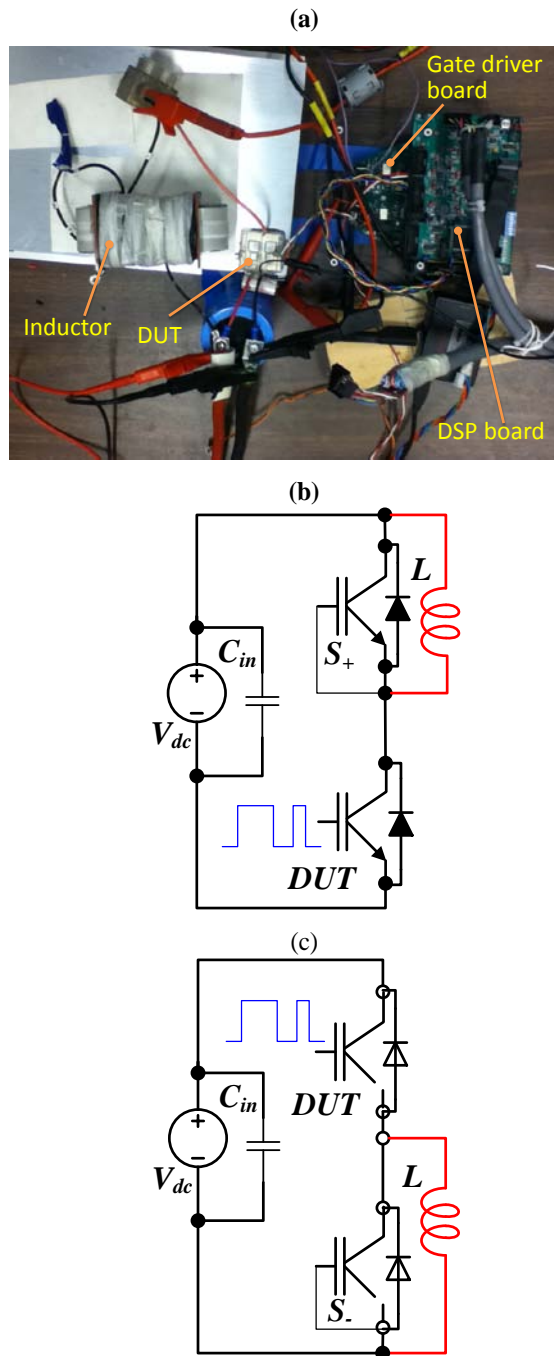


Figure II - 41: IGBT module characterization: hardware setup (a) and double pulse test circuits for the bottom IGBT (b) and the top IGBT (c).

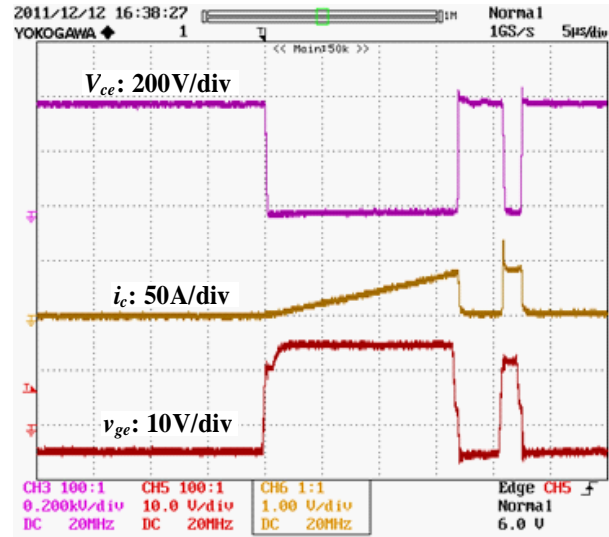


Figure II - 42: Double pulse test waveforms.

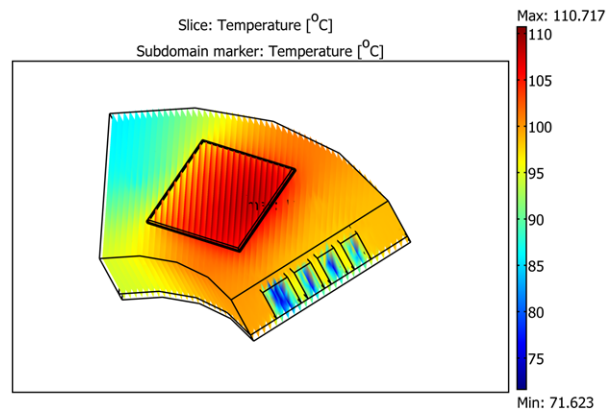


Figure II - 43: FEA results for the four-channel toroidal heat exchanger.

After the FEA results showed satisfactory thermal performance with the four-channel toroidal heat exchanger design, a 55 kW ring-shaped segmented inverter was fabricated (Figure II - 44). The use of heavy copper printed circuit board technology for interconnecting the power modules eliminates the need for bus bars and greatly simplifies the inverter assembly steps. The prototype yields a power density of 17.1 kW/L and specific power of 15.6 kW/kg.

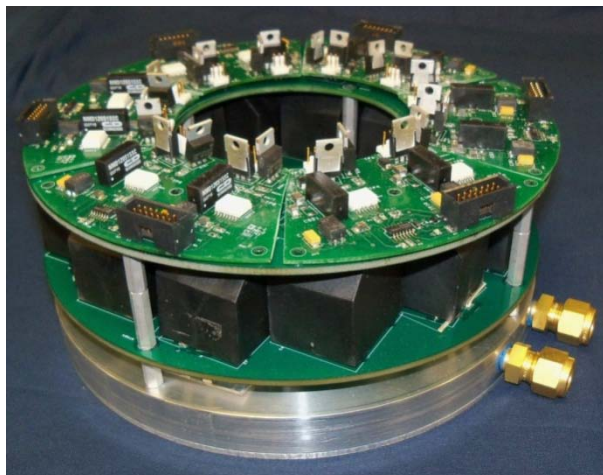


Figure II - 44: First 55 kW ring-shaped segmented inverter prototype using a four-channel toroidal heat exchanger.

The prototype was tested with both a resistive load bank and an induction motor. Figure II - 45 is a photo of the test setup. Figure II - 46 shows waveforms of battery voltage, V_{bat} , battery current, i_{bat} , three-phase output currents, i_a, i_b, i_c , and the phase-a split currents, i_{a1}, i_{a2} , with a resistive load of 15.2 kW. The battery rms ripple current is reduced from 4.21 Arms to 1.45 Arms, a 66% reduction. The waveforms of the three-phase output currents, i_a, i_b, i_c , also reveal significant reduction of high frequency ripples with the segmented inverter.

Figure II - 47 shows waveforms with an induction motor running at 783 rpm with a load torque of 92 N•m. The battery rms ripple current is reduced from 6.53 Arms to 0.9 Arms, an 86% reduction. Because of the distributed capacitors, capacitor ripple current cannot be measured. Significant reduction in the capacitor ripple current can, however, be inferred from the substantial decreases in the battery and motor ripple currents.

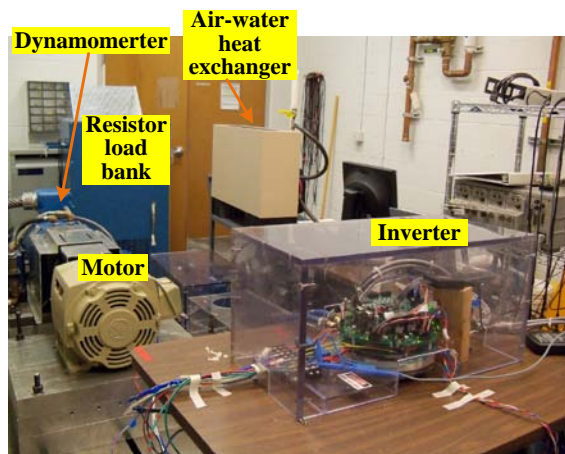


Figure II - 45: Test setup.

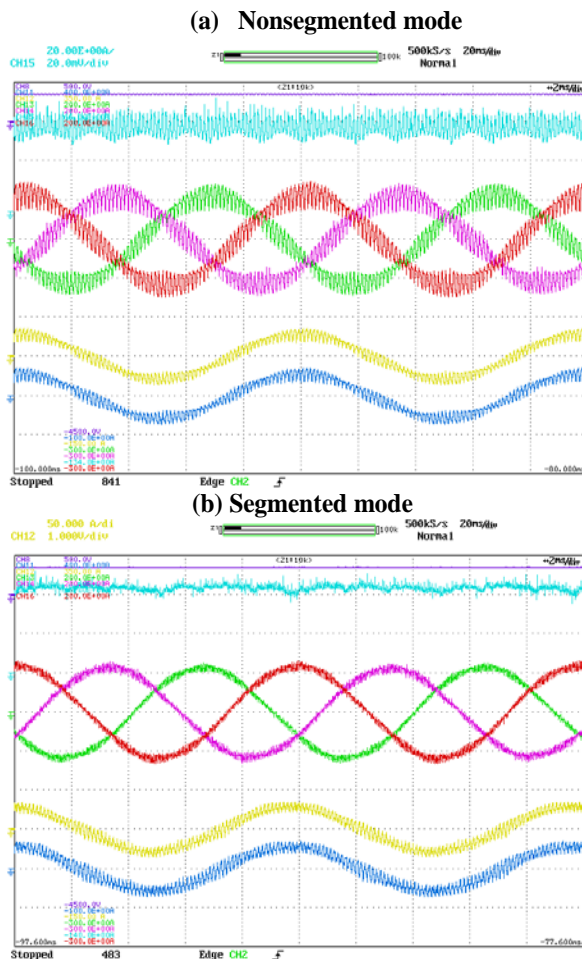


Figure II - 46: Experimental waveforms with a resistive load: (a) nonsegmented mode; (b) segmented mode. From top to bottom: V_{bat} : 500 V/div; i_{bat} : 20 A/div; i_a, i_b, i_c : 50 A/div; i_{a1}, i_{a2} : 50 A/div.

The second design uses a six-channel toroidal heat exchanger with the same outer diameter of 9 in., same inner diameter of 4 in., and same thickness of 0.75 in. It also uses IGBT modules rated at 600 V and 150 A that are better matched with the laboratory test motor for a lower dc bus voltage. Moreover, instead of the discrete block capacitors in the first design, a cylindrical capacitor is used and located in the center hole to better use the space and reduce the inverter height. Figure II - 48 is a photo of the second ring-shaped segmented inverter prototype. The second prototype design yields a power density of 17.8 kW/L and specific power of 15.6 kW/kg.

Figure II - 49 shows FEA thermal analysis results. With the six-channel design, the maximum junction temperature is reduced to 85°C from the 111°C for the four-channel design for an inlet coolant (WEG) temperature of 70°C. The FEA results indicate the six-channel design can keep junction temperatures below 125°C even at 105°C coolant temperature.

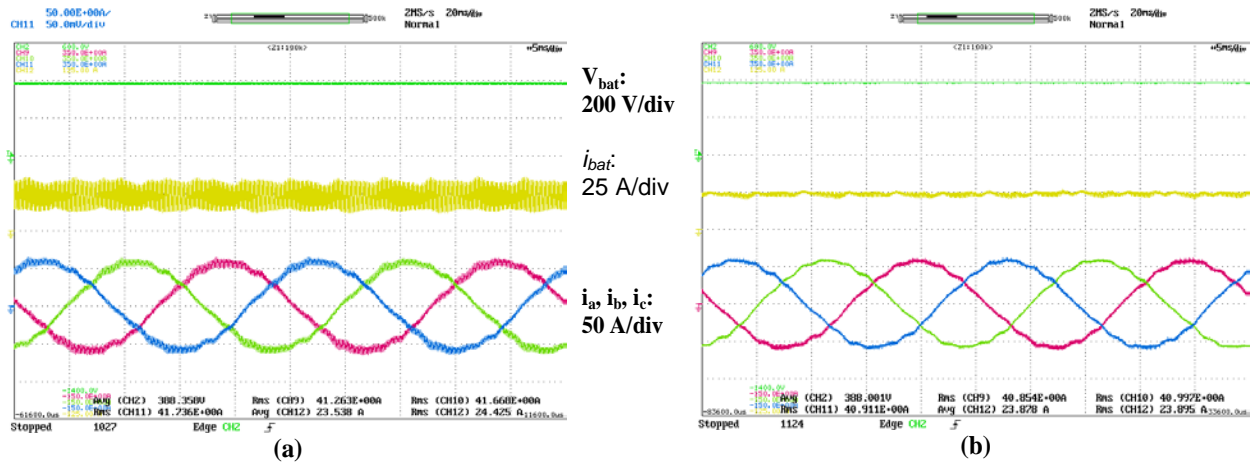


Figure II - 47: Experimental waveforms with an induction motor at 783 rpm and 92 N·m: (a) nonsegmented and (b) segmented.

The prototype was tested with both a resistive load and an induction motor. Figure II - 50 shows experimental waveforms with an induction motor running at 1,200 rpm with a load torque of 92 N·m. Again, significant ripple current reductions in the battery and motor currents are evident from the waveforms.

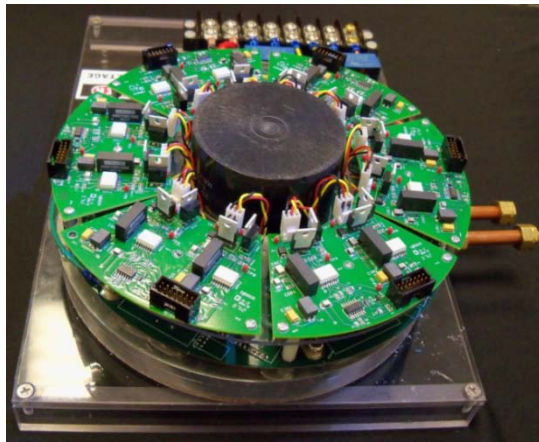


Figure II - 48: Second 55 kW ring-shaped segmented inverter prototype using a six-channel toroidal heat exchanger.

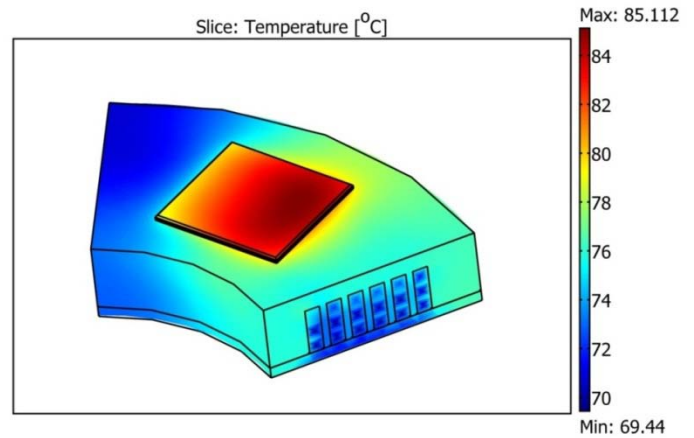


Figure II - 49: FEA results for the six-channel toroidal heat exchanger.

Conclusion

- The segmented inverter with a reduction of bus capacitance by 60% and an optimal package exceeds the DOE 2020 weight and volume targets.
- Test results demonstrated significant reductions of
 - 55% to about 75% in capacitor ripple current,
 - 70% to about 90% in battery ripple current, and
 - 60% to about 80% in motor ripple current
- Other Positive Impacts
 - Reduced battery losses and improved battery operating conditions due to substantially reduced battery ripple current.
 - Significantly reduced motor torque ripples (up to 50%) and reduced switching losses (50%).

Patents

1. G. J. Su, “Electrical Motor/Generator Drive Apparatus and Method.” US Patent Application 12/887,110, filed September 21, 2010.

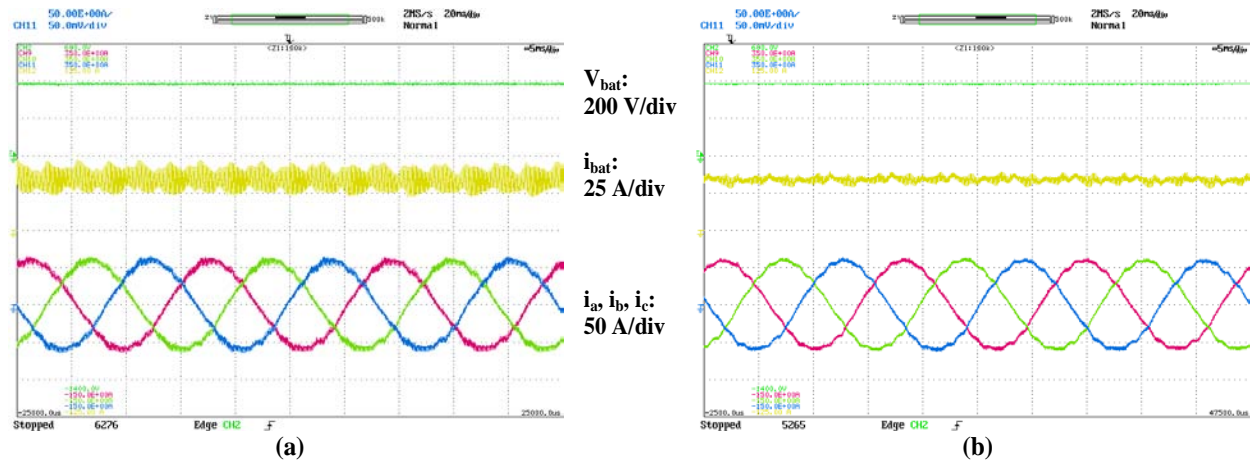


Figure II - 50: Experimental waveforms with an induction motor at 1,200 rpm and 92 N-m: (a) nonsegmented; (b) segmented.

Publications

1. G. J. Su and L. Tang, "A Segmented Traction Drive System with a Small dc Bus Capacitor," 4th *IEEE Energy Conversion Congress and Exposition (ECCE 2012)*, September 16–20, 2012, Raleigh, North Carolina, pp. 2847–2853.

References

1. J. W. Kolar, T. M. Wolbank, and M. Schrod, "Analytical calculation of the RMS current stress on the DC link capacitor of voltage DC link PWM converter systems," 9th International. Conf. on Electrical Machines and Drives, September 1999, pp. 81–89.
2. US Department of Energy, *Electrical and Electronics Technical Team Roadmap*, December 7, 2010, available online at http://www1.eere.energy.gov/vehiclesandfuels/about/partnerships/roadmaps-other_docs.html.
3. Electronic Concepts, Inc., Electronic Concept Datasheets, available online at <http://www.ecicaps.com/capacitors/features/ul3-series-unlytic-lt-sup-gt-reg-lt-sup-gt-ul31-ul32-ul34-ul35-series>

II.4 Converter Topologies for Wired and Wireless Battery Chargers

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Objectives

- Overall objective
 - Develop a 5 kW integrated onboard battery charger that fully uses the existing onboard power electronics components to reduce cost, volume, and weight and simultaneously provide galvanic isolation and the capability of charging fully depleted batteries.
- FY 2012 objective
 - Design, build, and test a 5 kW isolation converter (which is a part of the integrated onboard charger).

Approach

- Use the existing onboard power electronics components to reduce cost, weight, and volume and accomplish galvanic isolation.

Major Accomplishments

- Completed hardware design, fabrication, and test of a 5 kW isolation converter.
- Confirmed through testing that the goal of greater than 97% efficiency had been met (achieved maximum efficiency of 98.4%).

Future Direction

- Design, build, and test a 6.6 kW integrated onboard charger prototype using wide bandgap devices.

◇ ◇ ◇ ◇ ◇

Technical Discussion

Background

Plug-in electric vehicles (PEVs) are emerging as a pre-fuel-cell technology that offers greater potential to reduce oil consumption and carbon dioxide emissions than the hybrid vehicles currently on the market. In hybrid PEVs, the energy storage capacity of the battery needs to be increased significantly to enable a driving distance of at least 40 miles in an all-electric mode, the distance needed to substantially reduce oil consumption for daily commuting. A charger is also required to replenish the battery after it is depleted, typically done overnight to leverage energy costs by taking advantage of off-peak electricity rates [1].

Stand-alone battery chargers, however, impose an extra cost on already expensive plug-in hybrid electric vehicles (PHEVs) and have other limitations. A typical stand-alone battery charger for PEVs consists of a diode rectifier with power factor correction and a unidirectional dc-dc converter (i.e., it can only charge the battery) that uses power semiconductor switches, diodes, inductors, and capacitors, as shown in Figure II - 51. A charger with a low charging capability of 1 to 3 kW can cost almost 30% as much as the electric traction system for a mid-size PEV car (estimated at \$300 to \$400, about half of the DOE 2015 cost target of \$660 for the entire traction drive system). The limited charging capability results in a long charging time (6–8 h), which could negatively impact the acceptance of PEVs. The long charging times are of greater concern with battery electric vehicles (BEVs), which are equipped with larger capacity battery packs. Moreover, most of the onboard chargers on the market are unidirectional [i.e., can only charge the battery but are not capable of vehicle-to-grid (V2G) support] to keep costs low.

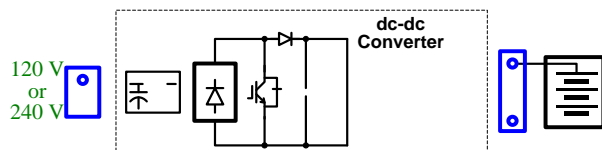


Figure II - 51: A schematic showing major components in a stand-alone wired battery charger.

To minimize the cost of the charger while simultaneously providing other desirable features such as V2G support and mobile power generation, a previous project, finished in FY 2009, examined the use of the power electronics and motors already onboard the vehicle to fulfill the charging requirements [2, 3]. The project demonstrated that, compared with a stand-alone battery charger, this approach imposes virtually no additional cost or significantly reduces the cost depending on the configuration of the onboard traction drive system. The proposed approach is to integrate the battery charging function into the traction drive system and eliminate or minimize the number of additional components. Because traction power inverters have a greater current-carrying capability, the integrated charger can reduce the charging time significantly. Another benefit of this approach is that it enables PEVs to function as mobile power generators and provide V2G support capabilities at little or no additional cost. An integrated charger prototype (Figure II - 52) using a traction drive comprising a 55 kW motor inverter and a 30 kW generator inverter was demonstrated with (1) capability of providing charging power of 20 kW, (2) 90% cost reduction compared to a standalone charger, (3) high efficiencies of 93% to 97%, and (4) mobile power generation and V2G operations.



Figure II - 52: An integrated charger prototype using a traction drive comprising a 55 kW motor inverter and a 30 kW generator inverter.

It has been found, however, that the integrated charger lacks galvanic isolation, which makes it difficult to meet safety requirements and to charge “dead” batteries. The

purpose of this project is, therefore, to propose an integrated onboard charger topology that uses the onboard traction drive system and the low-voltage converter to reduce the cost, volume, and size while simultaneously providing galvanic isolation and the capability to charge fully depleted batteries.

Integrated Onboard Charger

Figure II - 53 shows a conceptual block diagram for the new approach under investigation in this project that uses the onboard power electronics components and electrical motors to provide plug-in charging and discharging capabilities for PHEVs and BEVs. Figure II - 54 shows the previous topologies for using the onboard electrical drive system (without galvanic isolation) to provide plug-in charging and mobile generation capabilities for PHEVs. The new approach will similarly use the traction drive system components but also add galvanic isolation and the capability of charging batteries over a wide range of voltage levels. Details of the new circuit topology, however, will not be disclosed in this report because it is under patent review.

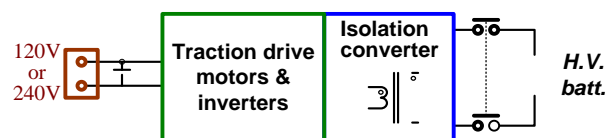


Figure II - 53: A conceptual block diagram for the new approach using the onboard power electronics components and electrical motors to provide plug-in charging and discharging capabilities with galvanic isolation for PHEVs and BEVs.

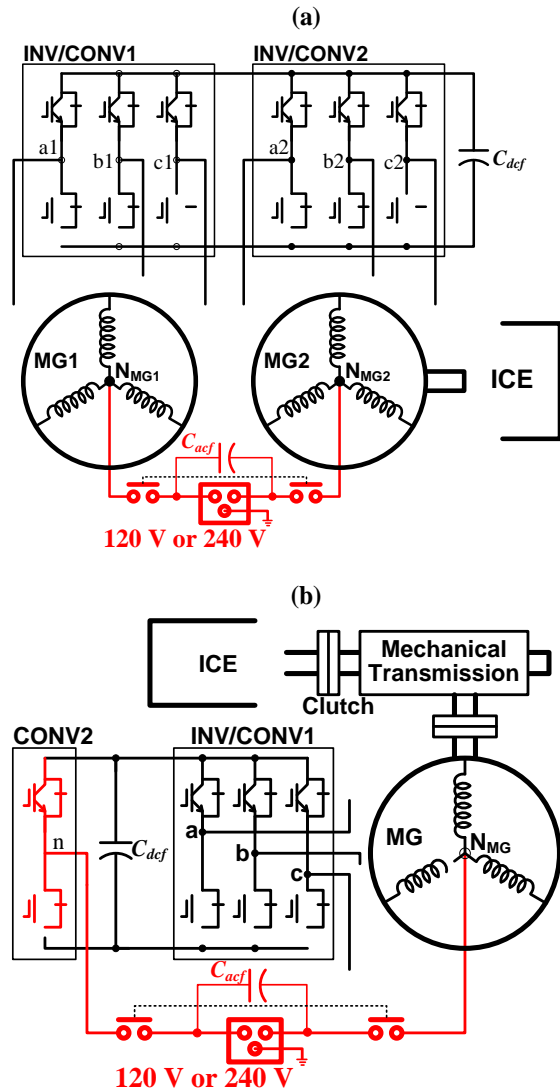


Figure II - 54: The previous topologies for using the onboard electrical drive system to provide plug-in charging and mobile generation capabilities for PHEVs: (a) for PHEVs using two inverters and motors and (b) for PHEVs and BEVs using a single inverter and motor. (Red denotes additional components necessary for the circuit.)

The onboard electrical drive system may consist of one or more electrical motor drive units, all connected to a common dc bus. Each motor drive unit typically uses a three-phase inverter/converter (INV/CONV) and a three-phase motor/generator (M/G) with a Y-connection of stator windings with a neutral point ($N_{M/G}$). At least one drive unit is coupled to the engine shaft through a mechanical transmission device. The basic idea is to use the M/Gs as inductors by connecting their neutral points to an external charging source to charge the battery or to external loads to supply power to them. The external charging source can be a dc or single-phase or three-phase ac power supply, depending on the number of onboard drive units. Figure II - 54 (a) illustrates an arrangement for a series PHEV in which two INV/CONVs and two M/Gs are used. For such vehicles, virtually no additional components except some wiring and connectors are required. An ac filter capacitor may also be needed to meet grid interface power quality requirements. For parallel PHEVs and BEVs, in which only one INV/CONV and M/G are used, two switches must be added, as shown in Figure II - 54(b).

All the switch legs in each INV/CONV collectively function as a single switch leg and the M/G as an inductor [i.e., its stator zero sequence impedance network (ZSIN)] consisting of three branches, each branch comprising the stator winding phase resistance and the stator phase leakage inductance, as shown in Figure II - 55. Together, the drive units form a single-phase or multiphase converter, operating in the charging mode, to regulate the dc bus voltage. In the generation mode, the drive units form a single-phase or multiphase inverter to supply external loads. In this mode, the M/G of the drive unit coupled to the engine shaft is driven by an engine to generate power to supply the dc bus and ultimately the external loads. Or power can be drawn from the battery for short operating intervals. An additional benefit of operating the three-phase converters as single leg converters is the reduction in harmonic current components resulting from interleaving the gating signals of the three legs.

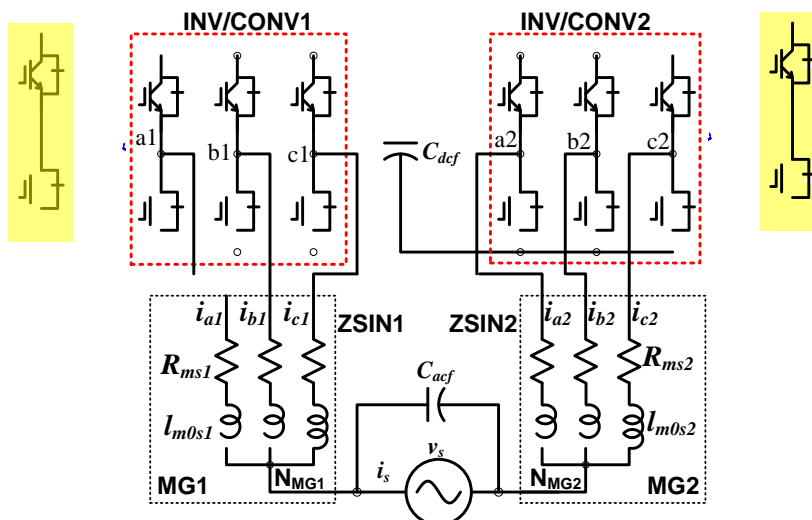


Figure II - 55: An equivalent circuit for the traction drive system in Figure II - 54(a) when operating in the battery charging mode.

Detailed circuit simulations were performed using PSIM¹ in FY 2011 to prove the concept and provide circuit design data for use in development of a prototype 5 kW integrated wired charger. Simulation results confirmed that the new topology can (a) achieve the goal of reducing cost, weight, and volume by 70%; (b) meet galvanic isolation requirements; (c) charge at nominal and fully depleted battery voltage levels; and (d) have high power factor and low current total harmonic distortion (THD). The THD factors are in the range of 2.8% to 6.6% and lower than 5% when charging rates are more than 1 kW. The power factors are in the range of 97% to 99.6% and greater than 98% when charging rates are more than 1 kW.

During the current fiscal year (FY 2012), a 5 kW isolation converter was designed, built, and tested as part of an integrated onboard charger. Figure II - 56 shows a three dimensional (3D) drawing of the 5 kW isolation converter design. The design uses 600 V rated silicon power metal-oxide semiconductor field-effect transistors (MOSFETs) and a planar transformer to form a galvanic isolated dc-dc converter. All the components are mounted on an alumina cold plate with a footprint of 6 in. by 7 in. Gate driver printed circuit boards are then mounted directly over the MOSFETs to eliminate wire connections between them. In addition, a control printed circuit board using a Texas Instruments TMS320F1208 fixed-point digital signal processor (DSP) controller is located on the top.

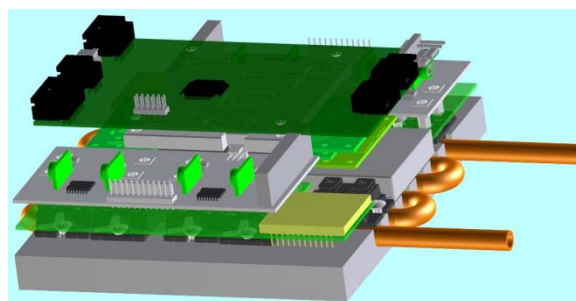


Figure II - 56: Three dimensional drawing of the 5 kW isolation converter design.

A 5 kW isolation converter prototype was fabricated according to the design. Figure II - 57 is a photo of the isolation converter prototype, and Figure II - 58 is a photo of the planar transformer, which is constructed using a flat ferrite core and printed circuit boards for primary and secondary windings. The planar transformer measures 5 in. × 2.5 in. × 0.78 in.

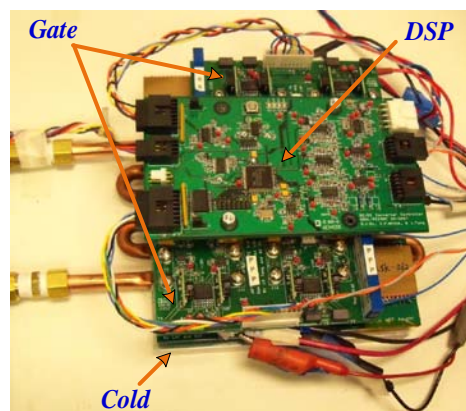


Figure II - 57: Photo of the 5 kW isolation converter prototype fabricated.

¹Simulation software from Powersim Inc.

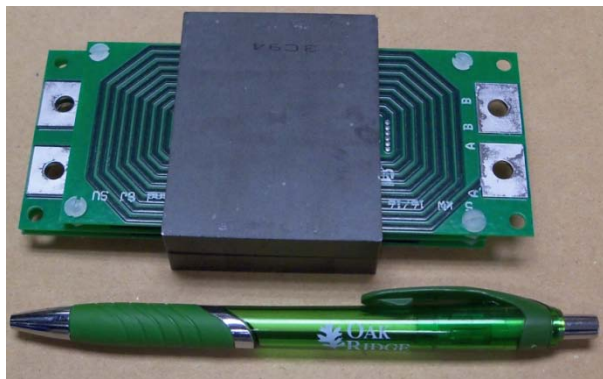


Figure II - 58: Photo of the planar transformer (footprint: 5 in. by 2.5 in.).

The converter prototype was tested with a resistive load bank. Figure II - 59 plots typical operating waveforms, in which V_{out} , v_{Tr_pri} , v_{Tr_Sec} , I_{out} , i_{Tr_Pri} , and I_{in} are output dc voltage, transformer primary voltage, transformer secondary voltage, output dc current, transformer primary current, and input dc current, respectively. Figure II - 60 gives expanded traces of the operating waveforms in Figure II - 59 showing the rising edges (a) and the falling edges (b) of the transformer voltage waveforms. Smooth transitions in the transformer voltage waveforms indicate soft switching operations.

Figure II - 61 plots measured converter efficiency vs. output power. The efficiencies are greater than 97% for output power levels up to 5 kW, and the maximum efficiency is 98.4%.

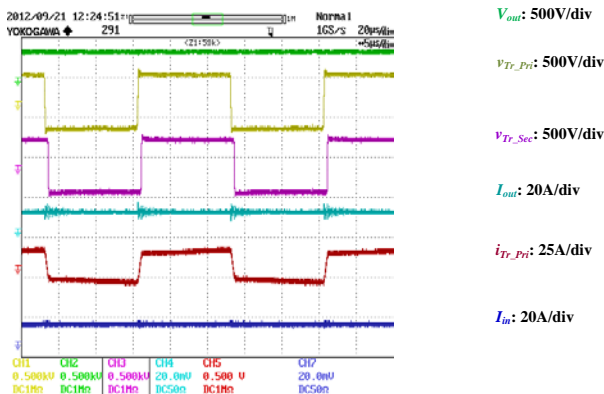
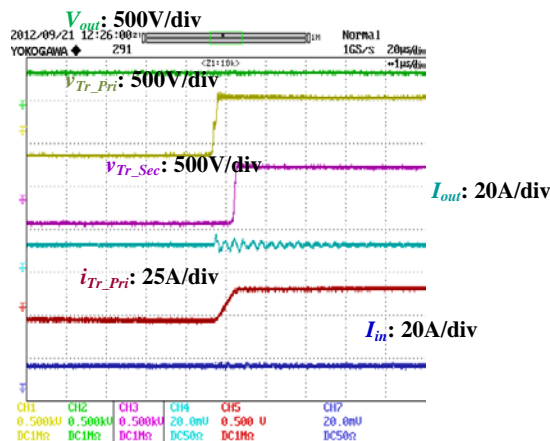


Figure II - 59: Operating waveforms showing from top to bottom: output dc voltage, V_{out} ; transformer primary voltage, v_{Tr_pri} ; transformer secondary voltage, v_{Tr_Sec} ; output dc current, I_{out} ; transformer primary current, i_{Tr_Pri} ; and input dc current, I_{in} .

(a)



(b)

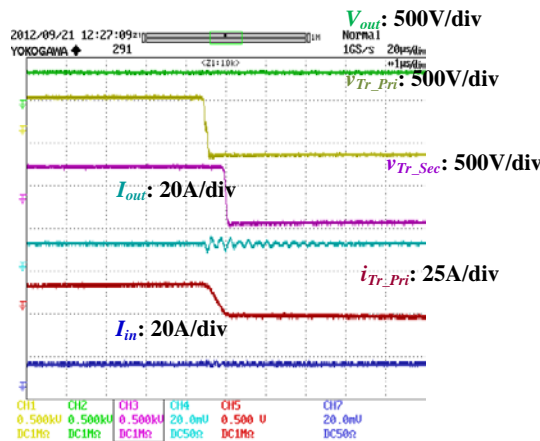


Figure II - 60: Expanded traces of the operating waveforms in Figure II - 59 showing the rising edges (a) and the falling edges (b).

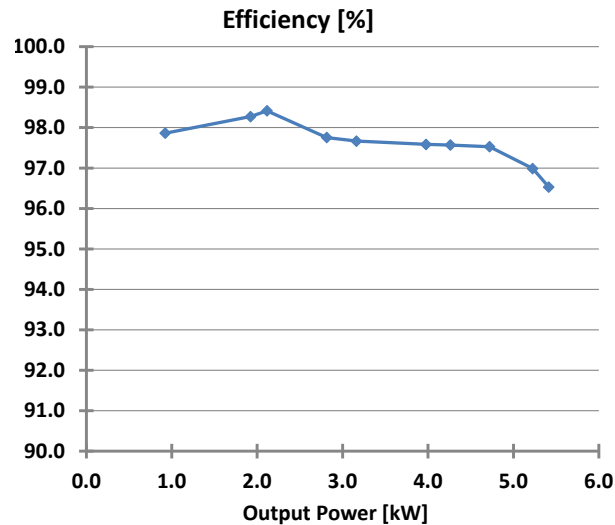


Figure II - 61: Measured efficiency of the 5 kW isolation converter.

2. G. J. Su, US Patent 7,733.039B2, “Electric Vehicle System for Charging and Supplying Electrical Power,” June 8, 2010.
3. L. Tang and G. J. Su, “A Low-Cost, Digitally-Controlled Charger for Plug-In Hybrid Electric Vehicles,” *IEEE Energy Conversion Congress and Exposition (ECCE)*, September 20–24, 2009, San Jose, California, pp. 3923–3929.

Conclusion

This project extends the previous approach of using the onboard power electronics components to provide plug-in charging functionality. The new approach under investigation in this project similarly uses the traction drive system components to reduce the cost, weight, and volume but also accomplishes galvanic isolation and provides the capability of charging batteries at a wide range of voltage levels. Detailed circuit simulation results proved the concept and showed high performance in meeting the utility connection requirements for power quality: (a) THD factors are in the range from 2.8% to 6.6% and lower than 5% when charging rates are more than 1 kW and (b) the power factors are in the range from 97% to 99.6% and greater than 98% when charging rates are more than 1 kW. Based on the simulation results an isolation converter for use in a 5 kW integrated onboard charger was designed, fabricated, and tested in FY 2012. Test results confirm efficiency greater than 97%.

Patents

1. G. J. Su, Invention disclosure 201202931, “Electric Vehicle System and Method for Recharging and/or Supplying Electrical Power,” 2012.

Publications

None.

References

1. *Advanced Batteries for Electric-Drive Vehicles*, Report 1009299, Electric Power Research Institute: Palo Alto, California, May 2004.

II.5 Highly Integrated Power Module

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Objectives

- Examine different technologies that could be integrated into a power module such that it contains the switching power device, gate drive, buffer, isolation, protection, and current sensing.
- Characterize a high temperature silicon-on-insulator (SOI) gate driver for use in an intelligent power module.
- Investigate input isolation schemes for the interface between a microcontroller and gate driver.
 - Design and construct prototypes to verify functionality of the input isolation schemes.
 - Compare and contrast designs to determine final solution for input isolation.
- Compare and analyze different buffer topologies to boost the output current from the SOI gate driver integrated circuit (IC).
 - Determine feasibility of high temperature buffer circuit and best topology in terms of current gain and cost.
- Optimize switching characteristics of high power silicon insulated gate bipolar transistor (IGBT) modules.
- Mitigate cross talk for wide bandgap (WBG) power devices in a phase leg configuration, leading to lower switching losses, fast switching speed, and high reliability.
- Develop a noncontact, low cost current and temperature sensor that could be integrated into a power module

Approach

- Characterize the operation of the gate driver across various temperatures using a temperature chamber and a tape heater configuration and testing with WBG power switches.
- Investigate capacitive and transformer-based isolation designs.
 - Construct prototype printed-circuit-board (PCB) level designs of the input isolation with discrete components.
 - Test and characterize the input isolation prototypes for functionality, temperature capability, and speed limitations.
 - Determine feasibility of on-chip isolation design.
- Examine different buffer topologies and choose candidates for further analysis and improvement.
 - Optimize the candidate buffer topologies by taking the driving capability, switching speed, circuit complexity, and cost into account.
 - Search for high temperature components suitable for buffer application.
- Design an active gate driver (AGD) which is capable of adaptively controlling the switching behavior of IGBT modules and reducing the switching time and loss in IGBTs.
 - Simulate the AGD with real component models in Saber.
 - Build the double-pulse-tester-based hardware, and verify the AGD through extensive measurements.
- Propose a novel gate assist circuit according to the intrinsic characteristics of WBG devices and the mechanism causing the cross talk for the sake of cross talk mitigation.
 - Fabricate a corresponding gate drive board to verify the effectiveness of the proposed gate assist circuit.
- Evaluate a commercial analog Hall-effect device with a prototypical current measurement layout.
 - Explore the use of a fourth order Chebyshev filter at the output of the Hall-effect circuit to remove the switching harmonics.

Major Accomplishments

- Completed more than 336 h of 200°C and 225°C reliability testing of the latest generation gate driver.

- Characterized gate driver charge pump operation.
- Completed additional testing of the gate driver with SiC metal-oxide semiconductor field-effect transistors (MOSFETs), junction field-effect transistors (JFETs), and bipolar junction transistors (BJTs).
- Constructed multiple prototypes for both capacitive- and transformer-based isolation schemes.
- Experimentally demonstrated the functionality of both isolation designs.
 - Transformer-based design verified with coils constructed on separate printed circuit board layers.
 - Capacitive-based design verified with both discrete capacitors and capacitors built into printed circuit board layers.
- Completed schematic design and simulations of an on-chip transformer isolation design.
- Compared all three proposed buffers to a 30 A rated commercial buffer IC, and determined that all performed better in terms of driving speed and cost less.
- Fabricated the prototype IGBT power module with an AGD.
 - Measured and compared the switching characteristics under different gate resistors and current levels.
 - Determined the AGD could reduce the turn-on switching loss (20% to 35%), turn-off switching loss (10% to 25%), turn-on delay (50% to 80%), and turn-off delay (50% to 80%) from low to high gate resistors compared to a conventional gate driver (CGD).
- Proposed a novel gate assist circuit for the cross talk mitigation for a phase leg using WBG devices.

Future Direction

- Integrate best candidate technologies into a high temperature power module for use with WBG power devices.
- Develop purpose-based gate driver ICs for the intelligent power module.
- Integrate the gate driver ICs into the power module.
- Finalize design and layout of on-chip design. Fabricate chips of isolation design.
- Test and characterize performance of chips.
- Investigate other chip technologies for higher isolation capability.
- Implement and test high temperature buffer.

- Adopt AGD and protection techniques applied to WBG devices.
- Develop power supply on a chip for use in module.



Technical Discussion

High Temperature Gate Driver

Characterization of an SOI highly integrated gate driver carried out this year included reliability testing at 200°C and 225°C. The gate driver was placed inside a temperature chamber in the configuration shown in Figure II - 62. The gate resistor (R_G) was 2 Ω and the load was 10 nF. The circuit was left in the temperature chamber operating for more than 336 h (2 weeks) at each of these temperatures. The results were positive, with the gate driver surviving both the 200°C and 225°C tests. The results for 225°C, for which the gate driver was left operating for 400 h, are shown in Figure II - 63.

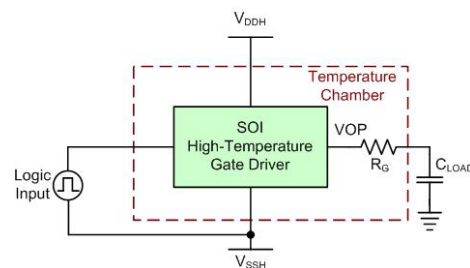


Figure II - 62: Reliability test configuration.

Other data taken include output current measurements using a chip-on-board (COB) gate driver. The COB approach removes the parasitics associated with the ceramic package and plastic/nylon socket by directly connecting the gate driver die, through bond wires, to the test board. The lower parasitics increase the accuracy of the measured drive current (Figure II - 64).

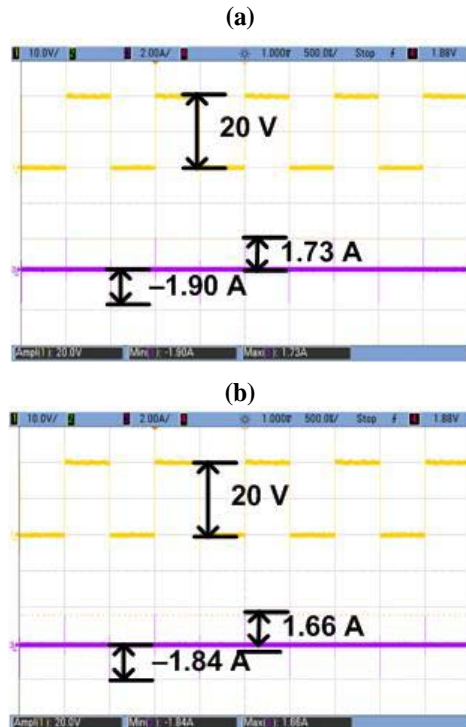


Figure II - 63: Results for 225°C reliability test driver output at (a) hour 0 and (b) hour 400.

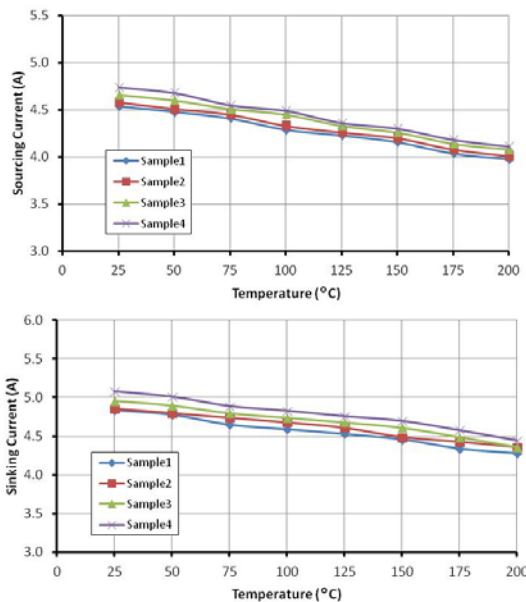


Figure II - 64: COB sinking and sourcing current.

Input Isolation

The control circuitry of the power module requires an isolation barrier for the interface between the logic-level control signal and voltage level of the gate driver that operates the high side of a power phase leg. The two input isolation schemes were capacitive and transformer designs.

The printed-circuit-board-level implementation of these designs allowed for both high temperature and high voltage isolation to be realized.

The first capacitive isolation prototype used high temperature capable mica capacitors that could block 1 kV. The revised PCB for capacitive isolation featured capacitors built into the PCB layers. The design of the capacitive-based isolation (Figure II - 65) is much simpler than that of the transformer-based isolation (Figure II - 66). Besides the capacitors and a couple resistors, it only requires a few extra discrete ICs. It needs a buffer, an inverter, two comparators, and a SR latch. After improving the driving capability of the inverter and buffer and the speed of the comparator for the revised PCB, the design demonstrated functionality at high speeds (beyond 1 MHz).

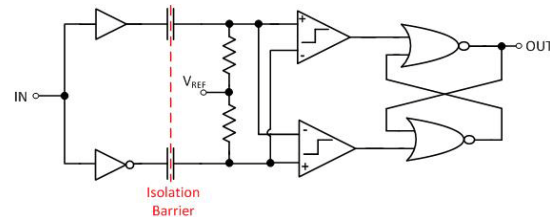


Figure II - 65: PCB capacitive isolation schematic.

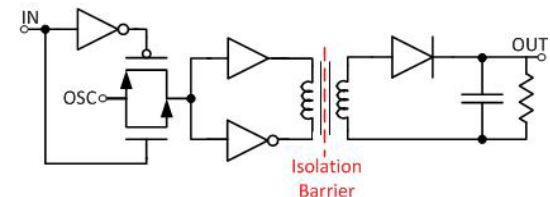


Figure II - 66: PCB transformer isolation schematic.

The transformer isolation prototype was realized with coils built into PCB layers. Transformers with varying diameters and turn ratios were investigated. This design required a local oscillator and mixer schematic to modulate the input logic signal to a frequency that the transformer could handle. This design also drew a much larger amount of current than the simple capacitive design. Power MOSFETs connected as inverters were added to increase the current drive of the primary coil of the transformer. The implementation of this design also uses current limiting resistors, a resonant capacitor, a diode, an RC demodulation circuit, and an output buffer. Functionality was displayed with a noticeable amount of delay. The main frequency limitation of this prototype is the oscillator and delays introduced from the rest of the circuitry.

The temperature capability of the capacitive- and transformer-based prototypes was determined by the discrete ICs used in the designs, which were limited to 125°C. The PCB integrated capacitors and transformers using polyimide material can be operated at much higher temperatures. Another advantage of the PCB integrated components is the high voltage isolation, 44 kV/mm.

After investigating the PCB level isolation designs, it was determined that a higher level of integration was desirable. This led to an on-chip transformer isolation design based on the design in [1]. The design is shown in Figure II - 67. This design is implemented in 5 V complementary metal-oxide semiconductor (CMOS) technology. The transformer size is small because of the high frequency used (gigahertz). This is currently being designed and simulated in a high temperature capable SOI technology. The isolation capability of the design is limited by the thickness between metal layers on the chip. Because the transformer requires routing of an internal node of a coil, it requires three or more conducting layers. However, a parallel plate capacitor may be implemented on two layers, which leads to higher voltage isolation. From this higher voltage isolation, the isolation barrier of the design is likely to be switched to the capacitors after the transformer. For the current chip design process, this can lead to a voltage isolation of about 2 kV.

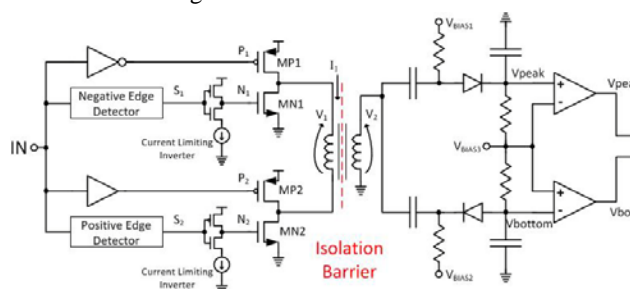


Figure II - 67: On-chip design.

Buffer

As a result of research on different buffer topologies, three topologies were determined to be good candidates for a high performance buffer. Circuit modifications and optimization were carried out to overcome their shortcomings, and the experiment results verified the performance of the proposed buffers.

1. Bipolar Junction Transistor Emitter Follower

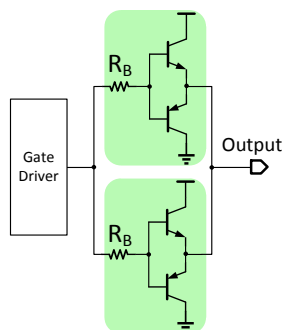


Figure II - 68: Parallel connection of emitter follower.

The emitter follower is widely used because of its easy implementation. Modern medium power BJTs can offer a transition frequency of 130 MHz at 60 V and 20 A rating. This gives a satisfactory speed for most

applications. When a large output current is required, parallel connection of buffers as in Figure II - 68 can improve the performance. With a parallel connection, the collector current of each transistor is halved and the beta drop due to high level injection and current crowding is mitigated because of the decrease of collector current. A parallel connection also reduces the parasitic impedance of the output branch. The base resistors R_B are added to improve current sharing: a larger base current in one of the transistors due to component variation will develop a larger voltage drop on its R_B and in turn reduce the base current of that transistor.

2. Double N-Channel Field-Effect Transistor Totem Pole

The SOI gate driver IC [2] can provide both high side and low side driving signals. This facilitates use of the double NFET (N-channel field-effect transistor) totem pole driver. The speed of this driver is largely dependent on the output resistance of the gate driver IC and the C_{RSS} of the NFET used in the buffer: when the high side NFET is turning on, the voltages of its gate and source rise at the same rate so that the C_{ISS} is “boot-strapped” out and most of the input current is flowing in C_{RSS} . At the transient of low side NFET turn-on, the input will also be clamped by C_{RSS} by the Miller effect until C_{RSS} is fully charged [3]. This can be seen by looking at the waveforms of the high side transistor during the turn-on transient in Figure II - 69; the waveforms for the low side transistor are similar.

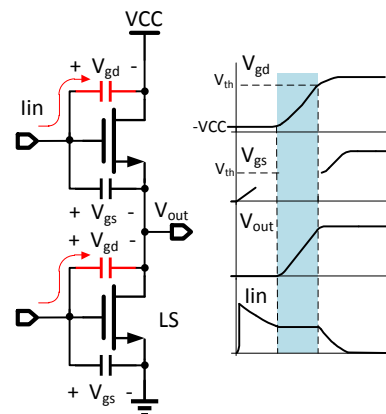


Figure II - 69: Double NFET totem pole buffer and its turn-on waveforms.

3. Complementary Metal-Oxide Semiconductor Buffer

As mentioned previously, the two main problems of CMOS buffers are large shoot-through current and the level inversion from input to output. By using the design shown in Figure II - 70, these two problems can be solved simultaneously. The two stage design ensures non-inverting operation. The transistors of the first stage can have lower current drive and smaller input capacitance while those in the second stage will be designed for the

large current required by the load. The resistor R_{lim} limits the shoot-through current in the first stage. Moreover, it generates dead time for the second stage: at switching transitions, the conducting second stage transistor is turned off quickly through the first stage transistor while the nonconducting one is turned on slowly through R_{lim} . As a result, the turn-on is delayed by the time constant consisting of R_{lim} and the input capacitance of the driver transistors, so that shoot-through is prevented. The value of R_{lim} will directly affect the performance of the buffer. A smaller value will increase the driving speed and current and decrease the propagation delay but at the same time increase the power dissipation in R_{lim} and decrease the safety margin of the dead time.

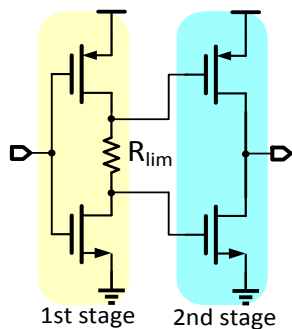


Figure II - 70: Two-stage CMOS buffer.

4. Experimental Results

To verify the analysis and optimization above, experiments were carried out to quantify the buffers' performance. The experiment setup is shown in Figure II - 71: the buffer is driven by the gate driver in [2], and the output is connected to a 28 nF load capacitor. The power supply of the buffer is -7 V and 15 V and the rise time t_r and fall time t_f are measured between 2 V and 13 V. The peak sourcing current I_{src} and sinking current I_{sink} are measured at the load with a Powertek CWT Rogowski current transducer. The typical experiment waveforms with both rising and falling edge are shown in Figure II - 72. All the experiments described in this report used this same setup for comparison purposes.

The performances of BJT emitter follower buffers were measured first. The BJTs used were Zetex FZT851 and FZT951. The results with and without the proposed parallel connection are plotted in Figure II - 73. From the figure, it can be seen that the buffer with parallel connection shows a larger output current and faster switching speed.

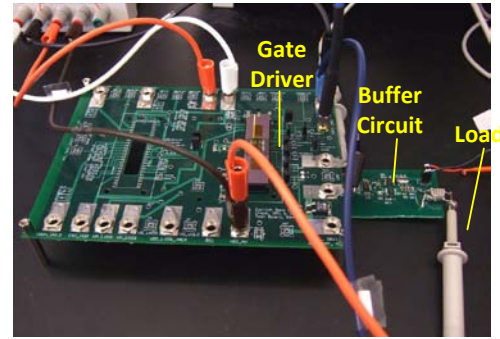


Figure II - 71: Experiment setup.

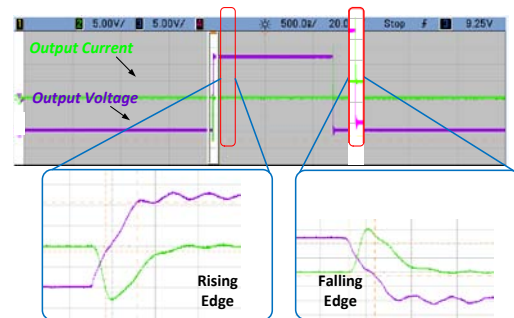


Figure II - 72: Typical experiment waveforms.

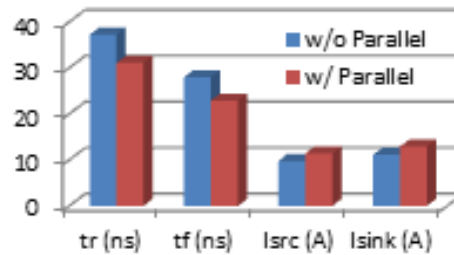


Figure II - 73: Performance comparison with and without parallel connection.

The performance of the double NFET totem pole buffer with different NFETs was measured with the same experiment setup, and the results are given in Table II - 3. The driving speed and output current are both inversely proportional to the C_{rss} of the NFET used. The eGaN FET from EPC offers exceptionally small C_{rss} and R_{on} , making it an ideal component for this buffer.

Table II - 3: Experimental results of double NFET buffer with different NFETs.

NFET Model	C_{rss} (pF)	t_r (ns)	t_f (ns)	I_{src} (A)	I_{sink} (A)
EPC2014 (GaN)	10.2	21.3	18.5	15.5	16.8
STD27N3LH5	19	24.2	23.9	12.5	12.9
PSMN013-30YLC	39	29.6	28.3	11.2	11.5
IRFR024N	65	33.1	32.8	10.2	10.8

The performance of the CMOS buffer was measured with different values of R_{lim} . The component used was a Fairchild FDS4897C, which has both P-channel FETs and NFETs integrated in the same package, and this configuration effectively reduces the parasitics. The results

are plotted in Figure II - 74. It can be seen that a trade-off must be taken when sizing this resistor. To obtain a balance between speed, power dissipation, and dead time, 18 Ω is chosen as the optimum.

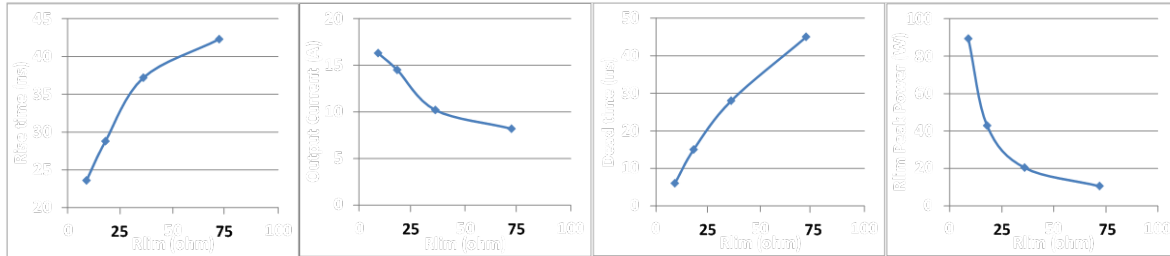


Figure II - 74: Experimental results of CMOS buffer with different R_{lim} values.

Table II - 4 summarizes the experimental performances of the three buffers discussed in this paper and that of a commercial buffer IC with a 30 A rated output current. All the buffers were measured under the same setup to get a good comparison. It can be seen that all three buffers show comparable or better performance and

lower cost compared to the commercial IC. Among these three topologies, the CMOS buffer is the choice if application is cost sensitive. The double NFET totem pole buffer with GaN FET achieves best performance, but at a higher cost. The BJT emitter follower shows good overall performance and acceptable cost.

Table II - 4: Comparison of three buffer topologies and a commercial 30A buffer

Topology	Component	t_r (ns)	t_f (ns)	I_{src} (A)	I_{sink} (A)	Cost (\$) ^a
BJT emitter follower	FZT851+FZT951 X 2	31.1	22.9	11.4	12.9	4.18
Two NFETs	EPC2014 X 2	21.3	18.5	15.5	16.8	5.40
CMOS buffer	FDS4897C X 2 + 18 ohm R_{lim}	27.8	18.8	14.5	16.3	1.80
Commercial 30 A buffer	IXDD630	36.4	27.0	12.0	13.0	7.78

^aBased on Digi-Key prices.

Active Gate Driver

The goal of the AGD developed for this task is to reduce the switching loss, delay, and total switching time while maintaining the switching stress and electromagnetic interference noise level during both turn-on and turn-off transients.

1. Turn-on Performance Improvement

The block diagram and the corresponding circuit implementation of the AGD for turn-on performance improvement are shown in Figure II - 75 and Figure II - 76. There are four function blocks: di/dt sensing, logic circuit, level shifter, and gate charger. This di/dt sensing network is used to detect the different switching stages, and the logic part is used to activate or deactivate the AGD at different stages. The level shifter serves as an interface between the logic part and gate charger controlled for gate current injection.

Comparisons with a CGD were made to investigate the operational performance of the proposed gate driver. The device used for the experimental test is a 600 V, 400

A Powerex IGBT module (CM400DY-12NF). The switching waveforms for the CGD circuit were acquired using a gate resistance of 10 Ω , which is a typical value for obtaining acceptable low-noise switching for this IGBT.

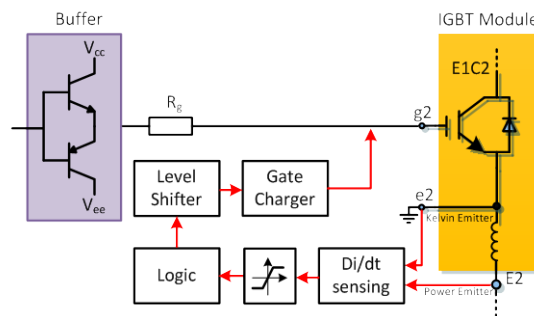


Figure II - 75: Block diagram of AGD (turn-on).

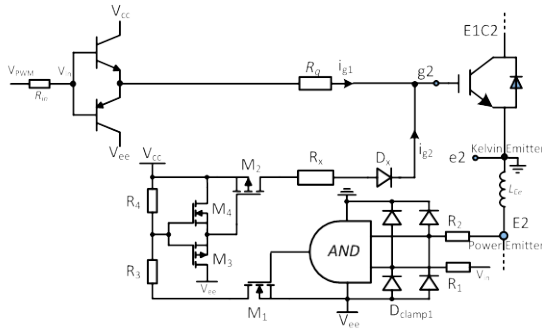


Figure II - 76: Circuit implementation of AGD (turn-on).

Figure II - 77 presents the turn-on switching waveforms at 300 V dc bus voltage and 200 A load for the CGD and AGD. The waveforms plotted from top to bottom are the gate voltage, collector emitter voltage, turn-on energy loss, and collector current. It can be seen that the proposed gate drive circuit reduces the turn-on delay time and the total switching time while keeping the same reverse-recovery current as that using the CGD. The Miller's plateau time is clearly visible for both drives. The duration for the CGD is 1.4 μ s. In contrast to this, when the proposed gate driver is used, the Miller's plateau duration is significantly reduced (0.35 μ s). The turn-on energy loss is also reduced with the AGD: 11.0 mJ compared to 14.9 mJ when using the CGD.

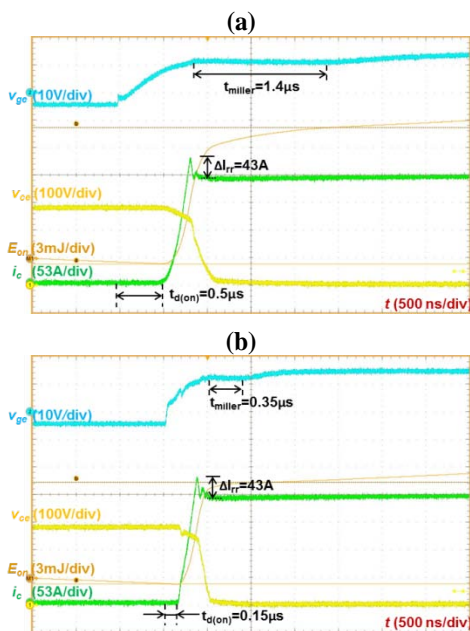


Figure II - 77: Comparison of turn-on waveforms for the two methods: (a) CGD and (b) proposed gate drive.

2. Turn-off Performance Improvement

The block diagram and circuit implementation of the AGD for turn-off performance improvement are shown in Figure II - 78 and Figure II - 79. Like the AGD for turn-on, it is also composed of four function blocks: di/dt sensing,

logic circuit, level shifter, and gate discharger. The functionality is similar except that the gate discharger is controlled to remove current from gate capacitance.

The experimental results with the same power module were obtained using the double pulse tester. A comparison of the turn-off switching waveforms at 300 V dc bus voltage and 200 A load current for the AGD and CGD is shown in Figure II - 80. The waveforms plotted from top to bottom are the gate voltage, collector current, turn-on energy loss, and collector emitter voltage. It can be seen that the proposed gate drive circuit reduces the turn-off delay time and the total switching time while keeping the same turn-off overvoltage (50 V) as that using the CGD. The Miller's plateau time for both is clearly visible. When the AGD is used, the Miller's plateau duration is significantly reduced: from 0.4 μ s for the CGD to 0.25 μ s for the AGD. The turn-off energy loss is also reduced: from 5.72 mJ when using the CGD to 4.48 mJ when using the AGD.

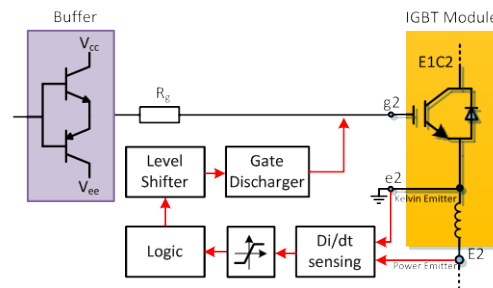


Figure II - 78: Block diagram of AGD (turn-off).

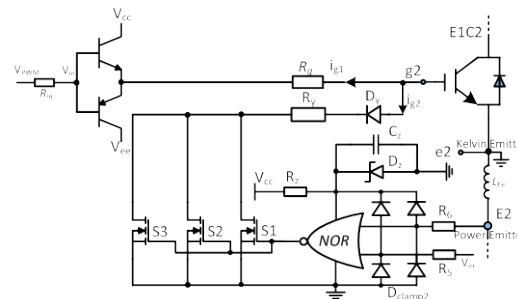


Figure II - 79: Circuit implementation of AGD (turn-off).

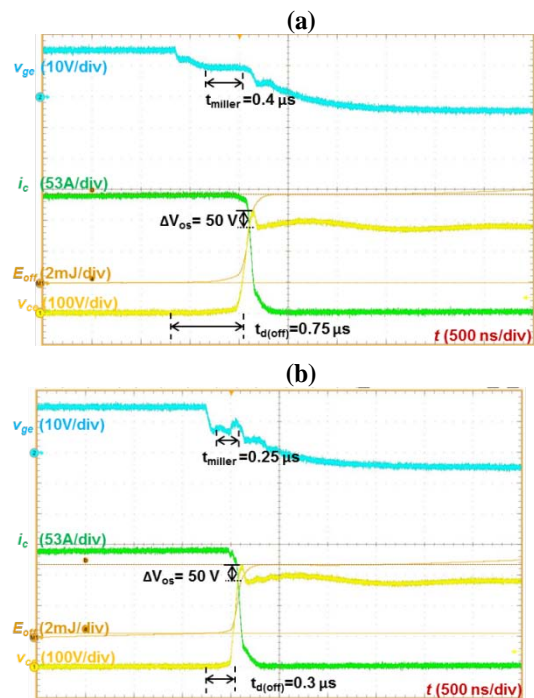


Figure II - 80: Comparison of turn-off waveforms for the two methods: (a) CGD and (b) proposed gate drive.

Cross Talk Mitigation

The WBG power devices have inherent capability for fast switching. However in the phase leg configuration, the interaction between two devices during the switching transient (cross talk) might increase the switching losses and reduce the reliability of the power devices and also limit the switching speed of the WBG devices [7]–[12].

Based on the intrinsic characteristics of WBG devices and the mechanism causing cross talk, a novel gate driver circuit to mitigate the cross talk without sacrificing the switching speed of the power device in the phase leg configuration has been proposed, as shown in Figure II - 81. In comparison with the traditional gate driver circuit, only one auxiliary transistor (S_{3_L} or S_{3_H}) and one capacitor ($C_{_L}$ or $C_{_H}$) is added between the gate to source terminals of each power device (S_L or S_H). During the switching transient of its corresponding power device (S_L or S_H), this auxiliary transistor (S_{3_L} or S_{3_H}) stays off to guarantee that there is no impact of this auxiliary transistor on the switching behavior of its corresponding power device (S_L or S_H). In addition, this auxiliary transistor (S_{3_L} or S_{3_H}) turns on during the switching transient of its complementary power device (S_H or S_L) to minimize the gate loop impedance of its corresponding power device (S_L or S_H) by means of a large auxiliary capacitor ($C_{_L}$ or $C_{_H}$). Therefore, the cross talk can be largely mitigated during both the turn-on and turn-off transients.

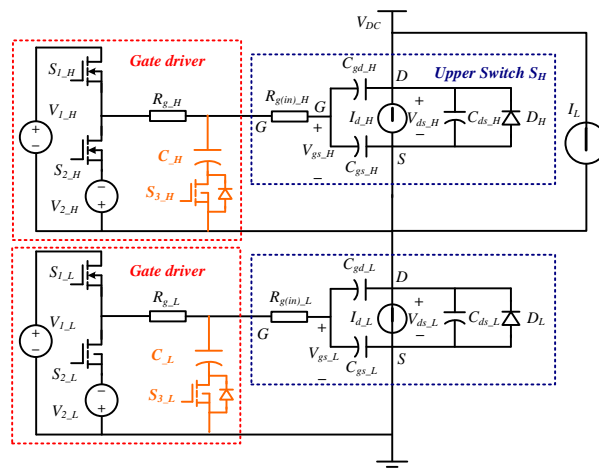


Figure II - 81: Novel gate driver circuit to mitigate cross talk in the phase leg configuration transistors.

Considering the fast switching capability of WBG devices, feed forward control was applied. Logic signals of auxiliary transistors can be easily synthesized based on the logic signals of the main power devices (S_L and S_H), as shown in Figure II - 82. According to the operation principle, the logic signals of auxiliary transistors are almost the same as those of their complementary main power devices except that the auxiliary transistors will remain on until the end of the turn-off transient of the complementary main power devices, as shown in Figure II - 82 (marked by shadow). Furthermore, only one power device in a phase leg and its gate signal will be effected, and it is the direction of load current that determines this affected power device. Accordingly, after monitoring the direction of load current, we can merely enable the auxiliary transistor of the affected power device and disable the other one so that the additional switching losses induced by auxiliary transistors can be reduced by one-half. Therefore, the six logic signals for the proposed gate driver circuit can be generated with the basis of control signals of power devices (S_L and S_H) from the microcontroller and the load current, as shown in Figure II - 83.

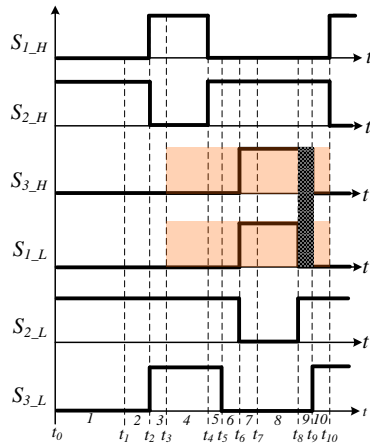


Figure II - 82: Logic signal for gate driver.

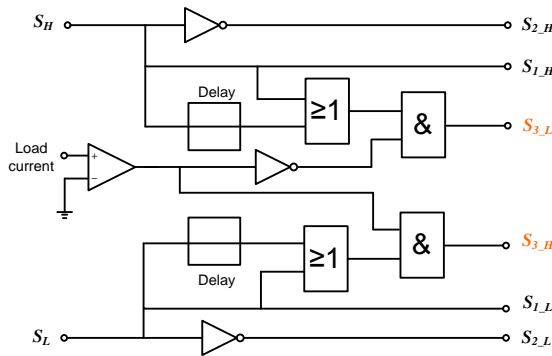


Figure II - 83: Logic signal generator.

A double pulse tester board with CMF20120D SiC MOSFETs was fabricated. Figure II - 84 displays the gate driver board with the proposed gate assist circuit, which consists of a Vishay Si7308DN silicon MOSFET with a 100 nF ceramic capacitor. To evaluate the effectiveness of the proposed gate assist circuit for cross talk mitigation, a group of comparison experiments to test the switching behavior of the main power devices with and without the gate assist circuit under the same operating conditions with gate voltage of 20/-2 V was conducted. Figure II - 85 shows the comparison waveforms under the operating condition of 800 V, 10 A with 10 Ω gate resistance. It shows that during the turn-on transient of the lower switch, the gate assist circuit does not reduce the switching speed and even improves the slew rate of drain-to-source voltage dv/dt from 23.1 V/ns to 24.7 V/ns. Additionally, turn-on energy loss of the lower switch $\Delta E_{on,L}$ and shoot-through energy loss of the upper switch $\Delta E_{on,H}$ are reduced by 36.7 μJ and 22.1 μJ, respectively, enabling a turn-on energy loss saving of about 16.4%. During the turn-off transient of the upper switch, by using the gate assist circuit, the spurious negative gate voltage of the lower switch is minimized from -8.94 V to -3.04 V, which is above -5 V, the maximum rating of negative gate voltage of the CMF20120D. More experimental data under four different cases, provided in Figure II - 86, indicate that the

proposed gate assist circuit can effectively mitigate cross talk and enhance switching performance.

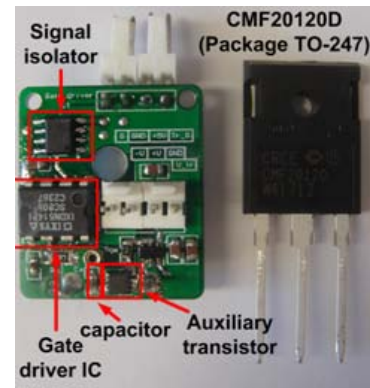


Figure II - 84: Gate driver board with proposed gate assist circuit.

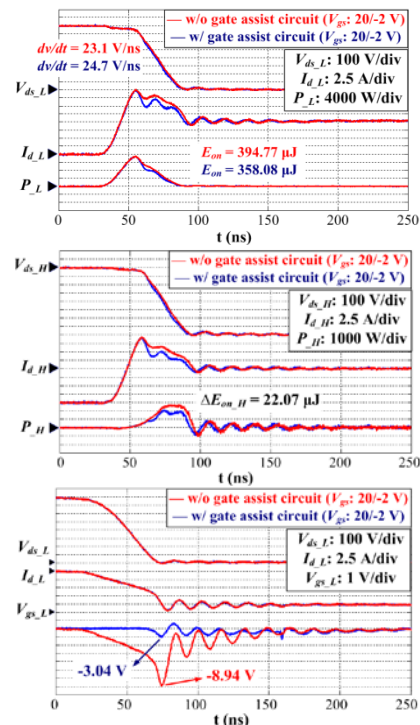


Figure II - 85: Lower and upper switch waveforms during turn-on transient of lower switch, and lower switch waveforms during turn-off transient of upper switch.

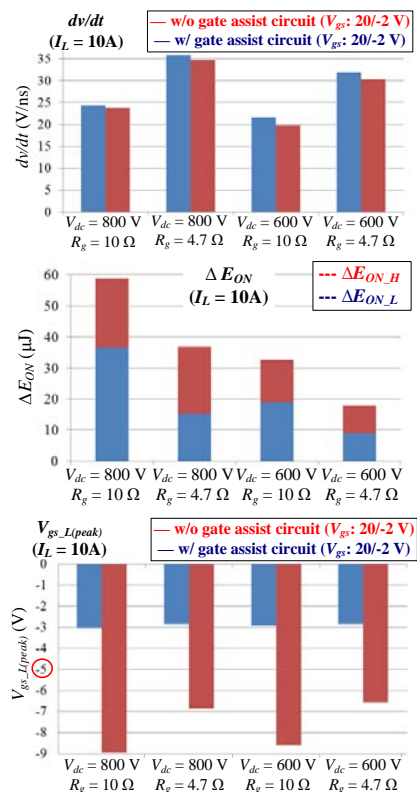


Figure II - 86: The proposed gate assist circuit improves dv/dt , reduces turn-on energy loss, and suppresses negative spurious gate voltage under four different cases.

Low-Cost Current Sensor

The Allegro A1324, which is supplied in a three-pin SOT23 package, was tested for measuring both dc and ac current waveforms. A long, flat strip of copper through which current is injected was fabricated on a printed circuit board. The trace width is about 3.6 mm, with the right side of the trace located 2.05 mm from the center of the Hall-effect device within the package. The Allegro A1324 device has a gain of about 5 mV/G. The output voltage of the device was measured for each ampere of current and converted to incident magnetic field.

The X-Fab Hall-effect sensor was also evaluated for its suitability for use as a current sensor; it is a proprietary standard cell primitive that is available in the XH018 CMOS process. No additional masks are required when it is used in combination with a double-diffused metal-oxide semiconductor module. The device exhibits a square-law behavior (much like a JFET) for current versus voltage, so maintaining a stable, well-controlled current to bias the device is important. A current source would satisfy this requirement. Additionally, the Hall device shows a significant temperature dependence such that the current decreases with increasing temperature, and the resistance temperature sensitivity is a higher order function of temperature. The bias circuitry and/or downstream

processing circuitry for the device will need to compensate for this behavior.

Conclusion

The results of high temperature reliability tests for the gate driver IC were positive, with the gate driver surviving both 200°C and 225°C tests. The COB approach removes the parasitics associated with the package and increases the accuracy of the measured drive current.

Multiple designs and prototypes for input isolation have been investigated. Both capacitive and transformer isolation prototypes demonstrated functionality. An on-chip solution for input isolation is the current focus for integration with the power module, which is currently being designed and simulated in a high temperature capable SOI technology.

Buffer circuits that can boost the output current from gate driver ICs were designed, analyzed, and optimized. Their performance was validated by experiments. All three proposed buffers performed better in terms of driving speed and cost less than a 30 A rated commercial buffer. The next step is to determine the best means to build a high temperature buffer.

A novel active gate drive circuit for silicon IGBTs was proposed and developed. The experimental results confirm that the proposed AGD has the capability of reducing the turn-on switching losses, delay time, and Miller plateau duration effectively during both turn-on and turn-off transients. Given that the auxiliary circuit only contains several small signal active devices and passive components, and does not require any independent isolated power supply, it is appropriate for chip integration.

According to the intrinsic characteristics of WBG power devices, a novel gate assist circuit has been proposed for cross talk mitigation in the phase leg configuration. The results of the double pulse tester with CMF20120D SiC MOSFETs verify that in comparison with the conventional gate drive, the proposed gate assist circuit improves the switching performance under different operating conditions. It offers a simple, efficient, and cost-effective solution for cross talk mitigation.

Patents

None.

Publications

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II.6 Air-Cooled Traction Drive Inverter

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Objectives

- Overall Objective
 - Demonstrate the feasibility of air cooling for power electronics thereby eliminating the existing liquid-cooled thermal management system while achieving the DOE Vehicle Technologies Program (VTP) 2015 power electronics power density target of 12 kW/L.
- FY 2012 Objectives
 - Simulate the selected air-cooled inverter architectures developed in FY 2010 through thermal and fluid simulations to predict the performance of the heat removal system.
 - Improve heat transfer design and evaluate the module thermal management system in collaboration with the National Renewable Energy Laboratory (NREL).
 - Complete module electrical design and finalize the air-cooled inverter design.

Approach

- Simulate the two air-cooled inverter concepts: Improve heat transfer design and evaluate the module's
- thermal management system in collaboration with NREL to down select an inverter design.
- Revise the models based on the balance of plant results from NREL: Continue to refine the thermal and fluid simulations on the selected inverter

architecture to study the performance of the heat removal system.

- Final design optimization: Finalize the inverter design and evaluate the system level impact of this technology.

Major Accomplishments

- Designed an air-cooled inverter using the inverter concepts developed in FY 2010.
- Developed a ductless design to eliminate the parasitic losses associated with ducts.
- Built a benchtop prototype module for evaluation of heat losses at different ambient temperatures.

Future Direction

FY 2013

- Refine the air-cooled inverter models developed in the FY 2012 NREL collaboration.
- Design high temperature modules and the gate driver.
- Build and test high temperature modules.
- Perform electrical parameter evaluation and control electronic design.
- Build and test a 10 kW prototype electrical module.
- Identify the technical challenges and finalize the design to build a 55 kW prototype.

FY 2014

- Build and test a 55kW full inverter system.

◇ ◇ ◇ ◇ ◇

Technical Discussion

This project builds on previous work performed in FY 2010. Parametric studies of two 55 kW peak power, 30 kW continuous power air-cooled inverter designs were conducted to determine their thermal performance and the boundary conditions of their components. The inverters were simulated over a range of parameters such as ambient conditions, inverter voltage, and switching frequencies.

For evaluating their relative performance, the same number of identical devices, same power curves, and same materials and material properties were used in both the designs. The parameters of the inverter designs were studied for steady state conditions and drive cycle conditions to show the difference in the parameters affecting the air-cooled inverter design. A total of 16 combinations of transient performance for the US06 Drive Cycle current distribution and up to 24 cases for steady

state were computed. The comparison of the two inverter designs is shown in Table 1. From Table 1 it can be seen that (1) the power density ratios for these air-cooled inverters are comparable to those of liquid-cooled systems, (2) both pressure drop and the blower power requirements are lower for the lower flow rate and they increase as the square of the flow rate, and (3) the values for the axial inverter are about 3 times those of the rectangular inverter design.

Table II - 5: Comparison of the performance of the two inverter design packages.

	Rectangular	Axial
Power density (kW/L)	12.01	12.4
Pressure drop (in.H ₂ O) @ 30 ft ³ /min	0.436	1.3
Pressure drop (in.H ₂ O) @ 60 ft ³ /min	1.64	5.0
Ideal blower power (W) @ 30 ft ³ /min	13.9	40.3
Ideal blower power (W) @ 60 ft ³ /min	104.5	312

Design Improvements

1. Mechanical Design

A new module was designed combining the two module concepts developed in FY 2010. The previous module design and the new module designs are shown in Figure II - 87–Figure II - 90. The heat sink was redesigned to improve the heat transfer coefficient of the module with the result that the new module has more surface area on the heat sink with the same volume as the old module. A significant change in the inverter design necessitated a change in the module design: the new module has all the power and gate drive traces routed to one end of the module. This change was made to make the module modular and also to make it a plug and play unit in the bus structure. This module additionally eliminates the use of the plastic housing; its all-metal housing will enable higher temperature operation of the inverter.

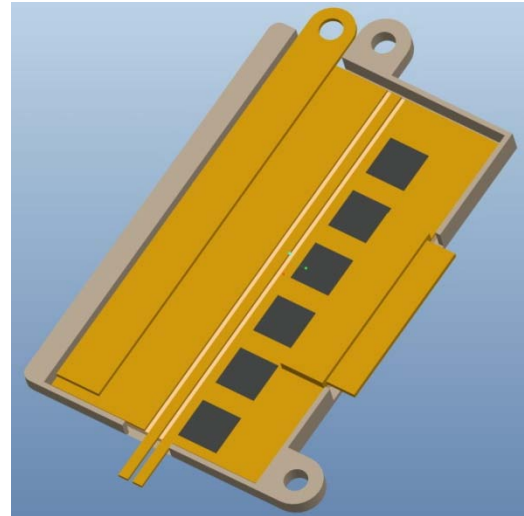


Figure II - 88: Cutaway of the old module design.

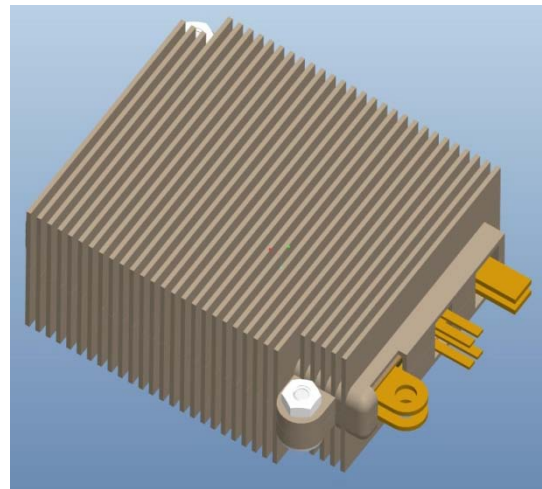


Figure II - 89: Full view of the new module design.

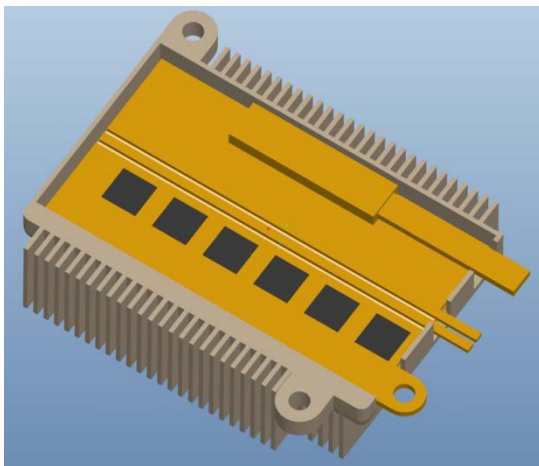


Figure II - 87: Cross section of the new module design.

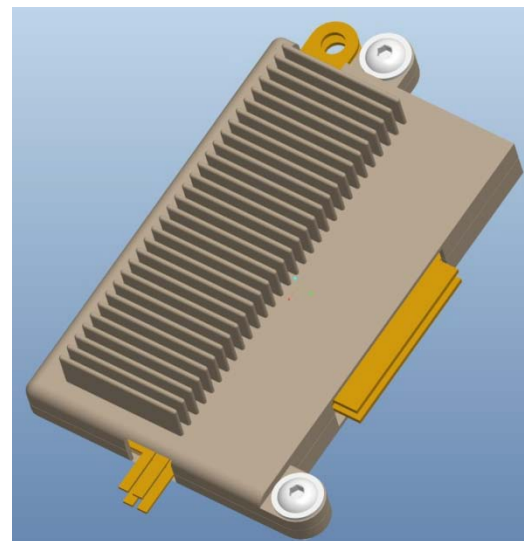


Figure II - 90: Full view of the new module design.

The full inverter package and the cutaway view of the entire inverter are shown in Figure II - 91 and Figure II - 92. The rectangular shape of the inverter was chosen because of the blower power requirements. The dc bus capacitor, bus structure, gate driver, and control boards with current sensors are placed in the metal housing. The modules are designed to be inserted into the bus structure and sealed around the module and the metal housing interface. The new module design enables the entire inverter to be sealed against moisture. The inverter volume is calculated to be 184.07 in.³ (8.65 in. × 5.5 in. × 3.8 in.).

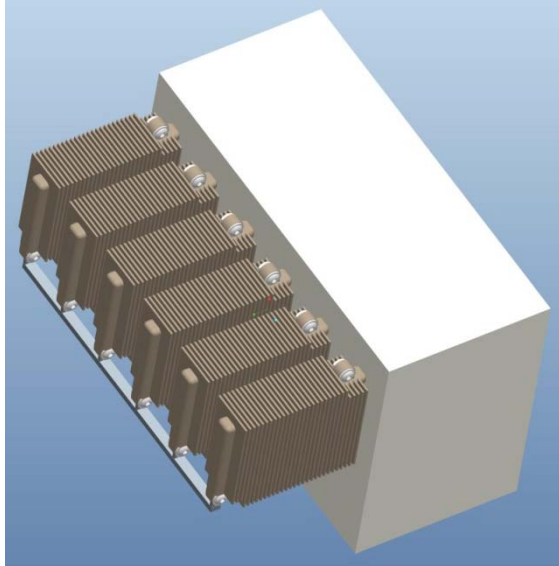


Figure II - 91: Full view of the entire inverter.

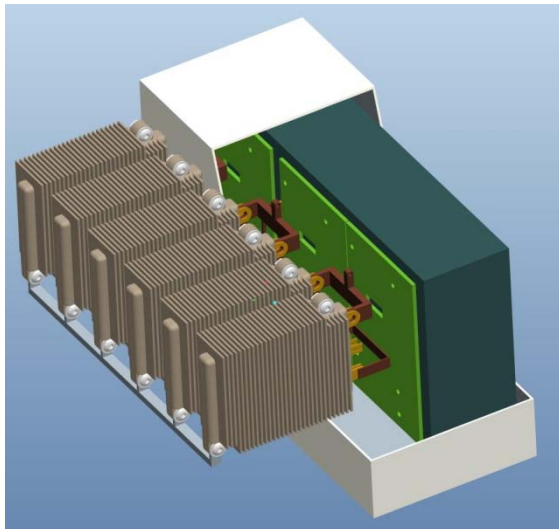


Figure II - 92: Cutaway view of the entire inverter.

2. Electrical Design

The current required for a 60 kW inverter is calculated to be about 220 A peak per phase, assuming the battery voltage to be 250 Vdc with a square wave mode of operation and the power factor (PF) of 0.6. This operating condition represents the worst case scenario peak power, through the inverter, driving a motor. The rectangular inverter was redesigned with new 1,200 V, 100 A SiC devices (63 A devices were used in the designs in FY 2010), and the new devices allow for several design improvements. The number of modules for the previous design was three per phase with 6 devices per module to accommodate the 210 A per phase ratings with 18 devices in total. With the higher rated new devices, the number of modules can be reduced to possibly two, with 6 devices per module for a total of 12 including the diodes. The lower losses in the new devices can also help to minimize the flow rate thereby reducing the total blower power required to cool the entire inverter. Moreover, the new devices enable lower inductance per module because of the reduction in number of devices per module.

The power loss of the new 100 A devices is shown in Figure II - 93 and Figure II - 94. The loss per device is calculated as a function of the power factor, operating voltage, peak current through each device ($210/6 = \sim 32$ A per switch), switching frequency, and modulation index. It can be clearly seen that for $M = 1$ the maximum loss, for a 175°C maximum junction temperature design, is roughly 30 W. The loss through the diode for $M = 1$ is about 14 W (Figure II - 95). The total loss per module is roughly 132 W. This number sets the design specifications for the heat removal system for the entire inverter for an operating junction temperature of 175°C maximum. The total loss for the inverter is simply 6 times the loss per module, which is about 800 W. It should be noted that for different power factors and values of M the losses would vary between the metal-oxide semiconductor field-effect transistors (MOSFETs) and diodes.

Device losses have been reduced by at least 30% from the device losses that were measured in FY 2010. Therefore, for the same operating conditions, the overall heat dissipation will be at least 30% lower. This difference in losses can be used to optimize the design in several ways. One way is to reduce the blower power required for the entire inverter. The other is to reduce the number of devices to handle the same power, thereby minimizing the cost of the semiconductor of choice. In general, tradeoffs in design will be weighed against the critical factors important in achieving targets.

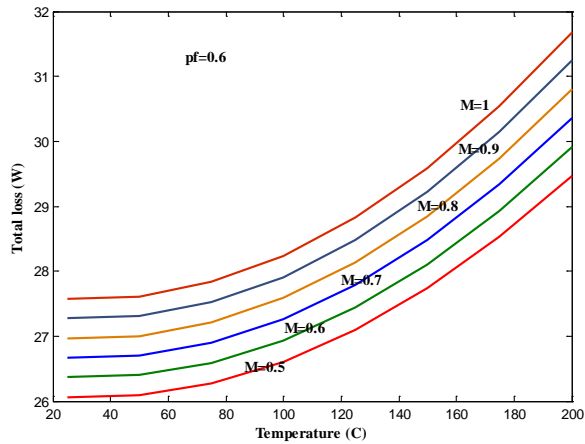


Figure II - 93: Loss per 1,200 V, 100 A SiC MOSFET at 250 Vdc, 32 A, 10 kHz, and PF = 0.6.

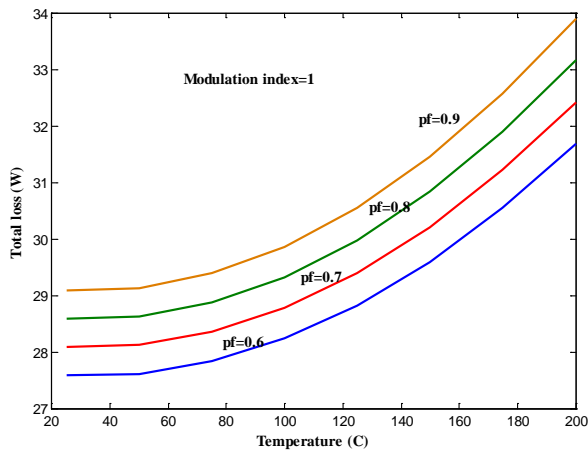


Figure II - 94: Loss per 1,200 V, 100 A SiC MOSFET at 250 Vdc, 32 A, 10 kHz, and M = 1.

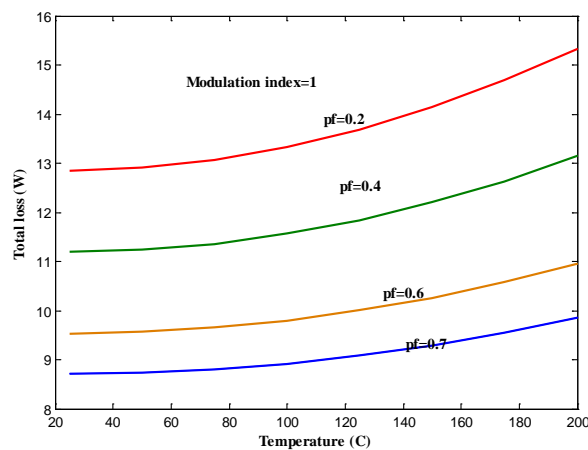


Figure II - 95: Loss per 1,200 V, 100 A SiC diode at 250 Vdc, 32 A, 10 kHz, and M = 1.

3. Electrical Parameter Analysis

The module was analyzed for electrical characteristics to identify the benefits of the module at the system level. This analysis was performed with the previous module design; however, the parasitic parameters will be very close to those for the new module (Figure II - 96). Each device in the design has two ribbon bonds instead of wire bonds. The parametric sweep was performed using Ansys Q3D software. A plot of the meshing is shown in Figure II - 97. The resistance and inductance of the module over a frequency range is shown in Figure II - 98 and Figure II - 99. The maximum inductance value is about 8 nH at 10 kHz per half of the module. The total will be at least 17 nH per module. The resistance is 200 $\mu\Omega$ for half of the module, and the total will be at least 400 $\mu\Omega$. The inductance value is much less than that for a 2010 Toyota Prius module, which is around 25.1 nH. The low parasitic inductance is very important for the fast switching wide bandgap devices so that the losses induced by these parameters will be less.

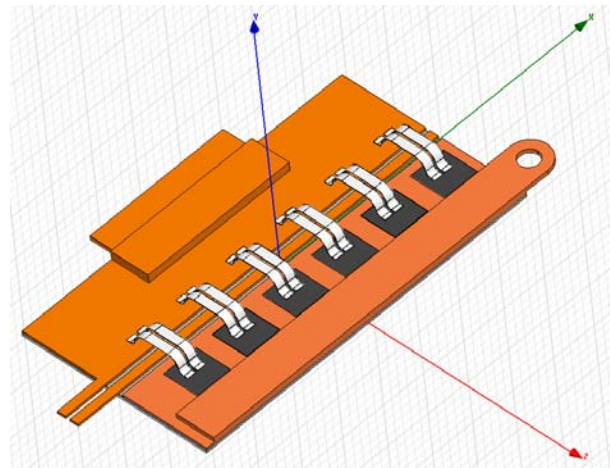


Figure II - 96: Half module with six devices without the module casing.

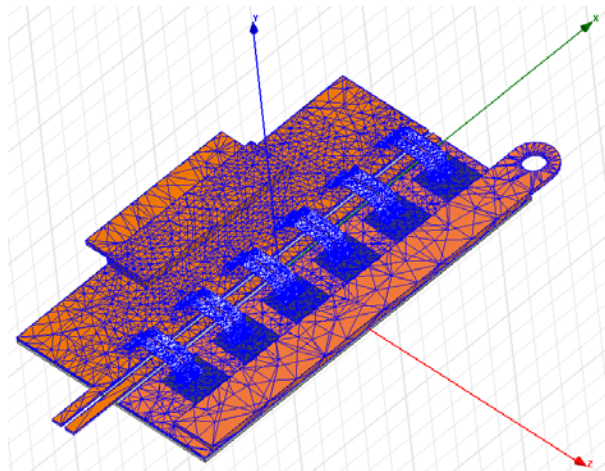


Figure II - 97: Q3D mesh plot of the half module with six devices.

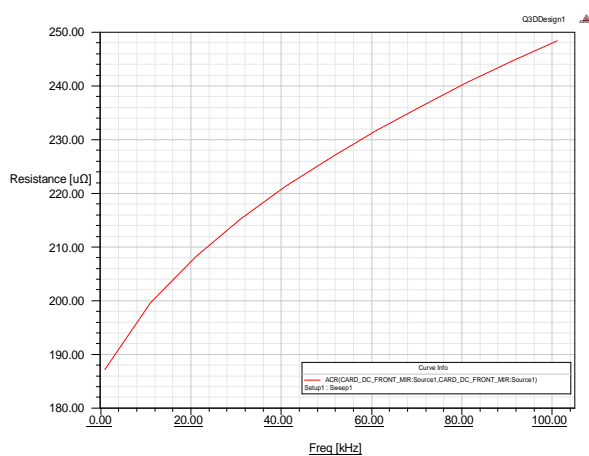


Figure II - 98: Plot of resistance of the half module over a frequency range of 0–100 kHz.

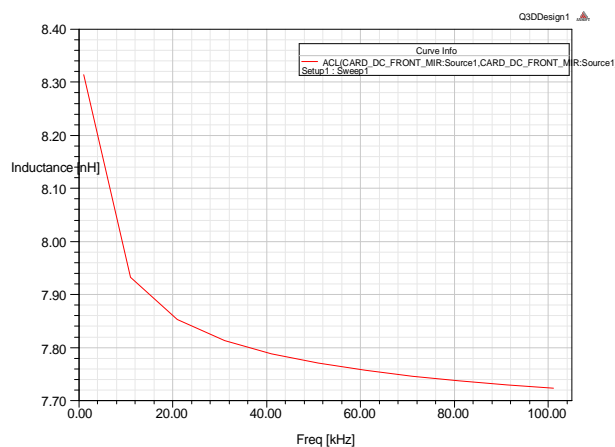


Figure II - 99: Plot of inductance of the half module over a frequency range of 0–100 kHz.

Prototype Module

1. Design and Fabrication

A quick benchtop prototype was built to determine performance of the innovative air-cooled heat sink technology and validate the modeling results. The test procedure was to set up a variable heat generation source for the heat sink, instrument the heat load and the heat sink, and assemble this into a fixture to test the heat sink with various heat loads under controlled air flow and air temperature.

First, a set of five TO-247 insulated gate bipolar transistors (IGBTs; P/N APT30GN60BC) were soldered side by side onto a direct bonded copper substrate. Next, the collectors, gates, and emitters of each of the five devices were connected in parallel as shown in Figure II - 99. After that, the card was attached to the heat sink with thermal grease, and both the heat sink and load were instrumented. Then the entire module was placed into a fixture designed to do two things: (1) keep 8.6 lb of pressure on each IGBT to ensure good connection to the heat sink and (2) allow controlled air to be forced through the heat sink fins without interfering with the heat load compartment of the heat sink, shown in Figure II - 100 and Figure II - 101. The air outlet of the module has a 6 in. long section divided into four 1 in. by 1 in. squares intended for air straightening and one hole per quadrant large enough for a hot-wire anemometer to be used to measure the velocity near the exit of the duct. Finally, two separate types of tests were performed. The first was to hold the junction of the IGBT constant at various flows and record the wattage required to reach the desired junction temperature, and the second was to keep the wattage constant over various flows and record the resulting junction temperature. The equipment used is shown in Figure II - 102 and Figure II - 103, and the general test setup is shown in Figure II - 104.

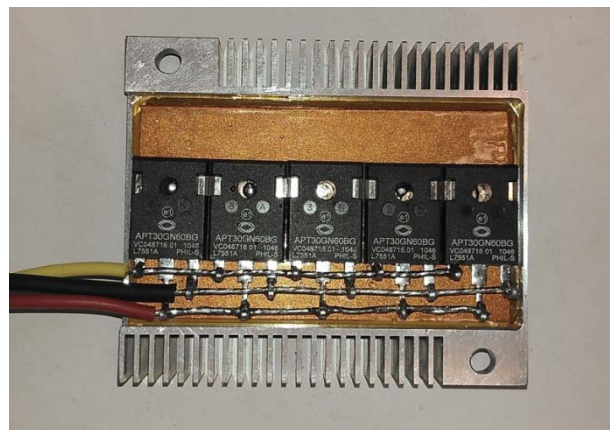


Figure II - 100: Variable heat load in new air-cooled heat sink topology.

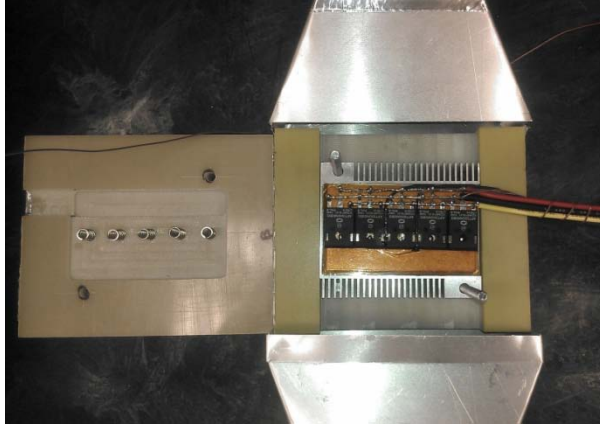


Figure II - 101: Inside of test fixture.

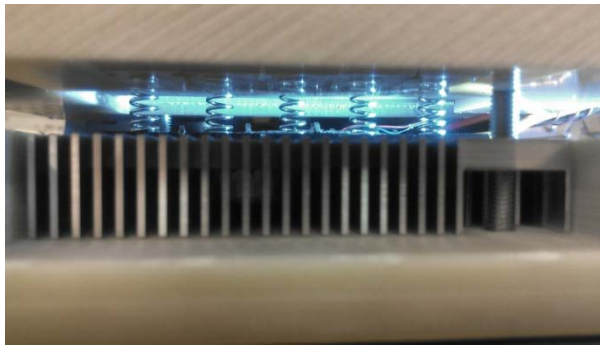


Figure II - 102: Assembly of test fixture.



Figure II - 103: Temperature measurement devices and assembled test fixture.



Figure II - 104: General test setup; Tempronic X-stream 4310 air temperature and flow control (on right).

2. Testing

2.1 Constant power tests at fixed air temperature

The heat sink was tested with a constant air temperature forced through it from the Tempronic 4310 X-stream. The first test run was at 25°C and constant wattages of 50 W, 75 W, and 100 W. Before each set of data was taken the flow from the 4310 was allowed to stabilize and was measured to verify it was close to the desired flow. A small Tenma power supply was used to supply voltage to the gate of the IGBTs. Lowering the gate voltage to the devices increases the resistance of the devices, allowing a larger amount of power to be lost through the devices with lower currents; this was adjusted to optimize the power requirements for the test. A Xantrex power supply was then used to apply the power to the devices and adjusted until it was stable at 50 W, 75 W, and 100 W. The voltage, current, and various temperatures, including inlet, outlet, device, base of the fin, and outside edge of the fin, were all recorded.

2.2 Constant junction temperature tests at fixed air temperature

The heat sink was tested with a constant air temperature forced through it from the Tempronic 4310 X-stream. The first test run was at 50°C, and the junction was brought up to constant temperatures of 100°C, 125°C, and 150°C. Before each set of data was taken the flow from the 4310 was allowed to stabilize and was measured to verify that it was close to the desired flow, and after each data point the flow was measured again. The flow rates were typically within 10% of one another. A small Tenma power supply was used to supply voltage to the gate of the IGBTs. Lowering the gate voltage to the devices increases the resistance of the devices, allowing a larger amount of power to be lost through the devices with lower currents; this was adjusted to optimize the power requirements for the test. A Xantrex power supply was then used to apply the power to the devices and adjusted

until it was stable at 100°C, 125°C, and 150°C. The voltage, current, and various temperatures, including inlet, outlet, device, base of the fin, and outside edge of the fin, were all recorded.

2.3 Test conclusions

Several challenges were encountered during the tests, and the setup was redesigned to overcome them. The challenges were primarily related to measurement of airflow through the module and measurement of inlet and outlet air temperatures. Additional testing will be performed in FY 2013 with the SiC MOSFET and diode module to further validate the heat sink.

Conclusion

A new air-cooled inverter was designed using the features of the axial and the rectangular inverter designs developed in FY 2010. The module was redesigned to improve the heat transfer, and plug and play capability was added to enable a modular inverter configuration. The new design enables the entire inverter to be placed in a metal housing and the design sealed against moisture, which is an important feature for automotive use. The electrical design was improved using higher rated devices, which enabled a reduction in number of modules for the entire inverter.

Patents

None.

Publications

1. M. Chinthavali, J. F. Christopher, and R. V. Arimilli, "Feasibility study of a 55-kW air-cooled automotive inverter," Applied Power Electronics Conference and Exposition (APEC), Orlando, Florida, February 2012.
2. M. Chinthavali, J. A. Tawfik, and R. V. Arimilli, "Design and analysis of a 55-kW air-cooled automotive traction drive inverter," IEEE Energy Conversion Congress and Exposition, Phoenix, Arizona, September 2011.

References

None.

II.7 Development, Test and Demonstration of a Cost-Effective, Compact, Light-Weight, and Scalable High Temperature Inverter for HEVs, PHEVs, and FCVs

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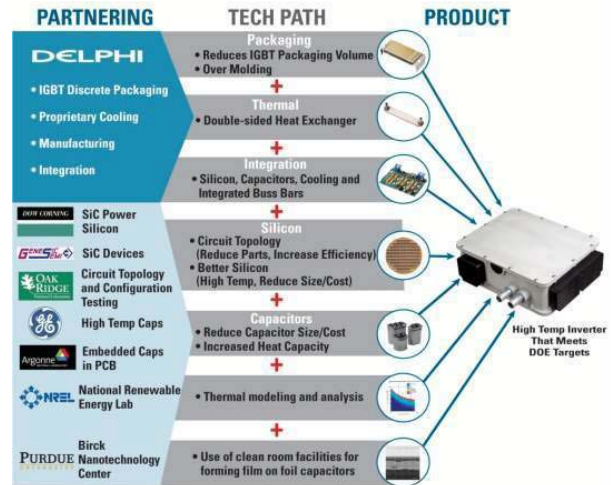
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Objectives

- Design, procure components, build and test high-temperature inverter
 - Design the previously selected inverter concept, perform component and subsystem development to optimize the inverter system, procure components, build and test the inverter. Identify with the U.S. Department of Energy (DOE) an appropriate motor/generator transaxle for testing and test inverter for compliance with DOE performance and cost objectives. Develop manufacturing study from selected design concepts and determine viability to reach the DOE cost and scalability objectives.

Approach

Work with our partners to develop the technologies required for DC bus capacitors, power silicon, packaging, thermal management and overall inverter system integration.



Major Accomplishments: Film Capacitors (GE)

- Formed a team comprised of Delphi, GE, SABIC, Dearborn Electronics, and GE's film metallizers, to investigate why the GE PEI capacitors were failing.
- A primary concern was areas of high resistance found on the failed capacitors, which had the appearance of "scratches."
- A Design of Experiments (DoE) was set in place to find and implement a corrective action to be able to manufacture the PEI capacitors needed for the inverter.
- After the DoE was completed, another set of experiments was performed on the capacitors made during the DoE. The experiment included the following:
 - Subject capacitors to 100V, 200V, and 400V DC (all at room temperature)
 - Age capacitors at 140°C for 24 hours (PEI caps only)
 - Subject capacitors to 600V at 130°C (PEI caps only)
 - Measure insulation resistance (IR)
 - Measure the capacitance and dissipation factor (Df) before and after testing at each voltage
- Root cause was determined and a corrective action implemented

- Based on the lessons learned from the investigations, more film has been extruded, metalized and formed into ~17 μF capacitors to be used to construct the DC-link capacitor.
 - Two different metallizations were implemented: 10 Ω and 20 Ω
 - Yield after testing of the 10 Ω parts was 93%
 - Yield after testing of the 20 Ω parts was 100%

	Capacitance after <u>Lead Attach</u>	Df after <u>Lead Attach</u>
Mean	16.84	0.183
Min.	16.63	0.166
Max.	17.10	0.208
Standard Deviation	0.10	0.009

- Test results for all four lots were similar

Future Direction

- Combine the ~17 μF 10 Ω and 20 Ω capacitor modules in blocks of 12 capacitors and test
- Combine the tested blocks into groups of 4 and test
- Package the groups of 4 blocks into DC-link capacitors (of 48 capacitor modules each)
- Deliver the DC-link capacitors to Delphi for integration with Delphi's DOE inverter



Major Accomplishments: Film-on-Foil Capacitors (Argonne National Laboratory)

- After continued work with a solution-based PLZT chemistry, it was agreed to focus on ways to form PLZT such that a single-step deposition process of PLZT could be used, to lower process cost.
 - Previous process was a CSD process
- Argonne is developing a GN process to form sub-micron PLZT particles.
 - Argonne has demonstrated its GN process can form sub-micron PLZT particles.
 - The resulting sub-micron particles have the same crystal structure as the bulk material.

Technical Discussion

The graph in Figure II - 105 summarizes the potential capability of different dielectric resins compared to today's baseline biaxially-oriented polypropylene (BOPP) film capacitors.

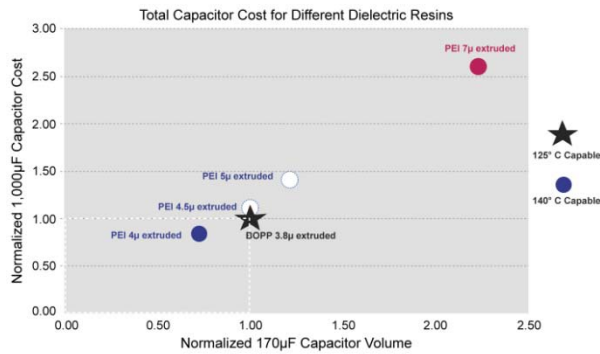


Figure II - 105: Capacitor Volume vs. Cost.

For this graphical comparison, the *processing cost per unit volume of capacitor module was kept constant*, the same as that for the BOPP, although it may be different for resins other than BOPP, especially in those cases where either the raw material cost or the processing cost to make the film by extrusion, or both, are substantially higher than the values assumed for BOPP.

PEI Capacitor Test Results

- Test results for one lot of the four lots in total, with approximately 75 caps per lot

Future Direction

- Current efforts are focused on producing a PLZT film using the sub-micron particles, to understand and document the sub-micron PLZT material properties as a film.
- Provide to Delphi sub-micron PLZT powders, with added dispersants, for evaluating different deposition processes for creating PLZT film-on-foil capacitors.

Technical Discussion

Argonne has demonstrated forming the sub-micron PLZT particles. (Figure II - 106).

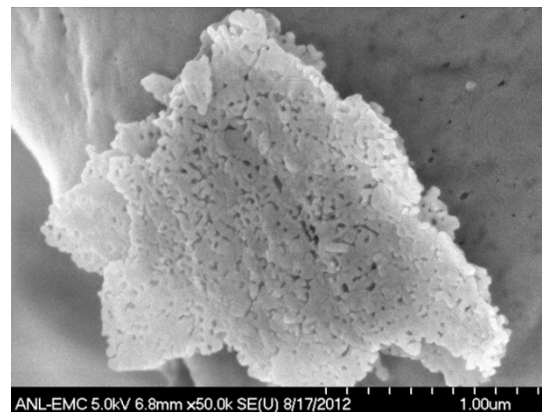


Figure II - 106: EM Picture shows the "flakey" nature of the PLZT powder agglomerates and the primary particles within the agglomerates.

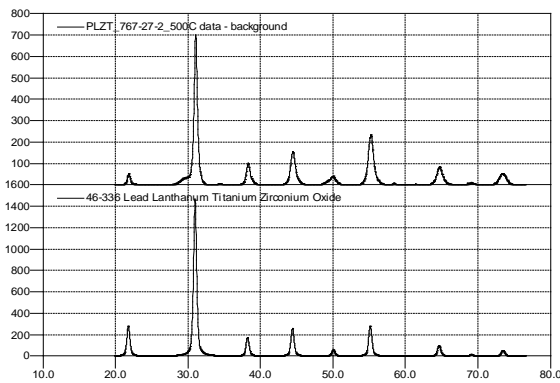


Figure II - 107: Argonne has also demonstrated that the sub-micron PLZT particles have the same crystal structure as the bulk PLZT material.

Major Accomplishments: 3C-SiC/Si (Dow Corning)

The Silicon-Carbide (SiC)-on-Silicon wafer growth work was ended for the program when it was determined that it would exceed the allotted timeframe to obtain the precursor material appropriately reformulated to eliminate the excessive background nitrogen doping in the SiC epitaxy.

Future Direction

Dow Corning continues work beyond this project to improve doping control and demonstrate 150mm 3C-SiC/Si wafers, including reformulation of their precursor material to eliminate the N_2 contamination.

Major Accomplishments: Thermal Modeling, Experiments and Analysis (National Renewable Energy Laboratory)

- Provided guidance/consultation on atomic scale calculations of thermal interface resistance between different materials.
- Provided guidance on test protocol for jet impingement cooling of Delphi's power switch packages and determination of long-term reliability of DBA/DBC, based on aluminum nitride substrates subjected to impingement cooling. Also provided the substrates to NREL.
- Provided guidance and Delphi's power switch packages for evaluation of two-phase thermosyphon cooling.
- Delphi provided samples of bonded Si substrates to NREL for evaluation of their ability to use the transient thermoreflectance technique to measure the thermal resistance of the bonded interface.

Future Direction

- Provided guidance for possible future projects of relevance to Delphi.
- Demonstrate measurements of interface thermal resistance using the transient thermoreflectance technique.

Major Accomplishments: Modeling and Test (Oak Ridge National Laboratory)

- ORNL's work on this project is basically complete until GE is able to deliver a working high-temperature PEI bulk capacitor later this year and Delphi is able to integrate the PEI bulk capacitor into its DOE inverter.
 - ORNL will perform additional confirmation testing for the inverter system on DOE's behalf, using Delphi's facilities, at the targeted higher ambient temperature (140°C) with 105°C coolant.
- Delphi delivered to DOE (via ORNL) the completed low-temperature test results for the high-temperature inverter.
 - Test results were based on an ORNL/Delphi test plan.
 - Delphi and ORNL reviewed the test results.

Future Direction

- When the high-temperature PEI capacitor is integrated and functioning in Delphi's DOE high-temperature inverter, ORNL will be invited to perform additional confirmation testing for the inverter system on DOE's behalf, using Delphi's facilities, at the targeted higher ambient temperature (140°C) with 105°C coolant, using the motor supplied by Delphi at Delphi's Corporate Technology Center (CTC) in Kokomo, Indiana.

Major Accomplishments: Packaging Thermal and Integration (Delphi)

- This year, the focus of our work was to understand and fix the problems associated with the GE PEI capacitor and then to build a PEI capacitor so high-temperature testing of our inverter could be completed.
 - Delphi anticipates its inverter testing to start in late-December 2012.
- Argonne has shown that the current glycine-nitride (GN) solution-based PLZT chemistry can be used to form sub-micron PLZT particles.
 - The chemical solution deposition (CSD) process has many deposition and recrystallization steps and, therefore, is not practical

- The GN solution-based sub-micron PLZT particles enables opportunities for other potentially lower-cost deposition processes enabling low-cost capacitor formation
- Sub-micron particle-based chemistries may allow aerosol, ink-jet, electrostatic or other deposition processes to be used to form capacitors with only a few simple process steps (enabling low cost). These processes are currently being investigated.
- Production costing for the inverter has been completed assuming 100,000 units per year.

Future Direction

- Resume our build and test of the high-temperature inverter, upon receiving high-temperature PEI capacitor from GE. A tested PEI DC-link capacitor should be available by mid-December.
- Integrate PEI capacitor into our high-temperature inverter and verify operation.
 - Complete inverter testing with 105°C coolant and 140°C ambient air and deliver the test results to DOE/ORNL.
 - Expect ORNL to verify inverter tests.
- Continue working with Argonne to define a deposition process to form capacitors using Argonne's sub-micron PLZT particles.
 - Evaluating with vs. without recrystallization (low temperature vs. high temperature)
 - Wound vs. stacked
 - Aerosol, ink jet, electrostatic and other deposition processes are being evaluated.
 - Focus is on defining the lowest-cost process
 - Work with our health and safety organization to determine safe practices for the deposition of sub-micron particles
 - Work with Argonne to determine dispersants (solution chemistries) to evaluate various deposition processes
 - Focus efforts on producing films to understand sub-micron PLZT material properties, such as:
 - Dk vs. temperature, frequency and voltage bias
 - Breakdown voltage
 - Stress strain of the PLZT on foil
 - Which foil: polymer for low-temperature process; metal for high-temperature process (requires recrystallization)?
 - Is recrystallization necessary?
 - Is patterning of the film required?
 - What surface roughness is required for the base substrate?

- Are there material phase changes during deposition?

- Complete final report

Technical Discussion

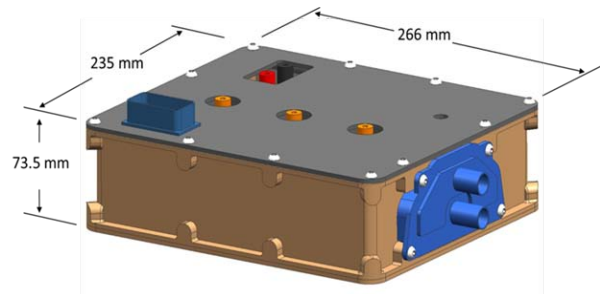


Figure II - 108: Delphi's DOE PEEM Inverter.

Conclusions

- Power device packaging provides at least 30% improvement in thermal resistance junction-to-coolant, compared to the “best” commercially available double-side cooled product today
- Advanced silicon devices provide conduction losses that are ~17% lower than target; total loss improvements are currently under characterization
- This project is developing a technical path to smaller, lower-cost, high-temperature bulk capacitors.
- Lower thermal resistance packaging will lower device losses and, thereby, enable use of less silicon
- Less silicon enables less silicon packaging
- Less silicon, less silicon packaging, smaller bulk capacitor together enable smaller inverter overall
- Overall, this project is resulting in smaller, lighter, easier-to-manufacture, lower-cost inverters, as well as higher temperature capability that could potentially also reduce the inverter's coolant system complexity, size/weight and associated cost.
- Scalable: capable of operating over a wide range of applications
 - Capable of 80A to > 460 A/phase output
 - Parts delete and part substitution, Si size, heat sink materials and design, component temperature ratings

Publications

1. G. A. Cameron, M. B. Hayes, H. S. Lee, and R. S. Taylor, *New Developments in Power Electronics*, EVS26, May 2012.
2. R. M. Fairchild, C. W. Berlin, D. H. R. Sarma, and R. S. Taylor, *Thin-film High Voltage Capacitors for*

Hybrid Electric Vehicle Inverter Applications,
IMAPS, September 13, 2012.

- These concepts will be used on future production inverter programs.

Patents

1. U.S. Patent No. 8,208,239 issued on June 26, 2012;
Contact Method To Allow Benign Failure in Ceramic
Capacitor Having Self Clearing Feature (Myers,
Taylor)

Thank you DOE for the opportunity...

- To work with GE Global Research on high-temperature film capacitors
 - This work has demonstrated a path to lower-cost and smaller/higher energy-density film capacitors for EDV inverters.
- To work with Dow Corning Compound Semiconductors
 - This work has resulted in the best performance to date for a 3C-SiC on Silicon film for use in potential future packaged power devices.
- To work with Oak Ridge National Laboratory on models to compare Si vs. SiC power devices
 - This work has enabled better trade-offs to optimize component cost vs. system cost and system efficiency for future commercial programs.
- To work with Argonne National Laboratory on film-on-foil capacitors
 - This work on the material has shown strong promise for developing a very compact (80%+ smaller), high-temperature and potentially substantially lower-cost capacitor (50%+ lower cost).
 - Future efforts to develop a process to convert the base PLZT material into capacitors could be a “game-changer” for the capacitor industry.
- To work with the National Renewable Energy Laboratory on thermal packaging and integration
 - This work has provided important insights that could be applied on future commercial programs.
- To work with our suppliers on advanced silicon devices
 - These state-of-the art devices are already being integrated in our product development programs for commercial production.
- To allow us to explore packaging concepts for inverter components, as well as the overall inverter system

II.8 Next Generation Inverter

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Objectives

- Develop the technologies and the engineering product design for a low cost highly efficient next generation power inverter capable of 55kW peak/30kW continuous power.
- The Inverter is to improve the cost of the power electronics to \$3.30/kW produced in quantities of 100,000 units, and the power density to 13.4kW/l, and a specific power of 14.1kW/kg to meet the DOE 2020 goals

Approach

- Engage with Tier 1, 2, and 3 suppliers along with National Labs to co-develop technology that reduces cost and increase efficiency, without increasing volume or mass.
- Ensure modularity and scalability of inverter to meet all vehicle applications.
 - Packaging
 - Consistent electrical characteristics and mechanical
 - Has to provide adequate cooling for the capacitor
 - Has to have low inductance
 - Has to adhere to global manufacturing processes

Major Accomplishments

- Requirements: evaluated HEV, EREV, and EV applications; completed specifications, and determined key feature constraints for modularity to enable scalability.
- Power module evaluation: acquired samples of conventional, encapsulated, and transfer molded; developed test plan; completed testing of transfer molded and one of two conventional modules.

- Capacitor: initiated traditional and individual bobbin designs and developed test plan.
- Gate drive and controller: worked with suppliers defining integrated chips; new chips acquired; test boards fabricated and testing initiated.
- Inverter: developed conceptual design and assessed

Future Direction

- Complete technology assessment and production cost assessment
- Design concept
- Detailed design
- Fabricate, assemble, and test inverter



Technical Discussion

The goal of this Cooperative Agreement is the development a Next Generation Inverter. The key goal is to reduce the production cost of a traction drive inverter while still making improvements in mass, volume, and reliability/durability. Traction inverter cost is a key barrier to economic viability of electric traction drives. This program is divided into four budget periods: technology assessment, technology development, technology build, and non-destructive confirmatory testing. The technology assessment phase includes the investigation through experimentation and evaluation of all key elements of the inverter. Technology development includes the concept and breadboard, and a final detailed design of the inverter. Technology build includes the procurement, fabrication of components, and the assembly of the inverter. Non-Destructive confirmatory testing includes environmental test setup, electrical verification, temp/vibe characterization and margining, and test support at national lab. The National Energy Technology Laboratory (NETL) awarded GM a Cooperative Agreement in September 2010. This report details work performed and progress under this program from October 1, 2011 through September 30, 2012. Progress under the program is as expected with some minor parts delays, but manageable within the Project Plan. This project is broken into seven major technical tasks.

Power Inverter Requirements

The development of proper specification for the inverter require vehicle and electric traction system be done in conjunction (Figure II - 109). A specification has been developed considering future vehicle needs for

HEV's, EREV's, and EV's. Investigation into a better understanding of temperature, current, and voltage during

operating points and their variability is being performed. This will lead to further refinement of the specification.

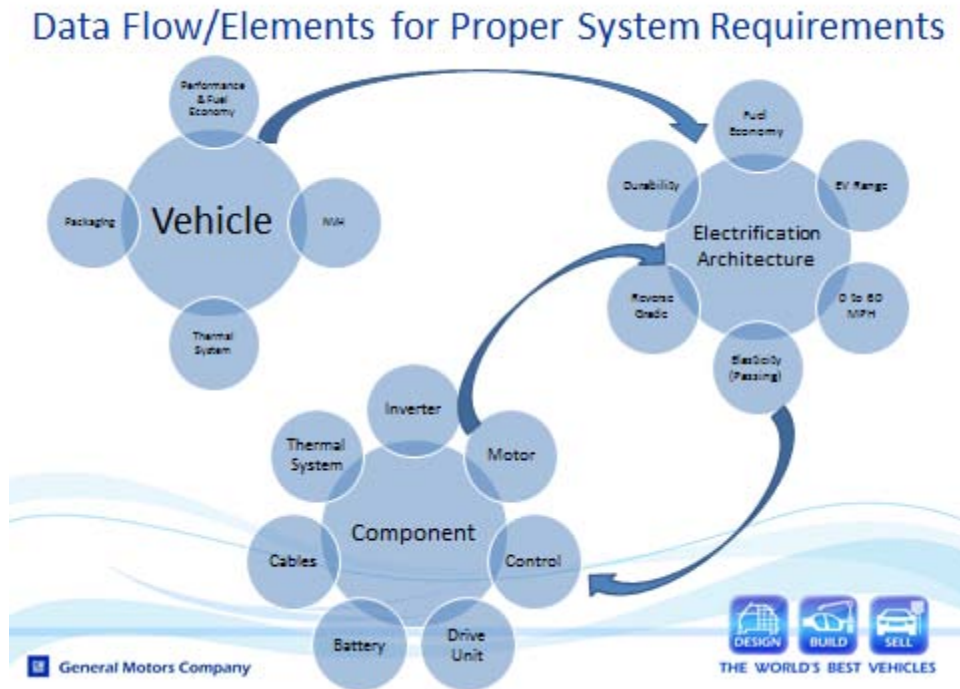


Figure II - 109: Data Flow/Elements for Proper System Requirements.

Inverter Evaluation and Assessment

Three technologies for the inverter power module are being considered: Conventional (Figure II - 110), Transfer Molded (Figure II - 111), and Encapsulated (Figure II - 112). Strengths and weaknesses are being determined for each in the area of packaging, durability, and reliability and how each fits future vehicle applications. Conventional and Transfer Molded parts are now under test. Test results have been provided back to suppliers and improvements made to the modules. Studies are being done for modularity and scalability for each technology. A math model has been produced using conventional module technology.

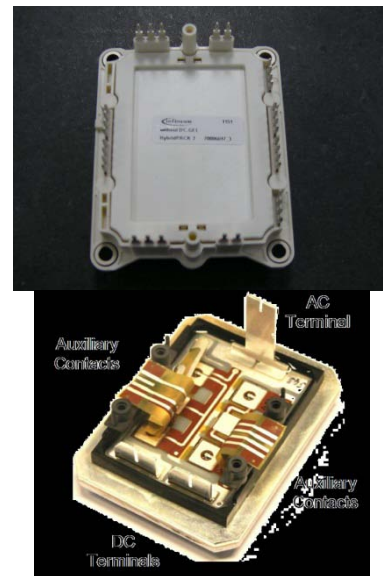


Figure II - 110: Conventional Based Modules.



Figure II - 111: Transfer Molded.

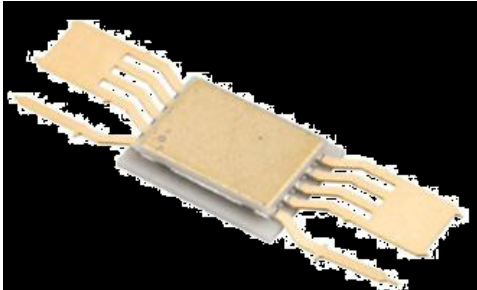


Figure II - 112: Encapsulated.

Vehicle Electric Traction System Coolant system

This effort is focused on understanding in detail coolant temperature and duration, and the correlation of these temperature profiles to electric drive profiles. Vehicle coolant system temperature profiles are being collected for the various electric drive vehicles. Investigations into possible areas of cost reduction are underway.

Power Module

This effort is to evaluate the individual technologies of power module: wide band gap (SiC and GaN), advanced silicon, and thermal. Evaluation of SiC has continued during this quarter with the focus on device cost and reduction in inverter losses. GM is working with SiC device suppliers and module manufacturers to create evaluation units. The latest Si devices have been incorporated into the Conventional based power module for evaluation. IGBT on-chip current and temp sense is being developed for fault protection. The module thermal system is being investigated to reduce cost and maximize performance. The thermal system includes the substrate, joint from substrate to heat sink, heat sink, and coolant manifold. Work has been jointly done with Tier 2 suppliers and non-traditional suppliers on each of the areas.

Capacitor

This effort will evaluate current and future capacitor requirements and methods of reducing total capacitance, and new films. A Tier 2 supplier was selected to develop a low cost bus capacitor (Figure II - 113). Design concepts have been generated by the supplier and are being evaluated. Additionally evaluation single bobbins

(Figure II - 114) representing the latest polypropylene film are expected to be delivered in the 4th quarter of 2012. Modularity and scalability of the capacitor bank is a key system level consideration in the potential solutions.

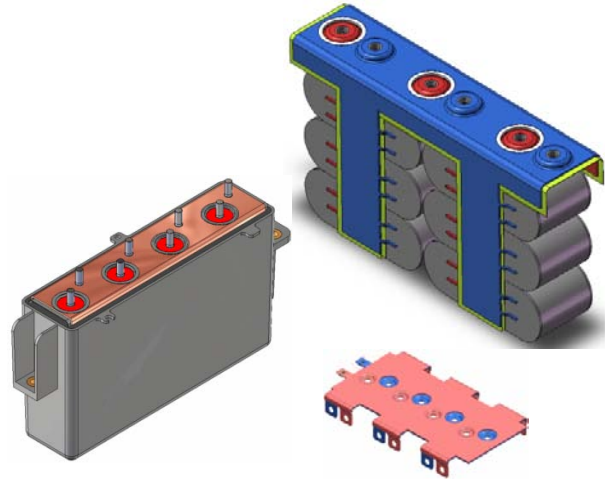


Figure II - 113: Example of Traditional DC Bus Capacitor.

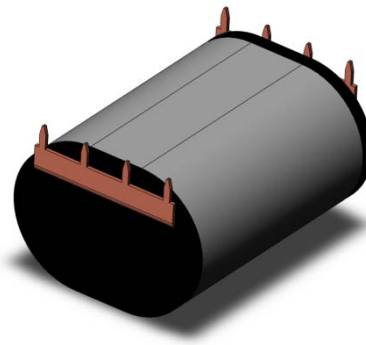


Figure II - 114: Example of Bobbin DC Bus Capacitor.

Gate Drive

This effort will evaluate new gate drive IC's and potential solutions being proposed by Tier 2 suppliers. A Tier 2 supplier is developing a new gate drive IC. First sample chips are expected early in the 4 quarter of 2012. The gate drive circuit has been designed considering the new IC.

Control Card

This effort will evaluate new processors and supporting circuitry. A control card design with the selected processor is complete and board delivery is expected 4th quarter of 2012. This board will be used to ensure control algorithms and software compatibility with the new processor, and to ensure that safety requirements will be met.

Concept

A conceptual design has been developed (Figure II - 115). An initial evaluation for cost, scalability, and modularity has been performed (Figure II - 116).

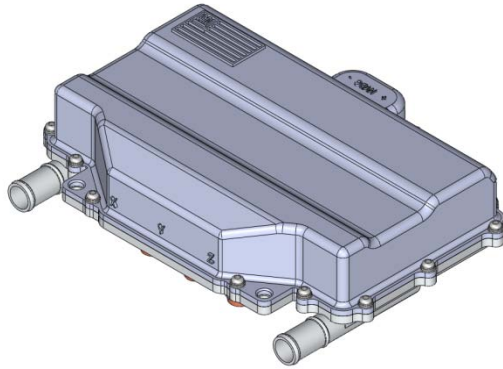


Figure II - 115: Design Concept.

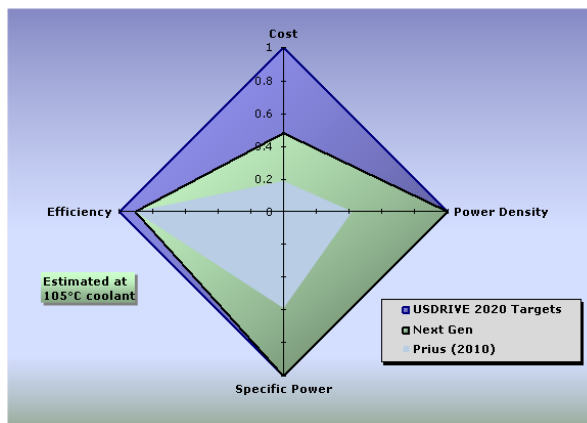


Figure II - 116: Comparison of current status to DOE Targets.

Publications

1. DOE Vehicle Technologies Program Kickoff
November 2, 2011
2. 2012 DOE Vehicle Technologies Program Review
May 15, 2012
3. DOE Vehicle Technologies Program Kickoff
November 14, 2012.

Conclusion

Overall progress under the program is consistent with the Project Plan. An inverter specification has been completed and cost drivers identified. Evaluation of Conventional, and Transfer Molded based inverters are continuing. The Encapsulated based inverter has been delayed to 4 quarter of 2012, but this is not expected to adversely affect the program schedule. Modularity and scalability study of a conventional based power module inverter has continued. Efforts are being done to create an evaluation SIC module with a device supplier and module manufacturer. A Power module thermal system is being worked to reduce cost. The capacitor supplier has developed design concepts. Gate drive design considering the new IC is under way. A control board has been designed and a board is expected in the 4th quarter of 2012.

II.9 High Dielectric Constant Capacitors for Power Electronic Systems

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Objectives

- Develop ceramic dielectric films that have potential to reduce size, weight, and cost, concomitant with increased capacitance density and high temperature operation, for capacitors in electric drive vehicle inverters.
- Current DC bus capacitors occupy a significant fraction of volume ($\approx 35\%$) and weight ($\approx 25\%$) of the inverter module, cannot tolerate temperatures $> 85^\circ\text{C}$, and suffer from poor packaging, and inadequate reliability.
- Traditional capacitor architectures with conventional dielectrics cannot adequately meet all of the performance goals for capacitance density, weight, volume, and cost.
- Meeting these goals requires a dielectric with high permittivity and breakdown field that tolerates operating at high temperature, is packaged in architecture with high volumetric efficiency, and exhibits benign failure features.

Approach

- Develop high-dielectric constant, high-temperature, low-cost ferroelectric $(\text{Pb,La})(\text{Zr,Ti})\text{O}_3$ (abbreviated as PLZT) dielectric films on base-metal foils (“film-on-foil”) that are either stacked on or embedded directly into the printed wire board (PWB).
- Stack high performance film-on-foils, produce prototype capacitor with termination, and characterize its properties.

- Develop a ceramic film fabrication methodology to produce dense films on flexible substrates at high production throughput.
- Use of base-metals and high-rate deposition techniques reduce the cost.
- Ferroelectrics possess high dielectric constants, breakdown fields, and insulation resistance. With their ability to withstand high temperatures, they can tolerate high ripple currents at under-the-hood conditions.
- Stacked and/or embedded capacitors significantly reduce component footprint, improve device performance, provide greater design and packaging flexibility, achieve high degree of volumetric efficiency with less weight, and offer an economic advantage.
- R&D efforts focus on examining the issues that underpin the performance of film-on-foil capacitors, establishing fabrication protocols that are commercially robust and economically viable.

Major Accomplishments

- Fabricated a $\approx 6 \mu\text{F}$ prototype capacitor by stacking film-on-foils. This multilayer stack was characterized as function of bias voltage, temperature, frequency and measured its ESR.
- Deposited PLZT films on thin ($< 20 \mu\text{m}$ thick) nickel foils. These film-on-foils on very thin metal foils can be wound in small radius of curvature.
- Evaluated residual stresses in film-on-foils fabricated on different types of substrates.
- Initiated the development of a new, high-rate film deposition process which has potential to produce thick, dense PLZT films at room temperature.
- Measured $k \approx 110$ & loss ≈ 0.004 (0.4%) at 300 V bias on a $\approx 3.0 \mu\text{m}$ -thick film (for comparison, k of polymer films are ≈ 3).
- Measured energy density $\approx 85 \text{ J/cm}^3$ on a $\approx 3.0 \mu\text{m}$ -thick PLZT film-on-foil at room temperature.
- Demonstrated film-on-foil PLZT dielectrics with dielectric breakdown field $> 2.6 \text{ MV/cm}$, and leakage current $< 10^{-8} \text{ A/cm}^2$.
- Demonstrated graceful failure mode by self-clearing method in single layer film-on-foil dielectrics.

- Dielectric films are thermally cycled (about 1000 cycles) between -50°C and $+150^{\circ}\text{C}$ with no measurable degradation in k.
- Highly accelerated lifetime tests (HALT) were performed at elevated temperature and high field stress to predict the lifetime of film-on-foils.
- Presented program status and future direction to DOE APEEM project kickoff, EE Tech Team, and Annual Merit Review meetings.
- Published nine papers in peer reviewed international journals and three papers in conference proceedings.
- Filed four patent applications.
- Presented the results at eight scientific conferences.

Future Direction

- The R&D effort in FY12 has demonstrated that the properties of PLZT film-on-foils are suitable for power electronics operating at under-the-hood temperatures. However, the spin coating method currently employed to make these film-on-foils requires too many processing steps. Processes such as aerosol deposition, colloidal spray deposition, and screen printing are known to produce thick ceramic and metal films on various substrates at rates much faster than that obtained with the current spin-coating process (e.g., ceramic films with thickness $>5\ \mu\text{m}$ are produced in a single coating step). In order to reduce the capacitor cost, we will develop aerosol deposition processes to fabricate thicker PLZT films capable of operating at 450 V. Sub-micron sized particles are essential for the success of the high-rate aerosol deposition process. To provide the sub-micron particles, the effort in FY13 will focus on the preparation of sub-micron-sized PLZT powders. After preparing the necessary powders, aerosol deposition process will be developed to fabricate thicker PLZT films in a single deposition step. This new technology has potential to produce wound ceramic film capacitors similar to those made with polymer films. The significance of the aerosol deposition process is its ability to produce high-temperature capable and high dielectric constant ceramic dielectric films at room temperature on variety of substrates (ex. plastics, polymer films, and thin metal foils) that are superior to the polymer dielectric films that are currently in use for electric drive vehicles. In collaboration with Penn State University, we will model heat generation and dissipation in single layer and multilayer PLZT capacitors. Modeling is important to understand thermal runaway conditions in multilayer capacitors.
- Stack high-voltage capable film-on-foils and produce a $\approx 10\ \mu\text{F}$ capacitor with termination.

- In collaboration with Pennsylvania State University and Delphi Automotive Systems, characterize the dielectric properties and high temperature behavior of film-on-foils and the stacked, multilayer capacitor made by the high-rate deposition process.
- Investigate electrode material and architecture to achieve benign failure in multilayers or wound capacitors.
- Optimize and scale-up the down-selected high-rate deposition process and fabricate prototype modules for DC link capacitor for power inverter.
- Fabricate films with improved breakdown strength and reduced loss via novel superstructure film growth mechanism.
- Identify industrial partner to manufacture ceramic film capacitors.



Technical Discussion

The overall project objective is to develop ceramic dielectric films that have potential to reduce size, weight, and cost, concomitant with increased capacitance density and high temperature operation, for capacitors in electric drive vehicle inverters. The purpose of this project is to build and test a prototype capacitor capable of meeting APEEM requirements. The performance of presently available capacitors degrade rapidly with increasing temperature and they occupy significant fraction of the inverter volume ($\approx 35\%$), weight ($\approx 25\%$), and cost ($\approx 25\%$). The ceramic dielectric capacitor R&D program at Argonne National Laboratory (Argonne) addresses the technology gap in an innovative manner. We are developing high performance, low cost capacitors that are either stacked on or embedded directly into the printed wire board (PWB). In these “film-on-foil” capacitors, a base-metal foil (aluminum, nickel, or copper) is coated with a high permittivity ferroelectric material, PLZT, via a chemical solution deposition (CSD) technique. Ferroelectrics possess high permittivity, breakdown electric fields, and insulation resistance. They can withstand high temperatures such that high ripple currents can be tolerated at under-the-hood temperatures. Use of base-metals reduce the cost of the capacitor. The stacked and embedded capacitors approaches significantly reduces component footprint, improves device performance, provides greater design flexibility, and offers an economic advantage for commercialization. This technology will achieve the high degree of packaging volumetric efficiency with less weight. Device reliability is improved because the number and size of interconnections are reduced. While this technology has primarily received attention for low voltage, high frequency decoupling capacitors, it can potentially be extended to the higher voltages of electric

drive vehicle systems. The vision of embedded DC bus capacitors is compelling and offers US automotive companies a substantial technological advantage over their foreign counterparts. The bulky coke-can-like banks of capacitors can be replaced by lengths of capacitors tucked flat and neatly underneath the active components and bus structure. While embedding the film-on-foil capacitors into the PWB is the ultimate goal, the short-term practical approach is to target high voltage, high temperature, stacked capacitors for the inverter applications using film-on-foil dielectric layers. The short-term target will address the important issues, namely, weight, volume, and cost advantages of the film-on-foils compared to the conventional, bulky, wound polymer capacitors. Our R&D efforts focus on examining the issues that underpin the performance of film-on-foil capacitors, establishing fabrication protocols that are commercially robust and economically viable.

We have developed a core technology for fabricating CSD PLZT on Ni foils with LaNiO_3 (LNO) buffer layers. CSD solutions were synthesized at Argonne, and films were deposited by spin coating. High purity (99.98% pure) nickel substrates with dimensions of $25 \text{ mm} \times 25 \text{ mm} \times 0.4 \text{ mm}$ were obtained from MTI Corp. (Richmond, California). They were polished by chemical-mechanical planarization (CMP) process. A root-mean-square surface roughness of $\approx 2 \text{ nm}$ was measured by atomic force microscopy (AFM) in the tapping mode with $5 \mu\text{m} \times 5 \mu\text{m}$ scan size. Prior to being coated, CMP nickel substrates were ultrasonically cleaned in distilled water, and then wipe-cleaned with acetone and methanol in sequence. The detailed procedure is reported elsewhere [1-5]. The LNO solution was spin-coated onto the substrate at 3000 rpm for 30 sec, pyrolyzed at $\approx 450^\circ\text{C}$ for 5-10 min, and crystallized at $\approx 650^\circ\text{C}$ for 2-5 min. This process was repeated five times to build the desired thickness with a final annealing at $\approx 650^\circ\text{C}$ for 20 min. The PLZT stock solution was spin-coated onto the LNO-buffered substrate at 3000 rpm for 30 sec. Films were then pyrolyzed at $\approx 450^\circ\text{C}$ for 10 min and crystallized at $\approx 650^\circ\text{C}$ for 2-5 min, followed by a final annealing at $\approx 650^\circ\text{C}$ for 20 min after repeating the coating steps to build up layers of sufficient thickness. By this process, we have fabricated PLZT films with thicknesses up to $\approx 3 \mu\text{m}$. Platinum top electrodes were then deposited by electron beam evaporation using a shadow mask. These electrodes had diameters of $250 \mu\text{m}$, $750 \mu\text{m}$, and 20 mm and thickness of $\approx 100 \text{ nm}$. Films with top electrodes were annealed at $\approx 450^\circ\text{C}$ in air for 2 min for electrode conditioning. A Signatone QuietTemp® probe system with heatable vacuum chuck (Lucas Signatone Corp., Gilroy, CA) was used for electrical characterization. For the electrical measurements, the Pt/PLZT/LNO/Ni heterostructure was contacted by a Pt top electrode pad with one probe and the substrate (bottom electrode) with the other. A positive applied voltage corresponds to the configuration where the top electrode is at a higher potential than the

bottom electrode. An Agilent E4980A Precision LCR Meter measured the capacitance and dissipation factor under applied bias field. A Radiant Technologies' Precision Premier II tester measured the hysteresis loops. The capacitor samples were immersed in Fluka silicone oil (Sigma-Aldrich) during high-field hysteresis loops and dielectric breakdown measurements. A Keithley 237 high-voltage source meter measured the current-voltage characteristics. The leakage current density was determined by fitting the current density relaxation data to the Curie-von Schweidler equation [6]. Residual stress in the film was studied by X-ray diffraction [7] method using a Bruker AXS D8 diffraction system.

The PLZT films grown on LNO-buffered Ni foils were phase pure with no preferred crystallographic orientation as shown by X-ray diffraction, and no crack or delamination was observed from SEM [1]. The use of LNO buffer allows the film-on-foils to be processed in air without the formation of a parasitic interfacial nickel oxide layer. The LNO also compensates for the roughness of the Ni foil and provides a smooth interface for the PLZT films, resulting in higher breakdown strengths. In addition, the LNO buffer helps to reduce the compressive strain in the PLZT films deposited on nickel substrates due to the thermal expansion coefficient mismatch between PLZT and metal foils [8].

Figure II - 117 shows the 2θ X-ray diffraction patterns measured on $\approx 2 \mu\text{m}$ -thick PLZT films deposited on LNO-buffered Ni and platinumized silicon (PtSi) substrates. The data indicate that both samples are well crystallized without preferred orientation. All peaks can be indexed accordingly (JCPDS 56-0900). The use of LNO prevents the formation of a parasitic interfacial nickel oxide layer. The LNO also compensates for the roughness of the Ni foil and provides a smooth interface for the PLZT film to grow on. Diffraction peaks from the nickel substrate and the LNO buffer film can be identified from the diffraction pattern shown in Figure II - 117a. The tiny peak at $2\theta \approx 36^\circ$, as indicated by a small open triangle on the XRD pattern for PLZT grown on PtSi (Figure II - 117b), is from $\text{Cu-K}\beta$ diffraction of Pt (111) plane. No crack or delamination was observed from SEM [9]. A close look at the two diffraction patterns shown in Figure II - 117 revealed that the PLZT peaks in Figure II - 117a shifted to lower angle when compared to those peaks for the same index shown in Figure II - 117b. With the regular θ - 2θ scan configuration, diffraction patterns are measured on these crystallites with the diffraction plan parallel to the substrate surface. According to Bragg's equation, a peak shift to lower 2θ angle indicates an expansion of d-spacing in the out-of-plane direction, as a result of compressive strains in the in-plane directions that are parallel to the substrate surface. Residual stress analysis by x-ray diffraction indicated compressive strain in PLZT grown on

LNO-buffered nickel substrate, but tensile strain in PLZT grown on PtSi substrate.

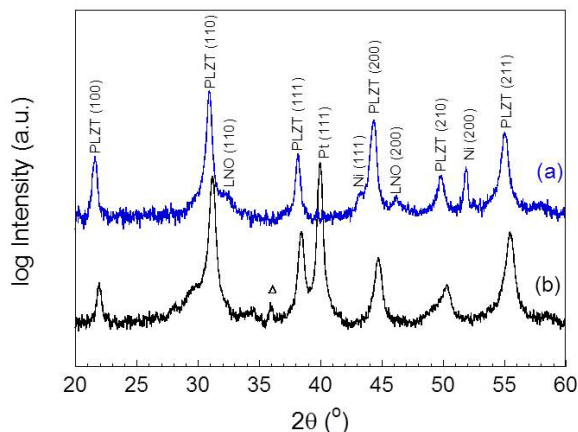


Figure II - 117: X-ray diffraction patterns of PLZT films grown on (a) LNO-buffered Ni and (b) Pt coated silicon substrates using chemical solution deposition processes.

The total stress σ_{tot} in a polycrystalline film results from both an intrinsic stress σ_{int} and thermal stress σ_{th} . The intrinsic (or growth) stress originates from the cumulative effect of structural imperfections that appear on the film during deposition. Its magnitude is largely determined by the deposition conditions. By contrast, thermal stress is the result of differences in the coefficient of thermal expansion between the film and substrates over the cooling range from the annealing temperature T_{ann} to the testing temperature T_0 . The thermal stress can be expressed as [9],

$$\sigma_{th}(T_0) = \frac{E_f}{1 - \nu_f} \int_{T_0}^{T_{ann}} (\alpha_f - \alpha_s) dT \quad (1)$$

and the corresponding strain by,

$$\epsilon_{th} = \int_{T_0}^{T_{ann}} (\alpha_f - \alpha_s) dT \quad (2)$$

where E_f and ν_f are the Young's modulus and the Poisson ratio of the thin film material, and α_f and α_s are the coefficient of thermal expansion for the film and the substrate, respectively. (Values used in this study are summarized in Table II - 6.) Assuming the sample is stress free at annealing temperature 650°C , calculations using Eqs. 1 and 2 predicated ≈ 120 MPa tensile stress ($\approx 0.1\%$ tensile strain) in PLZT deposited on PtSi substrates and ≈ 530 MPa compressive stress ($\approx 0.5\%$ compressive strain) in PLZT grown on LNO-buffered Ni substrate due to thermal expansion mismatch between the films and the underneath substrates.

Table II - 6: Selected physical properties of relevant materials.

	E (GPa)	ν	CTE, α ($\times 10^{-6}/\text{k}$)	Reference
Ni	200	0.31	13.4	10
Pt	168	0.39	8.8	11
Si	130	0.28	3.6	12
LNO*	70	0.30	8.2	13
PLZT	72	0.28	5.4	14

* Young's modulus (E) and Poisson ratio (ν) values for LNO are not available. We estimated these values based upon those for other perovskites. CTE = coefficient of thermal expansion.

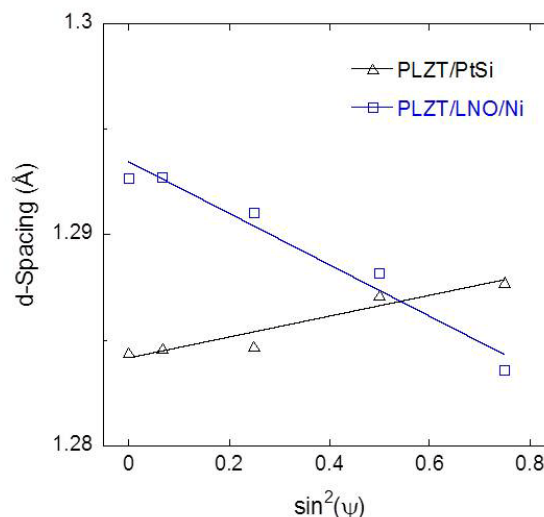


Figure II - 118: Lattice d-spacing as a function of $\sin^2\psi$ for PLZT films grown on LNO/Ni and PtSi substrates by chemical solution deposition.

Figure II - 118 shows lattice d-spacing as a function of $\sin^2\psi$ measured by x-ray diffraction on PLZT films grown on PtSi and LNO-buffered Ni substrates. These measurements were carried out on the PLZT (310) peak. The residual stress in the PLZT films can be determined from [7],

$$\sigma_\phi = \left(\frac{E}{1 + \nu} \right)_{(hkl)} \cdot \frac{1}{d_{\phi 0}} \cdot \frac{\partial d_{\phi\psi}}{\partial \sin^2 \psi} \quad (3)$$

where $d_{\phi 0}$ and $d_{\phi\psi}$ are the lattice d-spacing in a stress-free sample and that measured in a stressed sample that was tilted at ψ angle, respectively. We measured a tensile stress of ≈ 210 MPa in ≈ 2 μm -thick PLZT films grown on PtSi substrates. Even though this value is comparable to those reported by other groups [14,15], it is nearly twice as much higher than the value (≈ 120 MPa) calculated from Eq. 1 for the thermal stress in PLZT due to cooling from 650°C to room temperature. Ong et al. [14] has also reported similar difference between the in-plane stress determined from XRD curvature measurement and that estimated for thermal stress due to cooling. This difference can be attributed to stress produced during the crystallization process, i.e., the intrinsic stress. A compressive stress of ≈ 520 MPa was measured for PLZT grown on LNO-

buffered Ni substrates from XRD analysis. This value is comparable to the thermal stress (≈ 530 MPa) calculated for PLZT grown on LNO-buffered Ni substrate when the sample is cooled from 650°C to room temperature. This finding suggests that the thermal stress is a dominant contributor to the total residual stress in PLZT films grown on nickel substrates, whereas intrinsic stress formed during film growth is largely negligible. Residual stress measured using other diffraction peaks yielded comparable results.

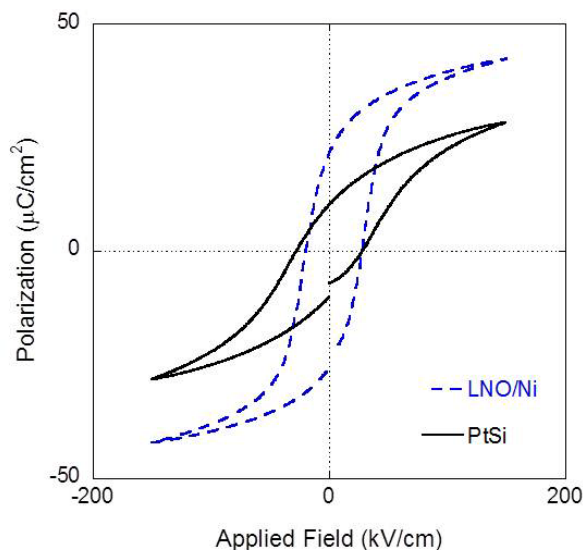


Figure II - 119: Polarization-field hysteresis loops measured at room temperature on PLZT films grown on LNO/Ni and PtSi substrates.

Figure II - 119 shows the polarization-field (P-E) hysteresis loops measured at room temperature on ≈ 2 μm -thick PLZT/LNO/Ni film-on-foils with Pt top electrodes using a field sweeping period of 10 ms (frequency of 100 Hz). From the P-E loop with a maximum applied voltage of 30 V (corresponding to an electric field of 150 kV/cm), we measured a remanent polarization (P_r) of ≈ 25.4 $\mu\text{C}/\text{cm}^2$ and ≈ 10.1 $\mu\text{C}/\text{cm}^2$, and coercive electric field (E_c) of ≈ 23.8 kV/cm and ≈ 27.9 kV/cm, for PLZT films grown on LNO/Ni and PtSi substrates, respectively. This difference in P-E loops can be attributed to the total strain in PLZT films. Lee et al. [16] reported that an increase in tensile residual stress leads to reduction in remanent polarization and saturation polarization, and an increase in compressive stress (decrease in tensile stress) results in a rise in remanent polarization and saturation polarization. Our experimental results revealed the same trend.

Figure II - 120 shows dielectric constant and loss as a function of bias field measured at room temperature for samples of PLZT grown on LNO/Ni and PtSi substrates. The data conformed to butterfly-shaped curves, which are typical for FE materials measured below the Curie temperature. At zero bias field, dielectric constant of ≈ 1300 and dielectric loss of ≈ 0.06 were measured for PLZT grown on LNO/Ni substrate, and dielectric constant

of ≈ 1350 and dielectric loss of ≈ 0.05 were found for samples deposited on PtSi substrates. Considering both samples consist of PLZT films of the same thickness (≈ 2 μm), they exhibit different field-dependent change, i.e., “tunability,” which can be expressed as,

$$\eta = \left[1 - \frac{\epsilon_r(E)}{\epsilon_r(0)} \right] \times 100\% \quad (4)$$

where $\epsilon_r(E)$ is the dielectric response in the presence of an external field E . We observed tunability of $\approx 55\%$ and $\approx 40\%$ at room temperature under 100 kV/cm applied field for PLZT deposited on LNO/Ni and PtSi substrates, respectively.

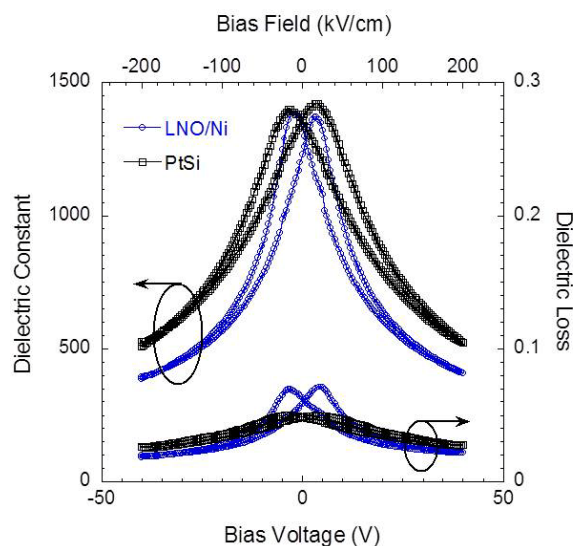


Figure II - 120: Field-dependent dielectric properties measured at room temperature on PLZT films grown on LNO/Ni and PtSi substrates.

Dielectric breakdown strength was measured on 250- μm -diameter capacitors with Pt top electrodes using the “top-to-bottom” electrode configuration. The applied voltage was increased by 5 V per second, and the breakdown voltage was determined with an 1- μA criterion. Weibull statistics [17,18] was employed for failure behavior analysis. The empirical two-parameter Weibull function for failure probability distribution, also known as the “cumulative distribution function,” can be written as,

$$F(t) = 1 - \exp \left[- \left(\frac{t}{\eta} \right)^\beta \right] \quad (6)$$

where β and η are fitting parameters, the Weibull modulus and mean value of experimental observable t , respectively. The Weibull modulus is a measure of sample distribution, high values of β corresponding to smaller variation. For breakdown field measurements, the parameter of interest is applied field. Mean breakdown

strength can be extracted from points where the fitting lines intersect with the horizontal line through $\ln(\ln(1/(1-p))) = 0$. We calculated the sampling cumulative distribution parameter p , using Bernard's approximation, from the following formula for each set of experimental data,

$$p = \frac{r - 0.3}{N + 0.4} \tag{7}$$

where N is the total sample number, and r is the sample sequential number.

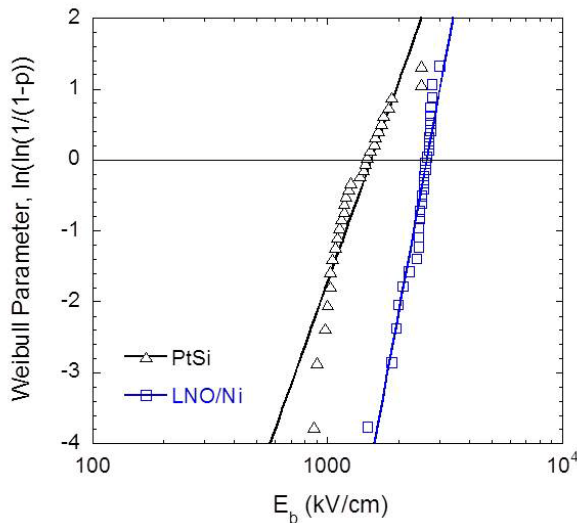


Figure II - 121: Weibull plot for breakdown field strength of PLZT deposited on LNO/Ni and PtSi substrates.

Figure II - 121 shows the Weibull plot of breakdown field strength obtained at room temperature from 30 capacitor samples of PLZT grown on PtSi and another 30 capacitor samples of PLZT grown on LNO/Ni substrates. The solid straight line is a least-square fitting to the two-parameter distribution function given in Eq. 6. We measured mean breakdown field of 1.5×10^6 V/cm and 2.6×10^6 V/cm, and Weibull modulus β of 4.0 and 7.8 for ≈ 2 - μm -thick PLZT grown on PtSi and LNO/Ni substrates, respectively. Weibull modulus is a measure of distribution of the data: the higher the value of β , the smaller the variation of the data. Thus, a higher modulus indicates a better representation of the sample-to-sample performance as measured by mean breakdown strength. The difference in breakdown property between PLZT grown on PtSi and that grown on LNO/Ni is a result of difference in residual stress in the samples.

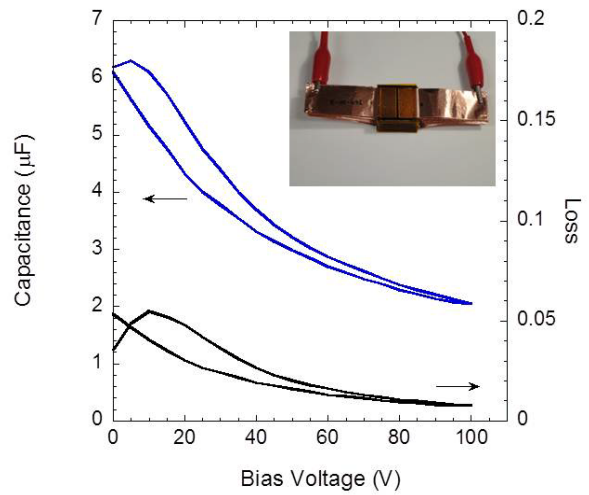


Figure II - 122: Capacitance and dielectric loss measured at room temperature as a function of bias voltage on a film-on-foil capacitor stack (shown in inset).

Figure II - 122 shows the capacitance and dielectric loss of a capacitor stack consisting of 18 film-on-foils. Each film-on-foil capacitor has copper ribbons attached as electrical leads. Testing was conducted at room temperature as a function of applied bias up to 100 V. We measured capacitance of $\approx 6 \mu\text{F}$ and dielectric loss of ≈ 0.05 for this stack at room temperature under zero bias. Both capacitance and dielectric loss decrease with increasing bias voltage. At 100 V bias, we measured capacitance of $\approx 2.1 \mu\text{F}$ and dielectric loss of < 0.01 .

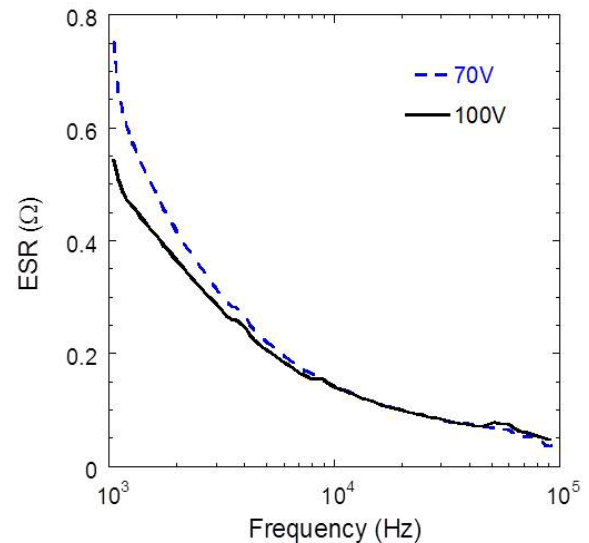


Figure II - 123: Frequency dependent ESR measured at room temperature for a capacitor stack consisting of 18 film-on-foil elements.

The equivalent series resistance (ESR) measured as function of frequency for the multilayer stack is plotted in Figure II - 123. The testing was conducted at room temperature under 70 V and 100 V applied bias. The

dashed line is for data measured with 70 V bias; and the solid line shows data measured with 100 V bias. ESR decreases with increasing frequency as expected from the following equation,

$$ESR = \frac{\tan \delta}{2\pi f \cdot C} \quad (8)$$

where $\tan \delta$ is the dielectric loss, f the frequency, and C the capacitance. We observed decrease in ESR as the bias voltage was increased from 70 to 100 V in the frequency range 1-10 kHz. At frequencies >10 kHz, the measured ESR with 70 V and 100 V bias are virtually identical. From the ESR measured on the small multilayer stack we calculated the ESR for a 1000 μF capacitor to be ≤ 1 m Ω at frequencies >1 kHz. This meets the APEEM goal of <3 m Ω for applications in advanced power inverters.

Polarization-electric field (P-E) hysteresis loops were measured for the multilayer stack that has film area of ≈ 36 cm² and a small area film (electrode diameter ≈ 750 μm). As shown in Figure II - 124, both capacitors exhibit comparable properties despite their huge difference (more than three orders of magnitude) in capacitance. This result demonstrates that the energy density and high voltage capability of PLZT film-on-foil capacitors are maintained upon scaling-up the film area by orders of magnitude.

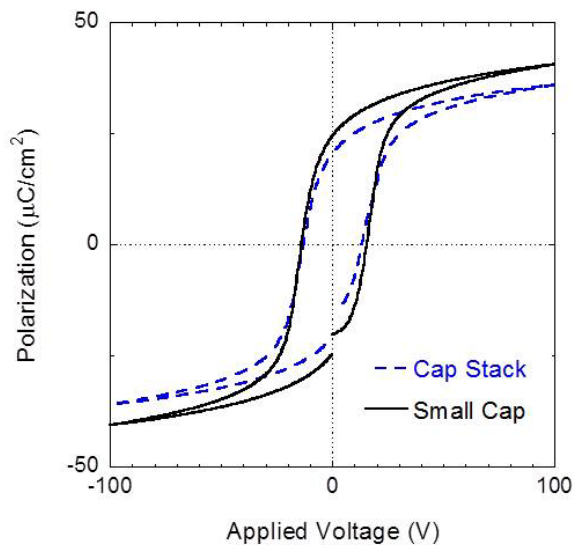


Figure II - 124: Hysteresis loops measured at room temperature as a function of applied voltage on a multilayer stack (dashed line; film area ≈ 36 cm²) and a small area film-on-foil (electrode dia. 750 μm).

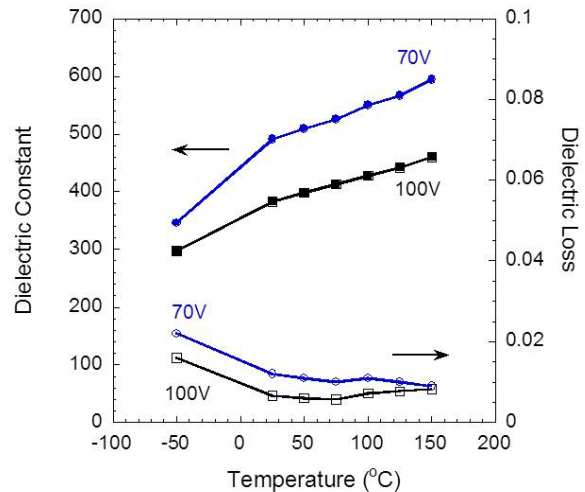


Figure II - 125: Temperature dependent dielectric properties of a film-on-foil measured at 70 and 100 V bias.

Figure II - 125 shows capacitance and dielectric loss measured for a film-on-foil at 70 and 100 V bias as a function of temperature. The dielectric constant (hence the capacitance) increases with increasing temperature. At -50°C, we measured dielectric constant ≈ 300 and dielectric loss ≈ 0.015 with 100 V bias. Dielectric constant increases while dielectric loss decreases with increase in temperature. At 150°C, we measured dielectric constant ≈ 460 and dielectric loss < 0.01 . The data on Figure II - 125 shows that the PLZT film-on-foils have high-temperature operational capability and high dielectric constant at high voltages.

Conclusion

We have developed a core technology for fabricating high capacitance density, high temperature ceramic PLZT films on base metal foils, called “film-on-foil” technology. PLZT film-on-foils have been fabricated with LNO buffer layers atop Ni foils, allowing the capacitors to be processed in air. At 1 kHz and zero bias, we measured dielectric constant of ≈ 700 and dielectric loss of 0.04 at -50°C, dielectric constant of ≈ 1150 and dielectric loss of ≈ 0.05 at room temperature, and dielectric constant of ≈ 1900 and dielectric loss of ≈ 0.03 at 150°C, respectively. Film-on-foil samples were characterized under high bias fields. We measured dielectric constant of ≈ 230 and loss of ≈ 0.008 (0.8%) at 100 V bias, dielectric constant of ≈ 140 and loss of ≈ 0.005 (0.5%) at 200 V bias, dielectric constant of ≈ 110 and loss of ≈ 0.004 (0.4%) at 300 V bias on a ≈ 3 - μm -thick PLZT film-on-foil sample. Film-on-foil capacitors with copper ribbon electrical leads were fabricated and characterized as function of temperature, applied bias, and frequency. At room temperature, we measured capacitance of ≈ 6 μF (unbiased condition) and 2.1 μF with 100 V bias. The properties measured show that these ceramic film capacitors have potential to meet the

APEEM goals. Our results and the research plans were presented at the VT program's APEEM project kickoff, Annual Merit and Peer Review, and EE Tech Team meetings. The spin-coating method currently used to make PLZT films requires too many processing steps. The primary emphasis of FY13 effort is to develop a high-rate deposition process to make these films.

Publications

We have over 50 publications and presentations, and few selected recent publications are listed below.

1. S. Liu, B. Ma, M. Narayanan, S. Tong, R.E. Koritala, U. Balachandran, *Microstructure and electrical properties of LaNiO_3 thin films by RF sputtering for the growth of $(\text{Pb,Lu})(\text{Zr,Ti})\text{O}_3$ films on silicon and nickel substrates*, J. Vac. Sci. Technol. A30, 061505, 2012.
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3. B. Ma, S. Liu, M. Narayanan, U. Balachandran, *Development of high dielectric strength ceramic film capacitors for advanced power electronic devices*, proceedings of the 45th International Symposium on Microelectronics (IMAPS 2012), San Diego, CA, Sep. 9, 2012 - Sep. 13, 2012.
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11. M. Narayanan, S. Tong, R. E. Koritala, B. Ma, V. Pol, U. Balachandran, *Sol-Gel Synthesis of High-Quality SrRuO_3 Thin-Film Electrodes Suppressing the Formation of Detrimental RuO_2 and the Dielectric Properties of Integrated Lead Lanthanum Zirconate Titanate Films*, Chem. Mater., 23, 106, 2011.
12. B. Ma, M. Narayanan, S. Liu, S. Chao, U. Balachandran, *Ferroelectric PLZT films grown on metal foils for power electronic applications*, proceedings of the 20th IEEE International Symposium on Applications of Ferroelectrics and International Symposium of Piezoresponse Force and Microscopy & Nanoscale Phenomena in Polar Materials, Vancouver, Canada, Jul. 24 - 27, 2011
13. M. Narayanan, B. Ma, R. Koritala, S. Tong, U. Balachandran, *Chemical solution deposition of high-quality SrRuO_3 thin film electrodes and the dielectric properties of integrated lead lanthanum zirconate titanate films*, proceedings of the 7th International Conference and Exhibition on Ceramic Interconnect and Ceramic Microsystems Technologies, San Diego, CA, Apr. 5-7, 2011.
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Patents

1. B. Ma, M. Narayanan, S. E. Dorris, and U. Balachandran, *Method for Fabrication of Ceramic Dielectric Films on Copper Foils*, Patent Application US 2010/0302706A1, published Dec. 2, 2010.

Awards

1. The ceramic film capacitor technology developed at Argonne National Laboratory, *Advanced Ceramic Film Capacitor for Power Electronics*, received the 2011 R&D 100 Award.

II.10 High Temperature Thin Film Polymer Dielectric Based Capacitors for HEV Power Electronic Systems

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Objectives

DC bus capacitors are currently the largest and the lowest reliability component of fuel cell and electric hybrid vehicle inverters. Capacitors represent up to 23% of both inverter weight and inverter cost and up to 35% of the inverter volume. Furthermore, existing DC bus capacitors cannot tolerate temperatures greater than 120°C. Our project goal is to develop an inexpensive replacement high energy density, high temperature polymer-based dielectric for DC bus capacitors for use in next generation hybrid electric vehicles (HEVs), plug in hybrid electric vehicles (PHEVs), and electric vehicles (EV). The improved capacitors will be based on novel inexpensive, high temperature polymer thin film dielectrics that have much of the chemical functionality of the known high temperature polymer Kapton®. Our technical goal is to enhance high temperature performance and volumetric efficiency compared to present dielectrics. Specific metrics include the development of polymer film dielectrics with dissipation factors of 0.02 or less at 150 °C. Synthesis, fabrication, and high temperature (room temperature to 150 °C) characterization of these dielectric materials is an integral part of the material development program. Inexpensive nanoparticle fillers will be utilized to further

reduce the capacitor size as both dielectric breakdown and relative permittivity are improved, while still maintaining the benign failure mode of polymer dielectrics. In addition, work will focus on transitioning the material to industry to produce rolls of the novel high temperature polymer dielectric film which will lead directly to the production of a prototype capacitor.

Approach

Sandia National Laboratory's (Sandia) capacitor research and development (R&D) program addresses the high temperature capacitor technology gap in an innovative manner. We are developing high performance, high temperature, low cost capacitors that are based on novel Sandia developed polymer chemistry. Capacitors fabricated using this polymer technology will achieve the high degree of packaging volumetric efficiency with less weight while maintaining a cost of less than \$0.03 per μF dramatically reducing high temperature polymer capacitor volume relative to state of the art high temperature polymer film capacitors. Our R&D specific efforts focus on producing polymer film at Electronic Concepts, Inc. (ECI) using a solvent casting technique and at Dr. Collin company using an extrusion technique which should lower the final dielectric material cost. In both cases, material will be produced in an appropriate quantity to fabricate prototype capacitors. Inexpensive nanoparticle fillers will also be used to further increase dielectric breakdown strength and improve relative permittivity in order to further decrease capacitor volume to meet the DOE APEEM program goals.

Major Accomplishments

- Fabricated and characterized two 0.5 μF packaged stacked capacitors in-house. Each packaged capacitor was end sprayed with Babbitt, end connected with soldered SnCu leads, and encapsulated in epoxy.
- Worked with Dr. Collin company to demonstrate the extrusion of the Sandia developed thin polymer film suitable for capacitor formation. Films as thin as 3 μm and lengths as long as 100 m were produced.
- Purchased and installed bench top extrusion equipment at Sandia in order to produce rolls of polymer dielectric.
- Screened a dozen different plasticizers effects on thin polymer dielectric mechanical, thermal, and electrical

properties and settled on a high temperature mellitate based plasticizer.

- Identified an inexpensive commercially available high T_g polynorbornene-based material as a possible next generation dielectric. The material has been used to produce thin films which have been electrically characterized to confirm the desired high temperature performance.

Future Direction

The R&D effort has demonstrated feasibility of using high temperature dielectrics for power electronics operating at high temperatures (>150 °C). Extrusion of the Sandia developed dielectric was demonstrated in FY12 in collaboration with Dr. Collin company. This extrusion resulted in the formation of a roll of 12 μm thick dielectric with a length of over 100 m. A high temperature plasticizer (bp >400 °C) was identified which provided optimum mechanical and electrical properties of thin polymer films. Work for FY13 will focus on transitioning the extrusion process for the production of rolls of polymer film to Sandia using a bench top extruder purchased from Dr. Collin company. The spools of extruded polymer dielectric will then be slit, metalized, rolled into capacitors, thermal sprayed, and packaged using high temperature potting materials. At least six prototype capacitors with capacitances of 5.0 – 10.0 μF or greater will be evaluated and benchmarked against APEEM goals. These initial prototype capacitors (rolled or stacked) will be evaluated by Oak Ridge National Laboratories as well as other research institutions including Penn State and Argonne National Laboratories. The prototype capacitors will also be evaluated at ECI. We will continue our effort in developing dielectric materials with improved performance focusing on the incorporation of nanoparticle fillers to increase the dielectric breakdown strength and relative permittivity in order to further increase the energy density and decrease the capacitor volume. FY13 will include a demonstration of extruded thin polymer film including nanoparticle fillers.



Technical Discussion

1.0. Commercially Available Capacitor Limitations

Polymer dielectric-based direct current (DC) bus capacitors are a required component within current inverters used in fuel cell, electric, and electric hybrid vehicle inverters. One of the reasons polymer-based capacitors are used in the inverter application is due to the failure mode. If the capacitor fails, it fails safely as an open (known as benign failure) rather than a potential fire or explosion inducing short. However, these polymer-based

capacitors are currently the largest and the lowest reliability component within the inverter and represent up to 23% of both inverter weight and inverter cost and up to 35% of the inverter volume. Furthermore, existing polymer DC bus capacitors cannot tolerate temperatures greater than 120°C. The main goal of this project is to develop a polymer-based dielectric which leads to capacitors that are capable of meeting the APEEM program goals.

2.0. Polymer Film Production Leading to Capacitors

We have studied a high temperature polymer dielectric which has been synthesized from very inexpensive monomers using a controlled polymerization based on the ring opening metathesis polymerization (ROMP).[1-4] The polymer has many of the same functional groups that are present in the known high temperature polymer Kapton® including the imide, ether and aromatic moieties. The polymer is shown in Figure II - 126A.

Previous attempts to cast dielectric films on a large scale using dichloroethane as the casting solvent at ECI yielded only small amounts of polymer dielectric film when using the initial Sandia developed dielectric shown in Figure II - 126B.

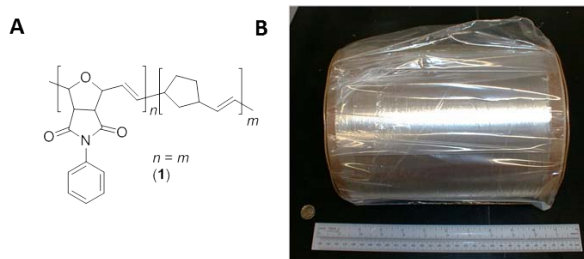


Figure II - 126: A) Structure of the high temperature polymer dielectric polymer and B) Spool of the high temperature polymer dielectric produced at ECI.

It was noted during this time that the polymer solutions used for solvent casting were not stable for long periods of time. For example, a typical procedure to produce polymer film started by dissolving the polymer into an appropriate solvent such as dichloroethane to produce a solution suitable for casting experiments. Unused polymer solution would be stored in air usually over a weekend. Polymer was precipitating out of solution and did not go back into solution upon heating or stirring when the polymer solution was examined later. These results are consistent with the crosslinking of the double bonds in the backbone of polymer 1 as shown in Figure II - 127.

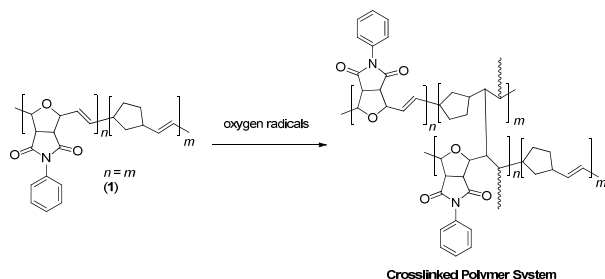


Figure II - 127: Crosslinking reaction that results in polymer precipitation from casting solutions.

Several experiments confirmed the initially observed crosslinking reactions. In one such experiment, free radical inhibitors were added to the dielectric polymer solutions. In all cases, the polymer solution stability was greatly improved by the addition of free radical inhibitor to dielectric polymer solutions. Two solutions of polymer both formed at concentrations of 7% (w/w) were compared optically, in one specific example. Solution A contained no free radical inhibitor, whereas, solution B contained the common free radical inhibitor 3,5-di-*t*-butyl-4-hydroxytoluene (BHT).[5] Solution A became cloudy after 48 h, whereas the solution B was still transparent. The solution that contained the free radical inhibitor BHT was not crosslinking due to inhibition of the side reactions that were leading to crosslinking.

Polynorbornene based polymers are highly unsaturated polymers which are quite prone to oxidative degradation which limits solubility in organic solvents (as shown above). Removal of the reactive double bonds was evaluated as a potential method to enhance polymer solution lifetimes, improve processing, and film formation. Hydrogenation of the olefin containing polymers was accomplished using tosylhydrazide as the diimide hydrogenation precursor. The hydrazide undergoes decomposition at elevated temperatures to form diimide at high temperatures, which is the reactive species responsible for hydrogenation.[6, 7] In large-scale production, less expensive hydrogenation processes could be used such as hydrogen gas used in combination with a heterogeneous or homogeneous catalyst.[8, 9] Hydrogenation of the polymer system **1** produced the desired hydrogenated polymer (**2**) which is shown in Figure II - 128.

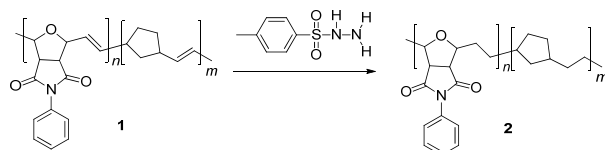


Figure II - 128: Hydrogenation of a model polymer dielectric.

Polymer **2** stoichiometry was optimized to provide optimal dielectric properties including breakdown strength which is shown in Figure II - 129. The breakdown strength

of the hydrogenated polymer increases as the imide content increases. The polymer with the greatest breakdown strength was scaled up and further characterized thermally. Between 26 and 30 parallel plate capacitors were fabricated with top-side electrodes having diameters of 6.3 mm. The bottom electrodes were a continuous film. All electrodes were Au, deposited using a sputter coater at rate of 16 nm/min for a total Au thickness of 50 nm. The metalized dielectric film was placed on a Cu ground plate and the top electrodes were immersed in Fluorinert FC-40 (Aldrich) prior to electrical testing to prevent arcing and surface discharge. Weibull statistics were used to analyze the breakdown field, which was determined to be 326 V/ μm (Figure II - 129) which results in a calculated energy density of 1.54 J/cm³ for the polymer formulation (where $n = 3m$, Figure II - 128) (72% imide).[5-7] No special effort was undertaken to ensure that particulates were not in the film which would lower breakdown strength. Presumably, if additional steps were taken to ensure minimal particulate inclusion by casting films within a clean room the breakdown strength could be greatly enhanced.

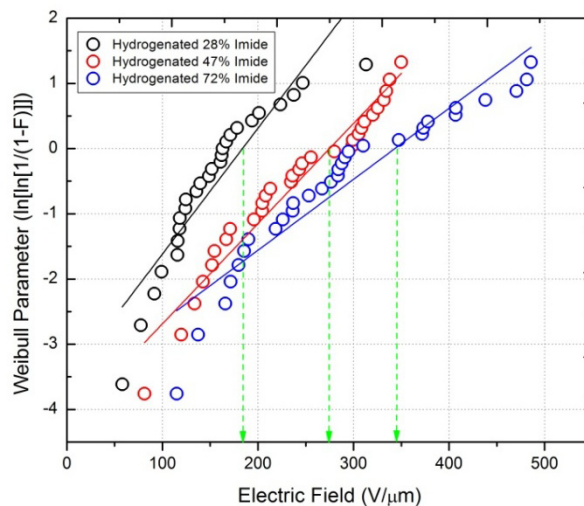


Figure II - 129: Breakdown strength of hydrogenated polymers as a function of imide content.

Thermal characterization of polymer **2** where $n = m$ produced a polymer with a relatively low glass transition temperature (T_g) of 100°C (data not shown) and capacitors produced using hydrogenated polymers with $n = m$ (48% imide) failed at temperatures less than 150°C (Figure II - 130). In this case, a capacitor is considered to have failed if the normalized capacitance drops below 90% of the original value. The data shown in Figure II - 130 is an average of capacitance for five capacitors as a function of temperature. Thermal characterization of polymer **2** where $m = 0$, resulted in a polymer with a T_g of 250°C (data not shown). Changing the copolymer stoichiometry

to $n = 3m$, followed by hydrogenation resulted in a polymer with a T_g of 175°C (data not shown).

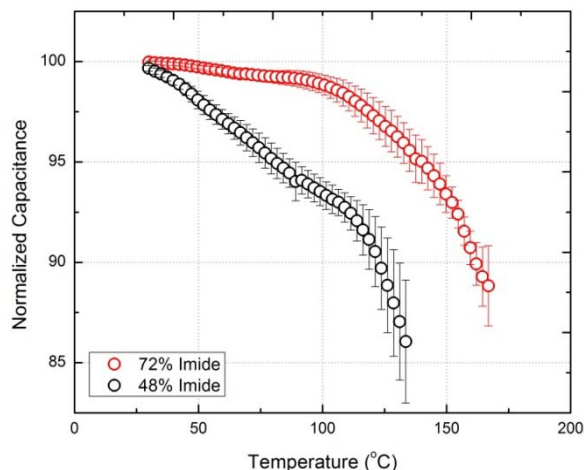


Figure II - 130: Average capacitor thermal performance $n = 5$ as a function of temperature.

Electrical characterization copolymer **2** where $n = 3m$, were performed as a function of frequency to determine what affect removal of the double bond had on the dissipation factor and dielectric constant. Removal of the double bond decreased the relative permittivity of the polymer but had little effect on the dissipation factor as shown in Figure II - 131.

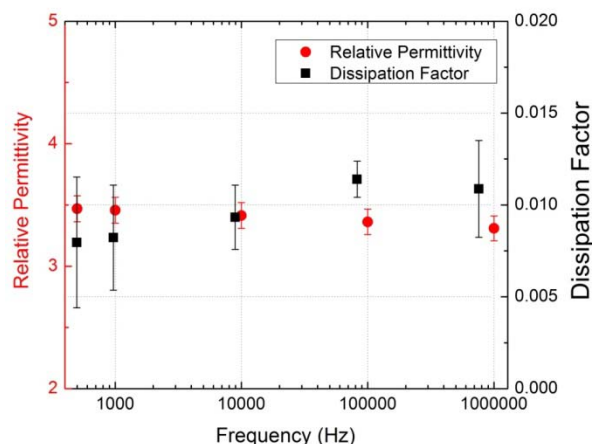


Figure II - 131: Dielectric properties as a function of frequency.

With initial electrical and thermal characterization in hand, the hydrogenated polymer synthesis was scaled-up and two kilograms of material were synthesized. One kilogram of dielectric was delivered to Dr. Collin company for extrusion experiments. The film is shown in Figure II - 132 as the material exits from the extrusion apparatus.



Figure II - 132: Sandia developed high temperature dielectric material extruded at Dr. Collin company.

The first run of dielectric material extruded at Dr. Collin company was brittle. Polymer dielectric films as thin as $12\ \mu\text{m}$ were produced without plasticizer. Initial attempts to minimize brittleness and lower the modulus of the dielectric film using plasticizer were successful. Polyethylene glycol (PEG, $M_w = 1000$) was selected (based on solvent casting experiments) as a plasticizer to be used during the extrusion process. The incorporation of the plasticizer enabled the extrusion of films as thin as $3\ \mu\text{m}$ thick. The use of the plasticizer enabled the extrusion of a roll of thin polymer dielectric as long as 100 m in length which was one of the FY12 critical deliverable/milestones.

3.0 Plasticizer evaluation to improve materials properties of extruded dielectric

While PEG enabled the extrusion of a 100 m long spool of polymer dielectric film, a consequence was a reduction in the ceiling operating temperature of capacitors. The plasticizer served to lower the T_g of the final material below 150°C (data not shown) which was undesirable for the final capacitor. In order to increase the T_g of the final dielectric, we evaluated several additional plasticizers including Terathane® which is a poly(tetrahydrofuran) as well as trioctyl trimellitate. We evaluated several molecular weights of Terathane® including 600, 1400, and 2900. Each plasticizer was loaded into the polymer at three loading levels including 5, 12, and 20% (w/w). The DSC traces for each loading level are shown in Figure II - 133. All loading levels of the lowest molecular weight Terathane® decreased the T_g of the final dielectric to temperatures close to or below 150°C (Figure II - 133A). Intermediate and the

highest molecular weight Terathane® decreased the T_g of the dielectric material slightly (Figure II - 133B and Figure II - 133C respectively). Trioctyltrimellitate

performed the best as it did not lower the T_g of the dielectric sufficiently.

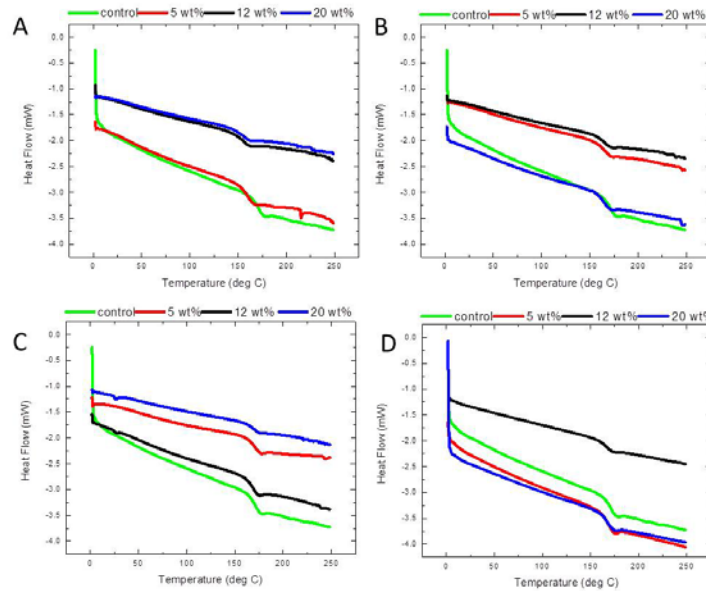


Figure II - 133: DSC curves for A) Terathane (650 mw), B) Terathane (1400 mw), C) Terathane (2900 mw), and D) trioctyl trimellitate.

Stress-strain data was collected on each of the polymer blends containing plasticizers. The individual stress-strain curves are shown in Figure II - 134. All polymer blend yield points were compared to a commonly

used polyester which had a yield point at 0.04 strain. The polymer blend with the highest strain at yield point was a polymer filled with trioctyl trimellitate.

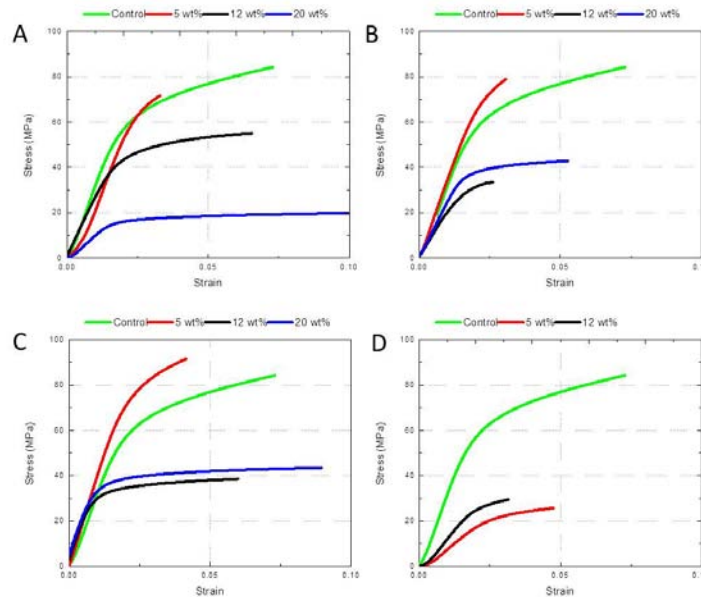


Figure II - 134: Stress-strain curves for thin films of A) Terathane (650 mw), B) Terathane (1400 mw), C) Terathane (2900 mw), and D) trioctyl trimellitate.

Dielectric breakdown data was also collected on the Terathane loaded blends. Polymer films were prepared using a solvent casting technique and as a result all polymer films were very thick with thicknesses close to 20

µm. Dielectric films were metalized with gold which was applied using sputter coating. In all cases the breakdown strength of the blends was higher than that of the pure high temperature dielectric. In the best case the breakdown

strength increased by over 150 V/ μm . All breakdown data are shown in Figure II - 135.

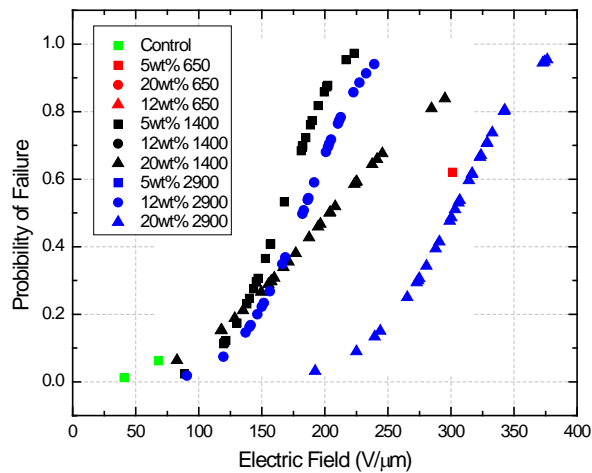


Figure II - 135: Dielectric breakdown strength of thick films of high temperature dielectric Terathane®.

4.0 Stacked Capacitor Fabrication and Characterization

Multilayer stacked capacitor formation has been demonstrated previously by using a hot press technique where the polymer dielectric ($n = 3$, $\sim 12 \mu\text{m}$) was layered iteratively with discrete Al layers ($4 \mu\text{m}$ thick). A schematic of the process is shown in Figure II - 136.

Heat was applied to raise the temperature of the polymer above the polymers T_g while applying a load of 500-1000 lbs. Dozens of capacitors were fabricated using the discrete Al/polymer dielectric configuration to confirm the viability of this technique. Capacitors fabricated using this technique had capacitances ranging from 2 to 16 nF. Device yield was only $\sim 50\%$ using the hot-press combined with discrete Al layers so two layers of polymer dielectric were used for a total of $24 \mu\text{m}$ thick dielectric layer, which greatly exceeds the DOE OVT program goals, but still provides a demonstration of capacitor fabrication.

FY12 included the fabrication of several large capacitors with the largest unpackaged capacitor having a capacitance of close to $5 \mu\text{F}$. Two larger capacitors ($\sim 0.5 \mu\text{F}$) were fabricated in-house using the layering technique. Discrete aluminum foil was used as the metal layer ($4 \mu\text{m}$ thick). Two layers of polymer dielectric ($\sim 12 \mu\text{m}$ thick) were used to minimize the possibility of film defect causing a short. Total film length used to fabricate the two capacitors was $\sim 110 \text{ m}$ in length. In the case of the in-house fabricated stacked capacitors, films were produced using a drawdown-based solvent casting technique. The capacitors were initially end capped using a conductive epoxy (silver loaded epoxy). The epoxy was smoothed and Babbitt was applied which enabled a SnCu lead to be soldered to the capacitor. Finally the capacitors were potted using a two part epoxy system. Images of the

capacitors prior to potting are shown in Figure II - 136A and potted capacitors are shown in Figure II - 136B.

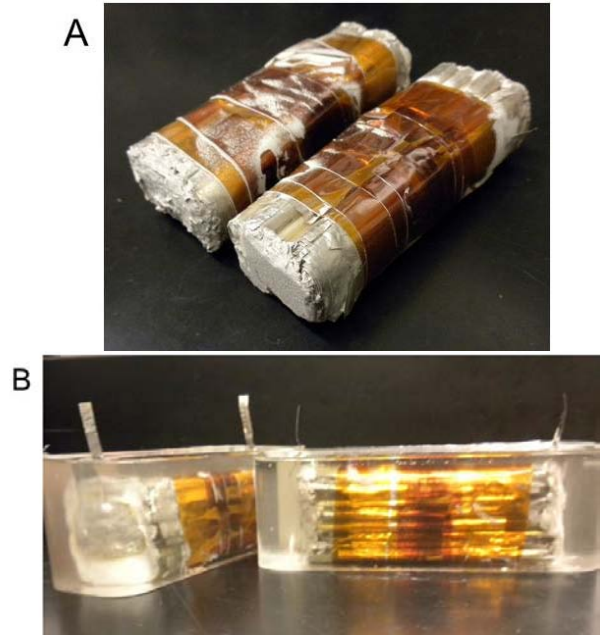


Figure II - 136: A) Capacitors which have been thermal sprayed with Babbitt to make end contacts and B) potted capacitors with SnCu leads.

Electrical characterization of the capacitors was performed prior to potting to determine the capacitance and dissipation factor as a function of frequency. The capacitance was under 500 nF; however, if pressure was applied to the face of the capacitor the capacitance would increase to over 500 nF indicating that the stacked capacitor fabrication method included void volumes filled with air. The potting process replaced the air voids with epoxy. Improvements minimizing air voids should be realized as we move to roll-to-roll processing for the fabrication of the capacitors in FY13.

Work for FY13 will include the transition of the extrusion process developed at Dr. Collin Company to Sandia. Extruded material will be used to fabricate rolled capacitors using traditional winding processes. The fabricated capacitors will be thermal sprayed to create end terminations and packaged using high temperature packaging materials. The high temperature capacitors will be evaluated in house and sent to collaborators at Penn State, ORNL, Argonne National Laboratories and ECI for further evaluation. In addition, further improvements in the relative permittivity and breakdown strength will be gained by the incorporation of nanoparticles and a demonstration of extruded dielectric containing nanoparticles will be completed.

Conclusion

We have developed a novel polymeric material that has superior high temperature dielectric properties. We have

demonstrated the fabrication of extruded rolls of our polymer dielectric with lengths as long as 100 m. We have also demonstrated the extrusion of thin polymer films with thicknesses as thin as 3 μ m. in collaboration with the Dr. Collin company. FY12 included the fabrication of two larger value stacked capacitors (~0.5 μ F) and the electrical performance was characterized as a function of frequency prior to packaging. The capacitors were thermal sprayed with Babbitt which allowed soldering of end leads. The capacitors were finally potted in epoxy. Process details need to be optimized to exclude air which will further increase the capacitance. Work in FY13 will remain focused on the scale-up of both film and capacitor production. The extrusion process will be transferred to Sandia and capacitors will be fabricated using both traditional roll-to-roll processing and the extruded polymer film which will be produced in-house. Further research will be focused on the inclusion of inexpensive nanofiller additives to increase the final capacitor energy density. A demonstration of extruded polymer film containing nanoparticles will be demonstrated in FY13. The Sandia developed polymer film and nanofiller are critical components that should enable high temperature, thin film, polymer dielectrics which will be used to fabricate high temperature DC bus capacitors with significantly reduced size and weight, and improved performance and reliability.

Acknowledgements

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II.11 Glass Dielectrics for DC Bus Capacitors

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Objectives

Commercial capacitors for hybrid electric vehicles (HEVs) and plug-in hybrid electric vehicles (PHEVs) do not meet US automaker's specifications for high temperature operation, cost and reliability. The objectives of this project are to develop high temperature capacitors that go beyond what is commercially available and to eliminate costly coolant systems within the HEVs and PHEVs. Ceramic capacitors have excellent high temperature performance and meet a majority of HEV and PHEV specifications for power electronic converters; however, catastrophic failure modes and cost are primary impediments to their use in hybrid vehicles. The goal of this project is to produce reliable glass capacitors without compromising the energy density (related to capacitor volumetric efficiency). Specific goals include:

- Characterize fundamental electrical properties of flat panel display glass that are related to DC bus capacitor reliability and ultimately the cost and performance of power converters for HEVs.
- Collaborate with Sandia National Laboratory and Argonne National Laboratory to understand breakdown strength and reliability of materials underdevelopment for DC bus capacitors.
- Scale-up glass capacitor technology by teaming with glass manufacturers and capacitor companies.

Approach

There has been a substantial world-wide expansion in flat panel display glass over the past decade. This plentiful material has excellent high temperature electrical properties. To use glass capacitors in HEVs the following approach is taken:

- Characterize glass materials at high temperature to predict reliability in DC bus capacitors.

- Develop self-healing modes in glass to avoid catastrophic failure power converter operation.
- Manufacture prototype capacitors for HEVs in collaboration with industrial partners.

Major Accomplishments

- Demonstrated that flat panel display glass can operate as a capacitor material for energy efficient hybrid vehicles at high temperatures. High temperature components will allow vehicle designers to eliminate costly coolant loops in HEVs.
- Fabricated and tested the first prototype capacitor up to high temperature (150°C) made by winding a glass ribbon.
- NDA signed with Corning, a major US glass manufacturer.

Future Direction

- Highly Accelerated Life Testing (HALT) is an important area of future R&D efforts. In our discussions with automotive manufacturers, component reliability and cost are key parameters for implementation of any new capacitor technology into a hybrid electric vehicle.
- Penn State has been working with flat-panel display manufacturers to reduce the glass layer thickness. Currently 50 μm thick glass sheets are available and 10 μm thick sheets have been fabricated at the laboratory scale. The final design for a high-temperature DC bus capacitor will require glass layer thicknesses between 5 and 10 μm.



Technical Discussion

There is general agreement within the automotive and power electronic communities that revolutionary approaches, drawing on diverse disciplines, will be necessary to develop the next generation of power systems for electric vehicles. New active and passive components need to be developed and manufactured which can operate at high temperature for long periods of time. In addition, component miniaturization is important to reduce the total volume and cost of the power electronic circuitry on board an electric vehicle. A summary of the results of this study is shown in Figure II - 137.

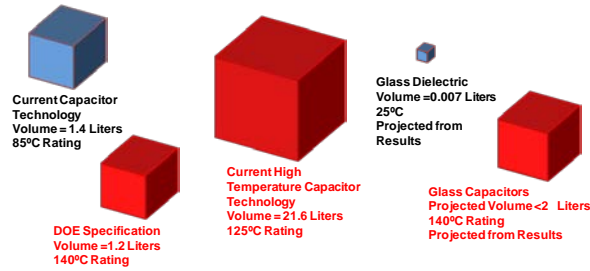


Figure II - 137: Volumetric comparison between DOE capacitor specifications, commercial capacitors and the projected capacitor volumes from the research at Penn State. All volumes shown are for a 1000 μ F and 1000 V capacitor.

The DOE specifications (Figure II - 137 lower left corner) were derived from discussions with the EE Tech Team and component manufacturers. Presently, high-temperature film capacitors (middle of Figure II - 137) have 18 times the volume of the DOE specification. The glass dielectrics explored in this study have the potential to operate above 140°C and the volume is much smaller than commercial high temperature capacitors (Figure II - 137 right side).

The key to the success of the glass capacitor is the excellent material performance. Table II - 7 shows a comparison between polypropylene and glass dielectrics. Polypropylene is the most common material that is currently used for DC bus capacitors. The dielectric permittivity of glass is three times higher than polypropylene which is important for capacitor miniaturization. The dielectric breakdown values, related to capacitor reliability, are similar between glass and polypropylene. The most important difference between polypropylene and glass is the temperature at which these materials either melt or transform. For polypropylene the melting temperature is 165°C and the glass material melts at much higher temperatures (>1000°C). The higher dielectric material temperatures translate to higher operating temperature for the DC bus capacitor. The final cost of the glass capacitor is still unknown because this electrical component is still in the development stages. It is anticipated that the overall material cost will be low for glass because this material is currently mass-produced for the flat panel display industry.

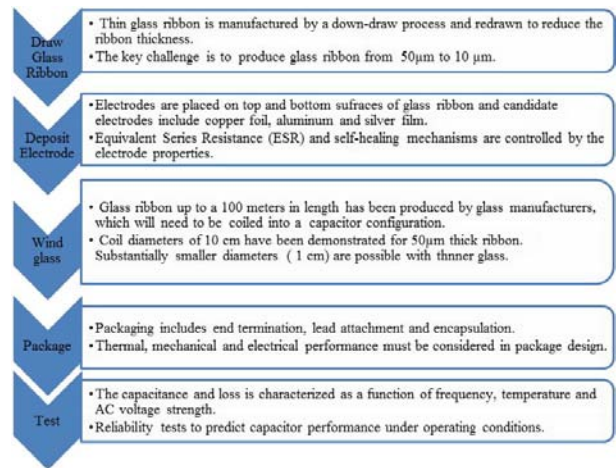
Table II - 7: Comparison of important materials for DC bus capacitors.

	Glass	Polypropylene
Minimum Thickness (μ m)	5	3
Annealing point/Tg °C	1225	165
Permittivity	6	2.2
AC loss	2×10^{-3}	2×10^{-4}
DC breakdown Strength	500 to 1000 V/ μ m	500 to 750 V/ μ m
AC breakdown Strength	200 V/ μ m	~200 V/ μ m
Cost	?	~\$10/lb [3 μ m, unmetallized]
Operation Temperature °C	300	105

Within the past year, Penn State has collaborated with NEG Corporation to manufacture the world’s first wound glass capacitor. The flow diagram for producing the coiled

glass capacitors is shown in Table II - 8. The fabrication process for the prototype capacitor begins with flexible glass ribbon (5 μ m to 50 μ m thick) and lengths of 3 m. Longer glass ribbons (100 meters) have also been produced by glass manufacturers. The glass surfaces are very smooth (RMS surface roughness values less than a nanometer) and the pristine glass has excellent mechanical properties. Previous reports have shown that a 5 μ m thick glass ribbon is able to be wrapped around the diameter of a pencil, which is important for coiled glass capacitor designs.

Table II - 8: Fabrication process for manufacturing DC bus capacitors.



After receiving the glass ribbon from the manufacturer, electrodes are placed on the both sides of the ribbon. Silver electrodes are deposited by spraying silver nanoparticles on the glass surface and no heat treatment is necessary to produce an electrode with low resistivity. The silver electrodes in this study have sheet resistances in the 10 Ω range, which is similar to evaporated aluminum resistances found for polypropylene capacitors. For large-scale production of glass capacitors, evaporated aluminum conductors will also be used for the conductor. Foil tabs are attached to the electrode along the length of the ribbon every 10 cm, so that the current paths are short. The electrode and tab configuration was designed to minimize the loss and equivalent series resistance.

Capacitor packaging is a critical step for meeting the demanding thermal, electrical and mechanical performance requirements of the capacitor for HEV applications. The glass ribbon is wrapped around the mullite mandrel which is a high temperature insulating material. After the winding step, a wire is attached to each of the conductor tabs and then terminated to the side of the capacitor. There are terminations on the top and the bottom of the capacitor. A high temperature capacitor was manufactured from flat-panel display glass and is shown in Figure II - 138. The specific conductor and winding configuration is shown in Figure II - 139. For the prototype capacitor, a spacer glass

layer is used to isolate the positive and negative sides of the conductor-coated glass layer.

The capacitor design was optimized for low equivalent series resistance, low inductance, and high temperature operation. The electrical properties (capacitance and loss) were characterized as a function of frequency and temperature with an Agilent impedance analyzer. High voltage properties were characterized with a high voltage power supply.

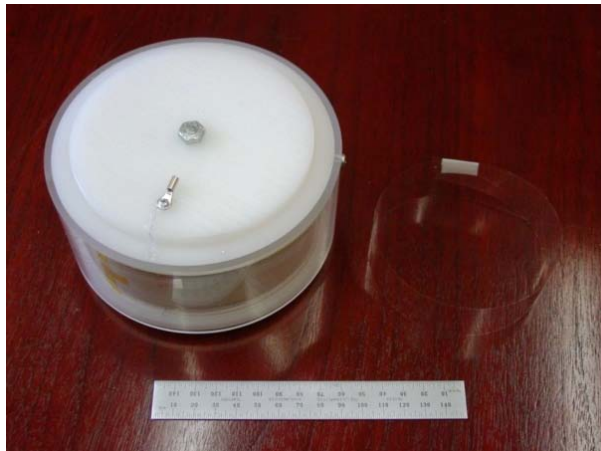


Figure II - 138: Top view of a functional DC bus capacitor (left side of figure) and a section of the wound glass ribbon (right side). Ribbon dimensions: 2.9 m long, 30 mm wide and 50 μm thick.

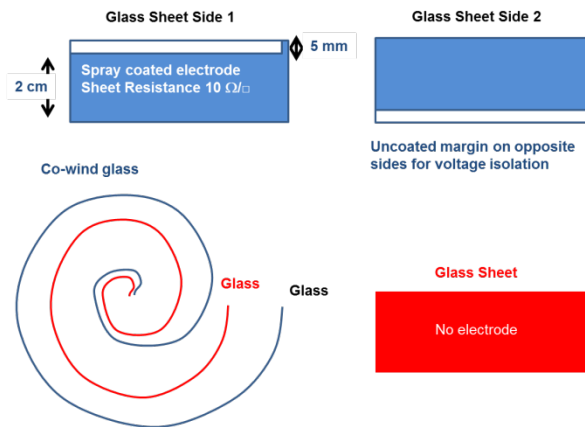
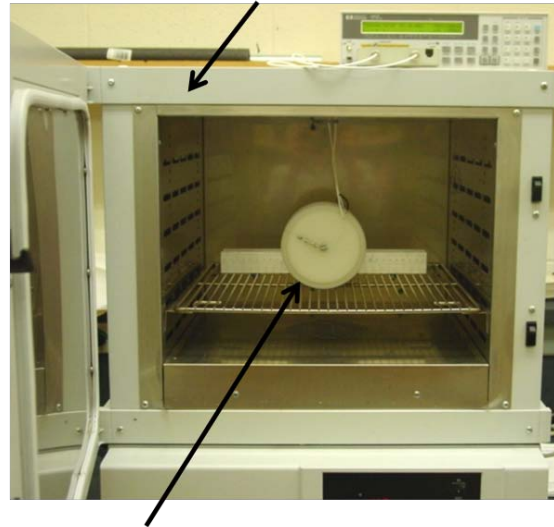


Figure II - 139: Winding configuration for a coiled glass capacitor.

The coiled glass capacitor is placed in an environmental chamber for testing at high temperature as shown in Figure II - 140. The temperature range explored is between room temperature and 150°C, which is a higher temperature than the DOE APEEM specifications of 140°C for a DC bus capacitor for an HEV power converter. The frequency range of interest was between 1 kHz and 10 kHz. The capacitor is a loss values did not change as a function of frequency or temperature. This capacitor performance was shown to be ideal for a DC bus capacitor that would operate in a switch mode power

supply with 10 kHz which frequency and without a coolant in the hybrid electric vehicle.

Environmental Chamber



Coiled Capacitor

Figure II - 140: AC capacitance testing of a coiled glass capacitor at temperatures up to 150°C.

Table II - 9: Performance of a Glass DC bus capacitor as a function of temperature and frequency.

Temperature	Frequency	Capacitance, nF	Loss
50°C	1 KHz	67.2	0.001
	10 KHz	67.1	0.002
100°C	1 KHz	67.6	0.004
	10 KHz	67.4	0.003
150°C	1 KHz	68.2	0.005
	10 KHz	67.9	0.003

High-voltage testing was also carried out on the coiled glass DC bus capacitor and the details of the test are shown in Figure II - 141.

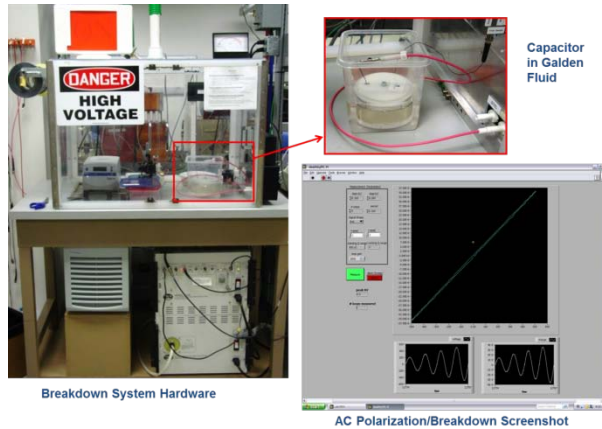


Figure II - 141: High voltage test of a coiled glass capacitor: the high-voltage test system that operates in DC air AC test mode with voltages as high as 30 KV (left side of figure), the capacitor was placed in an insulating dielectric fluid (upper right), the data readout showing the voltage waveform and integrated charge from the capacitor (lower right). The data show that this is a highly linear capacitor with very little loss up to voltages of 1000 Volts.

Conclusion

The outcome of this project is a cost effective process for manufacturing high temperature capacitors that will meet the US automaker performance specifications for HEV and PHEV applications. There are a number of glass manufacturers fabricating thin-ribbons that are flexible. Sufficient quantities of glass ribbon are now available for fabricating capacitors. Penn State has collaborated with a glass manufacturer (NEG) to investigate reliable prototype capacitors from glass-ceramic materials. Penn State has developed a polymer/glass composite laminate that promotes self-healing and this technology is currently being explored for large scale glass capacitors.

Thin glass sheet production has grown substantially because of strong demand from the flat panel display industry and a large investment in the development of new glass fabrication methods. Glass manufacturers have been able to develop a continuous sheet casting process with sufficient control to make significant lengths of thin flexible sheet. It is now possible to manufacture glass capacitors in a similar manner to polymer film capacitors that are presently used in hybrid electric vehicles. The manufacturing process is a major part of the component cost. The results of this study provide the demonstration that flat panel display glass is a viable material for high temperature DC bus capacitors for electric vehicles.

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Patents

1. M. Lanagan, N. Smith, H. Lee, C. Pantano, "Self-Healing High Energy Density Capacitors," Full patent submitted 2011.

II.12 Development of SiC Large Tapered Crystal Growth

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Objectives

- Demonstrate initial feasibility of totally new “Large Tapered Crystal” (LTC) approach for growing vastly improved large-diameter wide-band gap wafers.
- Open a new technology path to large-diameter SiC and GaN wafers with 1000-fold defect density improvement at 2-4 fold lower cost.

Approach

- Experimentally investigate and demonstrate the two key unproven LTC growth processes in SiC:
 - Laser-assisted growth of long SiC fiber seeds (Solvent-Laser Heated Floating Zone).
 - Radial epitaxial growth enlargement of seeds into large SiC boules.

Major Accomplishments

- 4-fold enlargement of SiC seed fiber crystal via radial CVD epitaxial growth.
 - Growth rates improved more than 2-fold (to ~ 180 $\mu\text{m}/\text{hour}$).
 - Crystal diameter enlargement to ~ 4 mm demonstrated.
 - X-ray defect characterization initiated.
- Development of hot-wall CVD process for realizing single-screw dislocation “hexacone” SiC seeds more suitable for well-ordered single-crystal fiber growth.
- Refining solvent fiber growth experiments using much smaller feed rods.
- Initiated laser-CVD fiber growth work via SBIR Phase III (Free Form Fibers, Inc., NASA funded).
- Replacement of failed of RF generator in NASA SiC CVD epitaxial growth system (NASA funded).

Future Direction

- Continue development of source material/feed rod compositions and processing for Solvent-LHFZ.
- Repair NASA SiC epitaxial growth system.
- Eliminate parasitic 3C-SiC from lateral CVD epitaxy by implementing coated graphite parts, improving temperature uniformity and altering gas phase chemistry.
- Carry out demonstration CVD growth of > 5mm diameter SiC boules.
 - Characterize to see if desired low-defect radial CVD growth is achieved.
- Grow larger fibers and boules fully demonstrating feasibility of LTC growth process.
- Launch joint development of full prototype LTC SiC growth system (simultaneous fiber growth + lateral growth to grow full prototype SiC boules) in collaboration with commercial and/or university development partners (FY14-15 - beyond current NASA/DOE agreement).
- Explore GaN LTC experiments. (FY15-16 - beyond current NASA/DOE agreement).

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Technical Discussion

Technical Motivation

It is generally accepted that the use of silicon carbide (SiC) power electronics could enable power systems that are significantly more efficient, lighter, and smaller than systems based on silicon (Si) electronics. Although some SiC devices (e.g., Schottky diodes and field-effect transistors (FETs)) have been developed, the energy-saving performance and reliability of SiC power devices are significantly degraded, and device cost significantly increased, because of a high density of dislocation defects (> 1000 per cm^2) in all commercially-available SiC semiconductor wafers. Eliminating these defects economically (i.e., down to densities < 1 per cm^2 while greatly lowering SiC wafer cost) would unlock SiC’s enormous (as yet unfulfilled) promise to revolutionize nearly all high-power electronic systems.

The reason for the high density of defects in commercial SiC wafers is that all current approaches for growing single-crystal SiC boules are fundamentally flawed. The problem with current SiC growth processes is that a high-density of screw dislocation defects (on the

order of 10^2 to 10^4 per cm^2) is necessary in order to achieve commercially viable SiC wafer growth rates. Unfortunately, many researchers (including NASA) have now shown that these same dislocation defects harm the yield, performance, reliability, and commercialization of SiC high power devices. If SiC is to fulfill its huge theoretical power device promise, SiC wafer dislocation densities must be brought down 100-1000 fold via a totally new crystal growth approach, yet be able to mass-produce larger-area wafers (at least 6-inches in diameter) at significantly lower cost.

Introduction to Large Tapered Crystal (LTC) Growth

A NASA Glenn Research Center (GRC) team (J. A. Powell, P. G. Neudeck, A. J. Trunek, D. J. Spry) recently patented (US Patent 7,449,065) a radically different SiC crystal growth concept that can mass-produce large-diameter SiC wafers wherein each wafer ideally contains only a single screw dislocation (in the center of the wafer). This new growth concept utilizes a revolutionary seed crystal configuration and two simultaneous growth processes in connected chambers for rapidly growing large single-crystal SiC boules with only one centrally-located screw dislocation (SD). Because this new process grows a large crystal with a tapered shape, we have named this the Large Tapered Crystal (LTC) growth process. The crystal growth initiates from a small-diameter fiber (with a single screw dislocation at its core) that is grown in a first chamber, from which it is withdrawn, as it elongates, into a second growth chamber where radial growth on the fiber produces a large tapered crystal. Each growth run produces a low-defect (ideally with a single screw dislocation) SiC crystal boule (100 mm diam.) at the top end of the LTC. A comprehensive technical description of the process and apparatus involved can be found in US Patent 7,449,065 that is now available online at the U.S. Patent Office website <http://www.uspto.gov>. This section presents a highly condensed summary of the contents of the patent.

Figure II - 142 illustrates schematic cross-sections of SiC crystals during steps S1, S2, and S3 of the LTC growth process. Each LTC growth cycle (except the very first cycle, as described in US Patent 7,449,065) starts with an LTC as the seed crystal as shown in Figure II - 142(a). The central axis of the LTC seed will be parallel to the crystallographic c-axis. During growth step S1, the small end (the fiber portion in chamber 1), as shown in Figure II - 142(b), will be grown in the c-direction and maintained at a diameter of less than 1 mm; the large end of the LTC will be maintained at some designated large diameter (e.g., 100 mm for commercial systems). Simultaneously with the axial growth of the small-diameter fiber in chamber 1, radial epitaxial growth enlargement of the large tapered section takes place in a growth chamber 2 during a growth step S2. Ideally, only a single screw dislocation (along the central axis) will be

present in the entire crystal. This single screw dislocation provides the necessary crystal stacking sequence for a given SiC polytype. This stacking sequence also establishes the sequence of atomic steps that propagate radially during growth in chamber 2. It is important to note that defects (i.e., screw dislocations) are not required for the radial growth in chamber 2. Indeed, the bulk of the crystal boule (except for the very small volume of the central fiber) is deposited by “step-flow growth” in chamber 2 (utilizing the crystal stacking sequence established by the small-diameter fiber).

Typically, the vertical growth rate parallel to the c-axis (on the small tip) will be much greater (e.g., the order of 1 mm/hour) than the radial epitaxial growth rate. Because of the large surface area of the tapered portion, moderate radial growth rates (e.g., about 0.1 mm/hour) will yield rapid bulk growth of the LTC in chamber 2. As growth proceeds in steps S1 and S2, the top of the tapered crystal enters an isothermal chamber 3 of inert gas atmosphere where no additional SiC is deposited. This enables a cylindrical (hexagonal cross-section) crystal boule to form as the large end continues to exit chamber 2 into the “no-growth” isothermal chamber 3. The top of the crystal is physically moved upward during growth steps S1 and S2 so that the bottom of the downward-growing small-diameter tip is maintained at the same position inside chamber 1.

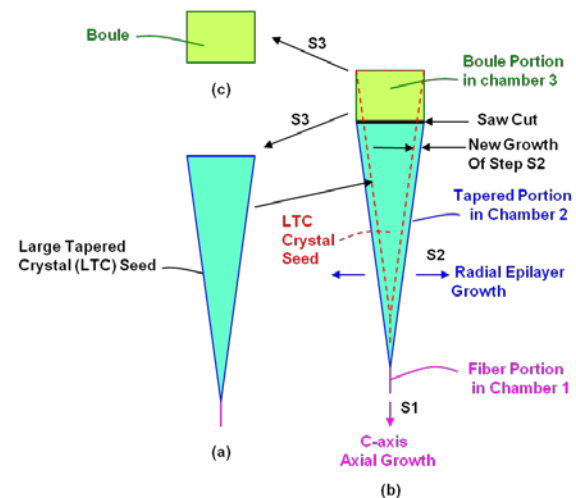


Figure II - 142: LTC Growth Process.

At the end of each growth cycle, the boule portion will be cut from the whole crystal in step S3 (Figure II - 142c), and the remainder of the LTC crystal will be used as a seed crystal in steps S1 and S2 of a subsequent growth cycle. Additional advantages of the LTC process are that boules can be grown at high growth rates and the process can easily be scaled up to larger diameter boules, resulting in increased wafer size and reduced wafer cost. Also, the process should be capable of boules of much greater length than is possible with current

SiC growth techniques. As noted in US Patent 7,449,065, only the very first LTC seed crystal will need to be grown in a preliminary and separate process from the LTC process cycle depicted in Figure II - 142.

The LTC growth process as presented above relies on two separate high-quality SiC growth processes taking place on different surfaces/regions of the same crystal, namely (S1) c-axis fiber growth and (S2) radial epilayer growth. Neither of these processes has been experimentally attempted or demonstrated for SiC in the manner/configuration that is proposed above. Therefore, the critical first objectives of this work is to separately demonstrate, for the first time, that both of these two new SiC growth processes can be successfully carried out.

SiC Radial Growth via CVD Epitaxy

The vast majority of the LTC boule will be formed by epitaxial radial growth on the seed fiber via CVD during step S2 (in chamber 2, Figure II - 142b). As the small diameter fiber expands, the LTC boule is expected to evolve towards a hexagonal cross-section whose outer surfaces will be “m-planes”. Maintaining commercially viable radial growth rates (on the order of 50-100 $\mu\text{m}/\text{hour}$) are essential to the LTC process. **However, the most fundamental question to be addressed by this early stage of research is to determine if the radial epitaxial growth expansion of a fiber introduces additional crystalline defects.** Previous efforts to grow in the (radial) a-direction by sublimation growth resulted in increasing stacking fault density [1], but these previous studies grew crystals in environments of much higher temperatures and stress (thermal and seed-mounting) than is proposed for the LTC process. At this time, there is no known source of high-quality single crystal SiC small-diameter fibers to use as seeds for experimental investigation of the radial expansion epitaxy of the LTC process. Therefore, the initial development experiments of the radial growth process have been conducted on simulated “pseudo-fiber” SiC crystals prepared from commercially purchased wafers and saw-cut into long rectangular fiber-like shape with both “a-face” and “m-face” radial growth surfaces (Figure II - 143). These pseudo-fibers are far from ideal in terms of their defect content and growth surface quality.

All growth experiments related to lateral expansion and SD isolation were performed in the horizontal flow hot wall CVD reactor that was constructed during the first year of DOE funding and has subsequently been modified this past year to allow for automated temperature measurement of the growth hot-zone by optical pyrometry.

Additionally, a new RF-generator (at cost of \$50K funded by NASA) replaced the 17-year old RF-generator that failed catastrophically in 2011 causing a 6-month delay to experimental work. The new generators are capable of being correctly tuned to enable uniform and stable heating of the hot-wall reactor. The reactor is capable of operating at temperatures in excess of

1700°C while flowing H_2 , SiH_4 , C_3H_8 and HCl at sub-atmospheric pressures.

Prior to initiating radial epitaxial growth, each SiC pseudo-fiber seed crystal is subjected to an aggressive in-situ high temperature ($> 1600^\circ\text{C}$) etch in HCl in the epitaxial growth reactor. The purpose of this etch is to remove some of the seed crystal surface that has been damaged by the saw-cut process. During this etch, enough crystal is removed from the pseudo-fiber seed that its shape becomes more of a rounded “sliver” as shown in Figure II - 144a. Figure II - 144b shows the pseudo-fiber seed sliver following radial epitaxial growth for 8.5 hours over two runs. The topmost region of this crystal (i.e., highest in the CVD reactor gas stream farthest away from the carrier mounting hole) expanded to a diameter of $\sim 2\text{mm}$ via radial CVD SiC growth. The crystal cross-section has evolved into a hexagonal shape, consistent with the hexagonal crystal structure of SiC. The hexagonal flat top of this crystal is believed related to fact that the pointed seed sliver tip did not contain a screw dislocation to enable further upward growth of the crystal in the c-axis direction. Yellow crystals of polycrystalline 3C-SiC formed near the base of the sliver in regions where the sliver was near or in contact with the carrier. Future efforts will require improved mounting methods to suppress the formation of 3C. Analysis by x-ray topography (Figure II - 144c) indicates that the seed polytype was successfully reproduced in the radial epilayer and the crystal is free of long grain strain. The growth time was 8.5 hours over two runs, so that the radial growth rate at the tip of the sliver is calculated to be almost $120\mu\text{m}/\text{hour}$. It is important to note that even though the crystal has formed a hexagonal shape with m-plane facets, the radial growth rate was well above the minimum growth rate of $50\mu\text{m}/\text{hr}$ for envisioned for commercial viability of the LTC process.

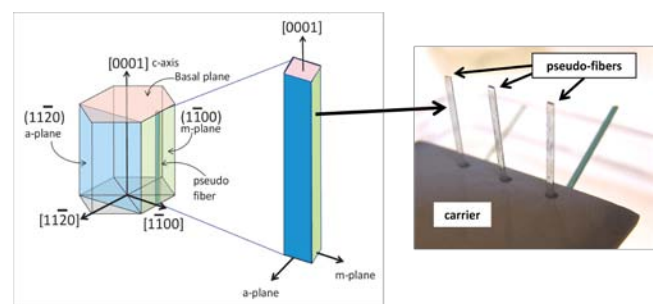


Figure II - 143: Illustration of “pseudo-fibers” used as imperfect seeds for initial experimental demonstrations of radial epitaxial growth. The pseudo-fibers are saw-cut from commercially purchased SiC a-plane or m-plane wafers forming long rectangular seed crystals. These are then mounted into an upright position for exposure to flowing CVD gas precursors using holes drilled in a graphite carrier.

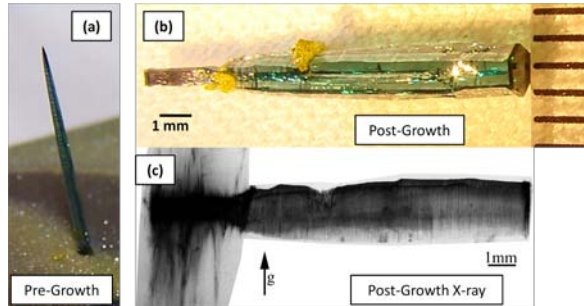


Figure II - 144: (a) SiC needle-like shaped sliver crystal protruding from graphite sample carrier following a high temperature HCl etch to remove saw-cut damage from the seed prior to initiating radial epitaxial growth (b) The same crystal following 8 hours of CVD epitaxial growth has laterally enlarged the sliver to ~2mm in diameter. As expected, the grown crystal evolved hexagonal crystal facets consistent with hexagonal SiC unit cell crystal structure. Some parasitic (yellow) 3C-SiC contamination is observed near where the crystal base mounted into the carrier. (c) A transmission X-ray topographic image of the grown crystal. The growth is homoepitaxial, and is free of long grain strain for regions away from the carrier.

Figure II - 145 illustrates the largest radially-grown SiC crystal we have experimentally produced to date. Yellow crystals of polycrystalline cubic (3C) SiC formed extensively at the base of this crystal where the sliver was in direct contact with the carrier. For regions away from the carrier where hexagonal SiC was grown, growth enlargement to a diameter of ~4mm was achieved. Indeed, the top of the sliver (furthest from the carrier) has evolved into a smooth tapered hexagonal shape as desired/envisioned for the fully-developed LTC process. It is hypothesized (but not yet confirmed) that screw dislocations near the tip of the crystal are driving growth along the c-axis direction (in addition to non-dislocation-assisted radial a- and m- growth directions). Closer to the carrier however, the main body of the crystal (i.e., region of thickest hexagonal polytype growth) still contains grooves running along the sides of the crystal. These grooves are believed to be an artifact of incomplete transition of the rounded rectangular initial growth seed cross-sectional shape at the start of radial growth towards equilibrium hexagonal crystal structure cross-section. With further “clean” (i.e., free of 3C-SiC nucleation) growth, growth fronts are expected to merge forming hexagonal crystal cross-section without grooves. Demonstration of increasingly larger-diameter radially grown “mini-boules” is planned for FY2013, including meeting the DOE/NASA agreement milestone of a 5 mm diameter demonstration crystal.

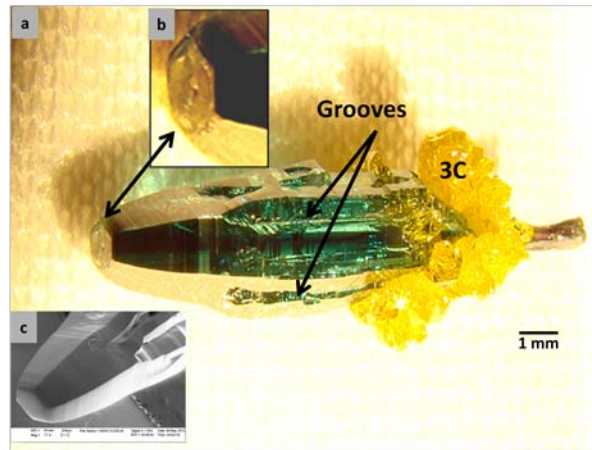


Figure II - 145: Optical (a, b) and (c) SEM images of ~4mm diameter “mini-boule” crystal produced via CVD radial epitaxial growth expansion from an imperfect “pseudo-fiber” seed. The left portion of the crystal features smooth tapered hexagonal growth facets desired for the LTC growth process. These grooves are believed to be an artifact of incomplete transition from rectangular initial growth seed cross-section towards equilibrium hexagonal crystal structure cross-section. Undesired abundance of yellow parasitic 3C-SiC nucleation is evident on the right side and occurred where seed fiber was mounted into the graphite carrier.

The “mini-boule” shown in Figure II - 145 was saw-cut into sections and polished (a challenging and time-consuming process given the small sample size) in order to carry out X-ray topographic studies of its defect content. Two transmission X-ray topographs recorded from one of these polished section are shown in Figure II - 146. It is important to note that this particular section of the crystal was at/near the carrier mounting hole where significant parasitic 3C-SiC deposition occurred. Some of the “grooved” region evident in Figure II - 145a is also captured in the Figure II - 146 images, but none of the “tapered facet” region was in this crystal section. The 11-00 (Figure II - 146a) and 0006 (Figure II - 146b) topographs selectively image only hexagonal polytype crystal, as 3C polytype crystal is excluded from these imaging conditions. A number of linear contrast features running vertically (i.e., parallel to $\langle 0001 \rangle$) in Figure II - 146a could be dislocation defects residing in the (0001) basal plane. However, the vast majority of these contrast features appear to originate in the darkest (i.e., most defective) horizontal center region of the crystal, which was the original seed sliver. With basal-plane defect contrast mostly suppressed by Figure II - 146b X-ray imaging condition, most of the defect contrast in the radial epilayer vanishes, and a micropipe becomes evident (running horizontal in Figure II - 146b) along the core of the original seed sliver.

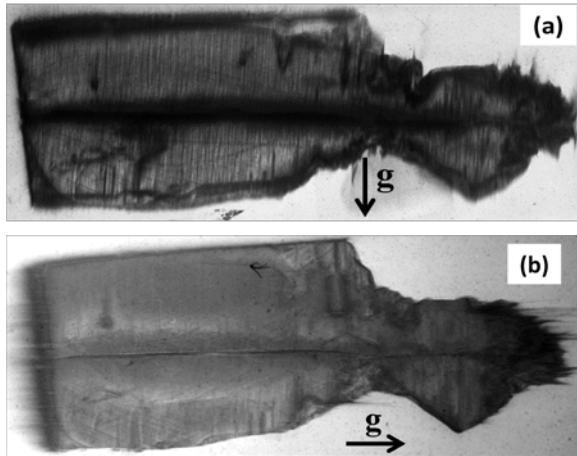


Figure II - 146: X-ray transmission topographs of a portion (sectioned and polished) of the crystal shown in Figure II - 145. The portion that was imaged is at/near the carrier attach point including some of the grooved section. (a) 11-00 imaging condition (b) 0006 imaging condition. Synchrotron White-Beam X-ray Topography (SWBXT) was carried out under subcontract by Stony Brook University using Brookhaven National Laboratory facilities.

Much further study into defect structure (and possible defect formation mechanisms) of this crystal as well as additional (larger-diameter) radially grown crystals are planned for the coming year. In particular, it is vital to determine if the radial epitaxial growth expansion intrinsically introduces additional crystalline defects. While some progress can be made with existing poor-quality pseudo-fiber seed crystals, it is imperative that higher quality SiC seed fibers become available. In addition to the high defect content of the pseudo-fiber seeds, the cross-sectional shape evolution (from rectangle to hexagon) is not consistent with envisioned LTC (wherein initial fiber starts with equilibrium hexagonal cross-section).

Fiber Growth via Solvent-Laser Heated Floating zone (Solvent-LHFZ)

Towards the end of realizing the needed high-quality single-crystal fiber of the LTC process, the Solvent-Laser Heated Floating Zone (solvent-LHFZ) growth technique is being developed. As previously reported (in the 2011 Annual Report for this task) solvent-LHFZ has grown single-crystal SiC epilayers on seed crystals, but has not yet produced high quality long single crystal fiber. These layers have been grown on the end of the same “pseudo-fiber” seed crystals that have been used for radial CVD experiments (described in the previous section and Figure II - 143). The small end of these that is dipped into the melt for growth is roughly (within 10°) the C face (000-1) of the cut crystal. Figure II - 147 shows the resulting growth front on the C-face seed crystal is comprised of many small hexagonal features that are in fact small individual growth fronts. This C-face growth surface contains many screw dislocations and therefore

many growth fronts are expected at the start of layer deposition. As growth proceeds, these small growth fronts collide trapping solvent rich material in the crystal, which in turn create additional defects. The undesirable compounding of defects nucleating from such a chaotic growth surface precludes the ability to grow a long single crystal fiber of acceptable high quality needed to realize LTC.

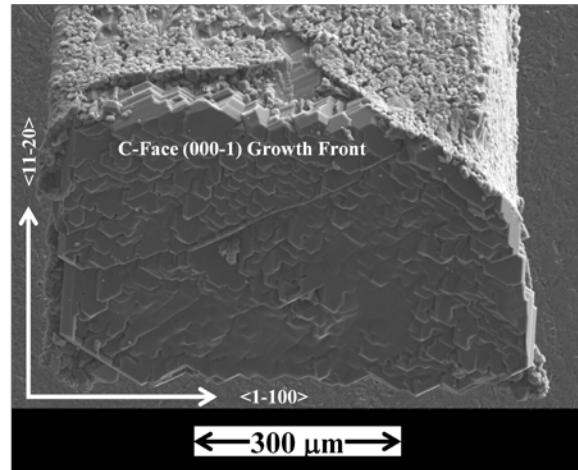


Figure II - 147: Scanning Electron Microscope image of (000-1) SiC surface produced by Solvent-LHFZ growth carried out on end of SiC pseudo-fiber. The surface is chaotic exhibiting 100s of hexagonally-faceted defect-assisted growth domains, some of which initiated at screw dislocations in the initial (poor-quality) seed sliver. As various growth domains merge, additional defects are undesirably formed, including voids that trap Fe-rich solvent into the crystal.

In order to grow a high-quality single crystal fiber, a seed crystal with a single dominant well-ordered growth front is needed. Figure II - 148 shows an example of such a seed crystal that we have recently (after considerable time and effort) produced. We refer to this as a faceted “hexacone” SiC seed crystal. These hexacone seed crystals are produced via hot-wall CVD epitaxy carried out on patterned mesas lithographically dry-etched into SiC wafer substrates. The pointed peak feature is the result of desired and well-ordered defect-assisted CVD growth at a single dominant screw dislocation. **A key technical challenge of upcoming experimental work is to seed Solvent-LHFZ growth using this pointed hexacone SiC crystal, and maintain this well-ordered growth front as the crystal is grown into an ever-longer fiber.**

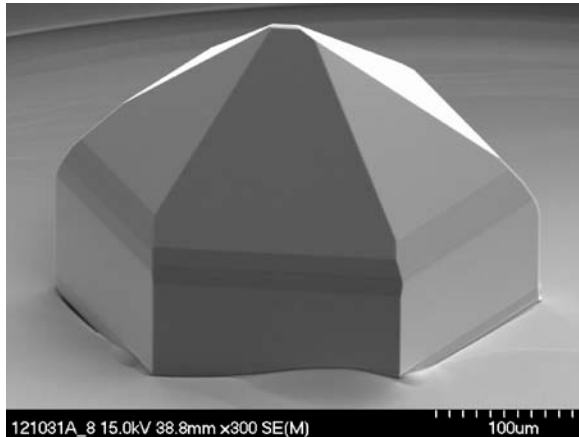


Figure II - 148: 4H-SiC "hexacone" seed crystal grown via hot-wall CVD epitaxy on dry-etched patterned 4H-SiC substrate. This seed is intended to promote single-domain fiber/layer growth driven by a single screw dislocation at the hexacone peak.

Some non-trivial engineering/equipment challenges need to be tackled in order to accomplish such experiments. For starters, it is far from trivial to hold and position small SiC substrates with hexacone seeds in a thermally stressed environment for dipping into the laser-heated melt. Another major challenge is that the diameter of the feed rod used as crystal growth source material for solvent-LHFZ needs to be reduced. In a review of optical floating zone techniques by Felgelson [2] the ratio of radius of the seed crystal to radius of the feed rod ($R_{\text{seed crystal}}/R_{\text{feed rod}}$) conducive to growth of fibers (larger than 0.1 mm diameter) is greater than 1/3. Since this ratio has been undesirably less than 1/4 in our early solvent-LHFZ experiments, smaller-diameter feed rods need to be implemented. Unfortunately, the past methods of pressing and sintering powers is limited to producing feeds rods of ~2 mm or greater in diameter. Therefore, chemical vapor deposition grown polycrystalline SiC rods, of diameters of 1 mm and 0.5 mm, have been purchased as the base material for the next generation of feed rods. Experiments are under way to see if Fe can be incorporated into the SiC rods in order to create the necessary Fe:Si:C ratio needed to grow SiC. Figure II - 149 shows an example of an initial polycrystalline-SiC feed rod refinement experiment. In this experiment, Fe powder was adhered to the outside of polycrystalline-SiC rod and the laser was used to heat the system. As temperature increased the Fe dissolved the SiC rod forming the melt visible in the figure. The seed crystal was brought down from the top and penetrated the liquid. This experiment demonstrated the ability to create a stable melt (a positive first step) but did not produce acceptable wetting of the SiC seed crystal and/or SiC growth. Furthermore, the method by which the melt was formed (heating Fe powder glued to the outside of the polycrystalline -SiC rod) is a crude method and difficult to control/reproduce results. Therefore, a significant amount of work remains to create acceptable feed rods at a

diameter of 1 mm or less with a proper balance of Fe:Si:C composition.

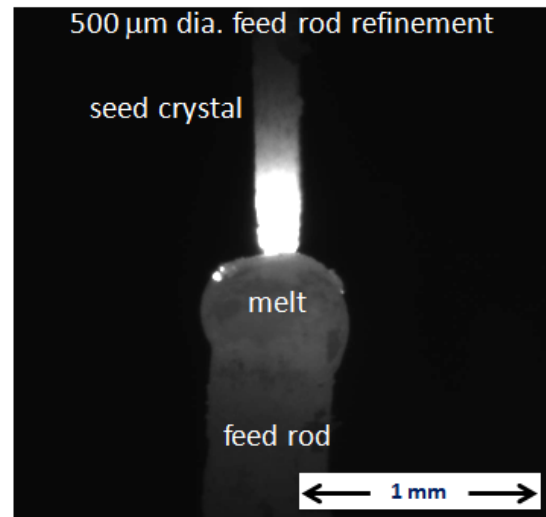


Figure II - 149: Long-range optical microscope image of an initial CVD-SiC smaller-diameter feed rod wetting experiment under laser-heating in the Solvent-LHFZ growth system.

Fiber Growth via Laser-Assisted CVD (NASA-funded SBIR Phase III)

Since the inception of the LTC growth process for SiC, it has been understood that successfully implementing single-crystal 4H-SiC fiber growth would likely prove the most difficult and challenging technical advancement. Thus, when additional NASA Glenn funds became available in April of 2012 to augment continuing (Dept. of Energy funded) LTC development efforts, a parallel technical path towards realizing 4H-SiC fiber growth was initiated. This path is being pursued via SBIR contract with Free Form Fibers, Inc. in Saratoga Springs New York that specializes (and holds patents) in laser patterned CVD growth of ceramics (including polycrystalline SiC). Work initiated in June and as of this writing (Nov. 2012) the company has almost completed modifications to one of its fiber growth systems in preparation for its attempts to laser-CVD grow single-crystal 4H-SiC fibers consistent with the LTC process.

Conclusion

If successfully implemented, Large Tapered Crystal (LTC) boules promise to greatly improve the cost and quality of wide bandgap wafers that will become the basis for realizing much more advanced high-power semiconductor switches. These devices in turn offer high-impact benefits to power conversion/management systems including utility power transmission and electric/hybrid vehicles.

Over the past year NASA Glenn has continued experimental studies of the two critical (previously un-

attempted) “fiber” and “radial” growth processes needed to realize Large Tapered Crystal (LTC) SiC boules. Significant understanding was gained and progress made toward project technical goals, including demonstration of a 4 mm diameter “mini-boule” via radial epitaxial expansion at commercially viable growth rates > 100 $\mu\text{m}/\text{hour}$. However, it will still be highly challenging to successfully complete all LTC feasibility demonstration goals/milestones during FY 2013. In particular, the “fiber growth” process is proving particularly challenging. Therefore, while work continues on developing laser-assisted solvent-based fiber growth at NASA Glenn, development of an alternative (parallel) technical approach for realizing single-crystal fiber growth has been initiated via NASA-funded SBIR Phase III.

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2. A.J. Trunek, P.G. Neudeck, A.A. Woodworth, J. A. Powell, D.J. Spry, B. Raghochamachar, and M. Dudley, Lateral Growth Expansion of 4H/6H-SiC a/m-plane Pseudo Fiber Crystals by Hot Wall CVD Epitaxy, *Materials Science Forum*, vol. 717-720, pp. 33-36, (2012).
3. A. Woodworth, P. G. Neudeck, and A. Sayir, A New Method to Grow SiC: Solvent-Laser Heated Floating Zone, presented at The 6th International Symposium on Advanced Science and Technology of Silicon Materials (JSPS Si Symposium), Nov. 19-23, 2012, Kona, Hawaii, USA

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1. Takahashi & Ohtani, *Phys. Stat. Solidi B*, vol. 202, p. 163 (1997).
2. R.S. Feigelson, *Journal of Crystal Growth* 79 (1), 669 (1986).

Patents

1. None this period. This project is based upon development of US Patent 7,449,065 Awarded 11 November 2008.

II.13 Electrical and Thermal Characterization, Modeling, and Reliability Simulation of Power Semiconductor Modules in Advanced Plug-in Hybrid Electric Vehicle Power Conditioning Systems and Motor Drives

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Objectives

The objective is to provide the theoretical foundation, measurement methods, data, and simulation models necessary to optimize power modules' electrical, thermal, and reliability performance for Advanced Plug-in Hybrid Electric Vehicle Power Conditioning Systems and Motor Drives.

Approach

- Develop dynamic electro-thermal Saber models, perform parameter extractions, and demonstrate validity of models for:
 - Silicon IGBTs and PiN Diodes
 - Silicon MOSFETs and CoolMOSFETs
 - SiC Junction Barrier Schottky (JBS) Diodes
- Develop thermal network component models and validate models using transient thermal imaging (TTI) and high speed temperature sensitive parameter (TSP) measurement.
- Develop thermal-mechanical degradation models and extract model parameters using accelerated stress and monitoring:
 - Stress types include thermal cycling, thermal shock, power cycling
 - Degradation monitoring includes TTI, TSP, X-Ray, C-SAM, etc.

Major Accomplishments

- In previous year (FY12), this project developed and validated models needed for this year's (FY13) and proposed next year's (FY14) simulations including:
 - dynamic electro-thermal semiconductor device models for Silicon IGBTs, Silicon PiN Diodes, Silicon MOSFETs, Silicon CoolMOSFETs and SiC Junction Barrier Schottky (JBS) Diodes
 - thermal network component package models for the Delphi Viper double-sided cooling power module and Virginia Tech soft switching power module

FY13 Accomplishments include:

- Used electro-thermal-mechanical simulations to evaluate thermal stresses in Delphi Viper double-sided cooling power module for nominal and fault operating conditions. This included extending the IGBT model to represent fault current and temperature conditions.
- Developed thermal-network-component models for representative cooling systems with NREL
- Used simulations to evaluate thermal stresses at module interfaces for Virginia Tech soft switching power module.
- Included liquid- and air-cooling thermal network component models in electro-thermal simulations of vehicle inverters.
- Performed thermal cycling, thermal shock, and power cycling degradation to characterize mechanical reliability properties of representative Virginia Tech modules. The module reliability characterization results are used to determine parameters for physics-of-failure models. The physics-of-failure models are then used to simulate damage and evaluate impact on Virginia Tech module life for vehicle driving cycle conditions.
- Extended NIST transient temperature measurements system (TSP) to include new thermal cross-coupling characterization capability needed for modules containing multiple temperature-dependent devices. Used the new system to perform cross-coupling thermal resistance measurements on Virginia Tech

modules and validated the cross-coupling performance of the thermal network component model for this module.

- Performed electrical short-circuit stress tests on Viper module to emulate possible fault conditions at various voltages, gate-drive conditions, and initial-condition temperatures.

Future Direction

- Calculate increase in thermal resistance at interfaces in Virginia Tech module due to thermal cycling damage and use changing thermal resistance in the thermal network during simulations (full electro-thermal-mechanical simulations).
- Develop electro-thermal models for advanced semiconductor devices including SiC MOSFETs, SiC JFETs and GaN diodes.
- Include liquid- and air-cooling thermal network component models in electro-thermal simulations of vehicle inverters.
- Include advanced semiconductor device models in simulations to optimize high current density, low thermal resistance, and soft-switching modules.



Technical Discussion

The goal of this work is to characterize and model advanced power semiconductor devices and power module package technologies being developed and considered for Advanced Plug-in Hybrid Electric Vehicle Power

Conditioning Systems and Motor Drives. The characterization includes full electrical and thermal performance, as well as stress and monitoring experiments necessary to characterize module and component failure and wear-out mechanisms. The component failure and wear-out results are validated with physical measurements of interface wear-out performed at NREL.

Dynamic electro-thermal models have been developed to represent the semiconductor device and power module characterization results, and have been implemented in the Saber simulator to aid in optimizing the advanced modules and packages being developed by DOE EERE Vehicle Technology Program’s Advanced Power Electronics and Electric Motors projects, e.g., the Soft Switching Power Module being developed by Virginia Tech, the High Current Density Double Sided Cooling IGBT Package being developed by Delphi, and advanced cooling technologies being developed and evaluated by NREL. The failure and wear-out data are represented by empirical expressions and included in the Saber models to enable calculation of component lifetimes and impact of degraded performance resulting from vehicle fault condition and driving cycle stress.

Figure II - 150 depicts the overall goal of the electro-thermal-mechanical simulation for Advanced Plug-in Hybrid Electric Vehicle Power Conditioning Systems and Motor Drives. It shows the models and parameter determination including thermal component, electrical component, and mechanical reliability. It also shows the simulation applications including electrical, electro-thermal, and reliability.

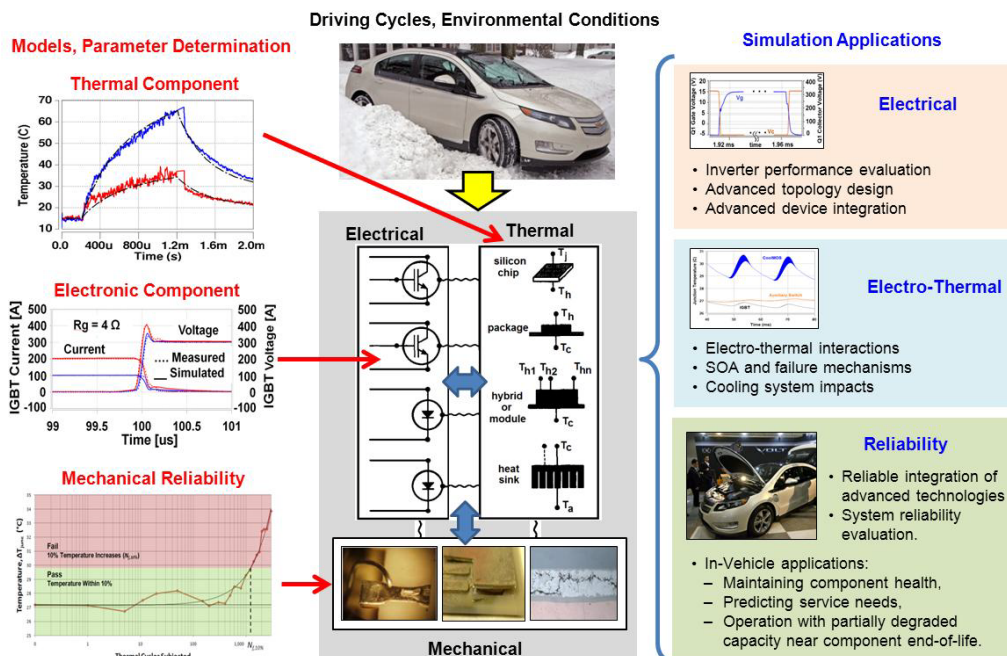


Figure II - 150: Goal of the electro-thermal-mechanical simulation.

Figure II - 151 shows a timeline and interaction of recent project accomplishments along with FY2013 milestones and goals described throughout the progress

report, and indicates the proposed FY2014 task using these results.

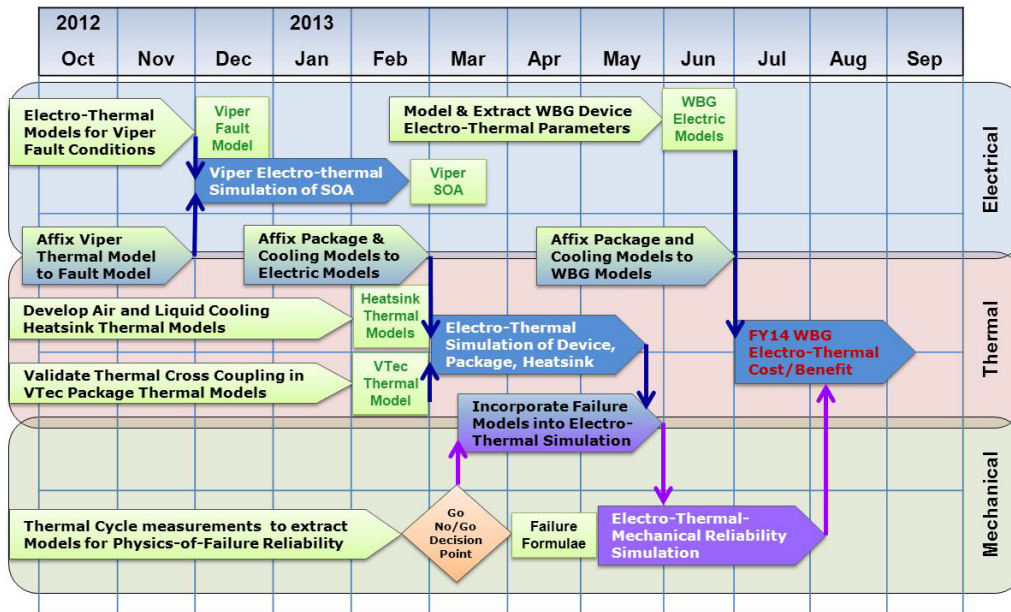


Figure II - 151: Timeline for 2013 project milestones.

Results for Delphi High Current Density Double-Sided Cooling Module:

Figure II - 152 shows a double-sided temperature-controlled heatsink that was developed for the Viper module. This heatsink uses a spring-loaded piston to apply a controlled four kg compressional pressure to the

device. A representation of this test fixture is shown in Figure II - 152 along with the Viper module. This heatsink actually has three thermocouples, although only the two that are in close proximity to the top and bottom of the module are represented in the figure. A third is located in the bulk of the heatsink.

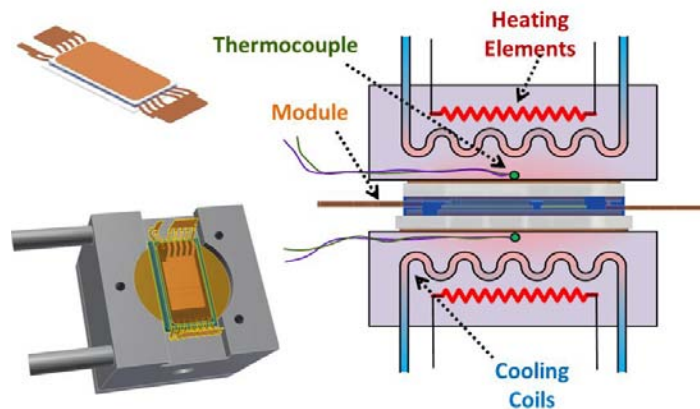


Figure II - 152: Delphi Viper module with heatsink.

Figure II - 153 shows the electro-thermal model for the high current density Delphi-Viper double-sided cooling IGBT module. The electrical component models predict electrical performance (a function of temperature) and device losses. Losses output the electrical model are input

to the thermal models which predict the instantaneous temperature distribution in the thermal network and feeds the junction temperatures back into the device electrical models.

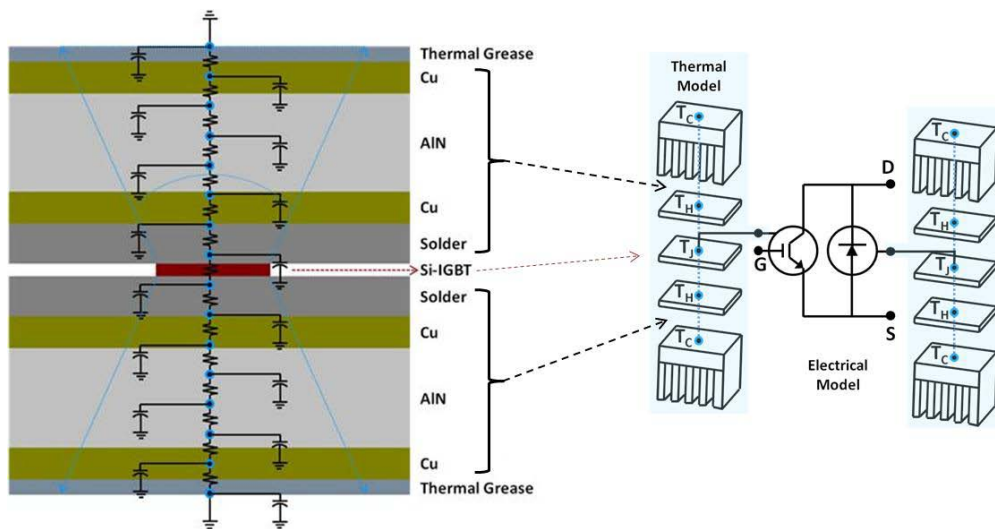


Figure II - 153: Electro-thermal model for double-sided cooling Viper module.

Figure II - 154 demonstrates model validation for the Delphi Viper high current density IGBT module (more detail on the validations are given in the previous year reports). The top left graph shows a validation result of output characteristics for the IGBT at 25°C. The validations were performed at different collector-emitter voltage (V_{CE}), collector current (I_C), gate voltage (V_G), and temperature (T). The bottom left graph shows a validation result of current dependence of inductive load turn off switching at a clamp voltage of 300 V at 25°C. The

switching validations were performed for different circuit parameters including collector-emitter voltage (V_{CE}), collector current (I_C), gate voltage (V_G), gate resistor (R_G), temperature (T), and clamp voltage (V_{Clamp}). Similarly, validations were also performed for the Viper Silicon PiN diodes. These validated modes are used to perform electro-thermal-mechanical simulations to evaluate electrical failure mechanisms and thermal stresses in Viper module for nominal and fault operating conditions as discussed below.

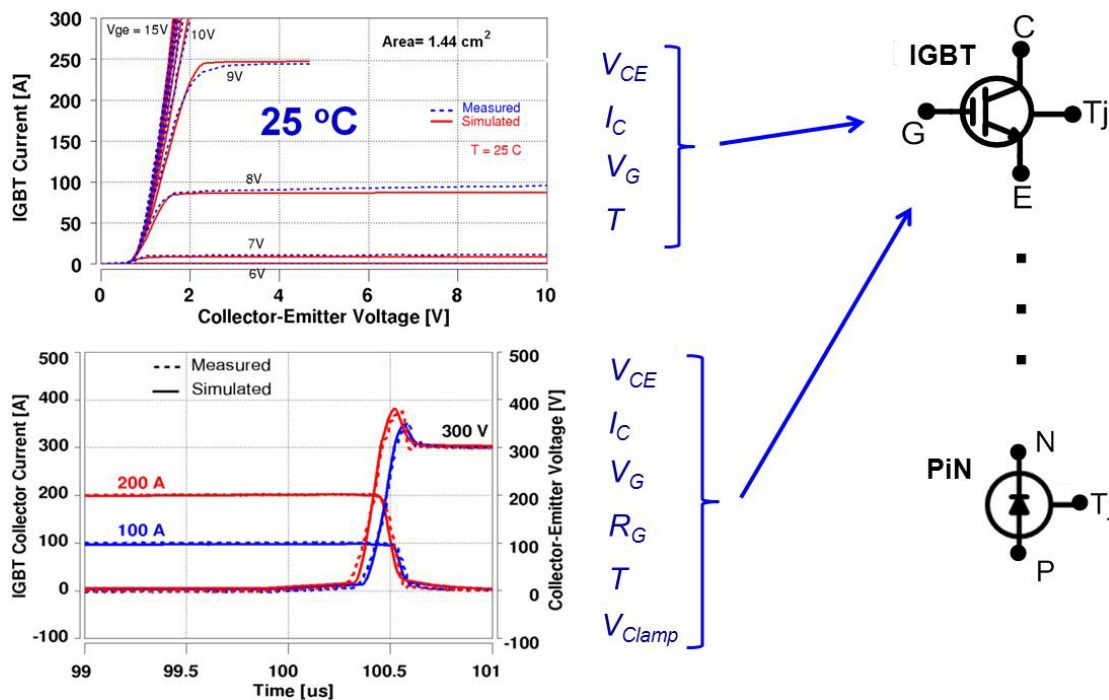


Figure II - 154: Validation of Delphi Viper electro-thermal semiconductor models.

Figure II - 155 demonstrates short circuit simulations and describes the resulting adiabatic chip heating for this condition. The left graph shows the collector-emitter voltage (V_{CE}), collector current (I_C), junction temperature (T_j), and total heat (Q_{Total}). The right graph shows how the

heat is distributed in each node within the chip during the fault condition. During the short duration fault condition, the heat does not diffuse significantly beyond the chip junction depletion region (shown by $E(t)$ at two voltages) and results primarily in local adiabatic chip heating.

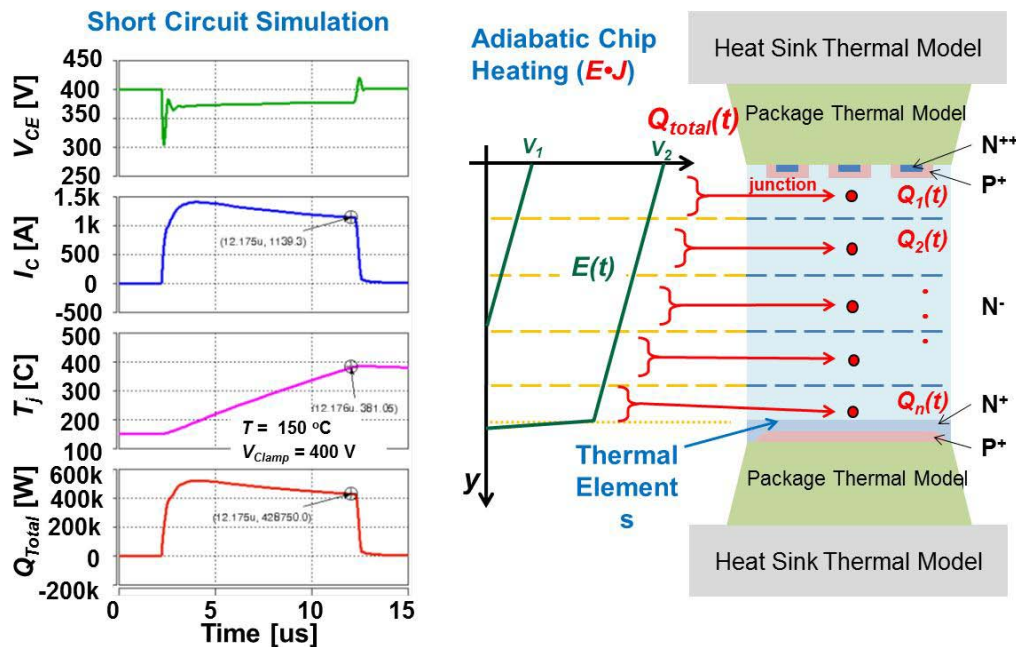


Figure II - 155: Electro-thermal simulation adiabatic heating for short circuit conditions.

Figure II - 156 compares measured and electro-thermal simulations for various Viper short circuit conditions. It shows the measured (dashed) and simulated (solid) IGBT voltage, IGBT current, and IGBT junction temperature (T_j) for a gate pulse width of 3 μ s, gate resistor of 2.2 Ω , temperature of 150 $^{\circ}$ C, and for different gate voltage pulse amplitudes (i.e., 9 V, 11 V, 13 V, and 15 V). Other conditions compared (not shown in this report) include several gate pulse widths (3 μ s, 5 μ s, 7 μ s, 10 μ s), two different gate resistors (2.2 Ω and 5.6 Ω),

different temperatures (25 $^{\circ}$ C, 75 $^{\circ}$ C, 125 $^{\circ}$ C, 175 $^{\circ}$ C), different clamp voltages (100 V, 150 V, 200 V, 250 V, 300 V), and different gate voltage pulse amplitudes (9 V, 10 V, 11 V, 12 V, 13 V, 14 V, 15 V). These comparisons are used to extend the Viper IGBT model to high-current with simultaneous high-voltage conditions using a short pulse to reduce heating during the pulse. Longer gate pulse widths extend the model validations to self-heating temperatures that are too high to be applied externally.

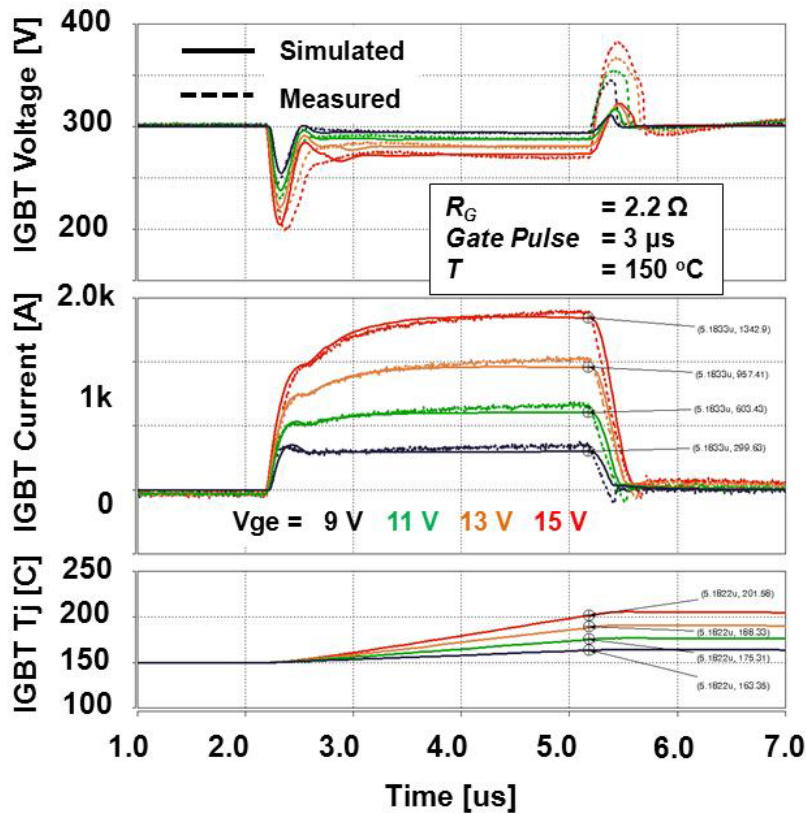


Figure II - 156: Viper module short circuit fault operating conditions.

For longer times than the short circuit pulse widths shown above, the heat generated during the fault conditions or other operations conditions diffuses from the die into the package and heatsink. To validate the thermal model for the Viper package, a well-controlled and well characterized temperature controlled test fixture is needed. Figure II - 157 shows the Viper module thermal test fixture (top picture) and the Viper module 262 W steady state ANSYS simulation for double-cooled test fixture (bottom picture).

Figure II - 158 on the left shows the comparison of simulated (dashed) and measured (solid) junction temperature (using TSP) for short duration (1 ms) high power (1175 W and 2820 W) pulses. Figure II - 158 on the right shows the comparison of simulated (black) and measured (red) junction temperature (using TSP), plate, and piston temperatures (thermocouples) as shown in Figure II - 157 for a low power (200 W) long duration (30 s) pulse.

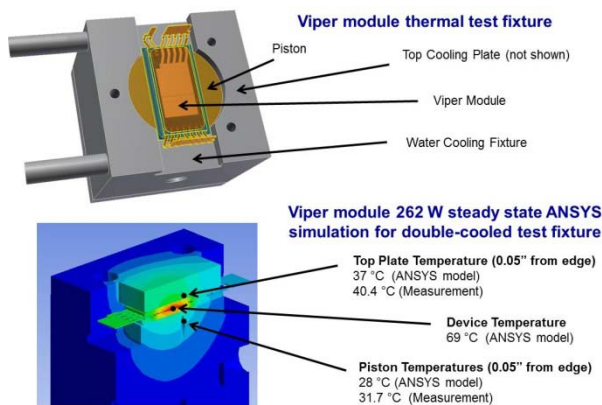
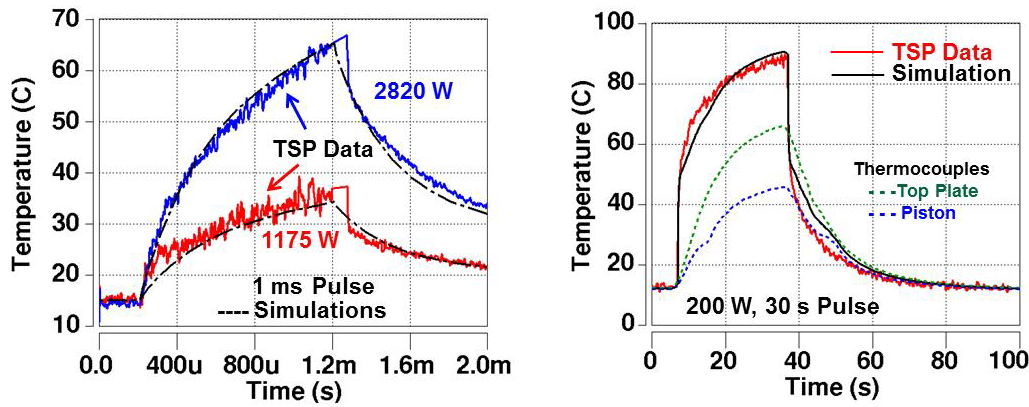


Figure II - 157: Validation of viper module thermal test fixture in steady state.



Comparison of simulated and measured Junction Temperature (TSP) for short duration, high power pulses.

Comparison of simulated and measured Junction Temperature (TSP), and Plate and Piston Temperatures (thermocouples) for a low power, long duration pulse.

Figure II - 158: Validation of thermal network component model for Viper module package.

Figure II - 159 shows simulation of the liquid-cooling thermal network component model for a double-side cooling Delphi-Viper module at the power level of 500 W and a pulse of 540 ms. The left graph shows the junction temperatures for the chip nodes, direct-bonded-copper

(DBC) nodes, and heat sink nodes. The heatsink model is parameterized in terms of chip area and location; the heatsink base thickness, material density, heat capacity, and thermal conductivity; fluid flow speed; and fin area, number of fins, and fin channel length.

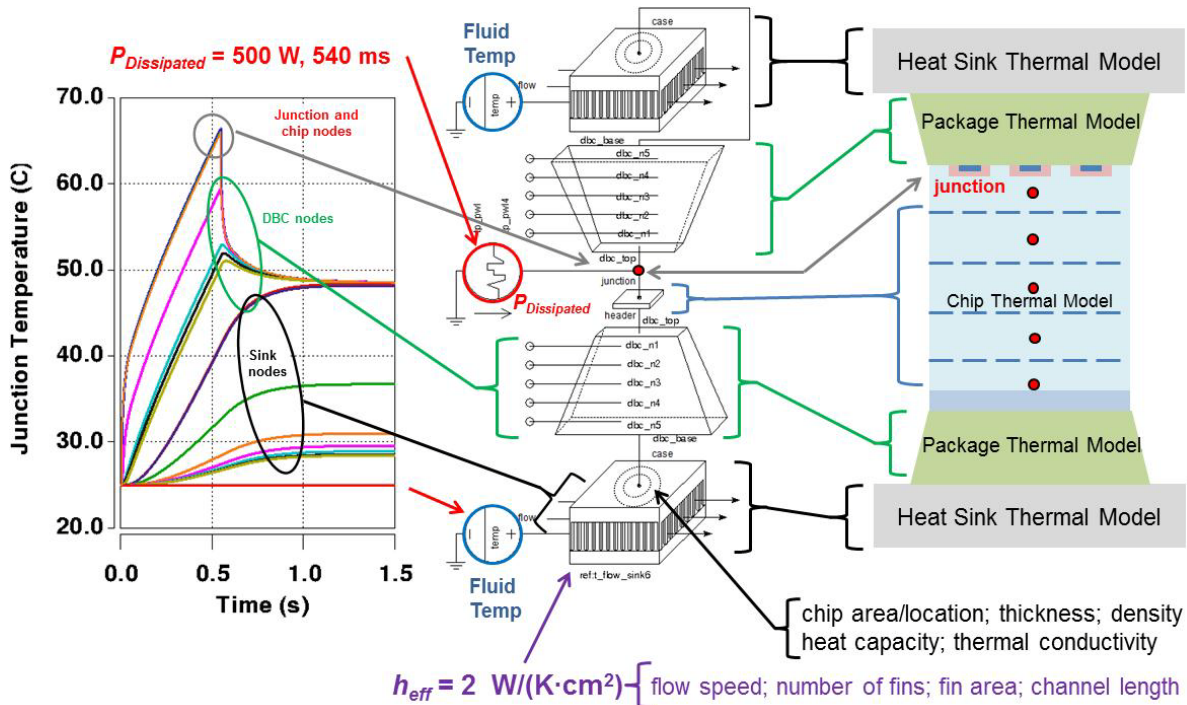


Figure II - 159: Demonstration of liquid-cooled viper module thermal simulation.

Results for Virginia Tech Soft Switching Module:

Figure II - 160 shows the Virginia Tech soft switching circuit diagram (top) and its module components.

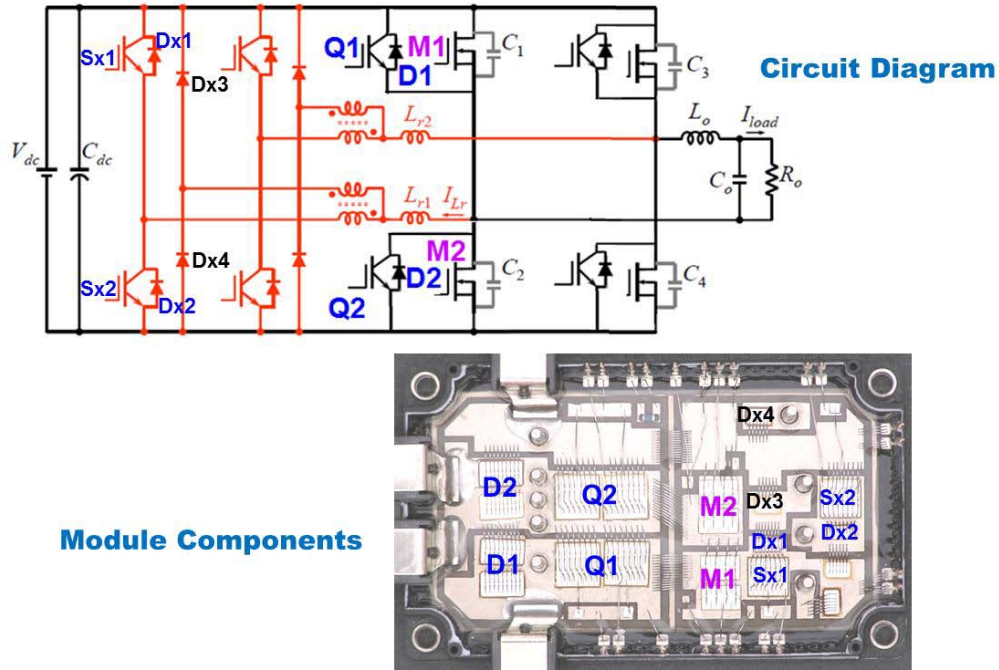


Figure II - 160: Application of Virginia Tech soft switching module.

Figure II - 161 shows the thermal network component model for the Virginia Tech soft switching module. The model parameterized in terms of the dimensions and die location within the module, and the materials thermal properties. The model calculates the thermal resistance and capacitance of the internal thermal nodes based upon these

parameters and the symmetry conditions of the nodes where thickness of the thermal elements represented by the nodes increases logarithmically with distance from the heat sources. The thermal coupling resistances are particularly important for this module thermal model due to the large number of electro-thermal devices within the module.

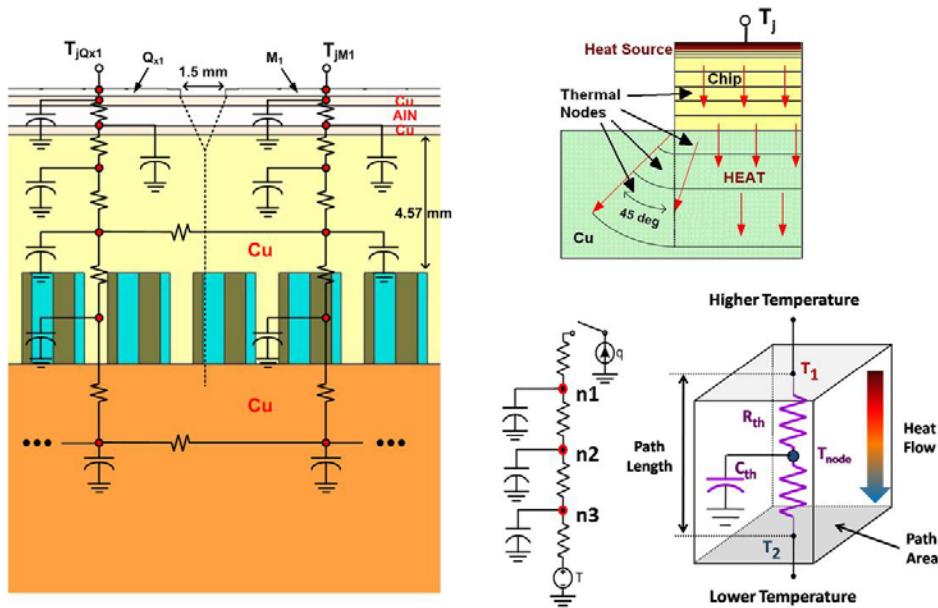


Figure II - 161: Thermal network component modeling.

Figure II - 162 demonstrates electro-thermal semiconductor model validation for the soft switching power module developed by the Virginia Tech program.

The top left graph shows of current dependence of inductive load turn off switching for the 600 V Silicon CoolMOS device at a clamp voltage of 300 V and gate

resistor of $22\ \Omega$ at 25°C . The bottom left graph shows the validation of current dependence of inductive load turn off switching for a 600 V Silicon IGBT at a clamp voltage of 300 V a gate resistor of $4\ \Omega$, and temperature of 25°C . The validations for both CoolMOS and IGBT were performed at different circuit parameters (not shown) including different collector-emitter voltages (V_{CE}), collector currents (I_C), gate voltages (V_{GG}), gate resistors (R_G),

temperatures (T), and clamp voltages (V_{Clamp}). Validation of static conditions were also performed similarly to those shown for the Delphi Viper module above. Validations were also performed for Silicon PiN diodes. More information on the validation of the electro-therma semiconductor models was given in the previous year's reports.

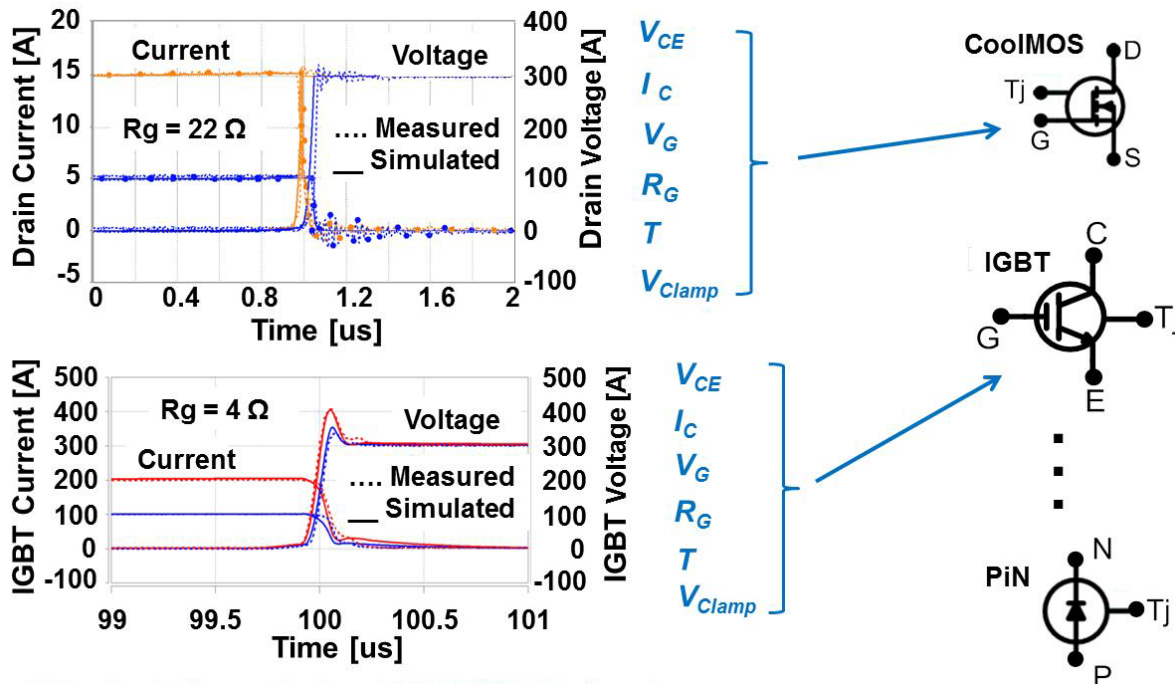


Figure II - 162: Validation of Virginia Tech module electro-thermal semiconductor models.

Figure II - 163 and Figure II - 164 show the time domain results of a full electro-thermal simulation of the Virginia Tech soft switching inverter under 50 kW condition.

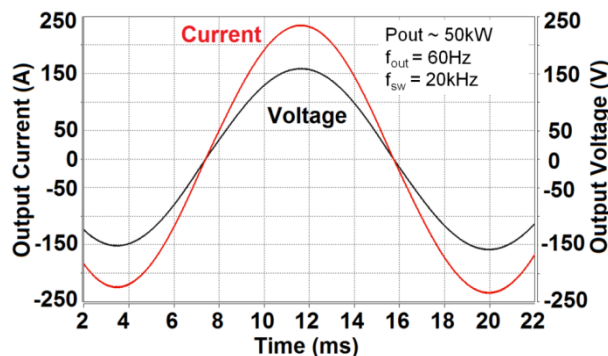


Figure II - 163: Inverter output voltage and current from full electro-thermal simulation.

Figure II - 164 shows the device voltage and current within a 20 kHz switching cycle under soft switching condition. The transformer current allows enough energy to discharge the main device (Q1) voltage to zero prior to

main device conduction enabling zero voltage switching condition. A dynamic dead time control is implemented which adjusts the turn on delays to allow for soft switching condition over the entire load range.

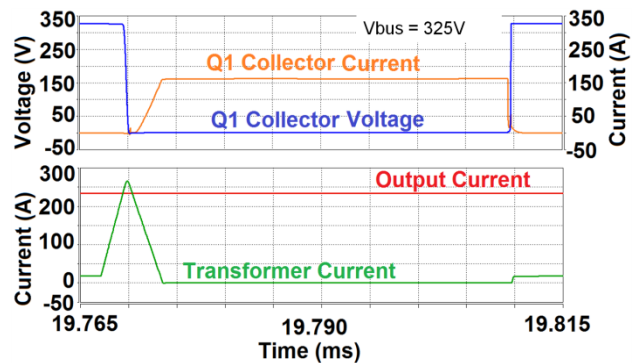


Figure II - 164: Device voltage and current showing soft-switching behavior Full electro-thermal simulation and optimization of soft switching crossover.

Figure II - 165 shows how the main devices Q1 and M1 share current during a switching cycle. Depending on the load current, either Q1 or M1 will dominate the current

conduction. This optimizes inverter efficiency by allowing MOSFET conduction at lower current levels and IGBT conduction at higher currents.

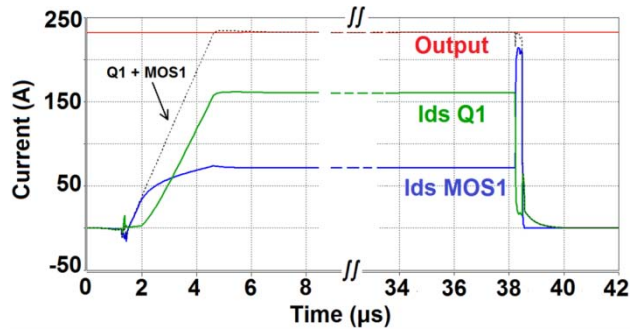


Figure II - 165: Current sharing behavior of main device Q1 and M1 within a switching cycle.

Figure II - 166 shows the TSP measurement system configuration including cross-coupling of heat dissipated in the IGBT that increases the temperature of the adjacent

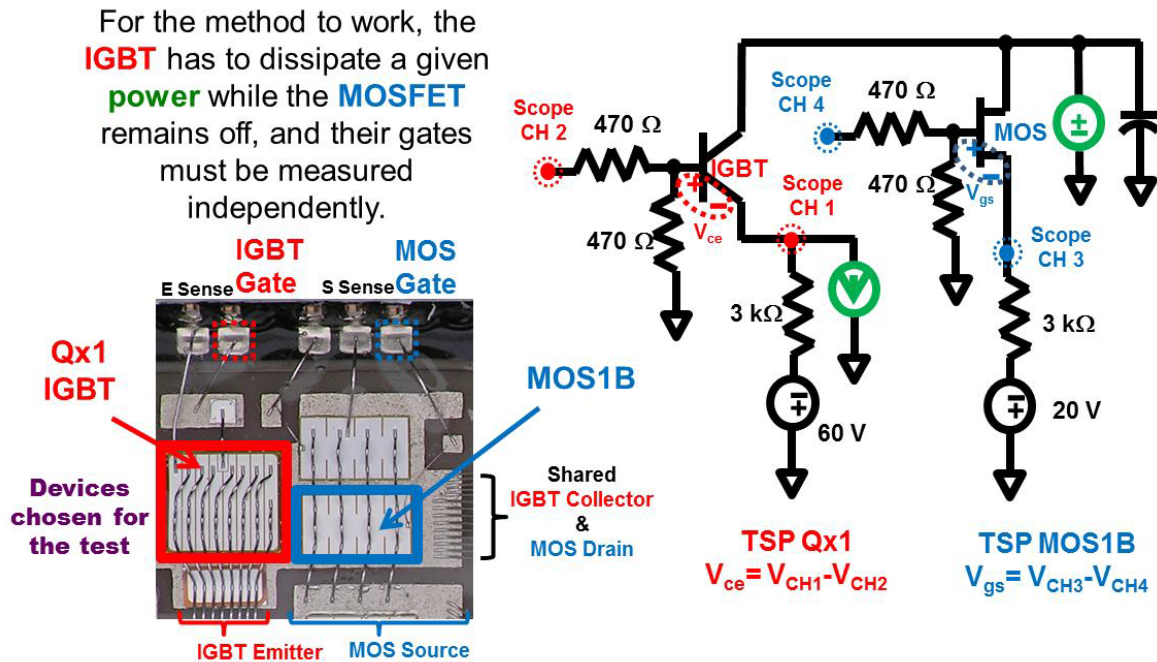


Figure II - 166: Cross-coupling TSP measurement.

Figure II - 167 shows the measured MOSFET junction temperatures due to thermal cross-coupling of the adjacent IGBT and MOSFET shown in Figure II - 166. To monitor how the temperature changed in the MOSFET junction, a 100 W-peak power pulse was applied with different duty cycles. Since the power was applied in the IGBT, its

MOSFET. During TSP calibration, the heat source is the hotplate temperature. During dynamic TSP measurement for a device, the heat source is the internal heat generated within the device during the heating phase. For the new enhanced cross-coupling TSP measurement, the temperature rise in the monitored device comes from the heat generated by an adjacent device. Both devices are individually calibrated for TSP, but the power pulse is applied only to the device that serves as the heat source.

junction temperature curves show the typical self-heating profiles of dynamic TSP measurements when the pulse is turned on and off. However, there is a thermal delay for the heat dissipated in the IGBT to diffuse through the thermal stack before it reaches the MOSFET junction.

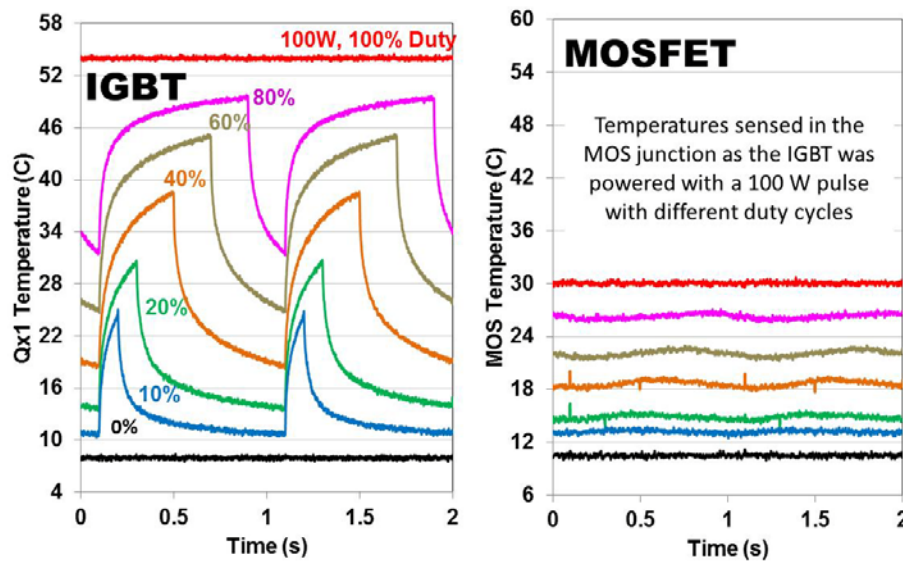


Figure II - 167: Cross-Coupling TSP measurements for IGBT and MOSFET in Soft Switching Module.

Figure II - 168 shows the thermal model validation of Qx1 using the cross-coupling TSP test system shown in Figure II - 166. Several pulse widths were used to validate different portions of the thermal stack. An additional

thermal path that accounts for the thermal capacitance of a thermal gel used within the device is added to the thermal stack at the top of the chip junction and validated using a very long power pulse (90s in Figure II - 168).

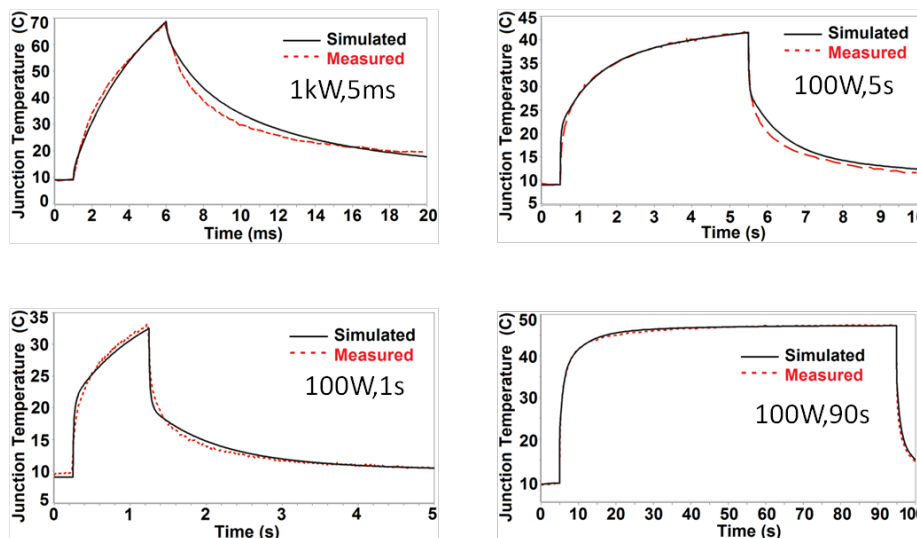
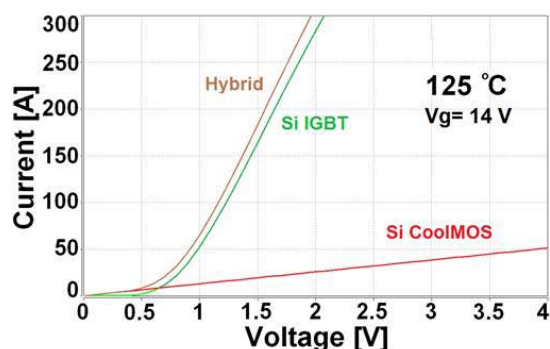
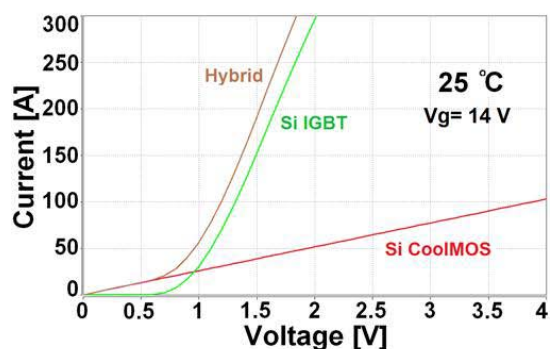


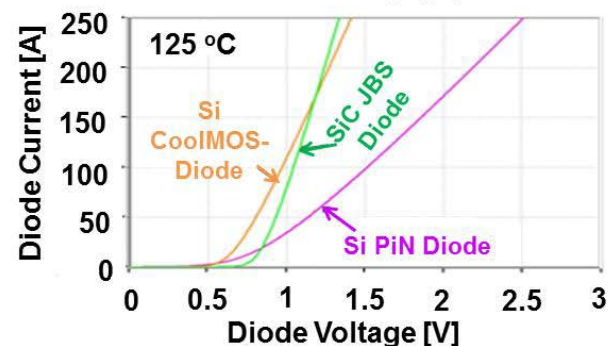
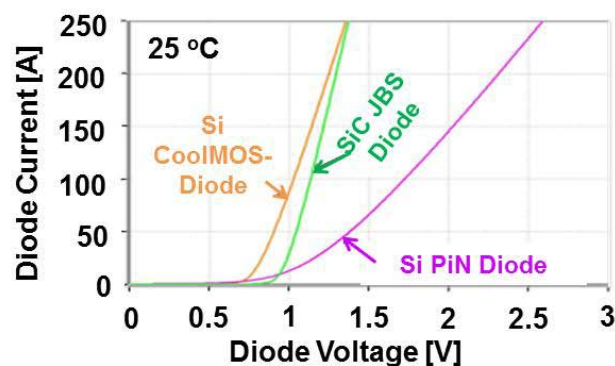
Figure II - 168: Thermal model validation of Qx1 using double TSP test circuit.

Figure II - 169 shows an example analysis of possible trade-offs for different semiconductor component selections in the Virginia Tech module. This demonstrates the analysis of current sharing of paralleled switches (Si IGBT and Si CoolMOS) and sharing of paralleled diodes (Si PiN, Si CoolMOS-body diode, and SiC JBS diode) at 25°C and 125°C. The left two graphs indicate that the hybrid switch (i.e., Si IGBT in parallel with Si CoolMOS) has lower on-state voltage drop at all current levels compared to discrete Si IGBT or discrete CoolMOS at

different temperatures. The right two graphs indicate that the SiC JBS diode has the lowest forward voltage drop at currents exceeding 250 A at 25°C and that the Si CoolMOS-body diode has the lowest forward voltage drop at currents below that. This crossover occurs at approximately 180 A for a temperature of 125°C. Careful consideration of the current sharing between diodes and resulting reverse recovery current versus temperature is necessary in this hybrid paralleled die module.



Analysis of current sharing of paralleled Switches (Si IGBT and CoolMOS)



Analysis of current sharing of paralleled Diodes (Si PiN, CoolMOS-body Diode, SiC JBS Diode)

Figure II - 169: Analysis of paralleled Si IGBT, CoolMOS, and diodes

Results for Mechanical Reliability Module Development:

Figure II - 170 shows the experimental method for package reliability prediction. The process first involves the determination of set of thermal cycling degradation parameters and the value ranges of chosen parameters. In this experiment, the thermal cycling parameters chosen are mean average temperature (T_{av}), temperature swing (ΔT), and dwell time at the min and max temperatures (t_{dw}) which are chosen because they best fit physics-of-failure modeling to determine reliability. Numerous modules (representative of the Virginia Tech soft-switching

module) are thermally cycled under all necessary parameter value combinations while being thermally monitored to detect and characterize buried thermal interface damage. Physics-of-failure models are then developed utilizing the collected degradation data sets in order to derive reliability predictions and operational thermal performance degradation equations. The physics-of-failure models will be used to perform full electro-thermal-mechanical simulations that predict the component life and degraded operation impact for vehicle driving cycle and fault conditions.

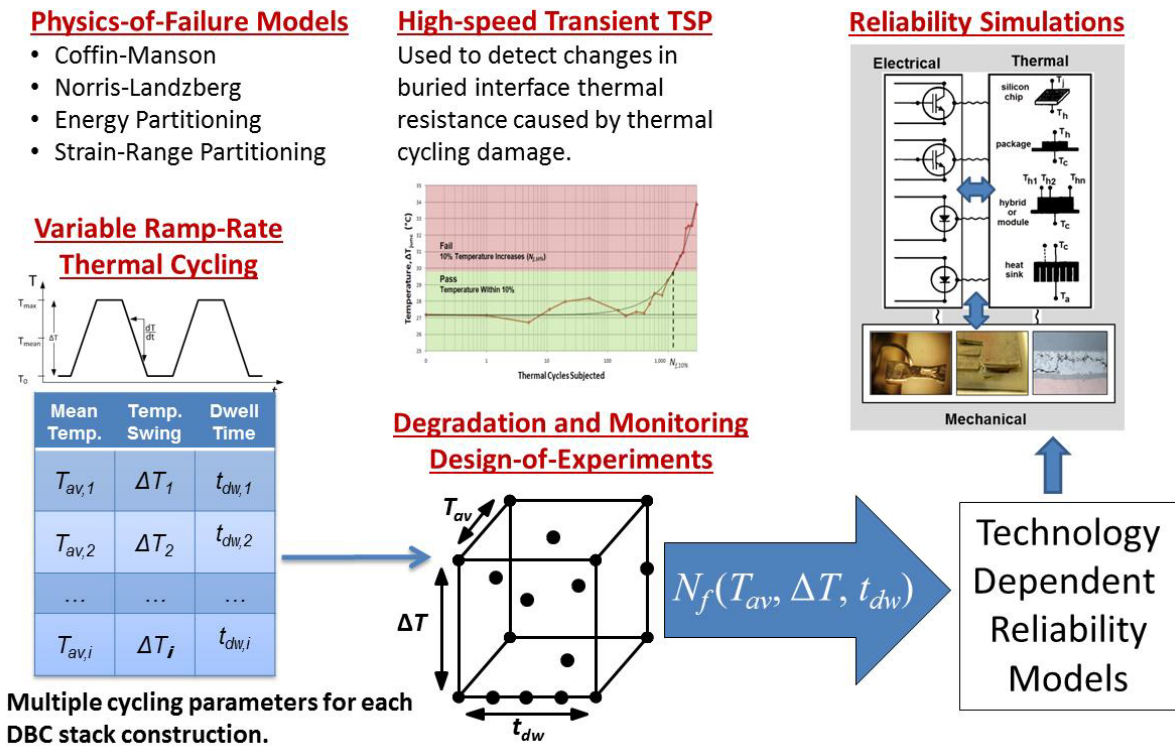


Figure II - 170: Package reliability prediction method.

Conclusion

This report summarizes the progress during 2012 towards FY13 milestones using results of FY12 work. The project includes the characterization and modeling of advanced power semiconductor devices and power module package technologies being developed and considered for advanced plug-in hybrid electric vehicle power conditioning systems and motor drives. The characterization includes full electrical and thermal performance, as well as stress and monitoring experiments necessary to characterize module and component failure and wear-out mechanisms. The validation results and simulation analysis are expected to provide confidence in the direction and progress of the Advanced Power Electronics and Electric Motors program as well as providing tools and methods for industry to more rapidly adopt the new technologies.

Publications

1. B. J. Grummel, H. A. Mustain, Z. J. Shen, and A. R. Hefner, "Reliability Characterization of Au-In Transient Liquid Phase Bonding through Electrical Resistivity Measurement," IEEE Trans. Compon., Packag., Manufact. Technol., submitted for publication Apr. 2012, accepted Dec. 2012.

2. B. J. Grummel, H. A. Mustain, Z. J. Shen, and A. R. Hefner, "Thermo-Mechanical Characterization of Au-In Transient Liquid Phase Bonding," IEEE Trans. Compon., Packag., Manufact. Technol., submitted for publication Feb. 2012, accepted Dec. 2012.
3. B. J. Grummel, H. A. Mustain, Z. J. Shen, and A. R. Hefner, "Comparison of Au-In Transient Liquid Phase Bonding Designs for SiC Power Semiconductor Device Packaging," in Proc. Int. Conf. and Exhibition High Temperature Electronics Network (HiTEN), Oxford, United Kingdom, 2011.
4. B. J. Grummel, H. A. Mustain, Z. J. Shen, and A. R. Hefner, "Reliability study of Au-In transient liquid phase bonding for SiC power semiconductor packaging," in Proc. 23rd Int. Symp. Power Semiconductor Devices & IC's (ISPSD), San Diego, CA, 2011, pp. 260-263.
5. -Mora, M.; Ortiz-Rodriguez, J.M.; Grummel, B.; Hefner, A.R.; Berning, D.; Hood, C.; McCluskey, P.; "Computer-controlled thermal cycling tool to aid in SiC module package characterization," Control and Modeling for Power Electronics (COMPEL), 2010 IEEE 12th Workshop on, vol., no., pp.1-6, 28-30 June 2010
6. McCluskey, F.P., and Hefner, A., Presentation at the Interagency Power Group Joint Mechanical and

-
- Electrical Engineering Workshop, Golden, CO. May 2010.
 7. Hefner, A., Keynote Presentation at the IMAPS International Conference and Exhibition on High Temperature Electronics (HiTEC 2010) Albuquerque, NM. May 2010.
 8. McCluskey, F.P., "Electrothermal-mechanical Modeling of Power Electronics Modules," Electronic Packaging Symposium, Niskayuna, NY. Sept. 2010.
 9. McCluskey, F.P., "Vehicle Inverter Power Module Electrothermal-mechanical Simulation and Reliability," IEEE/CPMT 2010 Workshop on Accelerated Stress Testing and Reliability (ASTR), Denver, CO. October 2010.
 10. McCluskey, F. P., and Hefner, A., "Electrothermal-mechanical Modeling of Power Electronic Modules," DOE Vehicle Technologies Program APEEM R&D Kickoff Meeting, Oak Ridge, TN. Nov. 2010.

III. Electric Machinery Research and Technology Development

III.1 Motor Packaging with Consideration of Electromagnetic and Material Characteristics

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Objectives

- Overall objectives
 - Develop more efficient electric machines based on investigation of lower loss materials and their processing.
 - Improve the continuous power from 54% to more than 58% of peak based on same thermal management system.
- FY 2012 objectives
 - Develop technologies that can improve the efficiency of a 55 kW traction drive electric machine by at least 1.5% averaged over its torque speed (m, ω) plane three to five most frequent operating points.
 - Use thermal material and process innovations to realize program goal.

Approach

- High torque, low speed regime, material focus on the following.
 - Electromagnetic design.
 - Conductor and winding design.

- Stator potting material, epoxy molded compound (EMC).
- Uniformity of stator core and winding temperature.
- Low torque, high speed regime, material focus on the following.
 - Electromagnetic design.
 - Magnetic steel—nonoriented vs grain oriented electrical steel (GOES) loss at high frequencies.
 - Quantify opportunity for higher grain oriented silicon steel (GOSS) texture and/or higher silicon steels.

The overall technical approach is (1) to reduce core losses across the full torque-speed map and (2) to even out the stator temperature across the lamination stack and windings through use of epoxy molding compounds. Figure III - 1 illustrates the high level technical approach in terms of the torque-speed map and what this translates to in terms of a representative plug-in electric vehicle (PEV) or all electric vehicle (AEV) operating over a combination of standard drive cycles. ORNL work uses the following drive cycle combination: the US Environmental Protection Agency (EPA) Urban Dynamometer Driving Schedule (UDDS) + US06 + LA92 + UDDS + the EPA Highway Fuel Economy Cycle.

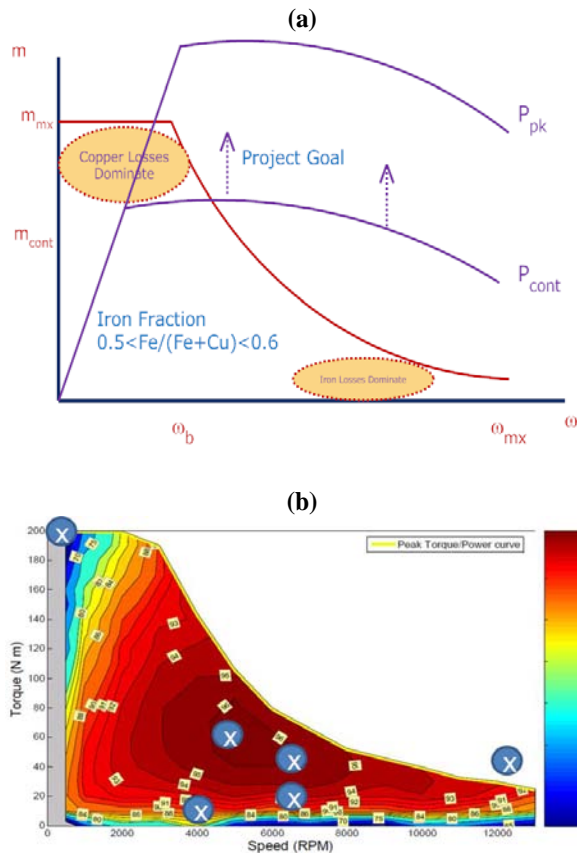


Figure III - 1: Project goal to improve continuous operating power across the full torque-speed map (a) and baseline efficiency map for a PEV (b).

The representative operating points shown in Figure III - 1(b), marked with “Xs,” are based on the 2010 baseline internal permanent magnet (IPM) motor operating under the following drive conditions, from upper left to lower right.

- Grade holding on 30% grade with driver only occupant
- PEV during urban cruise, 0% grade, zero wind, at V = 35 mph; $m_{MG} = 8.95 \text{ Nm}$; $n_{MG} = 4,063 \text{ rpm}$
- Dynamometer laboratory benchmarking base point: $P(V) = 30 \text{ kW}$; $m_{MG} = 60 \text{ Nm}$; $n_{MG} = 5,000 \text{ rpm}$
- PEV on continuous 6% grade, zero wind, $P(V) = 31 \text{ kW}$; $m_{MG} = 48.7 \text{ Nm}$; $n_{MG} = 6,385 \text{ rpm}$
- PEV on 0% grade, zero wind, at V = 55 mph; $m_{MG} = 15.6 \text{ Nm}$; $n_{MG} = 6,385 \text{ rpm}$
- PEV on 0% grade, zero wind, at V = 105 mph; $m_{MG} \sim 40 \text{ Nm}$; $n_{MG} = 13,000 \text{ rpm}$

Vehicle attributes used in the torque-speed mapping of Figure III - 1(b) are summarized in Table III - 1 for reference.

Table III - 1: Vehicle attributes for a representative AEV.

Vehicle		Traction Drive	
Curb mass	1,535 kg	Battery capacity	24 kWh
Gross vehicle weight rating	1,704 kg	Battery state-of-charge range	90%
All electric range	100 mi	Battery mass (included in curb mass)	294 kg
Aerodynamic drag coefficient	0.29	System voltage	360 Vdc
Coefficient rolling resistance	0.009	Motor peak power	80 kW
Frontal area	2.7 m ²	Motor continuous power	
Tire dynamic radius	0.3 m	Peak torque	280 Nm
Driveline gearing	7.94	Constant power speed ratio	4 : 1
Maximum grade	30°	Motor maximum speed	10.4 krpm
Maximum speed	92 mph	Motor corner speed	2.6 krpm
Zero to 60 mph time	10 s		

Major Accomplishments

- Completed baseline/comparator machine model.
 - Completed model and published as ORNL report (publication section).
- Completed loss survey of baseline machine and quantified major contribution sources as foundation for thermal material application.
 - Applied finite element analysis (FEA) to investigate the core loss in stator regions that have distinctive flux vector patterns.
 - Compiled the loss survey map as guideline for continued research.
- Completed fabrication of four 55 kW traction motor stators using selected magnetic and thermal materials and experimentally demonstrated the efficiency improvements in three-way comparison with baseline machine (2010 Prius stator).
 - Worked with Solepox and Cotronics on EMCs having thermal conductivities (TCs) > 3.
 - Developed application concepts that facilitate heat removal from traction motor stators.
- Fabricated experimental test station to energize the test stators with clean, three-phase power at specific frequency of interest. In this case frequency = 400 Hz to correspond to the traction motor operating in the regions listed as
 - PEV on continuous 6% grade, zero wind, $P(V) = 31 \text{ kW}$; $m_{MG} = 48.7 \text{ Nm}$; $n_{MG} = 6,385 \text{ rpm}$ and
 - PEV on 0% grade, zero wind, at V = 55 mph; $m_{MG} = 15.6 \text{ Nm}$; $n_{MG} = 6,385 \text{ rpm}$.
- Obtained valuable design experience based on motor fabrication using super core material.

Future Direction

Project future direction will move away from GOSS texturing efforts into a focused activity on the development of low cost, high silicon content lamination steel. It is well known in the electric machines industry that high silicon (6.5 wt %) has low loss, has virtually zero magnetostriction, is typically hot rolled to less than 0.2 mm thickness, and is useable in kilohertz frequency regimes. Unfortunately the grades of steel known as “super core” remain too expensive for widespread application in traction drive electric motors. This is because the process is a slow chemical diffusion technique having relatively low throughput.

ORNL will investigate alternative development methods based on strain softening processing for thin sheet Fe-6.5Si steel for core applications that are currently produced by silicon deposition followed by diffusion annealing. The goal of this work is to determine whether this processing technique will result in lower cost high silicon steel and to optimize the thermomechanical processing and post-deformation annealing of Fe-6.5Si sheet steel. There is significant ongoing effort to produce the sheet steel using thermomechanical processing including hot and cold rolling. Recent work is focusing on producing thin sheets in the thickness range of 0.2 to 0.3 mm using conventional ingot metallurgy to cast the steel composition followed by hot rolling and warm/cold rolling. A significant recent finding is the breakdown of the ordered precipitates above a critical deformation followed by strain softening of the alloy. This effect has been exploited to produce the sheet by cold rolling. The magnetic properties of the steel sheet produced by thermomechanical processing are reported to be equal to or better than the silicon diffused steel. The reported process variables in the literature are sketchy.

The intermediate warm rolling to introduce the strain softening and the subsequent cold rolling will be carried out using the state-of-the-art processing facilities at ORNL. The thermomechanical processing activity will be guided by processing-microstructure models that have been developed at ORNL over the years.

The initial phase will involve demonstration of proof-of-concept steel sheet preparation, which will involve making sufficient quantities of the steel sheet to make Epstein samples and testing the magnetic properties. This will be followed by a second phase that will involve scale-up of the process to produce wider core sheets to be used in motor design, evaluation, and prototype fabrication and testing.

It is important to also address the lessons learned during FY 2012 on laser cutting of super core material and the need for an additional machining step to treat small cross sections along the cut lines. Stacking this brittle material required fabrication of an enhanced holding

fixture to clamp the thin (0.1 mm) laminations. Stack welding was also problematic and required modifications to the welding procedure and introduced a slight skew into the stack. ORNL’s outside winding contractor also experienced difficulty handling the super core stack during winding and found a tendency to delaminate even though the organic/inorganic N1 coating and addition of DuPont Voltex 1175 adhesive should have maintained the stack integrity.

All four stators developed during FY 2012 will be used in full motor testing using two different rotors: (1) the original Prius rare earth magnet rotor and (2) an inert rotor of equivalent mass. This will facilitate segregation of spin fixture bearing loss and magnetic drag (core loss) in an unenergized condition. These results for core loss only can then be compared directly with results obtained in the testing reported here.

Planned testing consists of the following steps.

- Fabrication of an appropriate test fixture for testing in the ORNL Advanced Power Electronics and Electric Machines dyno facility at up to 10,000 rpm.
- Spin testing of the baseline, M19, potted M19, and JFE Super Core motors with inert rotors to validate air gap uniformity, balance, and bearing loss.
- Spin testing of the four motors using the Prius rotor with live magnets and mapping magnetic loss over the full speed range. Measurement of torque at each speed point and comparing these data with the core loss data shown in Figure III - 4.
- Stall torque and drive power measurements of each of the four motors to determine magnetic saturation effects on the peak torque.
- Summary of results.

◇ ◇ ◇ ◇ ◇

Technical Discussion

During this reporting period careful studies were made of the loss characteristics of an interior permanent magnet (IPM) traction motor (Figure III - 2), the 2010 Toyota Prius design. ORNL analysis showed that stator and rotor losses could be analyzed in four regions: (1) along tooth tips to about 15% of their overall length, (2) tooth body over 75% of the tooth length, (3) a band along the bottom of the slots that includes the base 10% of the tooth and 10% of the back iron, and (4) the bulk of the stator back iron. It was found that flux polarization in these regions pulsates with shallow circular polarization in region 1, strictly pulsating in region 2, very nearly circular in region 3, and shallow elliptical in region 4. A shallow elliptical flux profile does show some presence of circular polarization, but here it is mostly pulsating in character. These findings lead to the conclusion that teeth and back

iron would benefit from GOES having high GOSS texture. Unfortunately it is impossible at present to fabricate stator laminations possessing both radial and circumferential grain orientation.

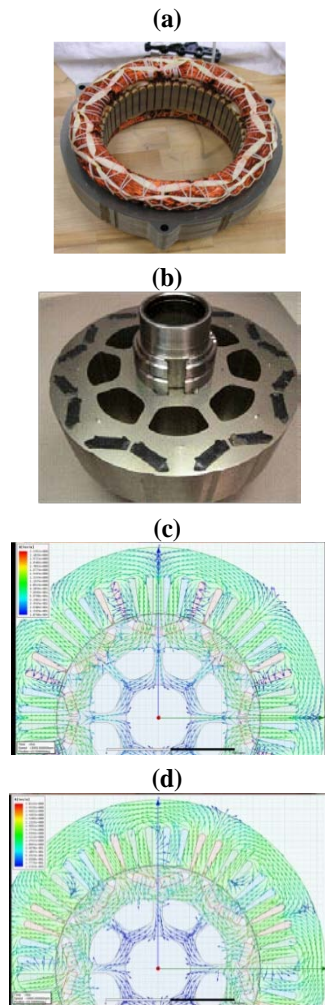


Figure III - 2: Illustration of the baseline IPM and example FEA plots used in loss evaluation. (Wound stator (a); permanent magnet rotor (b); and flux plots at $I_s = 0$ (c) and $I_s = 170$ A/Qe (d), both at $n = 3,000$ rpm.)

Electrical Steel Characterization Accomplishments

Electrical steels for motor manufacturing are characterized to 1.5 T up to 600 Hz excitation with flux in the 50/50 direction, meaning 50% rolling direction (RD) and 50% transverse (cross field). Figure III - 3 illustrates the behavior of flux patterns in the IPM stator and representative core loss curves for various mild steel grades. Notice that the lowest loss grades (Allegheny M6, AK parallel and AK Multi-frequency) have very low loss up to high induction levels (>15 kG/1.5T).

Electrical steels have been extensively characterized and tested over the years, mainly Epstein tests (see Lloyd and Fisher, 1909 [1], in which the authors discuss

modifications to the Epstein test method [2] by cutting the test material into strips 254 mm in length by 50 mm wide and arranging them into a square with additional material bent 90° to form the corners or simply stacked with overlapping butt joints). Lloyd and Fisher discussed testing of conventional lamination steels of the day, including those with 3% to 4% silicon content. Moses and Phillips [3] studied the accuracy of Epstein testing when grain oriented steel was used and found that stacking method differences can show considerably lower apparent loss. Epstein testing of steel samples in this project was performed at Tempel Steel following standardized procedures for sample preparation, corner joining/gaps, solenoid coil placement, and measurement.

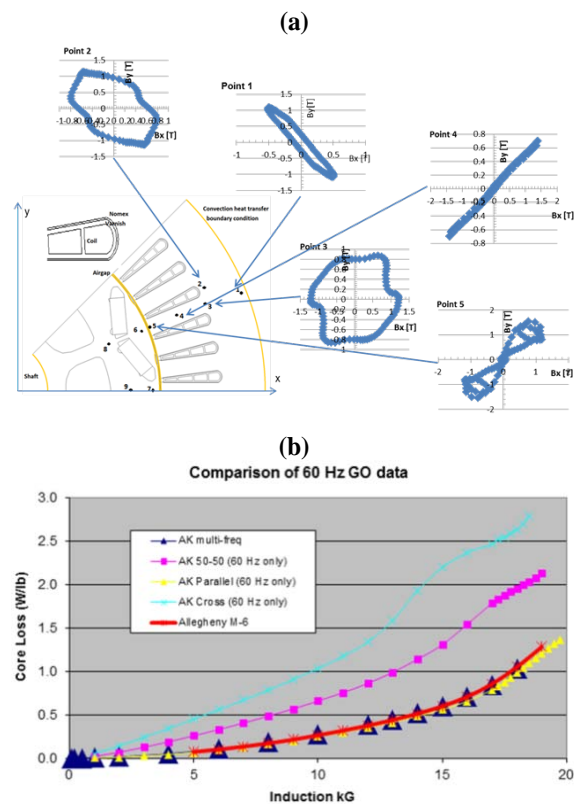


Figure III - 3: Flux polarization in the IPM stator (a) and core loss according to grain orientation (b).

Figure III - 4 summarizes standard Epstein core loss versus frequency results on various electrical steels over the normal test range of 50 Hz to 600 Hz at peak induction of 1.5 T. The samples were prepared so that 50% of the applied field was aligned with RD and 50% the transverse, the normal 50/50 testing method. In this figure the 29M15 AAS is similar to the lamination steel used in the Prius traction motor stator and rotor. Included are data on HF10 and other types. Note that because peak flux is held constant the conventional Steinmetz relation for hysteresis and eddy current components collapses to a single exponent on frequency.

At the test frequency of 400 Hz and 1.5 T the sample data illustrated in Figure III - 4 exhibit a specific loss of 13 to 18 W/lb, with notable differences in the slope of the loss curves. Steel such as HF10 exhibits higher loss at low frequency but lower loss at higher frequency, so it is useful in higher speed electric motors. Traction motor steel such as 19M15 exhibits lower loss at frequencies below 200 Hz relative to HF10, but then somewhat higher at higher frequency (higher speed operation). Included in this project was detailed evaluation of low loss, high silicon content electrical steel in the JFE Steel Corporation (JFE) 10JNEX900 (0.1 mm thickness with 2–4 μm organic/inorganic core coat). Figure III - 5 illustrates the Epstein test results of super core material.

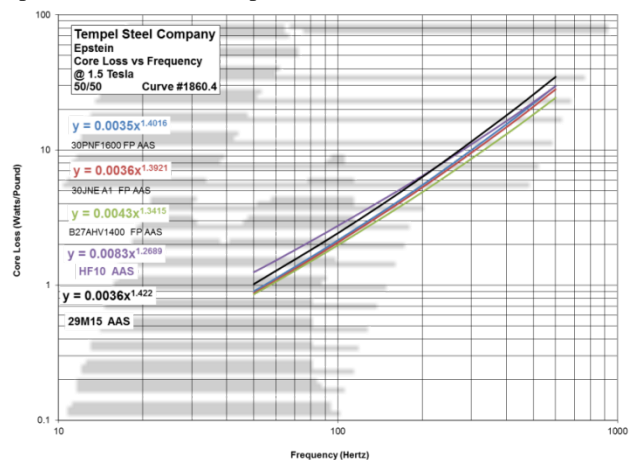


Figure III - 4: Core loss comparison of various steel grades and manufacturers. [Courtesy Tempel Steel.]

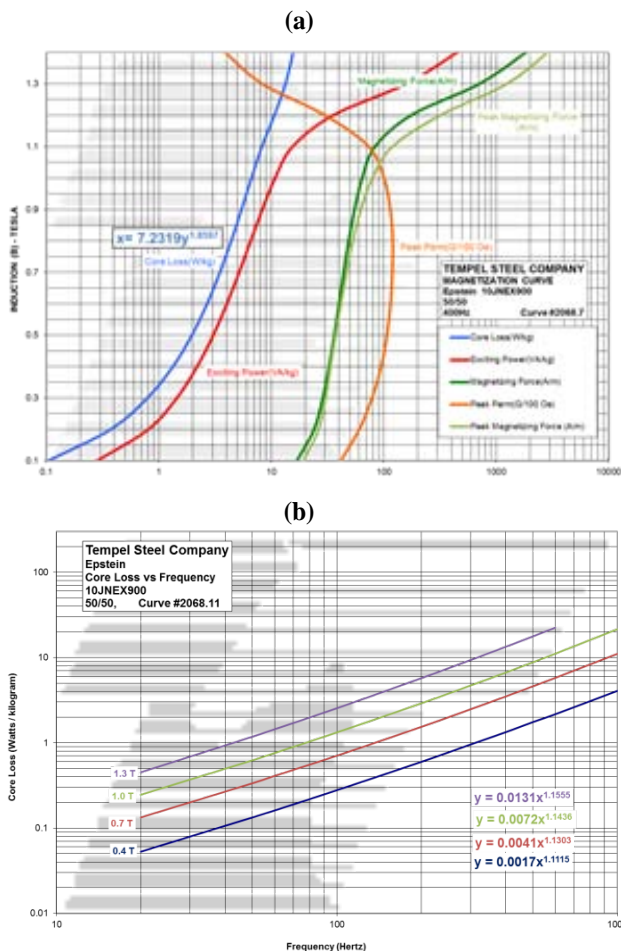


Figure III - 5: JFE 10JNEX900 Super Core 6.5% silicon steel characteristics. Core loss, exciting power, magnetizing force, and peak permeability, all vs frequency (Hz) (a). Core loss (W/kg) vs frequency with induction as parameter (b). [Courtesy Tempel Steel.]

Another objective of the project was to use thermal materials to aide heat removal from the stator core and windings to reduce peak temperatures and have more uniform thermal gradients across the stator. The materials used are a class of EMCs having TC ratings greater than 3 W/m-K (Figure III - 6).

Experimental Results

To definitively assess the benefits of lamination steels and potting compounds on motor losses and temperature profiles a battery of tests was devised that resulted in one-on-one comparison of each material change to a baseline comparator: the 2010 Toyota Prius stator. Figure III - 7 shows the stators fabricated using conventional M19 steel, 10JNEX900 Super Core, and M19 potted using Cotronics material and the production Prius stator. The fabricated stators were laser cut by Tempel Steel and stacked and welded per production techniques. The slot liner used was a 3M Innovative paper CeQUIN that has somewhat better thermal conductivity than traditional Nomex aramid paper,

both 10 mil in thickness. Aramid paper has TC = 0.115 W/m-K and 3M CeQUIN has TC = 0.195 W/m-K. The stators were wound

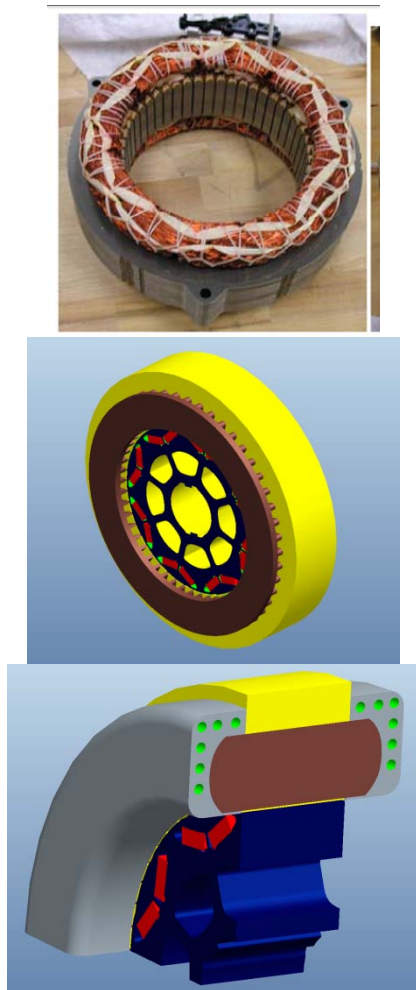


Figure III - 6: Illustration of EMC-potted stator and concept for future use in coolant channels. [Courtesy R. Wiles, ORNL.]

locally by TN Armatures using REA Pulshield SD #20 AWG magnet wire (brown coating) rated for inverter duty motors. The goal was to have an end turn height as close as possible to the production Prius traction motor formed windings. Experimental measurements of phase resistance and material mass confirmed very close agreement with the baseline stator. Table III - 2 and Table III - 3 summarize the experimental stator mass, copper winding mass, and phase resistance and phase inductance measurements. Based on the winding arrangement there is a slight difference in phase resistance and phase inductance. Note that phase inductance is consistently higher for phase A than B, and phase B is higher than phase C. This is the result in large part to end winding inductance differences due to the nonproduction stator windings exhibiting somewhat longer lead length on exiting the stator slots as can be seen in Figure III - 7. All

stator stacks were 50.8 mm in height, 264 mm outer diameter (OD), and 162 mm inner diameter.

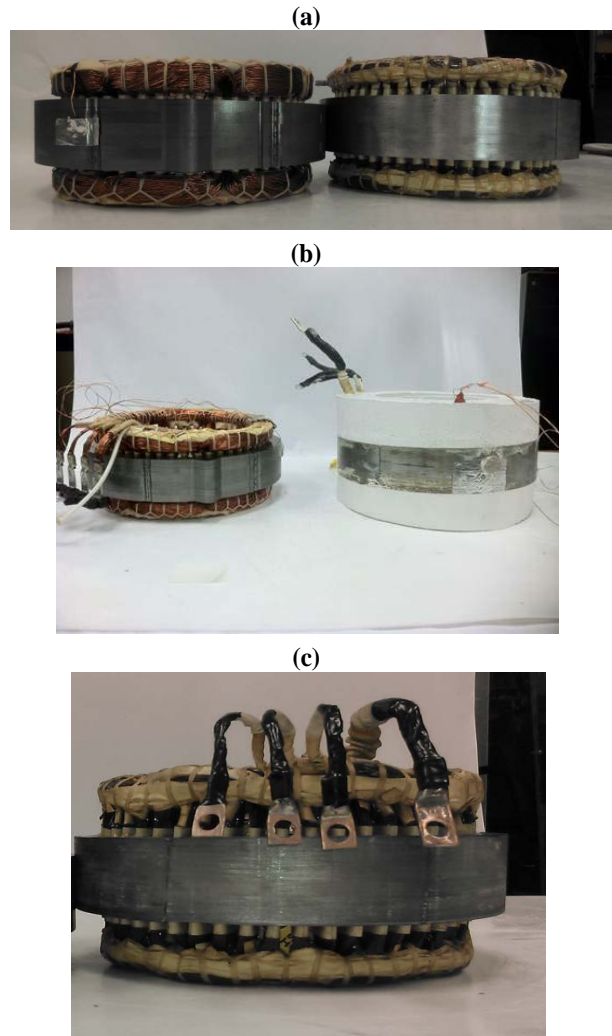


Figure III - 7: Experimental stators evaluated in convection tunnel: (a) left: 2010 Prius IPM baseline stator, right: 29M19C5 core stator; (b) potted M19 stator; and (c) JFE Super Core 0.1 mm lam stack.

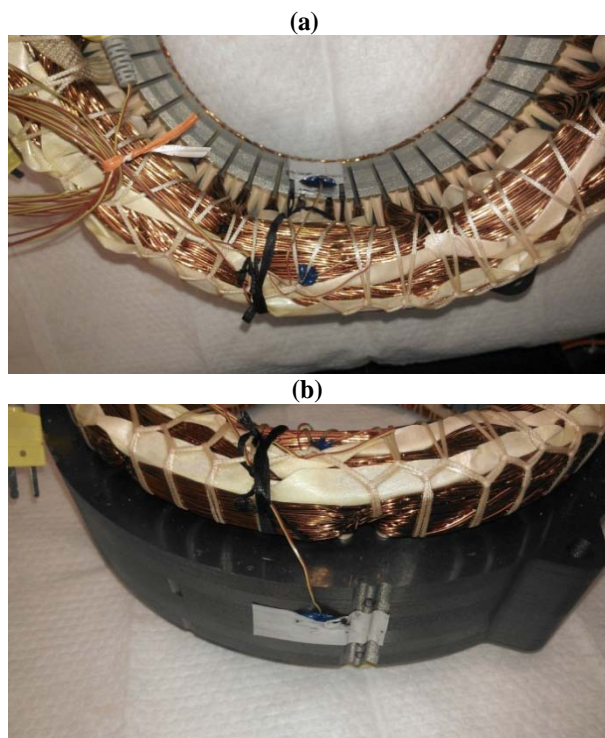
Table III - 2: Core and copper mass data of the test stators (no rotor).

Comparison Stator	Laminations (kg)	Copper (kg)	Assembly (kg)
2010 Prius	12.57	3.457	16.03
29M19C5 blank	12.53	3.46	15.99
29M19C5 potted	12.53	3.46	21.5
JFE 10JNEX900	11.47	3.46	14.93

Table III - 3: Phase to neutral resistance and inductance of the test stators (open bore data).

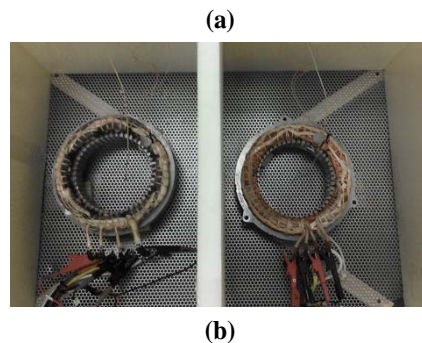
Comparison Stator	Phase	Phase to Neutral Resistance (Ω)	Phase to Neutral Inductance @400 Hz (μH)
2010 Prius	A	0.0820	856.64
	B	0.08155	823.00
	C	0.07725	783.37
M19	A	0.08339	959.02
	B	0.08271	935.13
	C	0.08275	926.70
JFE Super Core	A	0.08356	916.08
	B	0.08353	907.95
	C	0.08356	881.46

Temperature measurements were made in three locations, all along a radial line that included the tooth face on the stator bore, the end winding coil side, and the stator center on the OD. Thermocouple placement is shown in Figure III - 8 for reference.

**Figure III - 8:** Thermocouple placement on stator core (a) and phase winding (b).

Thermal evaluation was performed using laboratory equipment to energize the stators with clean sine wave current at a frequency representative of operation near cruising speed at zero grade with the traction motor

operating at 6,300 rpm and low torque point as shown in Figure III - 1. A Chroma programmable ac power source, Model 61512, was used to deliver 400 Hz frequency to the baseline and experimental stators connected in parallel, one per isolated convection tunnel. The Chroma ac source was set to 60 V_{rms}/phase, and the resulting phase currents were about 23 A_{rms}. The experimental hardware is shown in Figure III - 9 where the Chroma ac source requires an isolation transformer, in this case a 100 kVA, 480 V three-phase unit configured as four-wire wye input and five-wire wye output to match the Chroma input rectification stages.

**Figure III - 9:** Experimental hardware used for stator comparison testing: (a) twin convection tunnels with experimental stators; (b) test setup.

Stator input power was measured individually using Tektronix TCP A400 current probes connected to a pair of Yokogawa PZ-4000 power analyzers. Thermocouples were wired to a National Instruments NI9215 four-channel ± 10 V, 16 bit analog to digital converter interface to an NI cDAQ-9178 data logger running Lab View. Power dissipation in the stator core and copper windings was analyzed using measured input power per phase by the power analyzers, and the phase resistance data are listed in Table 3. The copper loss was determined using measured input current, and subtraction from input power yields the core loss power. Nominal power loss on the baseline stator was 210 W of which 54% was copper and 46% was core loss, nearly an even partition at 400 Hz.

Screen shots of the Yokogawa power analyzer phase data (Elements 1 through 3) and phase voltage and current waveforms are shown in Figure III - 10. With sinusoidal excitation the waveforms are relatively clean and harmonic

free so that core loss can be definitive at single frequency flux. Note the high level of reactive power indicating a relatively high Q inductive circuit.

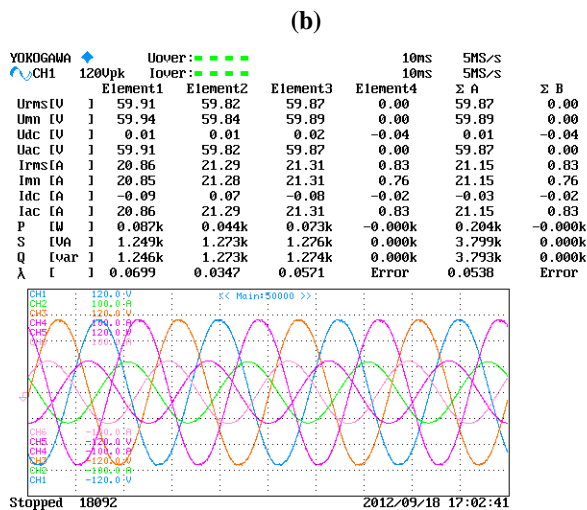
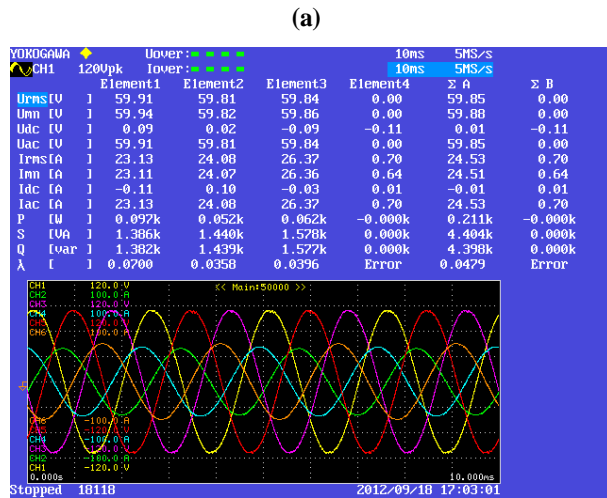


Figure III - 10: Experimental data for baseline unit (a) and M19 comparator (b).

Figure III - 11 summarizes the change in temperature (ΔT) relative to ambient air results for the four stators tested under the same excitation conditions. Note the progressive reduction in ΔT going from baseline M15 steel to the higher grade M19 and to JFE Super Core material. The steady state ΔT is about 10°C lower in each case.

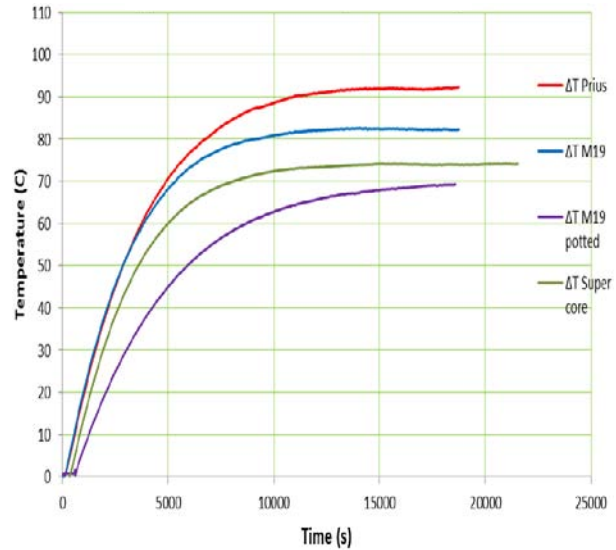


Figure III - 11: Experimental results for stator OD ΔT vs test time at 60 Vrms/phase and 400 Hz for the four stators tested.

The M19 potted core has significantly higher thermal mass and somewhat lower surface area for convection cooling so it will require substantially longer test time to reach steady state. The potted core also exhibits a substantial lag before the temperature begins to rise.

Conclusion

The original goal of this project was development of processing methods aimed at the implementation of GOES for stator and rotor laminations. Metallurgical processes can be developed that would result in zone dependent (100) orientation, but it would take more than 3 years so such activities have been postponed in favor of high silicon steel and thermal potting materials.

Traction motor losses dominate traction drive system efficiency and therefore must be minimized over the full torque-speed map rather than at a specific point or at constant torque such as 25% rated torque across the full speed capability of the machine. Cost and efficiency optimization dominate the industry wish list for AEV traction drive systems, so it is incumbent on ORNL to develop materials suitable for traction motor loss reduction.

This project demonstrated the substantial benefits of higher grade, somewhat more expensive steels (M19 vs M15), especially high silicon steel (6.5 wt %), that dramatically reduce core losses relative to the baseline production IPM motor. It was also demonstrated that stator winding potting significantly extends the stator thermal time constant and thereby promotes delivery of high peak powers of the traction motor over short durations. But thermal conducting materials are important to smooth out thermal gradients in the stator and lessen the probability of

thermally induced failures in the traction motor insulation systems, resulting in longer service life.

Patents

None.

Publications

1. J. M. Miller and R. L. Smith, *Vehicle Performance Metrics Applied to Electric Drive Vehicle System Research—Interim Report*, ORNL/TM-2012-xxx, Oak Ridge National Laboratory (in progress).
2. Pan-Seok Shin, John M. Miller, Tim Burrell, and Laura Marlino, *Thermal & Magnetic Analysis of Prius 2010 Motor by FEA*, ORNL/TM-2011/427, Oak Ridge National Laboratory, December 2011.
3. John M. Miller, “Permanent Magnets and Motors,” Trilateral EU-Japan-US Conference on Critical Materials for a Clean Energy Future, US Department of Energy, October 4–5, 2011, Washington, DC.
4. J. M. Miller, “National Laboratory Perspective on PEV’s,” presented at the Transportation and Electricity Convergence—Electric Vehicles, TEC-EV conference hosted by Texas A&M University, November 2–3, 2011, Houston, Texas.
5. John M. Miller, “New Materials and Processes Lead Way to PEV Traction Motor Efficiency Improvement,” presented at the Wisconsin Electric Machines and Power Electronics Consortium (WEMPEC) 30th Annual Review Meeting, University of Wisconsin-Madison, May 18–19, 2011.

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1. M. G. Lloyd and J. V. S. Fisher, “The Testing of Transformer Steel,” presented at the 26th Annual Convention of the American Institute of Electrical Engineers, June 28, 1909, Frontenac, New York.
2. I. Epstein, *Tektrotechnische Zeitschrift* 21, p.303, 1900.
3. A. J. Moses and P. S. Phillips, “Effects of Stacking Methods on Epstein-square Power-loss Measurements,” in proceedings of the IEEE, Vol. 124(4), pp. 413–415, April 1977.

III.2 Alnico and Ferrite Hybrid Excitation Electric Machines

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Objectives

- Overall objectives
 - Develop electric machines that minimize or eliminate the need for rare earth (RE) magnet materials, and
 - Have potential to match the baseline internal permanent magnet (IPM) performance metrics using low cost non-RE magnets
- FY 2012 objectives
 - Explore permanent magnet (PM) material choices suitable for use in hybrid excitation 55 kW plug-in electric vehicle traction motor.
 - Explore novel flux switching machine architectures and operating modes with potential to match baseline IPM performance levels.

Approach

- Renew investigation of ferrite and Alnico magnet machines.
 - Ceramic and Alnico magnets have excellent high temperature performance (>250°C).
 - Research machine architectures capable of high performance with low energy PMs.
 - Select flux switching design as candidate architecture suitable to accommodate Alnico or hard ferrite PM.
 - Determine coercivity bounds of enhanced Alnico and modified ferrite magnets, in the right structure and architecture, needed to match or

exceed baseline IPM performance, for future project work.

- Review and confirm characteristics of ferrite and Alnico magnets from -40°C to +120°C.
 - Ferrites contain mixed domains, some in opposition to the magnetization, and therefore, they produce weaker magnets.
 - Alnico (Al-Ni-Co-Fe) grades 5-7 and 8 exhibit domain wall movement that crosses grain boundaries resulting in low coercivity. Activities to enhance Alnico aim to develop more robust domain wall pinning and to increase coercivity by two to fivefold. Ames Laboratory has found a direct correlation between grain size and domain wall motion. It is desirable to have free domain movement within grain structures to enhance coercivity. More insights will follow from investigations into powder processed Alnico 8.
 - Alnico has high remanence but low coercivity. However, Alnico can tolerate high armature reaction transverse to the magnetization direction, a property that it may be possible to exploit for better performance.
- As a result of use of weaker magnets, the candidate electric machine must rely on higher speed operation (on the order of 23,000 to 28,000 rpm) and a gear reduction stage.
 - Research focused on characteristics of RE magnets and the weaker Alnico (Alnico8) and hard ferrite types such as barium and strontium oxide (SrO-6Fe₂O₃). Micrographs of the out of plane crystal structure taken by ORNL's Materials Science and Technology Division (MSTD) are shown in the charts in Figure III - 12 for reference.

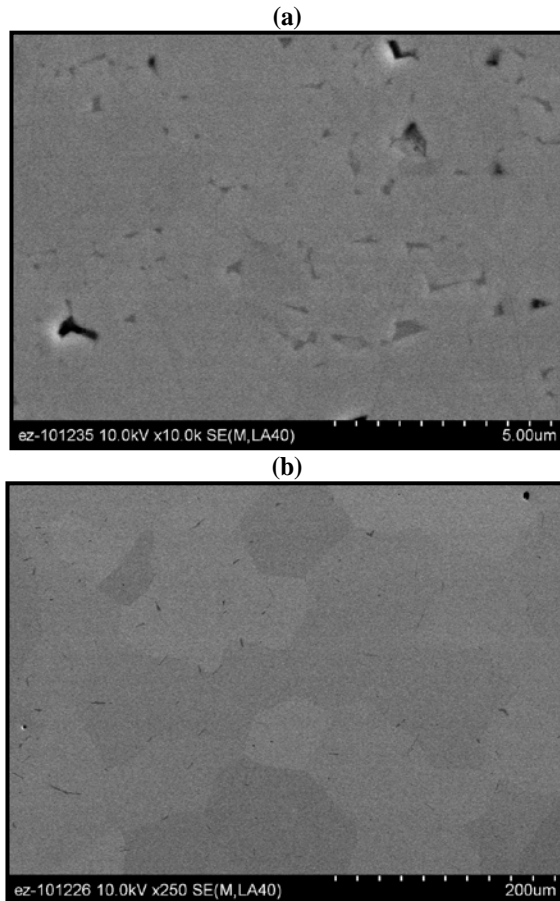


Figure III - 12: Micrographs showing out of plane crystal structure of (a) ferrite (SrO-6Fe₂O₃) and (b) Alnico 8.

Major Accomplishments

- Dismissed the transverse flux machine as a candidate because of its three-dimensional geometry and need for low flux soft magnetic composite materials, which leads to significant increases in costs [1–16].
 - Performed analysis of heteropolar architectures as candidates for future investigation if very low loss electrical steels are available. This machine is typically very high frequency and may not be well suited to high speed operation, but it is brushless and relies solely on wound field, PM, or hybrid excitation.
 - Selected the PM biased flux switching machine as a candidate for continued exploration because it admits ferrite and Alnico and because it can accommodate a field winding for hybrid excitation.
 - Expanded work on PM field excitation to include novel means of field weakening concepts and structures.
 - Filed invention disclosure on concept and experimental proof of concept.
- Collaborated with ORNL MSTD on new magnet material developments (ARPA-E program) and with Ames Laboratory for enhanced Alnico and modified ferrite designs.
 - Evaluated PM materials for improved understanding of coercivity (Figure III - 12)
 - Investigated applicability of ceramic magnet figure of merit, determining that
 - residual induction B_r and a permeance derived value of field strength H_x have more merit than the energy product and
 - total ceramic magnet volume is inversely proportional to $B_r H_x$ to meet a specific motor performance objective.
 - Investigated the contention that the energy product in Alnico magnets is in proportion to the volume of such magnets in an electric machine. The point here is that relaxation induction in Alnico after removal of current produced field is not substantially influenced by the field orientation so long as it lies within 90° of opposite to magnetization.
 - Determined that greater understanding of how the permeance coefficient influences this situation is required and researched ways to exploit this.
 - Developed deeper understanding of ferrite and Alnico PMs and exploited their strengths: near ideal recoil permeability of hard ferrite, the exceptional induction levels of Alnico, and the high temperature capability of both.

At maximum armature current, the armature reaction field, $H_{ar} = (N_s I_s)/L_m$, should not cause the main flux path permeance coefficient, P_c , to intersect the magnet normal characteristic past its knee. For ceramic and Alnico magnets the normal curve knee pulls into the second quadrant when the temperature falls below about 20°C. For traction motor applications the goal is a magnet having the highest possible magnetization, \mathbf{M} , and recoil as close to unity as possible. These metrics are shown in Figure III - 13, where maximum coercivity is \mathbf{M}/μ_r and maximum residual induction is $\mu_0 \mathbf{M}$.

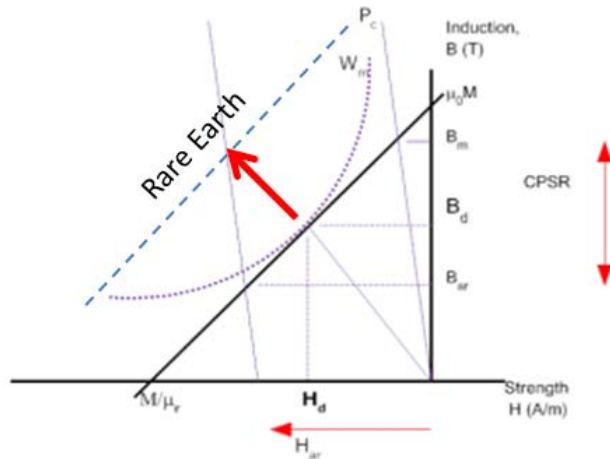


Figure III - 13: Essential characteristics of PMs. M = magnetization (A/m), \square = recoil permeability, B_r = residual induction (T), B_d and H_d = induction and field strength at maximum energy product point, and H_{ar} = armature reaction field strength (A/m).

The following equations summarize the importance of M , the recoil permeability, and the susceptibility χ_m as main components of recoil.

$$B = \mu_r \mu_0 H + \mu_0 M \tag{1}$$

$$@ H = 0: B_r = \mu_0 M \tag{2}$$

$$@ B = 0: H_c = -\frac{M}{\mu_r} \tag{3}$$

$$\text{energy product: } W_m = \frac{1}{2} BH = \frac{\mu_r \mu_0}{2} H^2 + \frac{\mu_0}{2} MH \tag{4}$$

$$B_d = \frac{\mu_0 M}{2} \quad H_d = -\frac{M}{2\mu_r} \tag{5}$$

$$\{B_d H_d\}_{\max} = \frac{B_r H_c}{4} \tag{6}$$

$$\mu_r = (1 + \chi_m) \tag{7}$$

The development for energy product [Eqs. (4)–(6)] illustrates why magnetization, M , is critical to PM motor development. This is why having the highest possible M and unity μ_r are so fundamental. Table III - 4 summarizes the recoil permeability, susceptibility, and temperature coefficient of induction for representative ferrite and Alnico magnet grades, and Table III - 5 gives average prices. Note that flux (induction) loss is higher in RE grades (NdFeB) and with SmCo or Alnico grades. In addition, the normal curve knee appears in the second quadrant when magnet temperature is high for NdFeB magnets but when temperature is low for ferrite and Alnico magnets.

Table III - 4: Low energy magnet characteristics.

PM type	Recoil permeability	Susceptibility	Temperature coefficient of induction (%/C)
Alnico 5-7	17	16	0.01
Alnico 9	7	6	
Ceramic 6	1.1	0.1	0.2
Ceramic 8	1.07	0.07	
SmCo	1.03	0.03	0.045
NdFeB	1.05	0.05	0.11

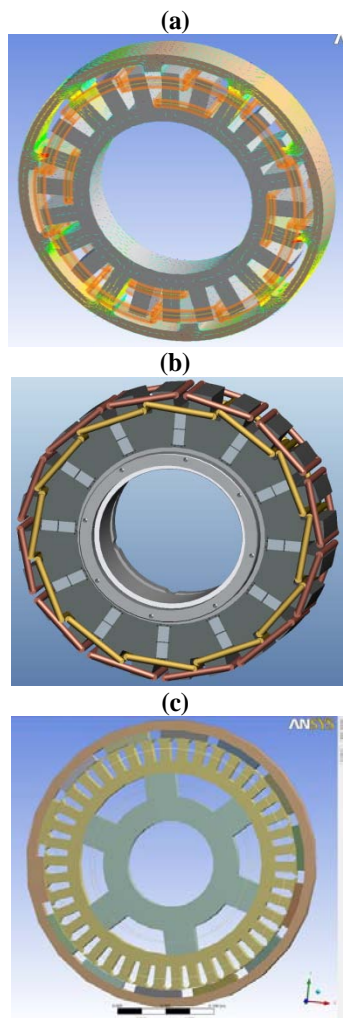
Table III - 5: Average prices of various permanent magnet types.

PM type	Price (\$/lb _m)
Alnico	44
Ferrite	1.2
NdFeB	135 ^a
SmCo	125

^aWas 160.

Future Direction

- Develop concept flux switching machine magnetic and electrical design capable of achieving 80% of baseline IPM performance.
 - Create simulation model for concept flux switching machine, and define parameters.
- Develop prototype hybrid machine using hard ferrite only and compare performance to baseline IPM machine.
- Validate simulation model based on prototype machine characterization.
- Refine prototype design to include low loss electrical steel and advancements in conductor and winding designs.
 - Refinement to include modified ferrite or enhanced Alnico when available.



Hybrid excitation electric machine concepts evaluated: (a) wound field flux switching, (b) hybrid flux switching, and (c) cross-field weakened surface PM.

Future direction in non-RE electric machine development will also include work on parallel flux

designs in which the magnet is not exposed to the full armature reaction of the main path flux. At present this is an emerging technical area that deserves further investigation. Figure III - 14 highlights the distinction between PMs in series with armature reaction and those where PMs can be in parallel with the main flux and thereby not be exposed to full demagnetization effects under heavy loading. The series PM case means the magnets are collinear with high H_c fields and thereby fully exposed to demagnetization, whereas in the parallel case, low H_c magnets may be useable. It is unclear pending future development whether Alnico can suffice for parallel implementations because even open circuit operation of an Alnico motor would permanently demagnetize it (e.g., pulling the rotor out of the motor stator bore).

The class of inductor machines [16] deserves further investigation, and that will be part of work moving forward. The following is an excerpt from Chapter 6 of Balagurov's text, "Induction (Inductor) Generator Design" [16].

Inductor generators are reliable and have simple design, they allow for high revolution frequencies. They can be designed for high frequency loads (thousands of Hz), during which they have the greatest advantages over other types of generators. The voltage in induction generators is easily regulated.

The main types of induction technologies can be classified by the following features:

1. *By application—generators, drives, converters*
2. *By location of the excitation system—homopolar or multipolar*
3. *By excitation system—electromagnetic excitation, or magnetic-electric excitation*
4. *By active layer structure—classic active zone with a single or dual pitch, or combined active zone with a single or dual pitch.*

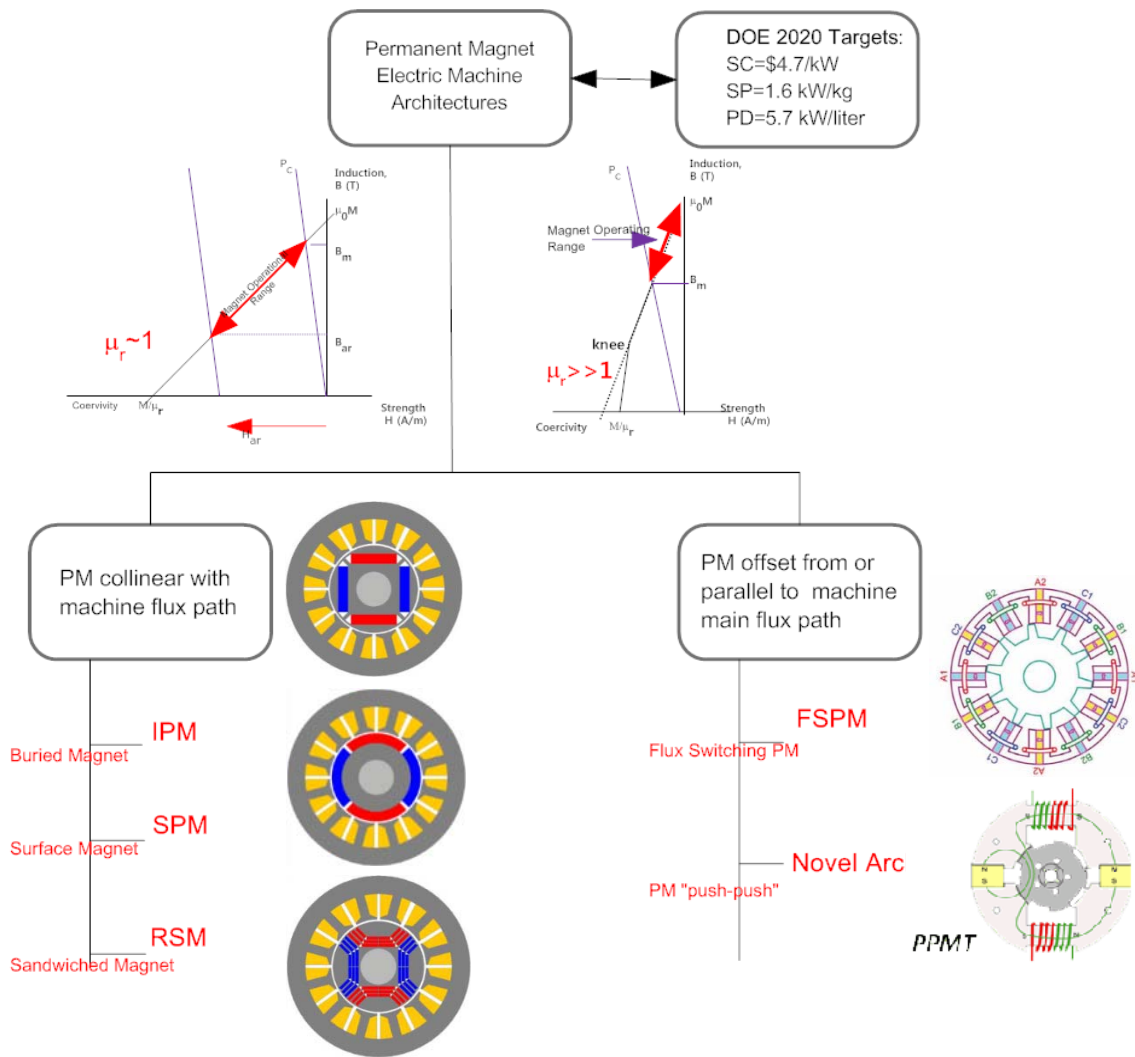


Figure III - 14: Technical direction of future traction motor designs.



Technical Discussion

The hybrid excitation machine currently being examined uses an outer rotor design and surface mounted ferrite magnets on the rotor. One field control concept that is being analyzed will weaken the torque at higher speed (or for a generator, reduce output when demand drops). The machine is weakened via saturation of the armature yoke by either series or orthogonal flux injection from a field coil strategically placed in the specially designed center hub. The armature and rotor in the outer portion of the machine use the armature yoke as part of their magnetic circuit, and the field hub shares the armature yoke to complete its magnetic circuit. When the armature yoke is brought closer to saturation from the separate field

winding, machine performance is reduced to the point where the yoke is fully saturated.

The center hub distributes the field flux appropriately in the armature yoke to push it into saturation when needed for control. Cross-field flux control is a vector sum process where the mild steel permeance is controllable, resulting in control of the machine flux.

The magnetic configuration and some electromagnetic finite element analysis (FEA) results are shown in Figure III - 15.

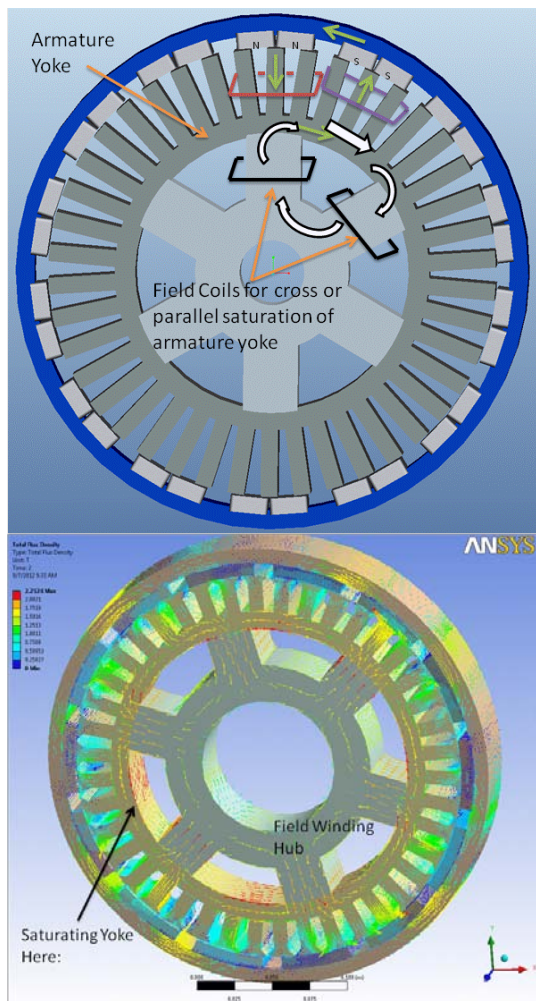


Figure III - 15: ORNL hybrid excitation design using ferrite magnets and cross-field saturation for control.

The torque profile shown in Figure III - 16 is from the FEA model, showing a few degrees of rotation for a single phase in the generator. The blue trace depicts maximum torque output, and the red trace shows the reduction in torque output due to the effect of the field-saturated armature yoke. Work is ongoing to improve the turndown ratio seen in the models from full torque to reduced torque, to improve output power control for generator applications, and to increase the constant power speed range (CPSR) for motor applications. The capability of flux control in the surface PM (SPM) motor represents a significant step forward in brushless dc and brushless ac motors. Increased capability means that armature current angle control would no longer be the limiting factor on CPSR.

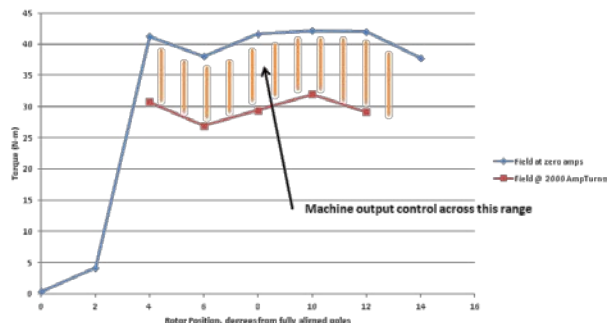


Figure III - 16: FEA data showing initial design results for flux control to vary output power.

The output turndown range shown in Figure III - 16 is for a dominant circumferential rather than a strong cross-field in the armature yoke of the prototype shown in Figure III - 15. This is expected from an inner field yoke having spokes aligned down the stator stack. With spoke skewing, the cross-field effect will be stronger, and that option will be analyzed and modeled in future work. For example, if the inner field hub spokes are skewed to span multiple armature poles, the field flux control will be stronger and more uniform. The design shown in Figure III - 15 is a 14-pole SPM with a three-phase, 42-slot armature, resulting in slots \div poles \div phases = 1 (SPP = 1). For SPP = 1, a wave wound armature will be used due to deep and narrow slots and the requirements for the copper packing fraction.

Project Redirection

Beginning October 1, 2012, this project (APE043) and a complementary project (APE035) merge into a larger scope traction motor research and development (R&D) task focused on lower cost and higher efficiency traction drive systems (TDSs). Two key system design factors will be exploited to determine whether TDS efficiency can be improved at lower cost through operation at the higher dc link voltage of the traction inverter and the higher speed operation of the traction motor. In this case, the traction motor insulation system must be rated for 800 V to >1,000 V at the traction inverter dc link (e.g., $360 < U_{ph} < 450 \text{ V}_{rms}/\text{phase}$) and meet Underwriters Laboratories (UL810A) and International Electrotechnical Commission (IEC60077) standards, which specify insulation withstand voltage or HiPot = $2U_{dc} + 1.5 \text{ kV} = 3.1 \text{ kV}$ to 3.5 kV.

Any new materials developed, including lamination materials explored and demonstrated in the sister project, will be used. There is also the potential to implement new nanostructure soft magnetic materials such as FINEMET, Somaloy, and nanocomposites. Heat generation in soft magnetic composites is a result of energy stored (B-H curve enclosed area), where high permeability materials store little energy and low permeability materials store more energy per cycle but require higher driving fields and correspondingly higher winding losses. Additional losses

occur at the permeable material-air boundary, where the flux fringes and introduces eddy currents in adjacent metallic conductors. It is preferable to use materials as motor cores that restrict magnetic domain wall motion in order to have low loss at high frequency [15]. According to Leary, Ohodnicki, and McHenry [15], in high power, low loss applications, it is best to use low permeability nanocomposites having “controlled anisotropy perpendicular to the drive field in a material that exhibits a high permeability and low coercivity as measured along the easy axis.” Silicon steels, for example, improve loss characteristics but retain domain wall pinning at grain boundaries and exhibit hysteresis loss that worsens with frequency. Going forward, the project will develop materials that show the potential for reducing loss, especially at higher frequencies (i.e., higher speed operation).

Conclusion

This project focuses on design and development of an electric machine architecture that will minimize or eliminate the need for RE magnet materials. During FY 2012, this included the following discoveries.

- Electric machine structures that
 - minimize PM exposure to high demagnetization fields and
 - incorporate materials suited to high speed operation—high frequency of flux in the mild steel components.
- Material work done in Advanced Power Electronics and Electric Motors project APE035 on motor packaging with consideration of electromagnetic and material characteristics is included in this project.
- Use of ferrite magnets reduces dependence on light and heavy RE materials (Nd and Dy, respectively); hard ferrite magnets unfortunately have only one-twelfth the energy of RE magnets and are much more susceptible to demagnetizing fields. This has spurred the use of novel electric machine architectures and methods of field control.
- Electric machine architectures suited to low energy magnets having only one-third the residual induction of RE magnets, which means operation at higher speeds and therefore rotor designs capable of withstanding the resultant hoop stress, especially at high temperatures.
- Moving to higher speeds in turn requires introduction of low loss electrical steels that are also affordable in a traction drive motor.

During FY 2013 this project will merge with its sister project, APE043, to create a more comprehensive motor development R&D task that will address higher speed operation, higher voltage operation, and attendant thermal

management of lower aspect ratio designs (e.g., $D/L \ll 1$) for mechanical robustness.

Patents

1. Invention disclosure S-124,305 IDSA#2745: Balasubramaniam Radhakrishnan, John M. Miller, Curtis W. Ayers, and Timothy A. Burress, *Novel Materials and Processes for Minimizing Core Losses in Stators*.
2. Invention disclosure S-124,371 IDSA#2806: John M. Miller and Curtis W. Ayers, *Hybrid Flux Switching Generator Utilizing Permanent Magnets for Field Excitation*.
3. Invention disclosure S-124,243 IDSA#2685: John M. Miller, Curtis W. Ayers, and Randy H. Wiles, *Flux Switching Generator for Exhaust Waste Heat Recovery*.

Publications

1. J. M. Miller and R. L. Smith, *Vehicle Performance Metrics Applied to Electric Drive Vehicle System Research—Interim Report*, ORNL/TM-2012-xxx, Oak Ridge National Laboratory (in progress).
2. Pan-Seok Shin, John M. Miller, Tim Burress, Laura Marlino, *Thermal & Magnetic Analysis of Prius 2010 Motor by FEA*, ORNL/TM-2011/427, Oak Ridge National Laboratory, December 2011.
3. John M. Miller, “Permanent Magnets and Motors,” Trilateral EU-Japan-US Conference on Critical Materials for a Clean Energy Future, US Department of Energy, October 4–5, 2011, Washington, DC.
4. J. M. Miller, “National Laboratory Perspective on PEV’s,” presented at the Transportation and Electricity Convergence—Electric Vehicles, TEC-EV, conference hosted by Texas A&M University, November 2–3, 2011, Houston, Texas.
5. John M. Miller, “New Materials and Processes Lead Way to PEV Traction Motor Efficiency Improvement,” presented at the Wisconsin Electric Machines and Power Electronics Consortium (WEMPEC) 30th Annual Review Meeting, University of Wisconsin-Madison, May 18–19, 2011.

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2. T. A. Burress, S. L. Campbell, C. L. Coomer, C. W. Ayers, A. A. Wereszczak, J. P. Cunningham, L. D. Marlino, L. E. Seiber, and H. T. Lin, *Evaluation of the 2010 Toyota Prius Hybrid Synergy Drive System*,

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 4. Timothy C. Moore, Amory B. Lovins, "Vehicle Design Strategies to Meet and Exceed PNGV Goals," SAE Paper 959106, SAE Future Transportation Technology Conference, August 4, 1995, Costa Mesa, California.
 5. Mitsubishi Cable Industries, *Rectangular Magnet Wire "MEXCEL"*, 7th edition, May 10, 2011.
 6. Shinichi Matsumoto, "Advancement of Hybrid Vehicle Technology," European Power Electronics Conference, EPE2005, Dresden, Germany.
 7. Abdul Rehman Tariq, Carlos E. Nino-Baron, and Elias G. Strangas, "Iron and Magnet Losses and Torque Calculation of Interior Permanent Magnet Synchronous Machines Using Magnetic Equivalent Circuit," *IEEE Transactions on Magnetics*, Vol. 46(12), December 2010.
 8. Marian Soinski, "Anisotropy of dc Magnetostriction in Cold-Rolled Electrical Sheets of Goss Texture," *IEEE Transactions on Magnetics, Letters*, Vol. 25(4), July 1989.
 9. Wojciech A. Pluta, "Specific Total Loss Components Under Axial Magnetization in Electrical Steel Sheets with Different Degree of Goss Texture," *IEEE Transactions on Magnetics*, Vol. 44(11), November 2008.
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 11. Katsumi Yamazaki, Takashi Fukuoka, Kan Akatsu, Noriya Nakao, and Alex Ruderman, *Investigation of Locked Rotor Test for Estimation of Magnet PWM Carrier Eddy Current Loss in Synchronous Machines*.
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 16. B. A. Balagurov, *Design of Special Electrical Alternating Current Machines*, Moscow, 1982 (no longer in print).

III.3 Unique Lanthanide-Free Motor Construction

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Objectives

- This project pursues new motor construction that eliminates, or significantly reduces, the use of rare earth elements while maintaining the attractive size, weight and efficiency features of rare earth permanent magnet motors
- The primary drivers for this work include:
 - Lack of transparency in the rare earth magnet supply market and its pricing structures
 - Significant rare earth price escalation in calendar year 2011
 - Need for small, lightweight, high efficiency, low cost motors for electric traction drives
 - New architectures and/or materials that eliminate rare earth materials while maintaining performance that is attractive for electrified vehicles
- The DOE motor specifications that are targeted for this work include:
 - 55 kW baseline design
 - Scalable to 120 kW or higher

Approach

- Pursue design that enables the use of low coercivity magnets
 - Unique magnet and supporting rotor geometry
 - Stator and rotor design features that reduce demagnetization fields
- Collaborate with FFRDC partners

- Ames Laboratory for incremental improvements in high flux, low coercivity magnet materials
- National Renewable Energy Laboratory for thermal management
- Oak Ridge National Laboratory for testing
- Period 1 (10/2011 thru 1/2013) focuses on the design of the electromagnetic circuit that will meet the DOE targets and be capable of manufacturing
 - UQM's focus is the electromagnetic design with existing AlNiCo technology
 - Ames Laboratory is pursuing increased performance of the AlNiCo material
 - NREL will provide assistance in the thermal management of the motor design
 - ORNL will provide testing of the motor
- Year 2: Build proof-of-concept motor and test with standard three-phase inverter
- Year 3: Build and test proof-of-design motor
- Bill of materials with costs and higher power design at program completion

Major Accomplishments

- Created the Interface Control Document (ICD) that includes DOE requirements and UQM specification objectives
- Defined target magnet parameters (including level of incremental improvements expected for proof-of-concept build)
- The electromagnetic design and FEA indicate that a motor using the current state on AlNiCo material will:
 - Meet the DOE target specifications
 - Maintain high power density
 - Maintain high efficiency typical of PM motors

Future Direction

Based on the analysis performed to date, future will continue as originally planned. This will include:

- Finalize the mechanical design in Period 1
- Continue to incorporate improvements in the AlNiCo material that Ames develops
- Work with NREL on the cooling of the motor
- Commence hardware build in Period 2

◇ ◇ ◇ ◇ ◇

Technical Discussion

- The electromagnetic design and analysis confirm that a motor using the current state on AlNiCo material will:
 - Meet the DOE target specifications
 - Maintain high power density
 - Maintain high efficiency typical of PM motors
- The mechanical design is underway
 - The next step of the design process will be to perform 3-D analyses to select one of the retention methods
 - NREL will assist in the design with regard to the thermal management issues
- Ames has identified possible methods to improve the AlNiCo magnet properties and will be pursuing them during FY2013

Conclusion

The primary conclusion that can be draw for the work to date is:

- Based on analysis a Lanthanide-free, permanent magnet motor can meet the DOE target specifications
- A proof-of-design should be built to validate these findings

III.4 Alternative High-Performance Motors with Non-Rare Earth Materials

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Objectives

Electric drive systems, which include electric machines and power electronics, are a key enabling technology for advanced vehicle propulsion systems that reduce the petroleum dependence of the transportation sector. To have significant effect, electric drive technologies must be economical in terms of cost, weight, and size while meeting performance and reliability expectations.

The objective of the GE Global Research “Alternative High-Performance Motors with Non-Rare Earth Materials” program is to develop a higher power density traction motors at a lower cost while simultaneously eliminating or reducing the need for rare-earth materials. Successful completion of this program will accelerate the introduction of hybrid electric vehicles into the U.S. road vehicle fleet and bring the added benefits of reduced fuel consumption and environmental impacts.

(A) Motor Development

- Develop advanced motor concepts including electromagnetic, mechanical, and thermal concepts.

- Build proof-of-principle machines to verify the design process as well retire the key risks.
- Design and build 55kW/30kW machines that meet the DoE specifications
- Develop cost model to estimate the advanced motors cost based on 100000 units/year
- Investigate the scalability of the developed concepts by evaluating 120kW/65kW machines

(B) Materials Development

The objective of the materials development tasks is to develop non-rare-earth containing motor component materials that enable non rare-earth containing motor designs that meet project performance goals.

Approach

(A) Project uniqueness:

- The project proposes a very comprehensive approach in terms of identifying the technologies that will meet the required performance
- The project will explore various motor topologies; some include no magnets at all and some include non-rare earth magnets
- Some of the motor topologies use only conventional materials while others will be enabled by advanced materials that will be developed under the project
- Advanced materials including magnetic as well as electrical insulating materials will be developed to enable the motors to meet the required set of specifications
- Advanced motor controls and thermal management techniques will also be developed.
- By evaluating the wide range of motor topologies and advanced materials, don-selected topologies/materials are expected to meet the required set of specifications

(B) Approach:

Motor Development:

- Perform tradeoff study of various motor topologies
- Identify promising scalable materials and produce coupons showing the expected properties
- Down-select promising topologies/materials
- Design/build/test 2-3 proof-of-principle motors
- Down-select final motor topology

- Design/build/test 3 identical motors as the key project deliverable(s)
- Develop cost model for the final motor

Materials Development:
 The materials development approach for Phase I of the project is to develop the structure/processing/properties relationships of four categories of motor components being made with novel materials. The Phase I materials tasks will produce and characterize samples of the new materials and will culminate in the selection of materials for scaled-up production in subsequent Phases.

Major Accomplishments

(A) Motor accomplishments:

- Finalized the motor topologies that will be evaluated and in the process of evaluating 9 of them
- Identified the theoretical properties for the advanced materials to be developed to use them in the motor topologies evaluation
- Most of the contracts with our external partners are in place and technical collaboration already started

(B) Materials accomplishments:

Each of the motor component materials have met the milestones assigned to them for the first year of Phase I

Future Direction

FY13

- Down-select 2-3 promising motor topologies
- Down-select promising advanced materials
- Build proof-of-principle motors/materials

FY14

- Test proof-of-principle motors/materials
- Final selection of motor topology/materials based on test results of proof-of-principle motors
- Initiate design for final motor (s)



Technical Discussion

(A) Motor Development:

Several motor topologies have been evaluated. Most of them completely eliminate rare-earth materials while few eliminate the most critical rare-earth materials. The figures below show comparison between the various options vs. the baseline rare-earth IPM motor. Even though the various topologies are at different maturity levels, some are showing promising performance in terms of power density and/or efficiency

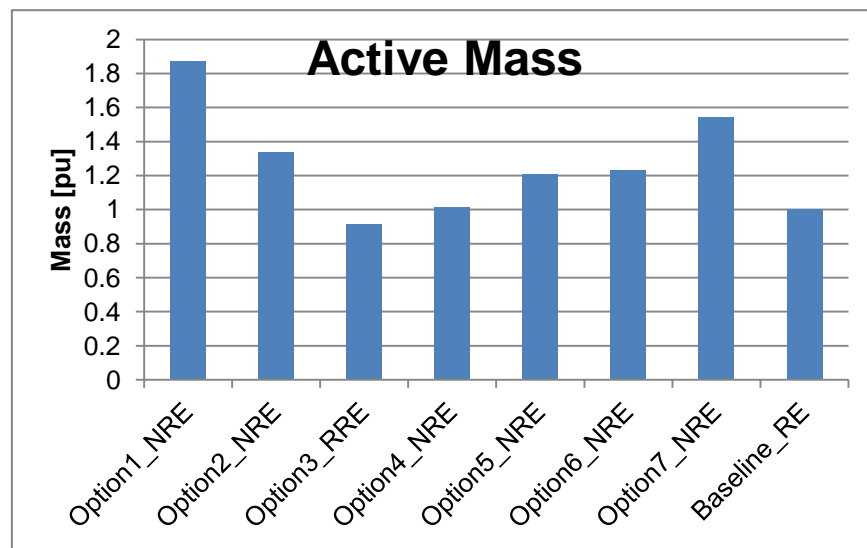


Figure III - 17: Comparison of motor topologies in terms of active mass.

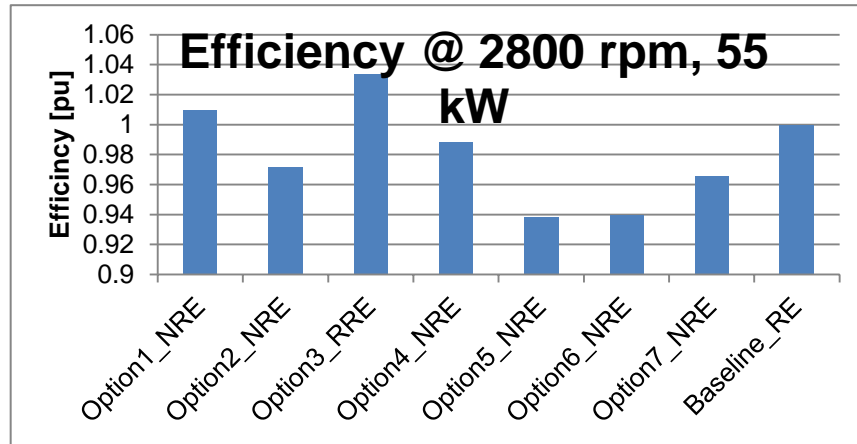


Figure III - 18: Comparison of motor topologies in terms efficiency @ 2800 rpm and 55 kW.

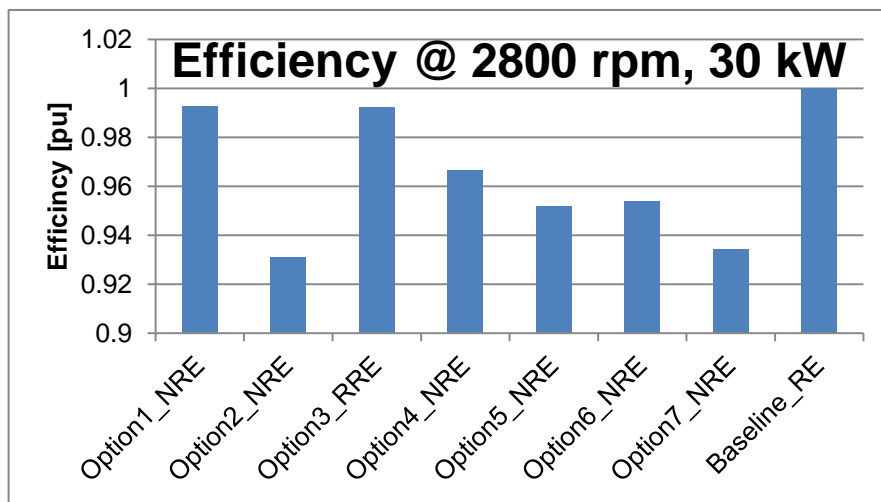


Figure III - 19: Comparison of motor topologies in terms of efficiency @ 2800 rpm and 30kW.

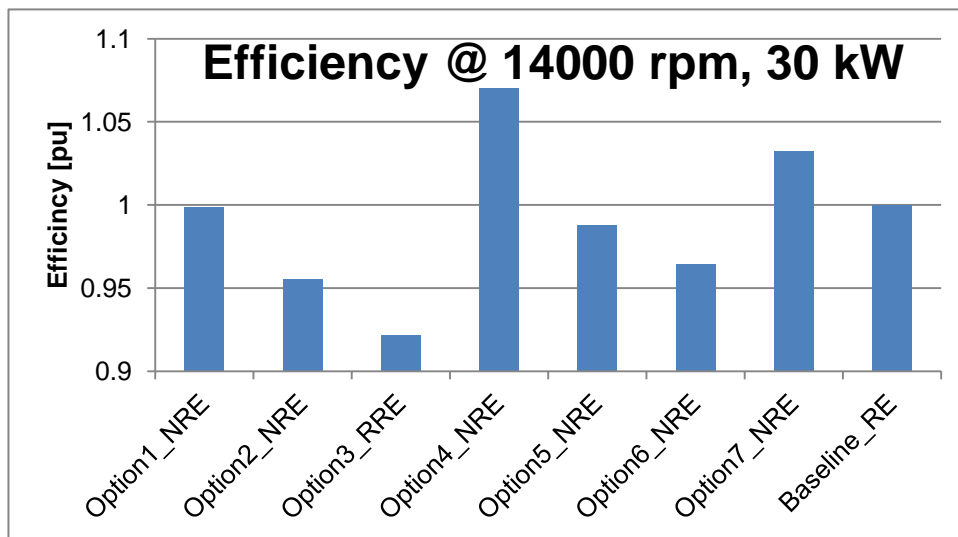


Figure III - 20: Comparison of motor topologies in terms of efficiency @ 14000 rpm and 55 kW.

(B) Materials Development:

Progress has been made in improving the performance of advanced magnetic and dielectric materials being used

as motor component materials. The systematical investigation of composition/processing/structure/property relations has strongly indicated that the measured

demagnetization behavior of non-rare-earth permanent magnet materials.

A single processing stream for producing improved steel laminates has been developed and the repeatability of the selected process has been demonstrated. The ability to roll the material to a 14 mil thickness, similar to that used in conventional motor laminations, has been demonstrated (Figure III - 21).



Figure III - 21: Sheets rolled to 14 mil thickness of improved soft magnetic laminates.

A series of polymeric films have been developed and evaluated. Two candidates have shown superior thermal performance to conventional polyimide film such as Kapton® film (Figure III - 22). The weight losses of films at 320°C were measured over the period of four to five thousand hours. At the end of five thousand hours, the weight losses of two high temperature (HT) film candidates are less than 3%, while Kapton® polyimide film showed more than 10% weight loss after only four hundred hours. Therefore, polymer film dielectrics that withstand operating temperatures in excess of 280°C have been developed for future insulation system development and motor integration.

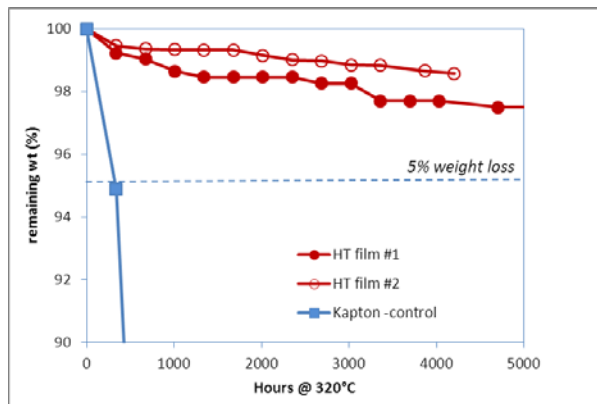


Figure III - 22: Remaining weight of films after aging at 320°C.

Conclusion

There is significant progress made in terms of evaluating the various motor topologies. Some of them show promising performance both in terms of power density and/or efficiency compared to rare-earth IPM motors. Also significant progress made in terms of developing the advanced materials. Coupons have been

produced and tested and some are showing promising results.

Significant progress has been made in developing advanced magnetic and dielectric materials for use as motor components. Structure/processing/properties relationships have been determined. Initial test coupons have been produced and characterized. All materials components have met their property milestones and work on all will continue into FY2013.

Patents

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2. US8,222,855B2 "System and method for non-sinusoidal current waveform excitation of electrical machines", July 17, 2012
3. US8274190, "Electric machine rotor bar and method of making same", September 25, 2012.

III.5 Permanent Magnet Development for Automotive Traction Motors

(Co-funded by Agreement 13295 – Propulsion Materials)

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Objectives

- Develop the materials and processes needed to fabricate high performance permanent magnets (PM) that can be used for advanced traction drive motors with an internal PM rotor design to meet APEEM goals for enhanced performance at elevated temperature (180-200°C) and reduced cost.
- Anisotropic magnets should be developed to satisfy the need for magnets with maximum magnetic energy density and minimum content of valuable materials. If possible, improved magnet forming processes and mechanical properties also should be developed to further reduce motor manufacturing costs and extend lifetime in service.
- While magnet materials meeting the technical specifications are currently achieved using rare earth (RE) permanent magnets, the market factors of rising RE demand, uncertain RE cost, and near total foreign control of RE supplies dictate that alternative non-RE magnets must be developed.

Approach

This program consisted in FY2012 of two major thrust areas.

- **Thrust Area 1:** Continued investigation of ***RE anisotropic*** permanent magnets, driven by industry needs, placing effort on generating anisotropic particulate for bonded magnets and on novel processing of sintered RE permanent magnets, exploiting the improved high temperature tolerance of the Ames mixed rare earth (MRE)-Fe-B alloys to minimize or eliminate the use of Dy.
- Developed aligned microstructures in MRE-Fe-B magnet alloy particulate with little or no Dy content, preferring controlled rapid solidification as a low cost route to make large gains in net-shape bonded magnet strength and reduced magnet cost and waste for simplified motor manufacturing.
- Refined processing of anisotropic sintered permanent magnets of MRE-Fe-B alloys with little or no Dy content by single stage hot deformation (SSH) to enable the maximum energy product to be realized in bulk magnets starting from Zn-coated amorphous flake particulate, using pressure-driven liquid phase densification/crystallization/sintering, and producing aligned nano-grained magnets.
- **Thrust Area 2:** New high strength ***non-RE anisotropic*** permanent magnets will be developed that meet the requirements for advanced interior PM electric traction motors. The investigation will involve theory and modeling efforts, as well as experimental synthesis of magnet compounds and prototype magnet fabrication and characterization.
- Near-term development of non-RE anisotropic permanent magnets is focused on attempts to improve the best of the non-RE systems, alnico, by using modern high-resolution characterization techniques to gain enhanced knowledge of coercivity mechanisms in existing alnico magnet types and, then, by developing innovative alloying and processing to improve coercivity and magnetic energy product using greater control of nano-structure and microstructure.
- Long-term development of new non-RE anisotropic permanent magnets also is pursued with significant input from theory and modeling, seeking to discover novel phases based on Fe-Co-X with beneficial

intrinsic properties, i.e., high Curie temperature, magnetization and magnetic anisotropy.

- If the new non-RE permanent magnet phases have insufficient magnetic properties as single-phase magnets, increased properties will be sought by further extrinsic manipulation, including use of a soft magnetic second phase to produce enhanced exchange coupling.
 - It should be noted that this task area is extremely high risk, but if successful it will revolutionize the cost structure of permanent magnet motors and reduce the reliance on foreign controlled commodities for hybrid and electric vehicle production.

Major Accomplishments

- Developed new single stage hot deformation (SSHD) method to fabricate fully dense anisotropic magnets from Zn-coated glassy $MRE_2(Fe,Co)_{14}B$ flake with reduced Dy content. Key parts of this development included design and implementation of a high purity method for Zn evaporative coating of magnet alloy flake particulate, innovative pressure and temperature cycle design, and TEM characterization that revealed Zn penetration of aligned nano-crystalline grain boundaries.
- Completed detailed microstructural and semi-quantitative chemical analysis, including 3-D atom probe studies, of non-RE commercial anisotropic alnico types 5-7, 8, and 9, in the finished magnet condition.
- Quantified differences in nano-scale morphology and structure between transverse (normal to direction of applied field during magnetic annealing) sections of alnico 5-7 with the classical (magnetic) bcc Fe-Co “bricks” and (non-magnetic) B2 AlNi “mortar” pattern in a ratio of about 2:1, (bcc):(B2), compared to the unusual alnico 8 & 9 pattern of “mosaic tile” with bcc Fe-Co faceted “tiles” and $L2_1(Ni,Co,Fe)_2AlTi$ matrix phase in a ratio of about 1:1, (bcc):(L2₁). The (magnetic) bcc:matrix ratio difference can be significant in the higher remanence/saturation of alnico 5-7.
- Discovered further nano-scale details of complex matrix phase in alnico 8 & 9, including discovery of pure Cu nano-rod phase at “points” of Fe-Co tiles and Fe-Co precipitates in the L2₁ matrix, as well as an unexpectedly high Co and Fe content in the matrix phase of both alnico 5-7 and 8 & 9, which seems to represent a “wasted” alloy addition, especially of valuable Co.
- Quantified more differences in nano-scale morphology between alnico 5-7 and 8 & 9, most importantly between the shape anisotropy for the bcc Fe-Co phase in longitudinal (parallel to direction of applied field during magnetic annealing) sections, where 5-7 has about 1:3 (width:length), compared to about 1:10 for 8 & 9. This shape difference can be significant in the much higher coercivity of alnico 8 & 9.
- Used magneto-optic Kerr effect (MOKE) observations to correlate length scale of apparent domain wall pinning sites to micron-scale features in cast alnico 5-7 and 9 magnets.
- Analyzed grain boundaries and product phases on micron-scale (with SEM) in commercial sintered (powder processed) alnico 8 finished magnets and identified composition of “contaminant” grain boundary phases.
- Performed theoretical analysis of possible impact from high Co and Fe content in matrix phase of alnico 5-7 and 8 & 9, using 3-D atom probe measurements, and determined that matrix phase in both alnico types may be ferromagnetic, which can negatively impact nano-scale interface effect on coercivity and points to possible benefits of alloy modifications or processing (annealing) changes to enhance coercivity.
- Used theoretical tools based on genetic algorithm (GA) on existing computer clusters and initial time on supercomputers (NERSC and Jaguar) to expand investigation of potential new Fe-Co-X phases, with special emphasis on alloying into Co_7Hf and Co_5Zr with Fe and other 4d and 5d elements and established some initial correlations with findings of exploratory experimental findings.
- Exploratory combinatorial synthesis work on Fe-Co-X systems, where X=5d and 4d (e.g., W, Ta, Mo, Hf) demonstrated (for X=Mo) formation of an aligned columnar structure with nano-metric spacing that demonstrated single permanent magnet phase behavior with a coercivity of about 2 kOe over a significant composition range, somewhat reminiscent of alnico.
- In experimental synthesis investigations, a capability for dual beam cluster deposition in an applied field was developed and demonstrated for producing aligned nano-metric exchange coupled magnet samples from separate sources of Fe-Co and Co_7Hf nano-particulate. In a similar pursuit, a chemical synthesis approach was developed for producing a nano-composite magnet sample of Fe-Co-W in a Fe-Co matrix.

Future Directions

- Continue focused work on improved processing of ***RE anisotropic*** permanent magnets, stepping up

studies on innovative processing of sintered (fully dense) anisotropic RE permanent magnets, exploiting the improved high temperature tolerance of the Ames mixed rare earth (MRE)-Fe-B alloys, pushing for little or no Dy content.

- Further develop SSHD method to fabricate fully dense anisotropic magnets from Zn-coated glassy $MRE_2(Fe,Co)_{14}B$ flake with lower Dy content and verify high temperature stability and perform preliminary experiments on comminution of finished magnets to generate anisotropic magnetic powder for experiments on producing high performance net shaped bonded magnets.
- In the effort to develop new high strength ***non-RE anisotropic*** permanent magnets that meet the requirements for advanced interior PM electric traction motors, accelerate the near-term prospects for enhanced alnico by continued efforts to understand coercivity mechanisms and the linkage to microstructure that can be controlled in bulk alnico magnets. Enhance progress on long-term magnet prospects by applying the increased speed of supercomputer calculations (using 45M node hours just granted on a FY2013 INCITE award to B. Harmon and K-M. Ho) to more focused composition regions of the selected Fe-Co-X systems, following the down-selection of promising magnet alloy compositions from early FY2012. In general, it is critical that the investigation maintains the close collaboration of theory and modeling efforts, of experimental magnet material synthesis work, and of detailed characterization studies on the new materials.
 - Provide detailed characterization results, including 3-D atom probe, TEM, and SEM, on heat treated commercial alnico samples and on experimental chill cast modified alnico alloy samples to allow improved selection of alnico compositions and development of better bulk magnet processing approaches, including advanced powder processing.
 - Expand use of MOKE, magnetic force microscopy (MFM), and hysteresisgraph measurements to observe domain wall pinning and hysteresis values for correlation with microstructural analysis results at all relevant magnifications to gain more complete and useful knowledge of alnico coercivity mechanisms.
 - Produce fully pre-alloyed alnico powder, initially centered on a preferred alnico 8 composition, and consolidate to full density with subsequent magnetic annealing and heat treatments designed on the basis of improved understanding of magnetic property optimization.

- Extend exploration with theoretical tools to investigate possible alnico interface/phase configurations and potential new Fe-Co-X phases on existing clusters and supercomputers (access from new INCITE award).
- Based on theoretical guidance, pursue promising regions of ternary Fe-Co-X systems for further investigation by full suite of experimental synthesis methods.
- Maintain WebEx contact and bi-annual workshops with team.

◇ ◇ ◇ ◇ ◇

Technical Discussion: [Research Highlight Examples]

New Understanding of Alnico Magnets Helps Design Improvements to Boost Properties for Drive Motors (Kramer, McCallum, Constantinides, Anderson)

Atomic-scale characterization and theoretical analysis provide clues about how rare earth-free alnico magnets can be improved for drive motor use with changes in processing and alloy design: Alnico magnets have been selected as the best near-term candidate to replace rare earth (RE) magnets in permanent magnet (PM) motors for HEV and PHEV drive systems. While these aluminum-nickel-cobalt-iron (Al-Ni-Co-Fe) PM alloys have been used widely since 1940s, their development was “on hold” for about 40 years; displaced by superior RE magnets, especially neodymium-iron-boron (Nd-Fe-B) which have a 5 times energy product (MGOe) advantage at room temperature. However, for traction motors, wind power generation and other elevated temperature uses (above 180°C), Nd-Fe-B has only a 20 MGOe vs. 10 MGOe margin over the best [1] alnico (type 9), which also has many advantages over Nd-Fe-B, including superior corrosion resistance and broadly available alloy constituents, although Co costs are relatively high.

Alnico magnets that can match Nd-Fe-B at motor operating temperatures basically will require increased resistance to field reversals, yet there is scant understanding of these “coercivity” mechanisms for alnico magnets, beyond a preference for high content of magnetic Fe-Co (bcc) “bricks” that are highly elongated for “shape anisotropy” in a non-magnetic “mortar” (matrix). Our new study uses modern atomic-scale characterization on 3 types of commercial anisotropic (strongest) alnico magnets.

Significant differences (see copper nano-rods) were found in the nano-scale morphologies and, especially, in the structural/chemical make-up of matrix phases for different alnico magnet types. One shocking observation was that the best alnico, which contains 1.5X the Co

content of the classical alloy, appears to “waste” nearly half of this Co by trapping it in the matrix phase that is supposed to be non-magnetic. Recent theory results suggest that this useless Co may even degrade the magnetic strength. These findings direct us to substitute lower cost elements, e.g., Ni, Cu, Mn, for the Co, if possible, saving up to 20% of the alloy cost and perhaps improving the magnets. Linked microstructure and magnetic domain observations showed that promise for raising alnico strength also lies at the 10-100 micron scale, prime for our powder metallurgy methods. These pathways to improved alnico should allow us to double the energy product and reduce the cost by at least 10%, in contrast to the predicted upward cost trajectory for Nd-Fe-B magnets, especially with significant added Dy for high temperature tolerance.

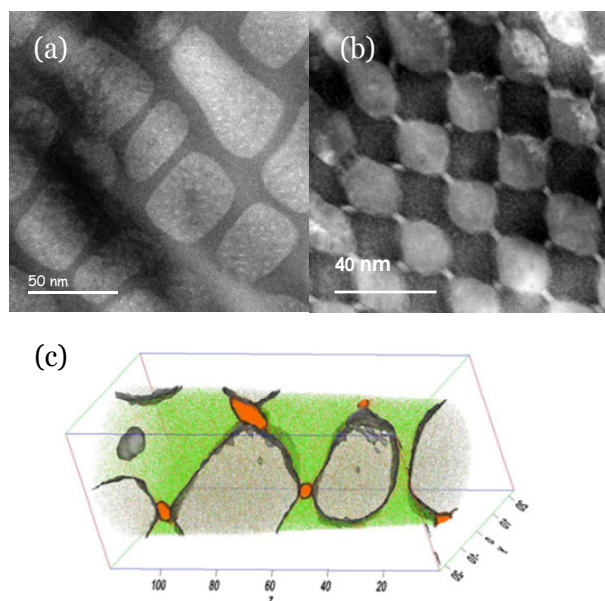


Figure III - 23: Collection of micrographs showing (a) STEM image of the 5-7 alloy showing the ‘brick-and-mortar’ morphology, and (b) shows a ‘mosaic-tile’ morphology in alnico 8. Atom probe tomography (c) shows the isolated copper (orange) at the ‘tile’ points in 8. The Fe-Co phase is light gray regions. APT was obtained with collaboration of M. Miller at the ORNL ShaRE User Facility, sponsored by BES.

Development of Single-Stage Hot Deformation for Anisotropic Magnets from Zn-coated MRE-Fe-B Flake Powder (McCallum, Anderson, Kramer)

Simplification of the process for conversion of amorphous melt spun flake particulate to anisotropic nano-crystalline magnets can also benefit from high temperature tolerance of MRE-Fe-B alloy to reduce Dy use: Commercial anisotropic magnets (termed MQ-III) used over-quenched flake particulate to avoid casting segregation/annealing, but needed very expensive two-stage hot deformation process (hot pressing and die-upset forging) to produce fully dense magnets from Nd-Fe-B alloys. Eventually the pressure of the marketplace force

MQ-III out of the commercial arena, i.e., it is no longer a commercial product. In our studies, a new single stage hot deformation (SSHD) method (see Figure III - 24) is being developed to fabricate fully dense anisotropic magnets from Zn-coated glassy $MRE_2(Fe,Co)_{14}B$ flake with high temperature stability and reduced Dy content [2].

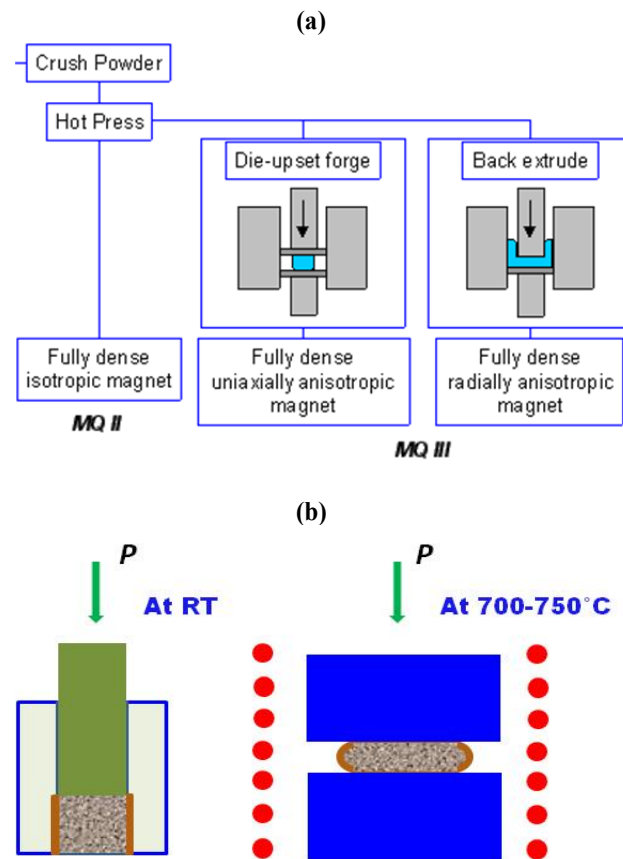


Figure III - 24: Schematic comparison of: a) two stage hot deformation in the MQ III process and, b) the pre-compaction step at room temperature (RT) and single hot deformation stage of the new SSHD process.

The idea of using a very small addition (ideally a very thin surface layer) of low melting Zn is for “lubrication” of the flake particulate during initial hot pressing just above the Zn melting point to promote re-arrangement and densification of the flake particulate to full density (Figure III - 25). A continued temperature rise at full pressure is intended to promote full crystallization of the flake under a uni-axial stress that promotes aligned growth of nano-crystals to ~30-60nm by ~150-300nm (Figure III - 25).

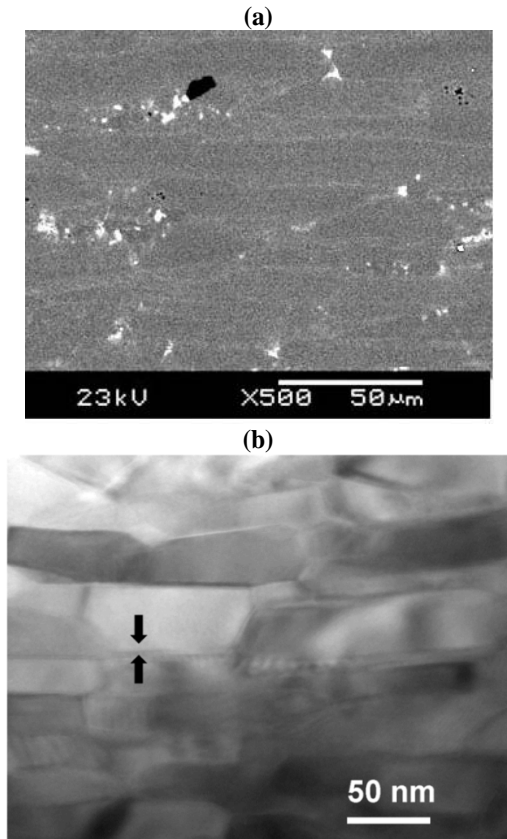


Figure III - 25: Micrographs showing, a) full densification for flake particulate 1% Zn addition (light contrast) as a surface plating and, b) TEM micrograph of aligned nano-crystalline grains within a transformed flake particle after pressing above the crystallization temperature.

SQUID magnetometer measurements indicate coercivity of 10.8 kOe and 21.3 MGOe for only 1% Zn content (sample in Figure III - 25a), showing ability for full consolidation. Further TEM studies are needed to probe interfacial reaction products at nano-grain interfaces. High temperature magnetometer measurements are needed to determine temperature coefficients of coercivity and remanence and to establish the lower limit of Dy needed to permit magnet operation above 180°C.

Computational Prediction and Discovery of Magnet Materials (Wang, Ho, Harmon)

This computational project is in close collaboration with experimental synthesis and processing groups lead by Ames Laboratory that are striving to meet the goal of the development of PM materials to meet performance and cost goals for advanced electric drive motors: Promising material structures have been explored in Fe-Co-X systems in a range of stoichiometries around target compositions which were identified as candidate new non-RE magnet alloys. Crystal and interface structures were predicted at the atomic level using a genetic algorithm (GA) with first-principles density

functional calculations for the energy and properties evaluations.

This research has been focused on computational prediction of crystal structures of HfCo_7 , $\text{Hf}_2\text{Co}_{11}$, $\text{Zr}_2\text{Co}_{11}$ and related alloys. The choice of systems was motivated by experimental observations that Hf-Co and Zr-Co alloys could be promising materials for high performance permanent magnet without rare-earth due to their high magnetic anisotropy [3,4]. The magneto-crystalline anisotropy K_1 of HfCo_7 alloy is 1.3 MJ/m^3 along with an appreciable saturation magnetic polarization J_s of 8.9 kG [3]. $\text{Hf}_2\text{Co}_{11}$ alloy also exhibits similar magnetic anisotropy to that of HfCo_7 phase. It was also reported that $\text{Zr}_2\text{Co}_{11}$ has high uni-axial anisotropy (1.1 MJ/m^3) and the Curie temperature is around 500 °C [5-7]. Moreover, doping Fe into HfCo_7 alloy and B into $\text{Hf}_2\text{Co}_{11}$ alloys was shown experimentally [12] to further improve the anisotropy and saturation magnetic polarization. However, the crystal structure of these alloys remains elusive. Different experiments [3, 7-12] suggested different crystal structures and the number of atoms in the unit cell proposed by experiment is also controversial and ranges from 16 to about 120 atoms. The uncertainty in the crystal structures greatly hinders further investigation and optimization of the structures and properties of the materials for high quality permanent magnets.

Using the computer time allocation on NERSC through the NISE program, a systematic search was performed to determine the low-energy atomistic structures for HfCo_7 , $\text{Hf}_2\text{Co}_{11-x}$ (Figure III - 26) and $\text{Zr}_2\text{Co}_{11-x}$ alloys (with $x=0.0, 0.5, 0.6, 0.8$ respectively) with the number of atoms in the unit cell ranging from 16 to 117. The computational algorithm and code used in this global structure search is the first-principles adaptive genetic algorithm (GA) code developed recently by our group at Ames Laboratory under the support of DOE-BES [13-15]. Through this global search, we predicted the lowest-energy structures for HfCo_7 up to 64 atoms per unit cell and those for $\text{Hf}_2\text{Co}_{11-x}$ (see Figure III - 27), as well as those for $\text{Zr}_2\text{Co}_{11-x}$ up to 117 atoms per unit cell. Preliminary comparison of the calculated X-ray diffraction spectra from our structure models with available experimental data [12] is very encouraging, e.g., for $\text{HfCo}_{5.25}$ (Figure III - 28).

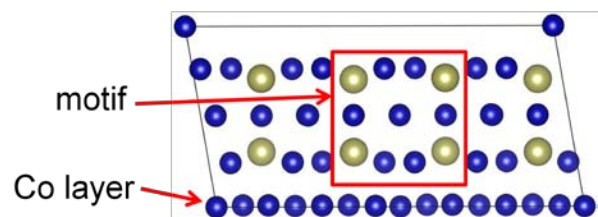


Figure III - 26: Example of atomic plane portion showing repeating motif from $\text{Hf}_2\text{Co}_{11-x}$ studies with GA code.

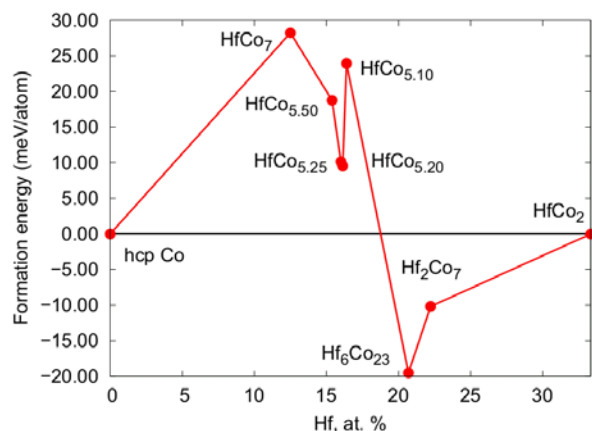


Figure III - 27: Summary of free energy of formation relative to hcp Co for calculated phases in Co-Hf.

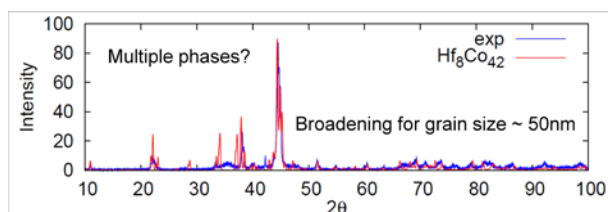


Figure III - 28: Comparison of calculated and experimental [3] X-ray diffraction patterns for apparent $\text{HfCo}_{5.25}$ phase.

As mentioned above in Figure III - 28, because of possible mixed phases in the experimental samples, careful analysis of experimental X-ray data in comparison with the X-ray spectra from the theoretically predicted structure models is underway. We are working closely with Prof. D. Sellmyer's group at University of Nebraska at Lincoln (UNL) and the experimental groups at Ames Laboratory (M. J. Kramer, W. McCallum, and I. Anderson) on these analyses in order to finally resolve the structures of these phases. At the same time, we also collaborate with Dr. V. Antropov's group at Ames Laboratory to study the magnetic properties of the structures obtained from our search. The preliminary results indicate that these structures exhibit reasonably high magnetic anisotropy and are promising for permanent magnetic applications.

Conclusions

In experimental research on RE magnets, the development of a new single stage hot deformation (SSHD) method to fabricate fully dense anisotropic magnets from Zn-coated glassy $\text{MRE}_2(\text{Fe,Co})_{14}\text{B}$ flake is promising as a manufacturing process for near-net shape fully dense sintered magnets with reduced Dy content. Alternatively, this relatively simple approach to generate aligned nano-metric grains may also be useful for crushing into micron sized equi-axed particulate that can be blended with a high temperature polymer and molded in-place into a rotor under an alignment field for further manufacturing

advantage. Both of these directions for the process need further development to add assurance that industrial adoption can succeed and both depend on reduction or stabilization of the market for RE supplies in the future.

If the RE market rises or continues in uncertainty, we believe that the best near-term non-RE permanent magnet option is a modified version of today's alnico, based on the Al-Ni-Co-Fe system. Since coercivity is the primary deficiency for alnico, the detailed microstructural and semi-quantitative chemical analysis of commercial anisotropic alnico types 5-7, 8, and 9 in the finished magnet condition has been critical for analysis of the nano-metric and micron-scale features that contribute to long standing differences in coercivity and remanence between 5-7 and 8 & 9. Although our observations can lead one to nano-scale reasons for increased coercivity in 8 & 9 due to a far greater shape anisotropy for the Fe-Co phase, compared to 5-7, other analysis methods (MOKE and SEM-EDS) of both cast and powder processed versions of 8 & 9 are starting to show that micron-scale domain wall pinning may be more important. This observation also agrees with the theory work of our ORNL team member that suggests that the Al-Ni based matrix phase in 8 & 9 may also be ferromagnetic, not the intended non-magnetic phase. Both of these findings have guided us to specific plans for new powder processing work in FY2013, since by this route it is possible to gain control and increase the probable micron-scale pinning sites in an approach that is very adaptable to large-scale manufacturing of magnets. On the other hand, the apparent nano-scale reason for increased remanence of 5-7 is supported by our observation of a significantly greater ratio of Fe-Co phase to matrix phase (2:1), compared to the surprisingly low ratio, only 1:1, for the 8 & 9 and is very likely to be the dominant explanation. The significance here is that a coercivity increase of about 1.5-2.0X that is coupled with a remanence that maintains that of 5-7 would be likely to raise the energy product of alnico to the minimum level needed for some advanced drive motor designs.

For the long-term pursuit of alternative non-RE permanent magnet materials, we believe that the expanded and targeted efforts and initial results of our Theory Group show the value of this portion of our team for this discovery process. A prime example of the growing value is revealed by the strong interaction of the experimental synthesis studies (at Nebraska) and the structural characterization efforts (at Ames and Nebraska) with the theoretical investigations using both genetic algorithm (GA) and DFT tools (at Ames) to approach specification of a promising metastable magnetic phase, $\text{HfCo}_{5.25}$, that can be further alloyed with Fe, B, and other elements. These further complex alloying studies will be facilitated greatly by the expanded supercomputer access afforded by our very recent INCITE award and by new experimental work that works in concert with the new theory findings.

Certainly, our exploratory combinatorial synthesis work on such Fe-Co-X systems, where X=5d and 4d (e.g., W, Ta, Mo, Hf, Zr) and other dopants (e.g., B, Si, N, C) has also demonstrated its worth in providing a rapid survey tool that is useful for both theory and experiment and the recent upgrade of high rate structural and magnetic analysis capabilities have made this even more valuable. The alloy specific experimental synthesis capabilities of cluster deposition and low temperature chemical synthesis have provided new results that show potential for producing aligned nano-metric exchange coupled magnet samples, where it is likely that the cluster deposition method can reach further into the metastable phase region for these new PM compounds. However, both methods can be useful for enhancement of the magnetization of new PM phases by enhanced exchange coupling.

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Patents

1. R. W. McCallum, Y-W. Xu, I. E. Anderson, K. W. Dennis, and M. J. Kramer, U.S. Patent Application (PCT) filed November 18, 2002, "Permanent Magnet Alloy with Improved High Temperature Performance," under examination.

Awards

1. Ames Lab proposal (Harmon, Ho, Wang) selected by the DOE (20 October 2012) to receive a 2013 Innovative and Novel Computational Impact on Theory and Experiment (INCITE) award.

IV. Systems Research and Technology Development

IV.1 Benchmarking of Competitive Technologies

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Objectives

- Provide status of nondomestic electric vehicle (EV) and hybrid EV (HEV) technologies through assessment of design, packaging, fabrication, operation, and performance during comprehensive evaluations.
 - Compare results with other HEV/EV technologies.
 - Distribute findings in open literature.
- Support U.S. DRIVE program planning and assist in guiding research efforts.
 - Confirm validity of the program technology targets.
 - Provide insight for program direction.
- Produce a technical basis that aids in modeling/designing.
- Foster collaborations with the Electrical and Electronics Technical Team (EETT) and Vehicle Systems Analysis Technical Team (VSATT).
 - Identify unique permanent magnet synchronous motor/inverter/converter/drivetrain technologies.
 - Ascertain what additional testing is needed to support research and development.

Approach

- Choose vehicle subsystem.
 - Evaluate potential benchmarking value.
 - Consult with DOE, EETT, VSATT, national laboratories, industry, universities, etc. as to which systems are most beneficial.
- Teardown inverter/converter and motor/transmission assemblies.
 - Determine volume, weight, specific power, and power density.
 - Assess design and packaging improvements.
 - Conduct tests upon magnets and capacitors.
- Prepare components for experimental evaluation.
 - Develop interface and control algorithms.
 - Design and fabricate hardware necessary to conduct tests.
 - Instrument subsystems with measurement devices.
- Evaluate hybrid subsystems.
 - Determine peak and continuous operation capabilities.
 - Evaluate efficiencies of subsystems.
 - Analyze other operational characteristics.

Major Accomplishments

- Finalized dynamometer testing of the 2011 Hyundai Sonata motor, and compiled data.
- Generated efficiency contour maps and continuous operation characteristic plots for the 2011 Hyundai Sonata.
- Selected and procured the 2012 Nissan LEAF for further evaluation because it is the first mass produced, full-size electric vehicle to be sold in North America. (Note: Previous efforts included similar studies of the 2004 Prius, 2006 Honda Accord, 2007 Toyota Camry Hybrid, 2008 Lexus LS 600h, and 2010 Toyota Prius subsystems.)
 - Performed design/packing studies of the 2012 Nissan LEAF inverter and motor, which revealed a wide range of design characteristics that are specific to the continuous duty requirements of electric vehicle drive components.

- Bypassed the 2012 Nissan LEAF motor inverter controls to allow full control over testing conditions while using the LEAF’s IGBT driver board to ensure consistent inverter operation.
- Assessed mass, volume, power density, and specific power of LEAF subsystems.
- Evaluated efficiency, performance, and other operational characteristics of the LEAF subsystems.
- Communicated effectively with EETT and VSATT to aid in discerning project direction, test plan, and test results.
- Procured and received the LEAF dc-dc junction box, primary charger, and electric vehicle supply equipment and began preparations for benchmarking in FY 2013.

Future Direction

- Benchmarking efforts will focus on technologies of interest to DOE, EETT, VSATT, and others.
- Approaches similar to that of previous benchmarking studies will be taken while working to suit the universal need for standardized testing conditions.



Technical Discussion

While most of the dynamometer testing of the 2011 Hyundai Sonata motor was completed in FY 2011, tests were finalized and data were processed in early FY 2012. Design and functionality assessments were given in the FY 2011 annual report for the benchmarking project. In FY 2011 and FY 2012, the primary motor and power control/converter unit of the Hyundai Sonata were characterized during efficiency mapping and other dynamometer test assessments. As shown in Figure IV - 1, motor efficiencies reached 94% from 2,500 to 5,500 rpm for power levels near 30 kW. Motor efficiencies very briefly reached 95% at 5,000 rpm and 30 kW, and thus a contour is not shown for 95% in the efficiency map. Inverter efficiencies, shown in Figure IV - 2, were above 98% for speeds above 2,000 rpm and were fairly low for low speed operation (~92% at 500 rpm). Many operation points for speeds of 4,000 rpm and higher yielded inverter efficiencies of 98.8%. System efficiencies, shown in Figure IV - 3, peaked at 93.6% at 5,000 rpm and 60 Nm and were above 90% for medium to high power levels above 2,000 rpm. Please note that the no-load condition includes dynamometer bearing, windage, and other losses, and therefore, the no-load torque is not zero. For ideal cases where a torque level of zero is achievable, the efficiency is 0%, but it can be observed that the efficiency quickly rises from 0% with torque. For example, the no-

load torque at 500 rpm was 1.4 Nm, and the corresponding efficiency was about 41%.

Although the published power rating for the motor is 30 kW, the motor was operated up to about 35 kW at 2,000 rpm and power levels above 30 kW were also reached for speeds up to 6,000 rpm. A gray trace that represents 30 kW operation is superimposed upon all efficiency maps. The motor is essentially a surface permanent magnet motor even though the magnets are retained within rotor laminations, and therefore torque generation is largely based upon permanent magnet forces, with very little reluctance torque capability.

Continuous tests were conducted with 50°C coolant for the following test conditions: 1,000 rpm and 15 kW and both 15 kW and 25 kW at 3,000 rpm and 5,000 rpm (Figure IV - 4–Figure IV - 6). Temperature measurements are plotted

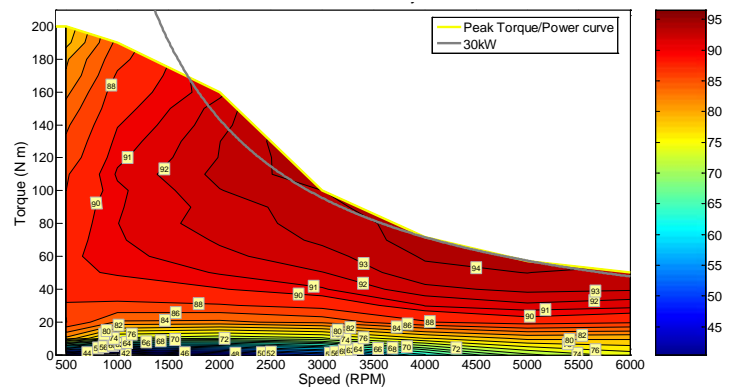


Figure IV - 1: 2011 Hyundai Sonata motor efficiency contour map.

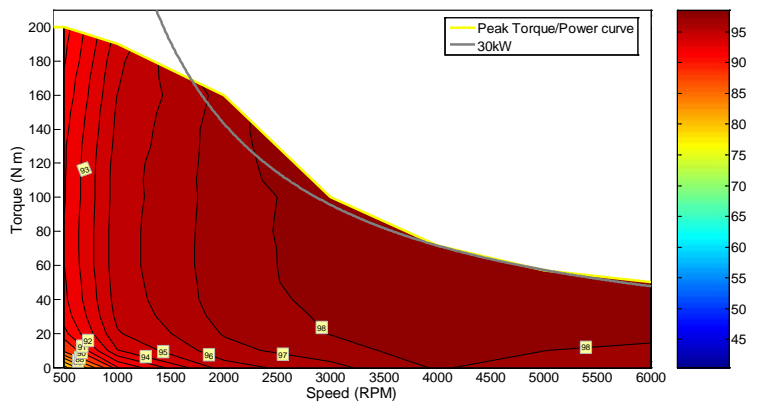


Figure IV - 2: 2011 Hyundai Sonata inverter efficiency contour map.

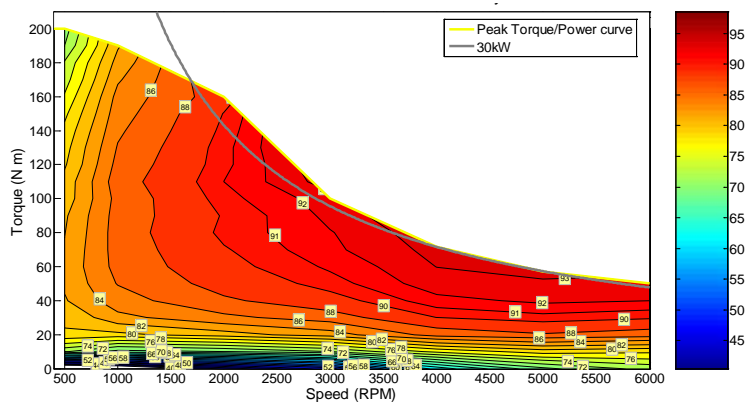


Figure IV - 3: 2011 Hyundai Sonata combined motor and inverter efficiency contour map.

versus time in Figure IV - 4, with thermocouples 1, 3, and 5 applied to the stator windings and 2, 4, and 6 located in the center of the cooling channel. Thermocouple 7 was located on the exterior of the housing at the 12 o'clock position, similar to the placement of thermocouple 2, and thermocouples 8 and 9 were located in the inlet and outlet of the oil cooling lines, respectively. For this test condition, 25 kW was maintained at 3,000 rpm for 30 min, where motor temperatures reached about 120°C and the inverter thermistor reached a temperature of about 80°C. Other tests were conducted, and the motor and inverter were operated at 15 kW and speeds of 3,000 rpm and 5,000 rpm for an hour without reaching 100°C. Operation at 25 kW and

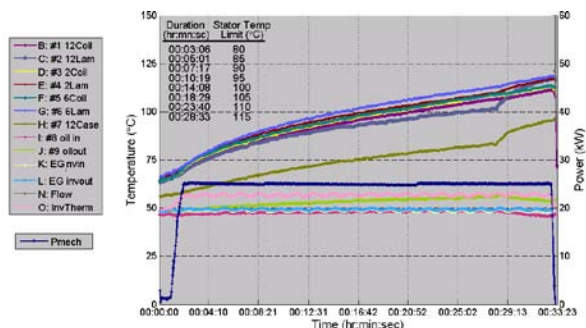


Figure IV - 4: 2011 Hyundai Sonata continuous tests with 25 kW at 3,000 rpm.

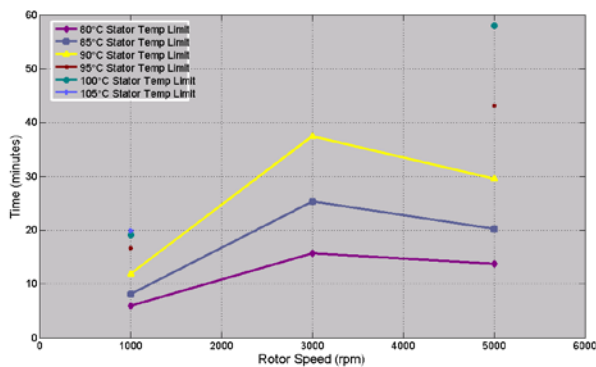


Figure IV - 5: 2011 Hyundai Sonata continuous duration capability with 15 kW.

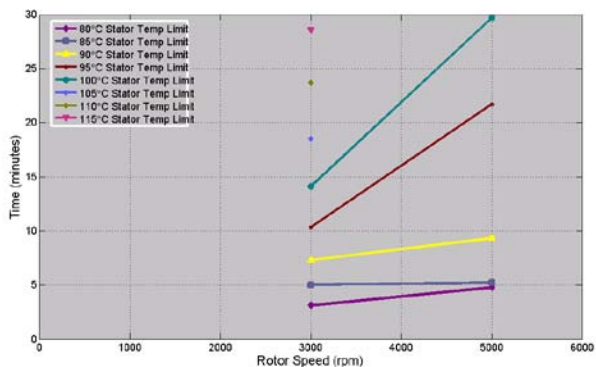


Figure IV - 6: 2011 Hyundai Sonata continuous duration capability with 25 kW.

5,000 rpm was maintained for 30 min, and stator winding temperatures reached about 100 C. Therefore, the continuous rating is close to published peak rating (30 kW) with 50°C coolant.

The Sonata hybrid starter-generator (HSG) has been analyzed for back-emf, locked rotor, and other characteristics below 6,000 rpm. During locked-rotor tests, about 150 Adc was needed to generate the rated torque of

43 Nm. This corresponds with a phase current of about 106 Arms.

The Nissan LEAF was given priority for benchmarking, and because the Sonata HSG test fixture needed improvement before high-speed tests, the Nissan LEAF electric motor was installed into the dynamometer test cell. The LEAF inverter was instrumented and the data acquisition prepared to collect electrical, mechanical power, pressure, and temperature data.

Published specifications for the LEAF indicate that the electric motor is capable of producing 80 kW and 280 Nm with a maximum speed of 10,390 rpm. The battery pack is rated at 90 kW and 24 kWh, with 48 modules and 4 modules in each cell. Argonne National Laboratory (ANL) on-the-road tests indicate that the pack voltage is between 350 and 400 Vdc most of the time. For extremely low state of charge conditions, battery voltages down to 270 Vdc were observed. At the time of purchase in early CY 2012, dealership prices for the motor, inverter, and transaxle were listed at about \$2,406, \$3,871, and \$1,562, respectively.

The Nissan Leaf inverter assembly, shown in Figure IV - 7, has a mass of about 16.2 kg. Dimensions are indicated, and the total volume is about 15.6 L with about 1.5 L of empty space below the raised portion of the lid of the inverter assembly. So it could be argued that the true volume of the inverter assembly is actually about 14 L. Inverter components are shown in Figure IV - 8. A thin, black plastic gasket is used to seal the lid of the inverter housing, whereas a liquid silicone sealant (similar to room temperature vulcanizing sealants) was used on many of the housings that were previously inspected. A 36-pin (only 25 are used) vibrant green connector interface includes various communication and power supply (low voltage) input lines. For electromagnetic interference (EMI) reduction and surge suppression, a large black ferrite clamp, made by KGS, is placed around the wire bundle between the green connector and a white 40-pin connector that interfaces with the control/interface board. The control/interface board includes voltage regulation for control and driver circuitry, communication circuitry, a microcomputer, and signal conditioning for feedback and output signals. The controller is implemented with a Renesas R5F71476FPV 32-bit RISC microcomputer that has 512 kB ROM and 16 kB RAM with 100 pins at a 0.5 mm pitch and a 16 channel 12 bit analog-to-digital converter. Position and speed feedback are carried out with a Tamagawa AU6803 resolver-to-digital chip, a common choice of most hybrid drives inspected thus far.

The main capacitor is a self-healing film capacitor made by Panasonic and rated at 600 V and 1,186.5 μF with a volume of about 1.45 L. Also within the main capacitor molding is a small 600 V, 1.13 μF capacitor and an integrated thermistor. Below the capacitor module is a dc bus bar infrastructure molded in a black composite. Large

dc conductors that interface with the battery have orange insulation and are about 1/0 AWG. A 15 W, 61 k Ω bleed resistor is connected directly to the dc interface. Two terminals for battery connectivity are located on the side of the bus bar infrastructure, and 12 terminals connect the capacitor to the power electronics modules. There are three separate power electronics modules (one for each phase), and each module has two dc terminals which connect to two terminals of the capacitor via the dc bus bar infrastructure. An ac bus bar with integrated current transducers (CTs) brings the ac output from the power electronics modules to the chassis of the inverter assembly. There are three CTs (one for each phase) with only one Hall effect integrated circuit (IC), whereas Toyota typically uses only two CT cores with two Hall effects ICs for redundancy.

The LEAF driver board circuitry is fairly consistent with approaches observed in the past, aside from the Camry's integrated driver circuit. A detailed understanding of the driver circuitry is required for a proper interface with ORNL's controller. As shown in Figure IV - 9, there are 6 insulated gate bipolar transistors (IGBTs) and diodes for each phase, with 3 in parallel for each switch, and a total of 18 IGBTs and diodes for the whole inverter. Switching of IGBTs for lower switches is powered by the same supply, a practice that is sometimes discouraged with high current and voltage systems such as these and especially with

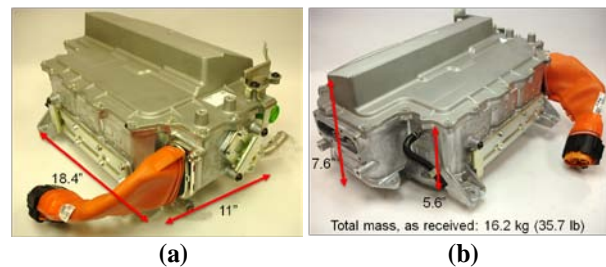


Figure IV - 7: 2012 Nissan LEAF inverter assembly: (a) x and y dimensions; (b) z-axis dimensions.

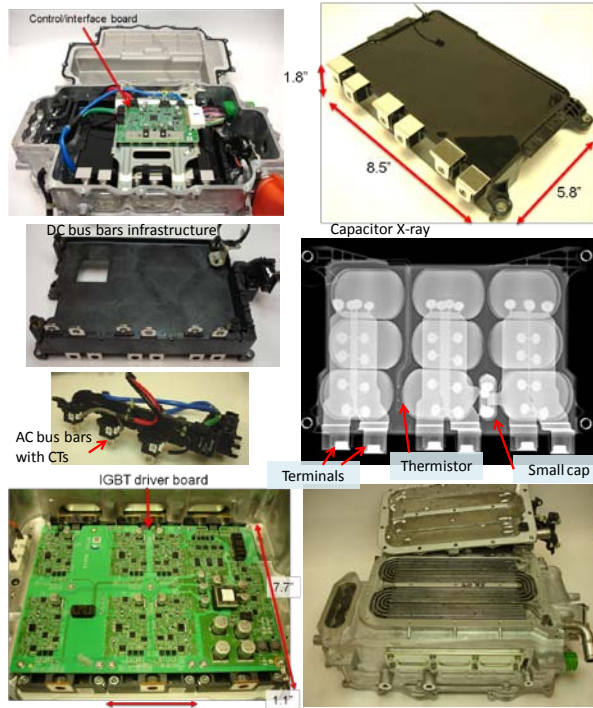


Figure IV - 8: The 2012 Nissan LEAF inverter components.

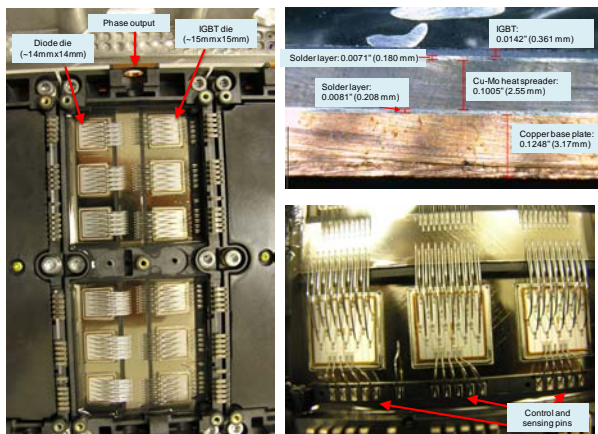


Figure IV - 9: The 2012 Nissan LEAF inverter power module and IGBT cross section.

multiple devices in parallel. Including the supplies for the upper switches, there are a total of four isolated supplies for IGBT switching. Signals from all three of the lower IGBTs on the V-phase on-chip temperature sensing diodes are passed through active filters for crude temperature feedback and over-temperature fault protection. For a given current flowing through the small p-n junction, which is separate from the IGBT, the resulting voltage varies with temperature, and therefore, the IGBT junction temperature can be approximated. The dc-link voltage is sensed after it is dropped with four 180 kΩ resistors (0.718 MΩ total), which are connected to the collector of the V-phase upper switch.

Through coordination with the ORNL packaging laboratory, the power module stackup was analyzed and is shown in the upper-right portion of Figure IV - 9. The IGBT is about 0.361 mm thick, and it is soldered to a 2.55 mm thick Cu-Mo heat spacer for matching of thermal expansion to avoid mechanical fracturing during thermal cycling. The Cu-Mo heat spreader is soldered to a 3.177 mm thick copper baseplate, which is at the bottom of the power electronics module. There are six copper baseplates in the inverter, and the three upper collectors are connected to the copper plate and the positive supply voltage and the three lower collectors are connected to the copper plate and the phase output. This may result in EMI problems as this can result in increased coupling to the chassis of the inverter. Since the copper baseplates must be isolated from the chassis, a thin silicon-based insulation sheet is located between the power electronics modules and the aluminum cooling interface, with thermal paste applied to each side of the insulation sheet. This is quite different from the modules in many of Toyota's products, and many IGBT packages on the market, as these products have the electrical insulator (typically an aluminum nitride or silicon nitride based ceramic) integrated in the module, and only one layer of thermal paste is needed since the baseplate is electrically isolated. Therefore, the LEAF thermal stackup (directly related to the capability of heat to be removed) is likely inferior to this type of design. The IGBTs are about 15 mm by 15 mm, and the diodes are about 14 mm by 14 mm. The IGBTs are estimated to have ratings of 800–1,000 V and 300 A each.

The LEAF has a direct drive traction system with a constant gear final drive ratio of 7.94. With stock 205/55 R16 tires and a 2% deformation factor, the rotational speed of the motor in revolutions per minute is roughly 109.4 times the vehicle speed in miles per hour. Therefore, motor speeds of 7,000 rpm and 10,300 rpm (the rated speed) correlate with vehicle speeds of 64.0 and 94.1 mph. As shown in Figure IV - 10 and Figure IV - 11, the total mass of the motor assembly is about 56 kg (123 lb) and the mass of transaxle/gear assembly (not shown) is 26.8 kg (59 lb). A small 12–8 switched reluctance motor made by DENSO is used to engage the parking gear. The transaxle has three gear axes, including the drive gear (connected to the motor), final gear, and differential. Interestingly, there are spring-loaded brush contacts which connect the shaft of the final gear to the chassis. This is likely implemented to reduce bearing currents, which can cause pitting and bearing damage, but the brushes are not in contact with the same shaft/axis that the motor rotor is connected to, so it would seem that bearing currents are still possible in the motor rotor bearing.

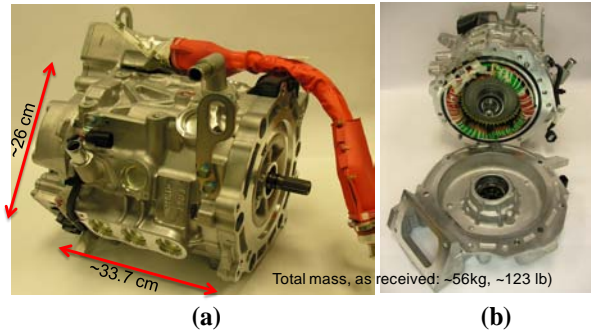


Figure IV - 10: The 2012 Nissan LEAF motor: (a) showing dimensions and (b) partially disassembled, showing end turns.

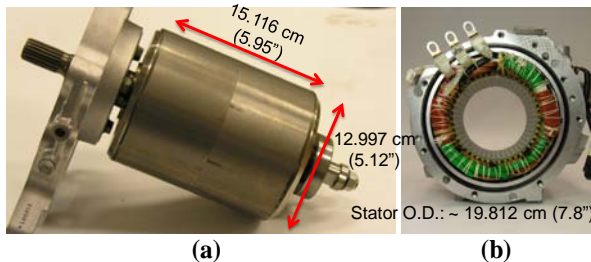


Figure IV - 11: The 2012 Nissan LEAF motor rotor (a) and stator (b).

The stator and rotor outer diameters are about 19.8 cm (7.8 in.) and 13.0 cm (5.12 in.), respectively, with a stack length of about 15.1 cm (5.95 in.). Overall, the design and shape of the motor closely resembles that of the Lexus LS 600h. It is an eight pole permanent magnet machine with 48 slots. The power conductors between the inverter and motor are about the size of a standard 3/0 AWG cable. Because the motor must be fully capable of handling continuous conditions, the size of the conductor must be quite large so the conductor resistance is lowered and therefore larger amounts of currents are possible without overheating. However, for a given slot size, increasing the size of the conductor (which actually comprises many small conductors, a.k.a. “wires in-hand”) decreases the amount of turns that can be placed in the slot, and therefore, a higher amount of current is required for a given torque. The cast aluminum motor housing has an exterior water jacket that has three loops with uniform cooling around the entire motor. Casting these types of cooling channels within the water jacket increases the complexity of the motor housing casting process. Many circular recesses are visible, which may serve as freeze-out plugs, but their primary purpose is likely for the casting process—to provide a mold for the cooling channels and for the removal of sand after a sand-casting process.

ORNL designed an adaptor shaft and support plate to interface the LEAF motor with the dynamometer test setup. The test setup is shown in Figure IV - 12. An ORNL controller is used to supply gate command signals to the input of the LEAF driver board optocouplers, thereby facilitating use of original equipment during the tests.

Using custom ORNL controls allows for operation at any point in the operation map for any desired amount of time as long as thermal limits are not breached. A nested d-q vector PI controller was used with speed-regulated PI control and space-vector modulation. Position feedback was implemented using the integrated LEAF resolver, which is relatively small and has 10 stator poles and 4 rotor poles. A coolant temperature regulator was used to maintain an ethylene-glycol coolant temperature of 65°C. Based on data from ANL on-the-road tests, ORNL picked a dc bus voltage of 375 Vdc because the battery voltage was mostly in the range of 350 to 400 Vdc, depending on the state of charge.

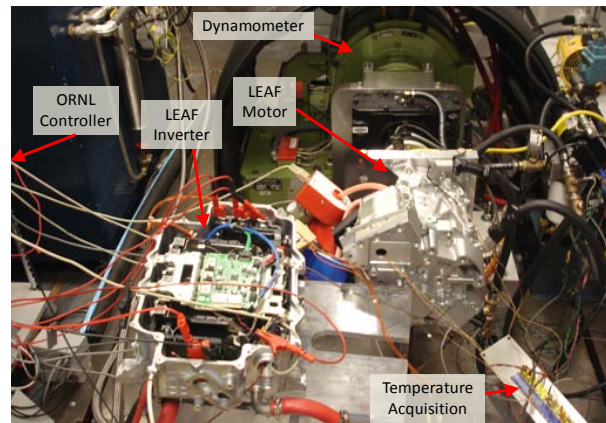


Figure IV - 12: The 2012 Nissan LEAF motor and inverter test setup with dynamometer.

Locked-rotor tests were conducted; the LEAF has a relatively low torque-per-amp ratio as almost 625 A were required to produce the published torque rating of 280 Nm. Similar to the 2008 LS 600h, high levels of magnetic saturation are not indicated in torque-per-amp values as current increases. These characteristics were expected based on the lower operation voltage of 400 V (compared to Toyota systems), large motor power lead size, and duty requirements of an all-electric vehicle. Motor temperatures were only slightly elevated when continuously applying current up to 200–300 A for tens of minutes. A considerable level of reluctance torque is observed from the graph in Figure IV - 13, where locked-rotor torque is plotted versus electrical position.

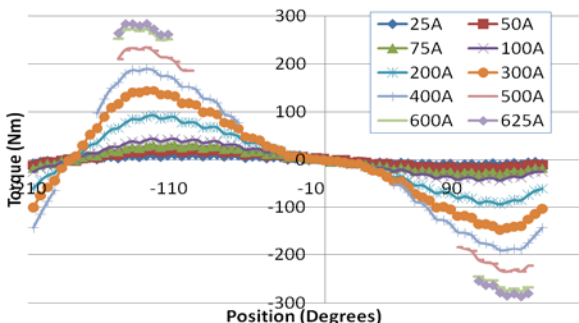


Figure IV - 13: The 2012 Nissan LEAF motor locked-rotor torque versus position.

Efficiency and performance mapping was conducted up to published torque and power ratings of 280 Nm and 80 kW, respectively. The peak torque capability of 280 Nm was reverified during rotational tests, with a maximum current of above 443 Arms required for peak torque at low speeds. Higher speeds require a slight increase in current to produce peak torque, and ultimately voltage limitations are reached near 4,000 rpm, and peak torque is not reachable. However, since a lower amount of torque is required to produce a given power as speed increases, a power level of 80 kW was reached at 3,000 rpm. Tests were conducted up to 85 kW from 3,000 rpm up to 10,000 rpm, and test conditions indicated that even higher power levels are attainable. Other secondary studies will be conducted before operating above published power levels, thereby avoiding the risk of fault or demagnetization until all secondary studies are complete.

The motor efficiency map in Figure IV - 14 indicates peak efficiencies above 97% between 5,000 and 9,000 rpm for high power levels. A very significant portion of the operation map yields operational efficiencies above 90%, and LEAF motor efficiency is below 70% only for low

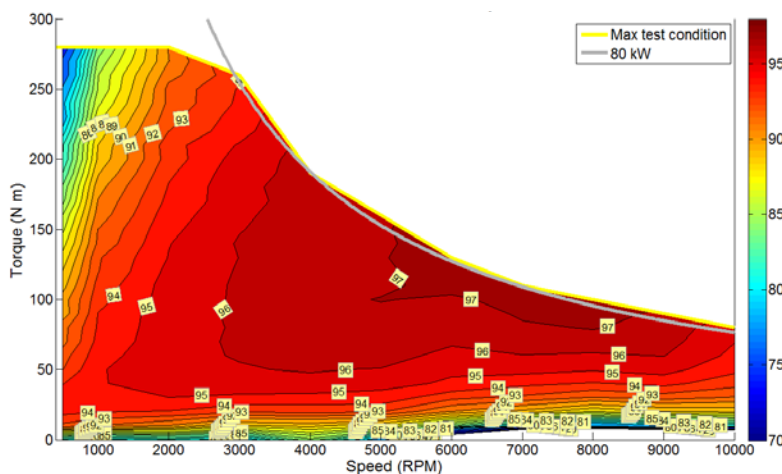


Figure IV - 14: The 2012 Nissan LEAF motor efficiency contour map.

speeds and low torques. The LEAF inverter was operated with the motor during tests, and the efficiency contour map for the inverter is shown in Figure IV - 15. Inverter efficiencies reached above 99%, and low speed efficiency gradients versus speed are observed. This is typical behavior because although high torque levels were produced, power levels were relatively low below 2,000 rpm, although switching losses were relatively constant, and therefore, low speed inverter efficiencies suffered. Combined motor and inverter efficiencies are shown in Figure IV - 16, where peak efficiencies above 96% are observed.

It was determined that the LEAF motor and inverter are capable of operating continuously at 80 kW and 7,000 rpm with 65°C coolant. The plot in Figure IV - 17 indicates the hottest motor temperature measurement and the inverter capacitor temperature versus time. A power level of 50 kW was maintained for 1 h with motor temperatures below 110°C, and then the power level was increased to 60 kW for 30 min, with motor temperatures stabilizing below 115°C. After increasing the power to 70 kW for another 30 min of operation, motor temperatures were below 125°C, and finally, an hour of operation at 80 kW yielded motor winding temperatures below 135°C and inverter capacitor temperatures below 80°C. The performance of the motor and cooling system are quite impressive considering the temperature rating of the motor wire is likely 180, 200, or 220°C.

Further studies on the capabilities of the LEAF motor and inverter are being conducted, and it is expected they will confirm that the components are capable of operating well above 80 kW. Currently it is not known whether the 80 kW power level is exceeded during operation of the vehicle, so the comparison

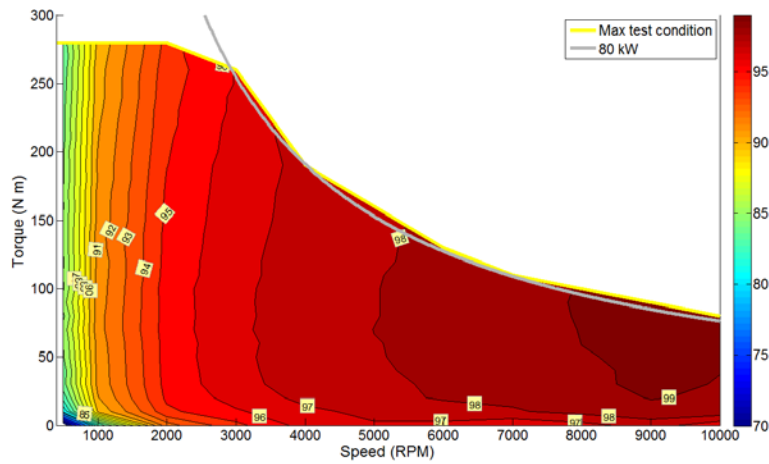


Figure IV - 15: The 2012 Nissan LEAF inverter efficiency contour map.

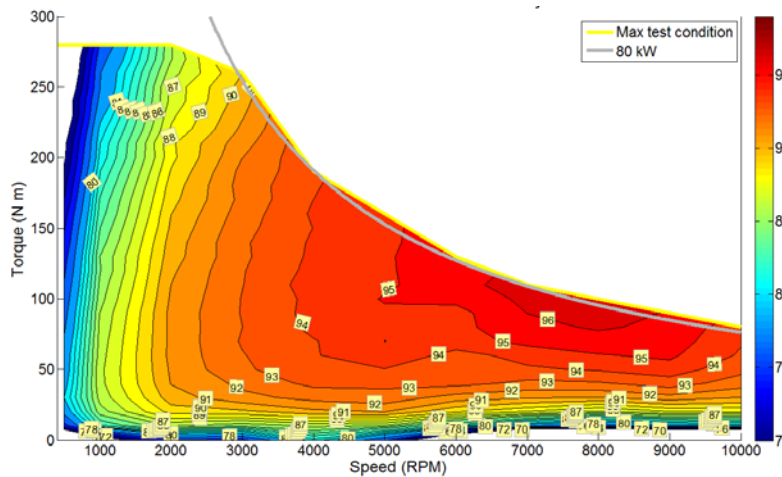


Figure IV - 16: The 2012 Nissan LEAF combined motor and inverter efficiency contour map.

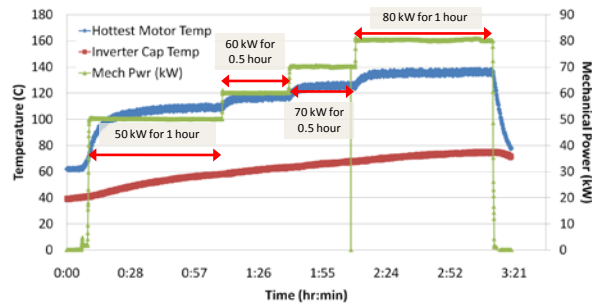


Figure IV - 17: The 2012 Nissan LEAF continuous power test at 7,000 rpm and various power levels.

with other benchmarked systems in Table IV - 1 assumes a power rating of 80 kW for the Leaf. Revised power density and specific power numbers may be published at a later date if it is determined that the system is capable of operating above published values. It should be noted that comparison of the Leaf and Sonata specific power and

power densities with other systems may not be completely direct because the systems were able to operate continuously at the published power level, whereas the continuous capability of the Toyota systems were often half or less than that of the peak power.

Table IV - 1: Comparison of specific power and power densities for various HEV components.

Component & Parameter	2012 Leaf (~80 kW)	2011 Sonata (30 kW)	2010 Prius (60 kW)	2008 LS600h Lexus (110 kW)	2007 Camry (70 kW)	2006 Honda Accord (12 kW)	2004 Prius (50 kW)
Motor							
Peak power density, kW/L	4.2	3.0	4.8	6.6	5.9	1.5	3.3
Peak specific power, kW/kg	1.4	1.1	1.6	2.5	1.7	0.5	1.1
Inverter <small>Excludes generator inverter (parenthetical values exclude boost converter mass/volume)</small>							
Peak power density, kW/L	5.7	7.3	5.9 (11.1)	10.6 (17.2)	7.4 (11.7)	2.9	4.5 (7.4)
Peak specific power, kW/kg	4.9	6.9	6.9 (16.7)	7.7 (14.9)	5.0 (9.3)	2.4	3.8 (6.2)

Conclusion

- Finalized performance and efficiency mapping of Hyundai Sonata motor.
 - Motor efficiency very briefly reached 95% but only for a very narrow operating range.
 - Inverter efficiencies reached above 98%.
 - System efficiencies peaked at 93.6% at 5,000 rpm and 60 Nm.
 - The motor operated up to 35 kW, although the published power level is 30 kW.
 - The motor was operated at 25 kW and 5,000 rpm for 30 min, and stator temperatures reached about 100°C.
 - The continuous power rating is close to 30 kW.
- Analyzed Sonata HSG.
 - About 106 Arms are required to produce the rated torque of 43 Nm.
- Benchmarked the NISSAN LEAF.
- Successfully interfaced ORNL controller with LEAF's inverter driver board.
- Motor size and shape are similar to Lexus LS 600h.
- Inverter power electronics modules require additional electrical insulation sheet, a potential compromise in thermal conductivity.
- Three IGBTs and diodes in parallel for each switch.
- Inverter mass and volume: ~16.2 kg and 14 L.
- Motor mass and volume: ~56 kg and 19 L.
- Motor efficiency peaked above 97% with considerable range above 90%.
- Inverter efficiency peaked above 99%.
- Combined inverter and motor efficiency peaked above 96%.
- Capable of operating at 80 kW continuously at 7,000 rpm and 65°C coolant.

Patents

None.

Publications

None.

References

None.

IV.2 Integration of Novel Flux Coupling Motor with Current Source Inverter

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Objectives

To integrate a nonpermanent magnet, brushless, novel flux coupling (NFC) electric machine and a current source inverter (CSI) to minimize capacitors and eliminate rare earth (RE) materials while simultaneously eliminating the dc link inductor in the CSI through the use of the external field coil in the NFC motor.

Approach

To partially use the excitation coil and core in the motor shown in Figure IV - 18(a) and its dc coil, Figure IV - 18(b), while using the series coil to function as an inductor for the CSI, Figure IV - 18(c), to develop an integrated motor/inverter system.

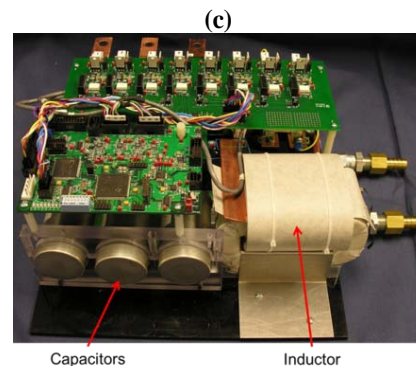
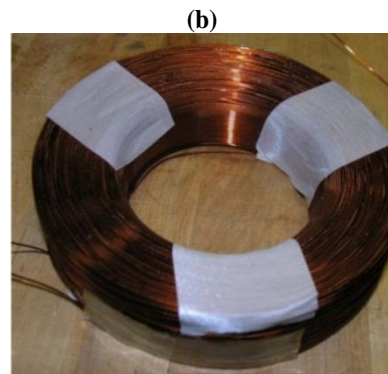
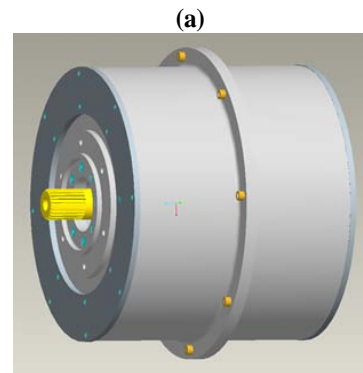


Figure IV - 18: The NFC motor (a) includes the CSI excitation coil and core (b). The goal of this project is to integrate a CSI (c) with the NFC motor shown in (a).

Major Accomplishments

- Improved the NFC motor design from the axial excitation to radial excitation, obtaining an NFC motor design with significantly shortened axial excitation length and higher torque.
- Investigated various possible coil and core arrangements for the integration based on the

available POCs prototype NFC motor that has two long excitation cores.

- Built PSIM models of the NFC motor and CSI to study the system performance of a CSI-based NFC motor drive and optimize the control algorithms.

Future Direction

- Simulate new NFC design with system to gauge improvements in power density and torque production.
- Continue to optimize the performance of the integrated system and assess the commercial potential.



Technical Discussion

The 2012 Improved Radial Gap Novel Flux Coupling Motor

The axial length of the 2011 NFC prototype motor (Figure IV - 19) was greatly reduced in the new design developed in 2012 by putting the stationary excitation core and coils inside the rotor. The new design is not shown due to export control issues. In the 2012 design the leads of the excitation coils are brought out through the motor's hollow shaft. The shaft can also be used to provide thermal management as coolant can flow in and out of the shaft to cool the excitation coils. The excitation core is supported by the bearings located in the rotor, and the rotor is supported by its bearings located inside the housing end brackets. One end of the rotor can be opened for inserting the excitation core inside the rotor before securing the end of the rotor to the rotor assembly.

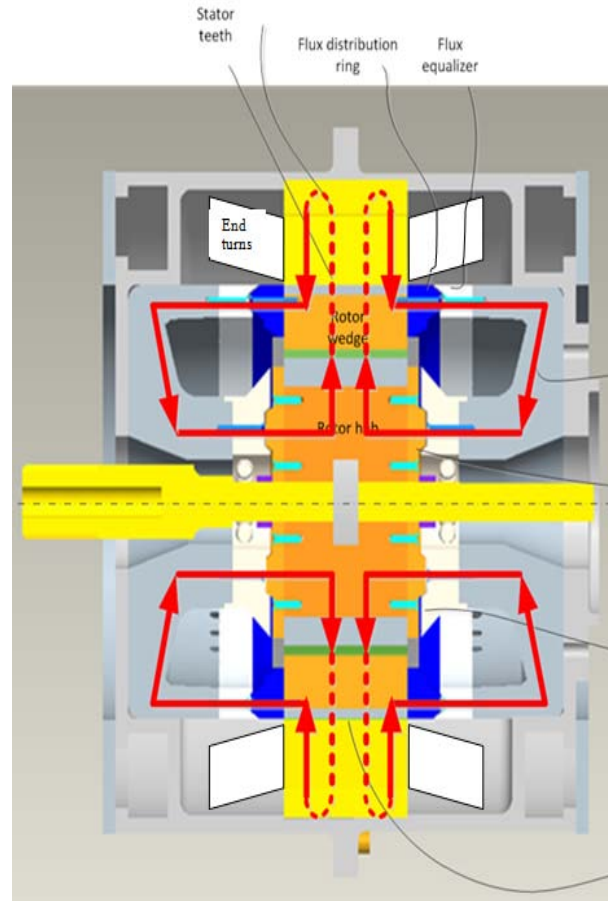


Figure IV - 19: The first NFC prototype motor.

The stationary excitation core in the second generation NFC motor does not have any noticeable torque (only 0.012973 Nm in a sample simulation) because there is negligible low saliency between the excitation core and the rotor. The total torque includes both the reluctance torque and the rotor excitation torque and is produced by the rotor interacting with the stator.

Table IV - 2 shows calculated torque values for the second generation NFC motor design at 200 A locked rotor current and 10 A excitation current. The new design targeted the performance of the 2007 Camry RE interior permanent magnet (IPM). The 141 Nm peak torque is close to the Camry motor's peak torque of 155 Nm at 200 A.

Table IV - 2: NFC motor torques vs rotor electric positions at 200A phase current with the same stator core outer diameter, inner diameter, and core length as the Toyota Camry.

Conductor a Phase Angle	Conductor b Phase Angle	Conductor c Phase Angle	Stator Tq Torque	S Tq Torque	N Tq Torque	Rotor Tq Torque
150.	270.	390.	117.06	-78.235	-43.947	-122.18
165.	285.	405.	131.66	-83.983	-52.22	-136.2
180.	300.	420.	138.14	-83.138	-58.321	-141.46
195.	315.	435.	136.37	-76.143	-62.074	-138.22
210.	330.	450.	124.62	-65.09	-60.191	-125.28
225.	345.	465.	99.983	-47.673	-52.649	-100.32
240.	360.	480.	63.285	-24.164	-38.893	-63.057
255.	375.	495.	1.937	12.147	-12.978	-0.8307
270.	390.	510.	-55.405	36.748	20.539	57.286
285.	405.	525.	-80.558	47.785	34.81	82.596
300.	420.	540.	-80.93	46.368	36.151	82.519
315.	435.	555.	-75.673	44.844	32.182	77.026
330.	450.	570.	-67.819	43.457	25.529	68.986
345.	465.	585.	-53.253	38.913	16.065	54.978
360.	480.	600.	-33.123	30.064	5.4847	35.549
375.	495.	615.	-5.4105	14.521	-6.5462	7.9751
390.	510.	630.	19.455	-0.34486	-16.89	-17.235
405.	525.	645.	27.938	-9.6295	-16.63	-26.259
420.	540.	660.	22.074	-9.5315	-11.628	-21.159
435.	555.	675.	8.3788	-4.0278	-3.661	-7.6887
450.	570.	690.	10.091	-9.6323	-0.9452	-10.578
465.	585.	705.	33.074	-28.654	-6.3543	-35.008
480.	600.	720.	64.015	-49.985	-17.268	-67.253
495.	615.	735.	91.729	-65.89	-30.214	-96.104
510.	630.	750.	117.06	-78.235	-43.947	-122.18
525.	645.	765.	131.66	-83.983	-52.22	-136.2

The objective of the new design is to optimize the motor to produce smooth torque with high power density and efficiency through the use of adjustable rotor excitation fields. Additionally the design eliminates the need for stator field weakening in the constant power region and can tolerate high temperature operation. A significant design objective is to achieve or exceed the performance of an RE IPM machine (2007 Camry).

Work is ongoing to optimize the reluctance torque and the thermal capability of the excitation windings. To date the results are promising.

Integration of Novel Flux Coupling Motor and Current Source Inverter

The total inductance value required by the CSI prototype is 372 μH . If we have two series excitation coils, each coil would need to provide an inductance value of 186 μH . Simulations in 2012 were based on the POC

prototype motor with two relatively long axial excitation cores, which was the design tested in 2011.

Two simulations were conducted (see Figure IV - 20), and two different high frequency series coils for the CSI inductor were analyzed. One, shown in Figure IV - 20(a), was based on transposed iron wires with a thin coating of electric insulation to increase the self-leakage inductance of the coil as well as its flux conduction capability. The dc flux field coil is used to produce the dc flux to the rotor and the series coil functions to supply the CSI inductance. The second simulation [Figure IV - 21(a)] was based on all copper coils for both the dc excitation and the CSI series coils.

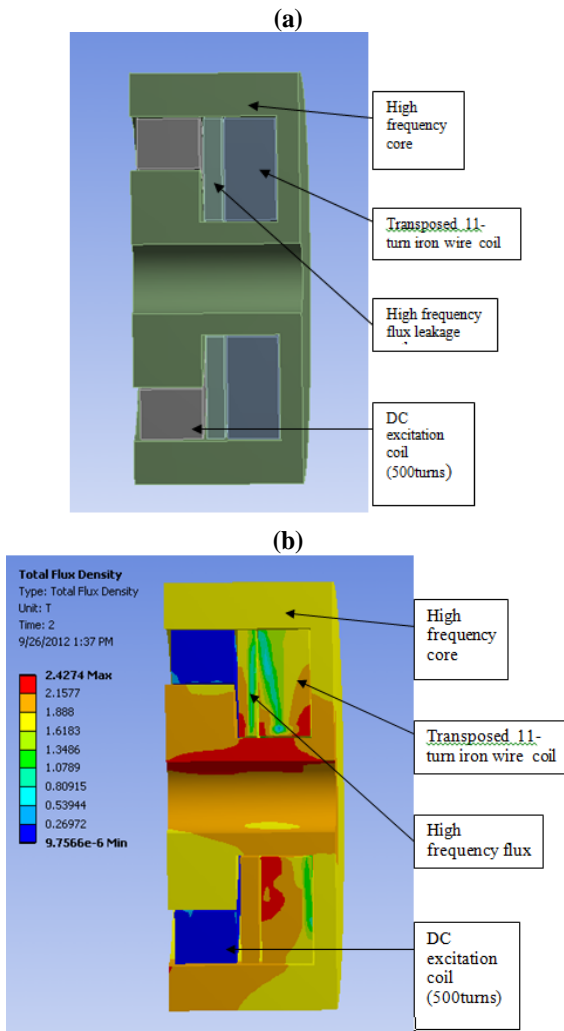


Figure IV - 20: Axial excitation core of an NFC motor with transposed iron wires for the CSI series coil (a) and the flux distribution for the excitation core (b).

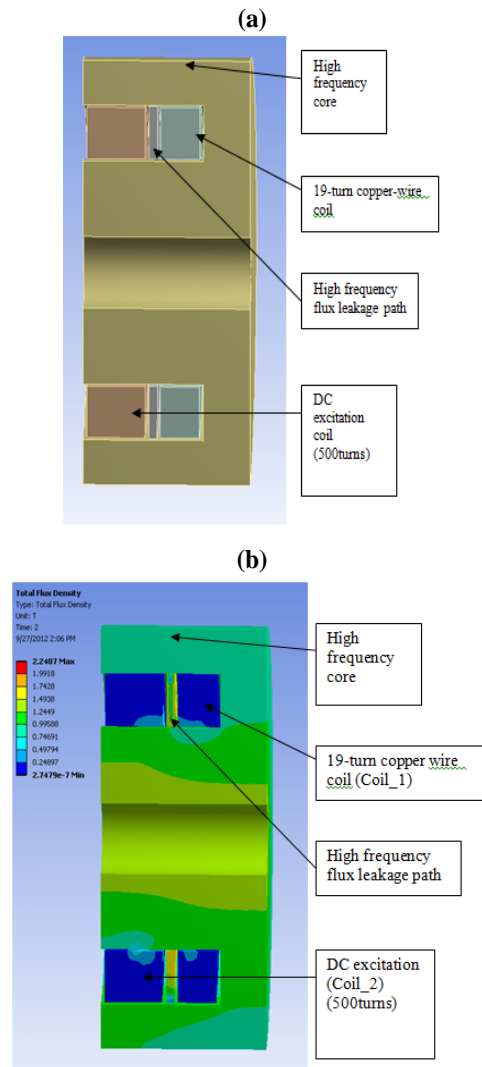


Figure IV - 21: Axial excitation core of an NFC motor with 19-turn copper-wire CSI series coil (a) and flux distribution for the excitation core of this NFC motor (b).

Transposed Iron-Wire Current Source Inverter Series Coil

In this study, the CSI series inductor coil was made of transposed iron wires coated with thin insulation. As shown in Figure IV - 20, this coil has 11 turns. Figure IV - 20(a) shows that the transposed 11-turn iron-wires coil also serves as a magnetic flux path for both the dc and ac fluxes. Fewer turns are needed for the required inductance value of the CSI because the iron wires and the high frequency flux leakage path provide a good flux path for this coil. The iron resistivity is about 7 times the copper resistivity; therefore, a large conductor cross-sectional area is expected. The flux distribution for the excitation core is shown in Figure IV - 20(b).

The self-inductance value of the transposed 11-turn iron-wire (coil_1) from the simulation is 183 μH , as shown

in Table IV - 3. This meets the required 186 μH inductance for the stand-alone prototype CSI necessary to match the rating of the NFC motor. The large dc excitation (coil_2) inductance is 0.24745 H. The iron coils construction with iron wire serves to enhance the dc flux.

Table IV - 3: Calculated inductance of the iron-wire CSI series coil.

	Conductor_Coil1 (H)	Conductor_Coil2 (H)
Conductor_Coil1	1.8253e-004	-2.0811e-003
Conductor_Coil2	-2.0811e-003	0.24745

Copper-Wire Current Source Inverter Series Coil

The flux distribution simulation shown in Figure IV - 21(b) confirms that the copper-wire CSI coil can function properly for producing sufficiently high inductance for meeting the CSI requirement of the stand-alone CSI test module in the excitation core of the NFC motor.

The self-inductance value of the 19-turn copper-wire (coil_1) from simulation, as shown in Table IV - 4, is 191 μH . This meets the required 186 μH for the inverter. The dc excitation coil_2 inductance without the iron-wire CSI coil in the core is 0.13288 H, which is less than the 0.2475 H shown in Table 2 for the core with iron-wire CSI coil.

Table IV - 4: Calculated inductance of the copper-wire CSI series coil.

	Coil_1 (H)	Coil_2 (H)
Coil_1	1.912e-004	-7.3405e-005
Coil_2	-7.3405e-005	0.13288

Novel Flux Coupling Motor Simulation Study

To study the NFC motor’s performance under a CSI, a PSIM model including an NFC motor and a CSI was built, as shown in Figure IV - 22. A dc-dc interface was used between a voltage source and the CSI.

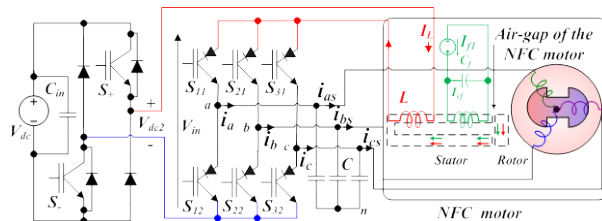


Figure IV - 22: System diagram of the NFC motor driven by a current source inverter.

In the NFC motor, there are two field windings: one is the traditional dc field winding (shown in green in Figure IV - 22); the other is the CSI inductor winding

(shown in red). The total air-gap flux of the NFC motor is generated by the two currents.

The motor’s performance was calculated and compared with the 2010 Toyota Prius motor with the same armature current of 240 A; the total field current changes from 2 A up to 12 A. Figure IV - 23 shows the output torque vs current angle with different field currents; the curve for the 2010 Prius motor is also shown. When the NFC field current is more than 12 A, the torque of the NFC motor is higher than that of the Prius motor.

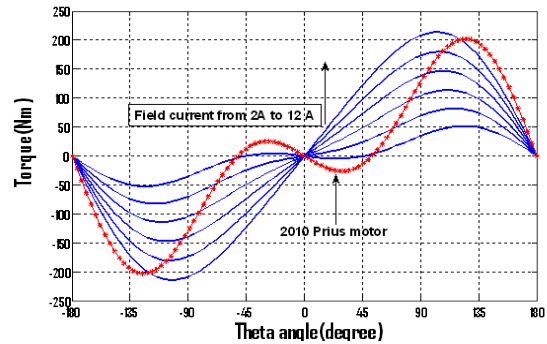


Figure IV - 23: NFC motor and 2010 Toyota Prius motor torque curves.

Figure IV - 24 shows the armature current vs total field current with different output power levels; the field current affects the armature current significantly. For example, at 1 power unit (PU) output power, the armature current can vary from 280 A (with 6 A field current) to 140 A (with 14 A field current).

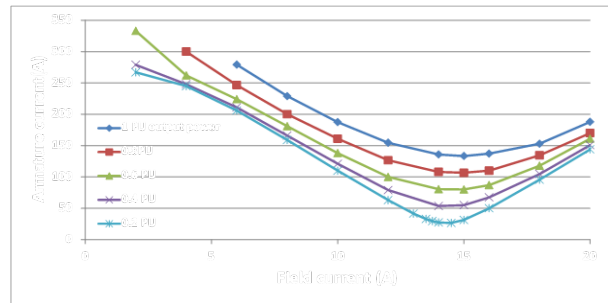


Figure IV - 24: The armature current vs total field current of the NFC motor at 5,200 rpm.

Similarly, Figure IV - 25 shows the power factors of the NFC motor vs total field current with different power levels. Generally, at higher output power levels, the power factors are higher. The field current greatly affects the power factor. At 0.2 PU, the power factor changes from 0.12 to about 1.0, while the field current changes from 2 A to 15 A.

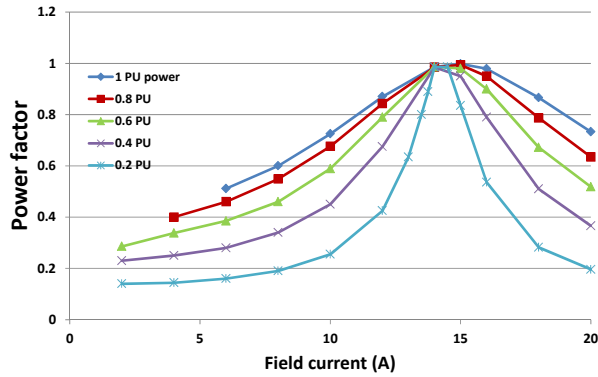


Figure IV - 25: Power factor of the NFC motor vs field current at 5,200 rpm.

Figure IV - 24 and Figure IV - 25 demonstrate that the NFC motor has a higher power factor and lower armature current at around 14–15 A field current.

Figure IV - 26 shows the key waveforms of the NFC motor at steady state. From top to bottom, the three-phase current, CSI inductor current, motor speed, dc-dc converter duty ratio, and electromagnetic torque and load torque are shown. The motor speed is 5,200 rpm, the load torque is 135 Nm, and the peak current is 230 A. The output power is about 75 kW. The CSI inductor current is about 400 A. The output current is very sinusoidal, and the inductor current follows the reference current very closely and its ripple is small. The motor speed is very stable.

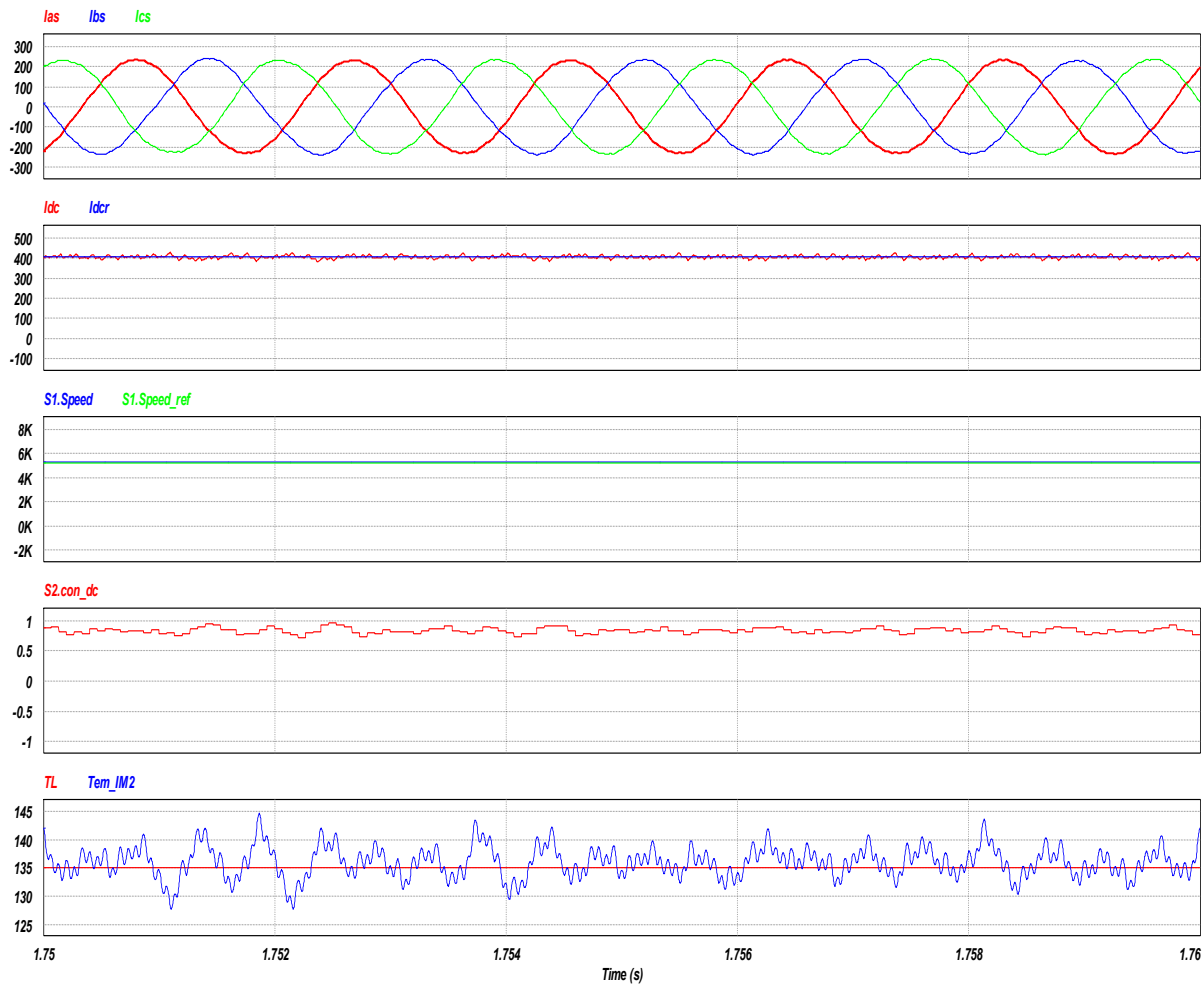


Figure IV - 26: Key waveforms at steady state with 135 Nm load at 5,200 rpm; peak phase current is 230 A, and dc-dc inductor current is about 400 A.

Dual Field Excitation

Instead of using one winding to generate air-gap flux, two windings (i.e., CSI inductor current and dc field winding current) are used to generate air-gap flux.

Figure IV - 27 and Figure IV - 28 show the simulation results of the study. Some key waveforms were shown to demonstrate the performance of the drive. From top to bottom, they are the three-phase current, electromagnetic and load torques, reference and actual inductor current, and total equivalent field current and rotor speed.

In Figure IV - 27, the NFC motor air-gap flux was generated by the CSI inductor current with only 8 A; the dc field winding shown in Figure IV - 19 was inactive. The operating conditions used for Figure IV - 28 were the same as those for Figure IV - 27 except for the field winding

current—in this case, both the dc field winding and CSI inductor winding were used and each generated 50% of the total air-gap flux.

Both cases have similar current, torque, and dc current waveforms. However, due to the ripples in the CSI inductor current, the output torque shown in Figure IV - 27 had higher ripples (30 Nm in Figure IV - 27, 15 Nm in Figure IV - 28). The output currents of Figure IV - 27 also had higher current ripples than those shown in Figure IV - 28. Hence, using both dc field winding and CSI inductor winding for field excitation (i.e., dual excitation) can reduce the torque ripple and output current distortion and achieve better performance than using CSI inductor winding alone.

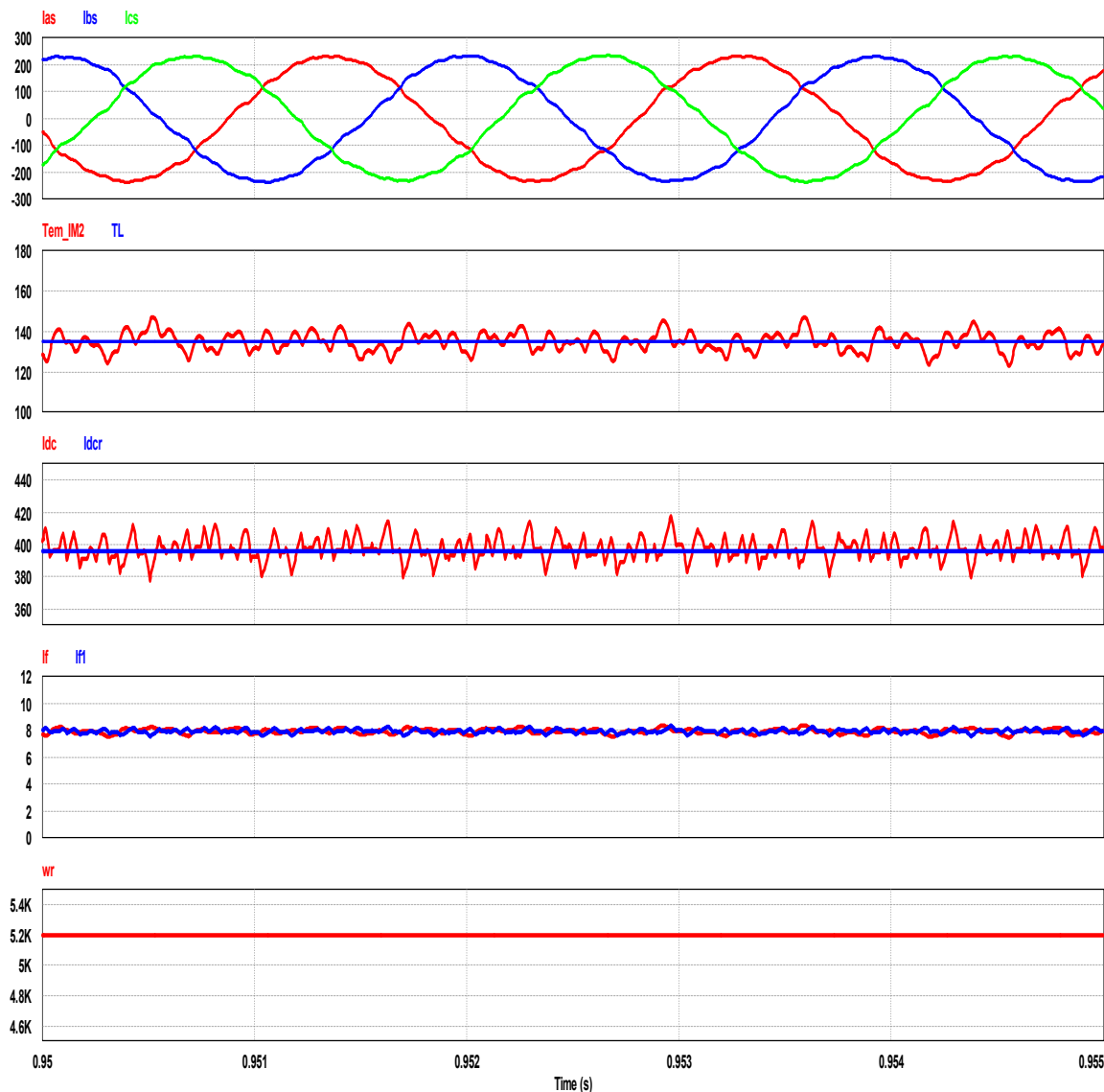


Figure IV - 27: Using the CSI inductor current as the only field current.

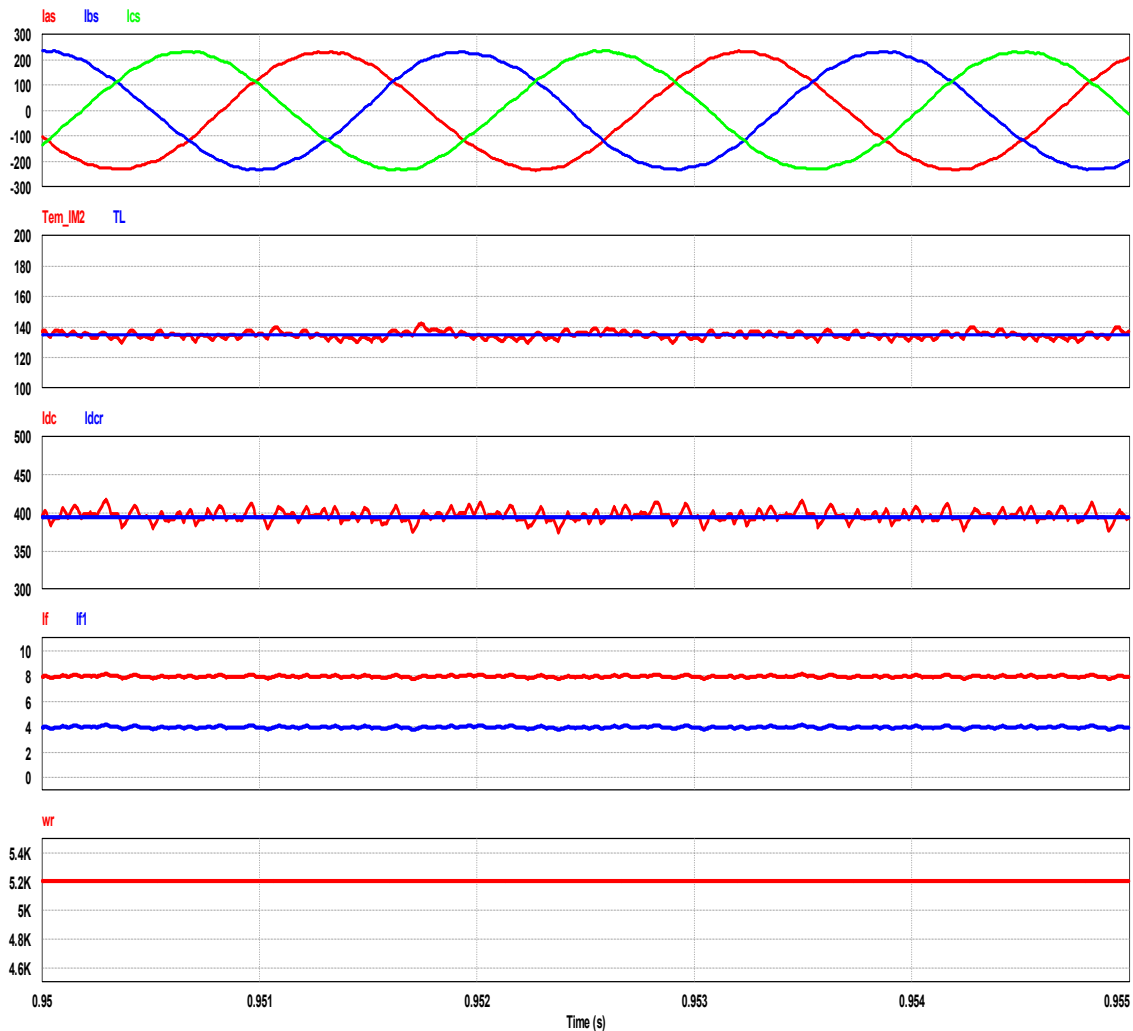


Figure IV - 28: Dual field excitation-using both dc field winding and CSI inductor winding as field excitation (4 A field current + 4 A dc inductor current).

Conclusion

1. Improved the NFC motor design from axial excitation to radial excitation; a significantly shortened axial excitation length with a higher torque NFC motor design was obtained.
2. Demonstrated the concept of partial use of the excitation coil and core in the motor and also the series coil for the CSI inductor with either iron-wire or copper-wire series coils for the CSI. The iron-wire coil makes the dc flux flow easier due to more iron in the core.
3. Demonstrated that using dual field excitation (i.e., CSI inductor winding and field winding) can reduce torque and output current ripples of the CSI.

Patents

1. John S. Hsu, *Novel Flux Coupling Radial-Gap Motor*, US patent application U.S. 61/709,188, in process.

Publications

1. John S. Hsu, "Integration of Novel Flux Coupling Motor and Current Source Inverter," in *Oak Ridge National Laboratory Annual Progress Report for the Power Electronics and Electric Machinery Program*, ORNL/TM-2011/263, Oak Ridge National Laboratory, October 2011, pp. 146–152.

References

None.

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Objectives

- Provide technical guidance and strategic input to the DOE Advanced Power Electronics and Electric Motors (APEEM) technology development manager on how DOE initiatives may best be used to implement the latest research opportunities for meeting the Vehicle Technologies Program (VTP) traction drive system (TDS) requirements and targets.
- Investigate, demonstrate, and assess the initial feasibility of research opportunities.

Approach

- Prepare a report that applies standard drive cycle inputs to the model of a representative all electric vehicle (AEV) and in doing so maps out the most frequent operating points in the AEV traction drive motor's torque-speed operating space to provide guidance on electric motor and power electronic research. This approach recognizes that the most efficient AEV TDS is not necessarily the one having the highest efficiency electric motor or the highest efficiency power inverter, but rather the most efficient system that exhibits highest efficiency where the bulk of stored energy is processed for propulsion.
- Participate in a series of DOE strategy workshops to address APEEM's research priorities in order to meet the DOE Energy Efficiency and Renewable Energy EV Everywhere Grand Challenge.

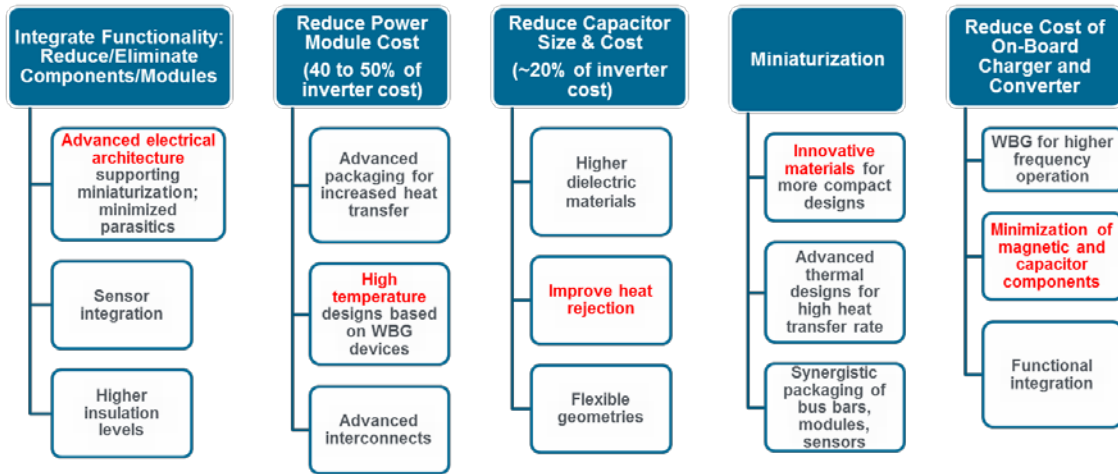
Major Accomplishments

- Completed an interim report on Vehicle Performance Metrics Applied to Electric Drive Vehicle System Research.

Future Direction

- Investigate research opportunities to determine their initial feasibility and contribution to achieving affordable and highly efficient TDSs while meeting DOE's 2020 targets for specific power (SP) and power density (PD).
- Provide system level modeling and simulation; cost assessments; and research strategy development with an emphasis on alternative electric machines (EMs), wide bandgap (WBG) semiconductor integration, power electronics (PE) packaging, and supporting electric drive component research.
- Provide technical guidance on the key areas of APEEM research highlighted in Table IV - 5.

Table IV - 5: A strategy to reduce power electronic cost.



Technical Discussion

Vehicle Performance Attributes

Figure IV - 29 illustrates vehicle performance metrics applied to electric drive vehicle system research. In this depiction, energy from the rechargeable energy storage system (RESS) is processed by the TDS, consisting of the power electronic inverter (or converter-inverter cascade, if used) and the traction motor, on to the gearbox. The five interfaces are

- input power,
- output power,
- control and communications,
- thermal management (cooling loops), and
- structure and packaging.

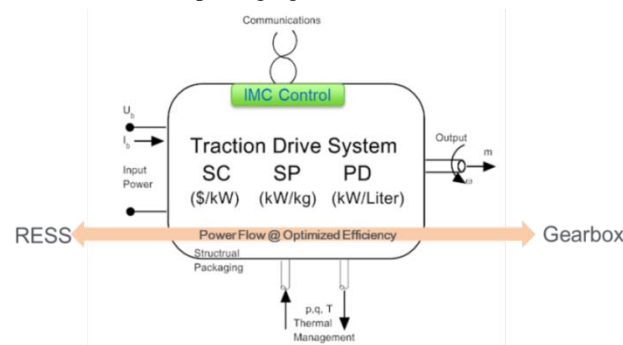


Figure IV - 29: The five interfaces of a TDS.

The two most crucial interfaces are the RESS to power electronics and the traction motor to gearbox as these two interfaces are exposed to the full propulsion

power load of the vehicle, whether motoring or in regenerative braking mode. The control and communications interface ensures that driver commands for torque and speed are properly delivered, and the thermal management interface ensures that the power electronics, control electronics, and electric motor operate within nominal temperature limits.

In recent decades the performance of electric traction drives has improved through innovations at the TDS input and output interfaces. The input, or PE interface system voltage, has increased by more than a factor of 2 in the past 17 years. The output, or electric motor interface to the driveline speed, has increased by more than a factor of 2 over this same period. Figure IV - 30 illustrates the trends in PE voltage and electric motor speed for plug-in electric vehicle (PEV) traction drives. As shown in this chart, both PEV traction motor speed and PE system voltage are clearly on the rise, especially motor speed. The 2010 plateau in motor speed is due mainly to interior permanent magnet (IPM) motor rotor limitations on structural stress. The subsequent rise in motor speed is based on the Tesla Motors induction motor, rated at 15,300 rpm. Another contributor is the program goal to increase motor speeds substantially to eliminate the need for rare earth (RE) magnets. PE on the other hand have reached a voltage plateau mainly due to automotive reliance on existing high volume industrial market modules.

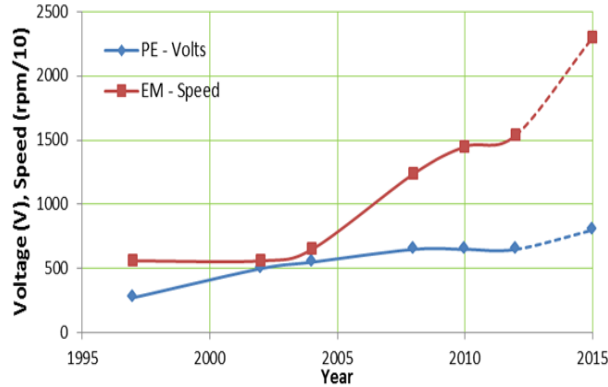


Figure IV - 30: Trends in PE voltage and electric motor speed for PEV TDSs.

A number of subsystems are required to meet all the driver and occupant expectations in the AEV. Figure IV - 31 identifies the main power electronic and electric motor subsystems that are required at a minimum. These supporting subsystems are

- **battery charger**—necessary for plug-in hybrids and electric vehicles;
- **bidirectional boost converter**—steps up the battery voltage when the traction system requires a higher operating voltage than the battery can supply;
- **electric motor**—converts electrical to mechanical power for the wheels;
- **inverter**—converts direct current (dc) to alternating current (ac) for the electric motor; and
- **dc-dc converter**—steps down the high battery voltage to power ancillary systems such as lighting, brake assist, and power steering, and accessories such as air conditioning and infotainment systems.

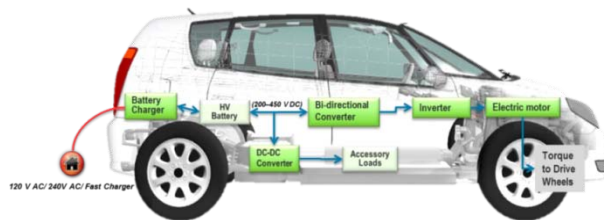


Figure IV - 31: Architecture of an AEV.

All of the AEV architectural elements that form the TDS can be summarized as shown in Figure IV - 32. In this view the major interfaces are described in more detail along with starting concepts for power electronic voltage levels and traction motor speed range. For optimum overall efficiency the TDS controls maximize the traction inverter and motor efficiency as a pair, not individually. The goal of the TDS control is to minimize waste heat generation so that the burden on the thermal management system is minimized and thereby its cost. In the following charts power semiconductor devices (PSDs) used in traction

inverter power electronics must be rated for system voltage range, U_d , and nominal value, U_{do} .

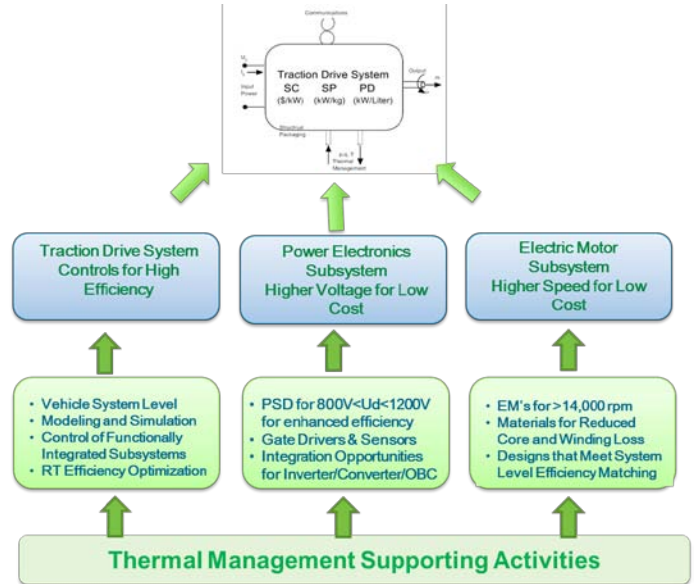


Figure IV - 32: Architecture of an AEV TDS and its thermal management.

Full TDS efficiency is maximized in the following manner.

- Highest possible operating voltage of the power inverter.
- Lowest possible switching frequency that minimizes audible noise (air and structure borne) while maximizing voltage applied to the traction motor without undue generation of distortion.
- Highest possible operating speed of the traction motor without incurring excessive core and copper loss.
- Electric motor architecture best suited to low cost such as non-RE designs.

The following two subsections will highlight the innovation opportunities needed for AEVs to become mass market affordable and at acceptable efficiency in the conversion of RESS energy to useful work in vehicle propulsion.

Power Electronics Subsystem

In today’s AEV traction drive applications the power electronics operate over a nominal $250 V_{dc} < U_d < 400 V_{dc}$ range using silicon PSDs rated at $650 V_{dc}$ for robustness in a sustained voltage-temperature-vibration environment. Trending to higher voltage is foreseen by industry leaders [1]. Figure IV - 33, excerpted from [1], shows that at $U_{do} = 650 V_{dc}$ metal-oxide semiconductor field-effect transistors (MOSFETs) and insulated gate bipolar transistors (IGBTs) based on silicon technology already demonstrate the robustness, low cost, and high performance demanded in high power modules. But taking TDS efficiency to the next

level will demand, at least as indicated by early top level simulation work, moving to system voltages of 800 V_{dc} and potentially to 1,000 to 1,200 V_{dc}. At 800 V the devices must be rated 1,200 V to 1,300 V to realize similar levels of robustness and low cost.

An example will help clarify the motivation for moving to higher system voltages. It is clear that the majority of power inverter cost is in the power module, on the order of 30+%. It is also well known that power module cost is a strong function of the switch transistor peak current and thermal environment (discussed below). The nominal 55 kW traction drive electric motor operating from a 330 V_{dc} battery requires up to 250 A_{pk} in its phase windings to generate the peak torque demanded during acceleration and grade hold. To clarify these statements, the TDS performance must be met when the RESS is at 50% state of charge (SOC), and therefore its voltage may drop to the bottom of the system voltage range

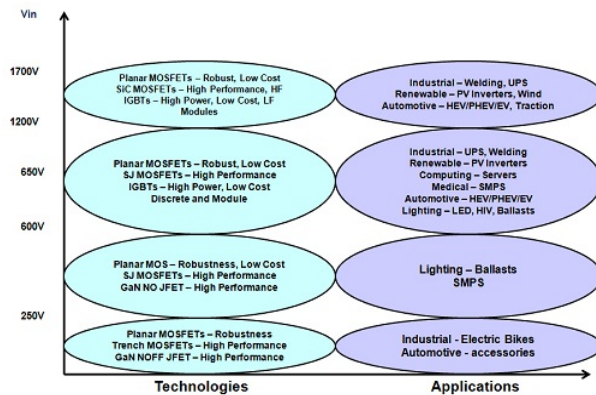


Figure IV - 33: Power electronic semiconductor device technology and applications [1].

during peak current draw (250 V_{dc} at 240 A when TDS efficiency is $\eta_{em} = 92\%$ overall for 60 kW delivered to the power inverter).

$$U_{ph} = \left\{ \begin{array}{l} \frac{\sqrt{2}}{\pi} U_{d0} = 0.45 U_{d0} (V_{rms}) \text{ in SSSW} \\ \frac{\sqrt{6}}{\pi} \frac{U_{d0}}{2} = 0.385 U_{d0} (V_{rms}) \text{ PWM} \end{array} \right. \quad (1)$$

Using Eq. (1) for six step square wave (SSSW) waveform at low RESS voltage and peak power results in

power electronic continuous phase current, I_{ph} , according to the following.

$$I_{ph} = \frac{P_{pk}}{3\eta_{em}(0.45 U_{d0})} = 181 A_{rms} \quad (2)$$

This puts the inverter switch current at just over 250 A_{pk} so that die area must be sized to accommodate this peak current continuously. It would be incorrect to interpret this peak power demand from the motor as a transient operating point on the inverter. It is not; it is a continuous rating. If the system voltage were increased to 800 V_{dc}, with the same motor power, Eq. (2) now predicts an inverter switch current of 56.65 A_{pk}, a reduction of 78%. Therefore, unless the high voltage power devices are very expensive, this should result in substantial power module savings.

Keep this in mind while examining Figure IV - 33, and note that the top two technology bubbles straddle the 800 V to 1,200 V operating region being proposed for PE.

This technical report offers guidance to ORNL and National Renewable Energy Laboratory researchers on the development and prototype demonstration of a full TDS based on WBG semiconductor and non-RE EMs with an overall goal of cost reduction and drive miniaturization. Figure IV - 34 is a flow diagram showing both the PE and electric motor development steps leading to a functional TDS demonstrator. The TDS program flow is best explained by following the top to bottom PE and EM columns. Figure IV - 29 illustrated the major interfaces of the full traction drive system. Figure IV - 34 takes this into account, showing top level system modeling and simulation to establish the overall requirements. These requirements are then cascaded to electric motor research and to PE development following WBG PSD procurement and characterization at the power module level. It is at this stage that necessary thermal materials and simulation work support the module design that can meet the system requirements. Electric motor development proceeds with in-depth assessment of the major classes of machines, reluctance, induction, and hybrid excitation types, and selection of one most suitable for full TDS deployment. Thermal management innovations are also factored into both PE and EMs work at this stage.

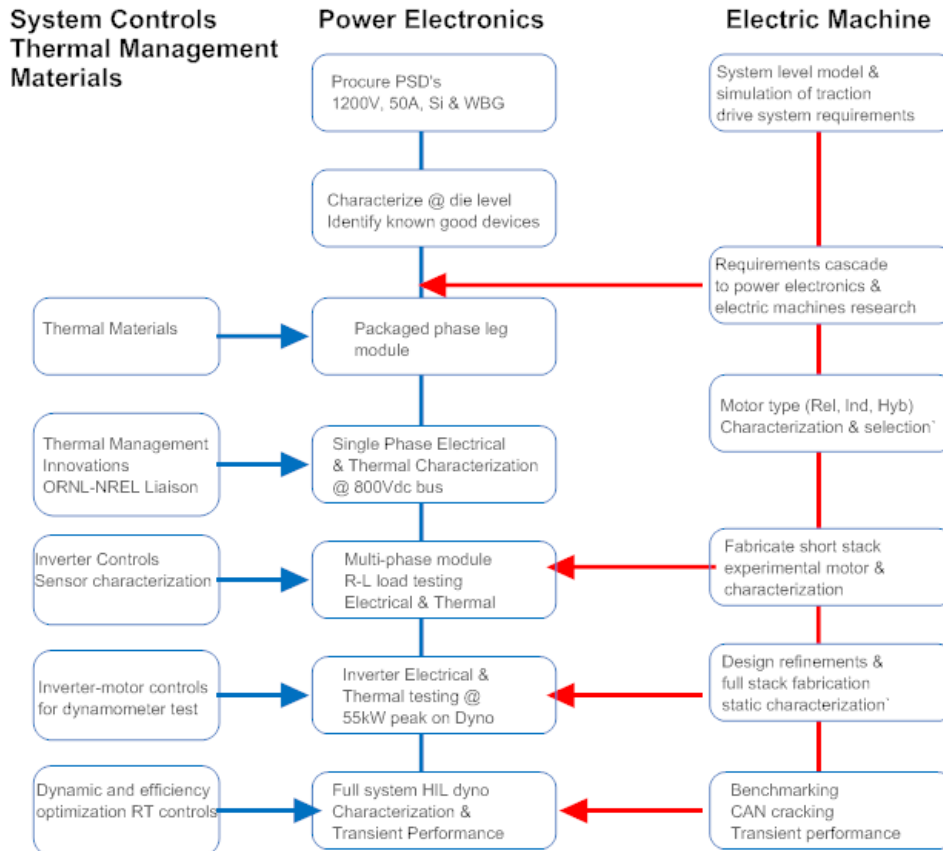


Figure IV - 34: Power electronic and electric motors program flow for TDS development.

A pivotal point in the traction drive program is the PE stage showing single phase electrical and thermal characterization and the point at which thermal management innovations are put into practice in a WBG based module. The purpose of focusing on the single phase hardware characterization is that this affords the development teams the opportunity to do hardware validation at a much simpler stage than full power inverter and to do thermal performance validation. Figure IV - 35 illustrates a conceptual single phase test based on conventional midpoint converter architecture. The single phase test equipment will be used to evaluate prototype WBG power modules developed at ORNL, along with the attendant gate driver and signal conditioning matching electronics.

Note that single phase testing and characterization as described in Figure IV - 35 must be done at a bus voltage of 800 V_{dc}, and it must be controlled to synthesize the nominal electric machine phase current waveshape and amplitude plus the base and switching frequency to be used in the subsequent electric motor tests.

Following this single phase test is the move to multiphase testing under electric motor equivalent inductor-resistor (R-L) loading. This will be the first point

at which a stator load is used and representative inverter-motor-controls leading to tests on a short stack electric motor.

The PE and EM program flow shown in Figure IV - 34 concludes with full stack electric motor testing using the fabricated WBG based power module and full inverter, all rated for 800 V_{dc} operation, along with the first full stack electric motor rated at 55 kW. TDS validation is then done on a dynamometer.

The lowest row in Figure IV - 34 takes the TDS validation to its highest level by putting it on a high performance dynamometer with an appropriately rated battery eliminator suited to 800 V_{dc} bidirectional power flow in a hardware-in-loop (HIL) environment. HIL testing comprises both load (torque) and speed transient response that characterize the electrical performance at extremes along with transient thermal performance. This is also the point at which efficiency optimizing TDS controls would be introduced and implemented.

Electric Motor Subsystem

Automotive electric traction motor speed has increased from 6,500 rpm in the 2002 to 2004 era to 13,500 to 14,400 rpm in the 2010 to 2012 era. This same time period has seen the performance of the traction motor

improve from 2004 at 50 kW for 45 kg of electromagnetic mass and $SP = 1.11$ kW/kg to the present 60 kW peak based on 22.7 kg of stator and rotor iron, stator copper, and rotor magnets. This yields an $SP = 2.64$ in 2012 (note the DOE SP 2015 metric is 1.3 kW/kg). However, because of the RE magnets used, the rotor magnets alone cost more than \$200, and the 2015 SC of \$7/kW is virtually consumed by magnet cost alone. That is why emphasis must be put on keeping driving system costs down and efficiency up.

Figure IV - 34 captures the major activities involved in development of the full TDS but not how the contending classes of EMs are appraised and down selected. Figure IV - 36 showcases the major classes of EMs considered for TDS application: reluctance (variable reluctance machines); induction; and various synchronous machines such as permanent magnet (interior and surface), wound field, and hybrid excitation. Figure IV - 37 shows cross sections of the dominant EM types.

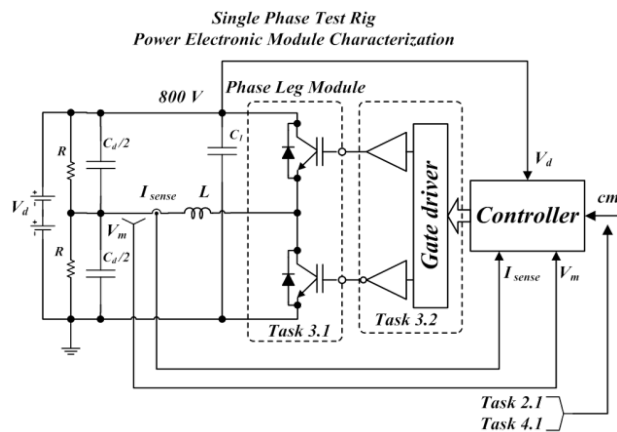


Figure IV - 35: Power electronic single phase characterization.

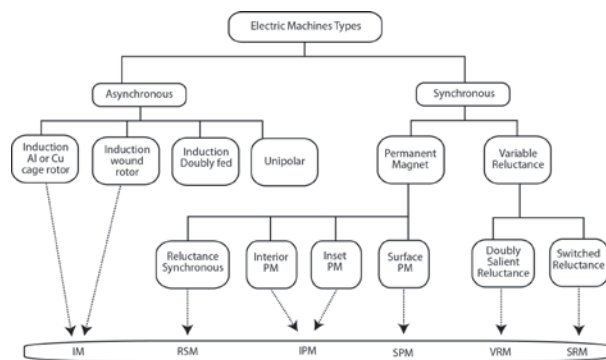


Figure IV - 36: EM types.

System Simulation

System simulation at the top level is necessary to cascade the vehicle performance attributes and metrics to the electric drive subsystem for focused research into PE and EM projects. To accomplish this, a representative AEV model will be simulated using a combination of five

drive cycles in the sequence: Urban Dynamometer Drive Cycle (UDDS) + US06 + Highway Fuel Economy Test (HWFET) + LA92 +

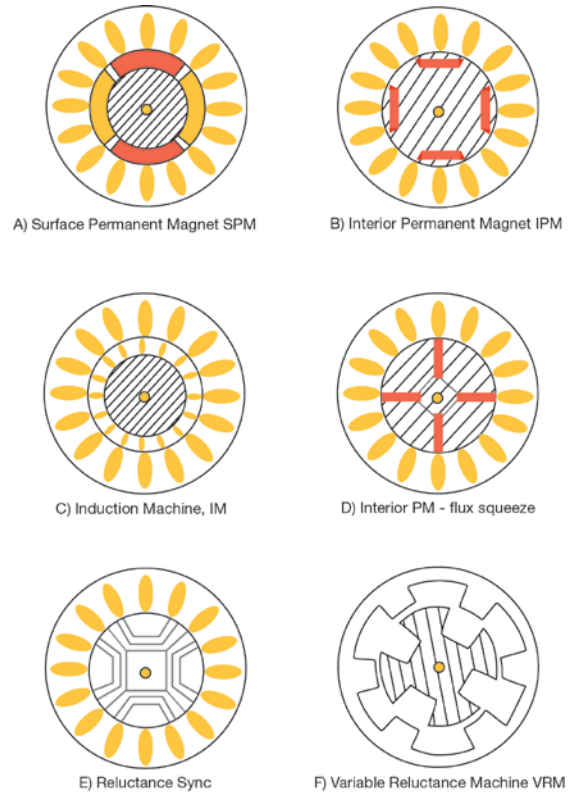


Figure IV - 37: Electric motor types.

UDDS to best approximate real world driving. Table IV - 6 lists the AEV attributes that will be used in the study.

Figure IV - 38 through Figure IV - 41 illustrate the drive cycles that will be used and their attributes. Note that the five-cycle combination results in a total drive time of 5,544 s (1.54 h) covering a total distance of 69.17 km (43 miles) for an average speed of 27.91 mph.

The representative AEV when exposed to the composite drive cycle must deliver the performance highlighted in Figure IV - 42, not necessarily including towing capacity and wide-open throttle (WOT) speed as these are modified for AEVs.

The AEV propulsion system is governed by Eq. (3) which summarizes the content of the vehicle model based on attributes listed in Table IV - 6. Headwind, V_w , and grade (α) are included in Eq. (3), although drive cycle simulations only treat the case of level terrain and zero headwind. These same constraints are imposed in the top level system simulation work described here.

$$P(V) = M_v V V + 0.5 \rho_{air} C_d A_f (V - V_w)^3 + g M_v C_{rr} \cos(\theta) V + g M_v \sin(\theta) V \tag{3}$$

Vehicle propulsion power as a function of vehicle speed, $P(V)$, in Eq. (3) consists of inertial power, aerodynamic drag, rolling resistance, and grade effect. The performance attributes cited in Figure IV - 42 are better appreciated by considering the forces acting on a vehicle

on a grade (Figure IV - 43), where forces are listed as F , resistance R , and drag D . It is important to recognize that in system modeling and simulation the standard drive cycles are based on level terrain ($\theta = 0$) and zero headwind, $V_w = 0$.

Table IV - 6: Vehicle attributes of representative AEVs.

Vehicle		Traction Drive	
Curb mass	1,535 kg	Battery capacity	24 kWh
Gross vehicle weight rating	1,704 kg	Battery state of charge range	90%
All electric range	100 miles	Battery mass (incl. in curb mass)	294 kg
Aerodynamic drag coefficient	0.29	System voltage	360 V _{dc}
Rolling resistance coefficient	0.009	Motor peak power	80 kW
Frontal area	2.7 m ²	Motor continuous power	—
Tire dynamic radius	0.3 m	Peak torque	280 Nm
Driveline gearing	7.94	Constant power speed ratio	4 : 1
Maximum grade	30°	Motor maximum speed	10.4 krpm
Maximum speed	92 mph	Motor corner speed	2.6 krpm
Zero to 60 mph time	10 s		

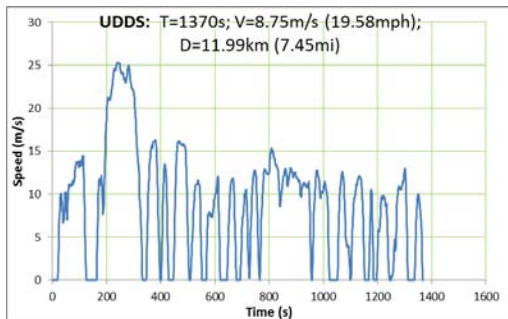


Figure IV - 38: Urban Dynamometer Drive Cycle (UDDS).

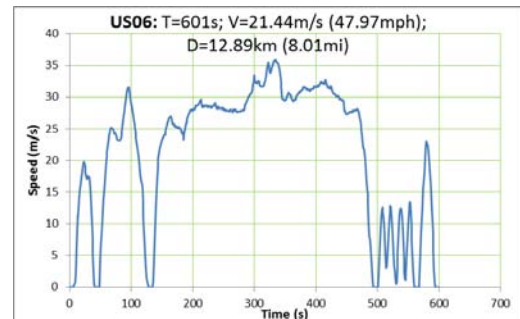


Figure IV - 40: High speed drive cycle (US06).

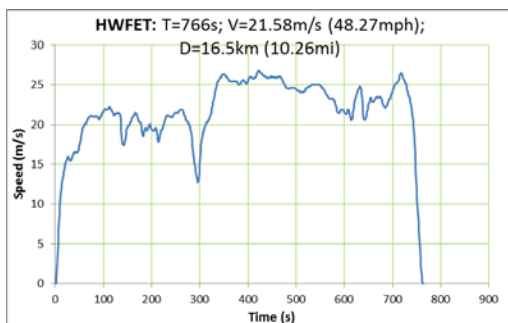


Figure IV - 39: Highway Fuel Economy Test (HWFET).

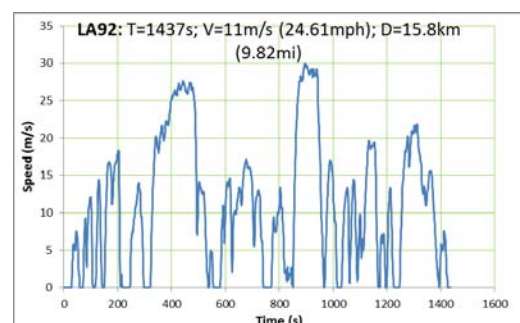


Figure IV - 41: Los Angeles 92 drive cycle (LA92).

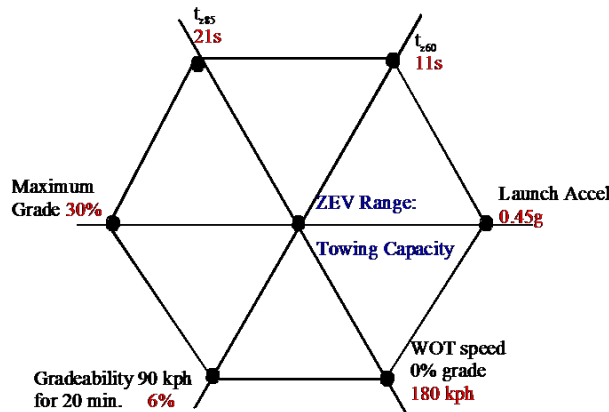


Figure IV - 42: Representative AEV performance attributes.

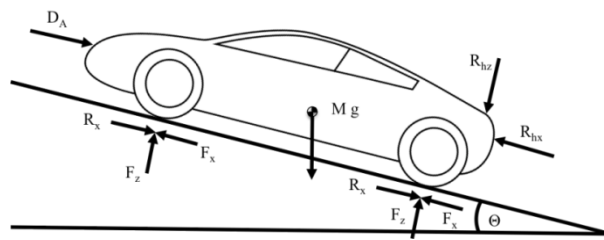


Figure IV - 43: Forces acting on AEV on grade (used with permission from [2]).

Figure IV - 43 clarifies the metric on maximum grade shown in Figure IV - 42 to show how grade puts a very high demand on TDS motor torque. This performance attribute is amplified further in Eq. (4), where parameters that directly influence the maximum achievable grade (i.e., grade hold) are highlighted. Specifically, maximum grade is directly proportional to driveline gearing, g_{dl} , and peak motor torque, m_{pk} , and inversely proportional to gravity, g ; tire dynamic rolling radius, r_w ; and gross vehicle mass, M_v . For example, in Eq. (4) a higher vehicle mass and the same grade capability means that motor peak torque or driveline gearing or both must increase. But changes in these TDS attributes also have side effects; for instance, higher motor torque means a larger traction motor or higher gear ratio. If the gear ratio is higher, then the traction motor must be capable of higher maximum speed.

$$\theta = \sin^{-1} \left\{ \frac{g_{dl} m_{pk}}{g r_w M_v} \right\} \quad (4)$$

These influences are shown more clearly in Figure IV - 44 for the Nissan Leaf AEV, where driveline gearing and tire rolling radius are selected to meet a $V_{WOT} = 92$ mph target and the motor peak torque sufficient for acceptable grade capability.

Figure IV - 44 illustrates the energy consumption contours of a commercial AEV when driven on the US06

cycle only. The goal of this top level simulation is a similar full TDS energy consumption map for the five-standard-drive-cycle composite. Then the high throughput zones will be clearly identified for cascading to the PE and EMs. Figure IV - 45 is an example showing a peak power and peak torque traction motor contour plot with a high efficiency plateau of 96% for the IPM motor in the region of 60 Nm and 5,000 to 6,500 rpm (IPM rated 13,500 rpm maximum).

In Figure IV - 45 a strawman set of the six most frequent operating points is overlaid on the traction motor torque-speed characteristic to convey the intent of top level system simulation providing requirements to the PE and electric motor subsystems. These particular sets of points are exemplars for the following.

- 2010 HEV on 6% grade, driver only, $P(V) = 31$ kW; $m_{MG} = 48.7$ Nm; $n_{MG} = 6,385$ rpm
- Close to the map point used in benchmarking for peak efficiency
- Case of $V = 55$ mph on 0% grade; $m_{MG} = 15.6$ Nm; $n_{MG} = 6,385$ rpm
- Urban cruise, $V = 35$ mph on 0% grade; $m_{MG} = 8.95$ Nm; $n_{MG} = 4,063$ rpm
- WOT performance, at $V = 105$ mph sustained; $m_{MG} = 45$ Nm; $n_{MG} = 12,190$ rpm
- Dyno laboratory benchmarking base point, about 30 kW (continuous power requirement in DOE targets); $m_{MG} = 60$ Nm; $n_{MG} = 5,000$ rpm
- Maximum grade hold/climb requirement (Figure IV - 42) illustrative point; $m_{MG} = m_{pk}$ Nm (maximum stall torque of the traction motor); $n_{MG} \sim 0$ rpm to ~ 100 s rpm

It is the intent of this VTP program to apply the standard drives presented in this section, using an AEV model per Table IV - 6, to expand and clarify the results illustrated in Figure IV - 44.

APEEM's programs are directed toward TDS cost reduction and efficiency improvement and are being accomplished through material innovations, PE and electric motor architectures, and packaging innovations. Matsumoto [3] offers some relevant guidance in this respect, the main point being that the increase in system voltage from 500 V in 2003 to 650 V in 2005 facilitated a 20% reduction in power inverter volume (Table IV - 7). That trend is expected to continue, and Matsumoto says that Toyota is targeting a PD of 50 kVA/L by 2020 in a power converter unit using SiC.

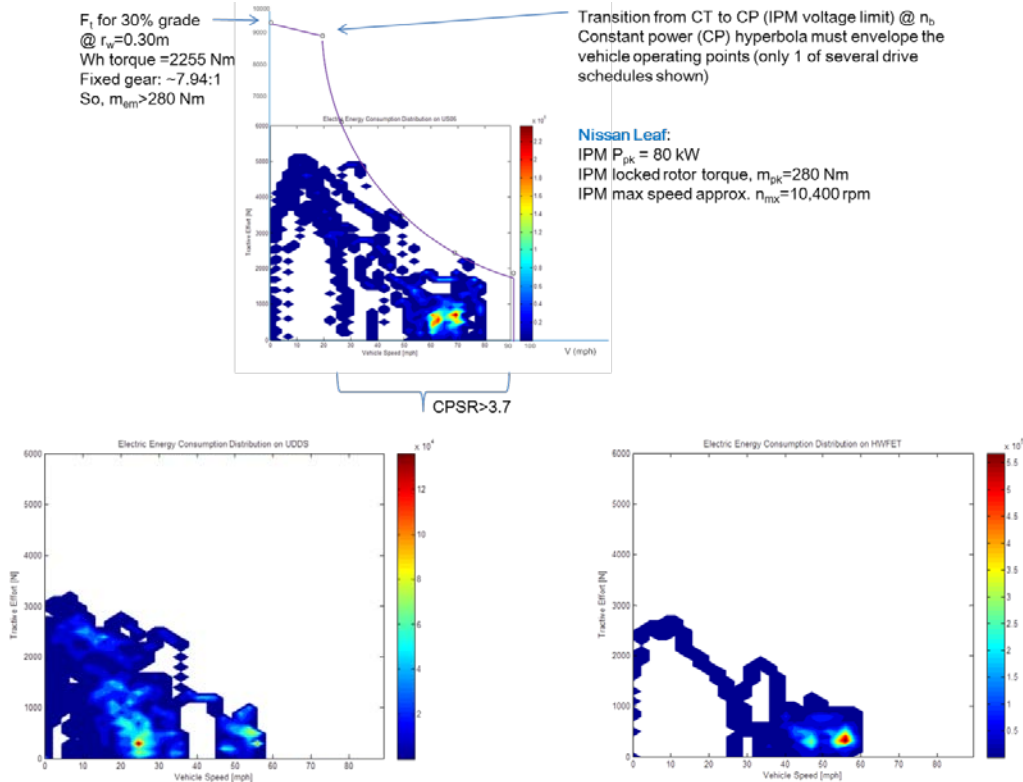


Figure IV - 44: Nissan AEV drive cycle energy consumption mapped to its traction motor. (Top) traction motor capability curve superimposed on US06 energy consumption map. (Bottom) UDSS and HWFET energy consumption maps. (Note: The labels in the figure provide most of the AEV traction drive and drive line parameters.)

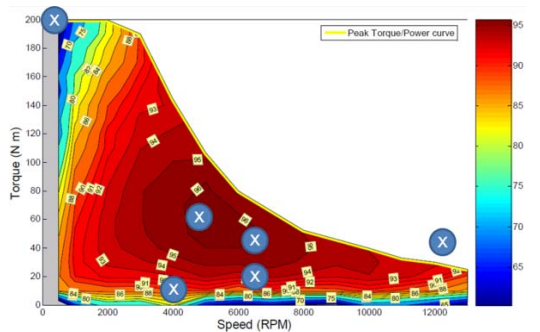


Figure IV - 45: Prius IPM motor efficiency contour for $U_{d0} = 650 V_{dc}$ (excerpted from TDS reference [3]).

It is insightful to contrast the performance metrics of today’s best in class internal combustion engine (ICE) hybrid vehicle power plants and transmissions with those of AEVs such as the Nissan Leaf. Because of the limited power range of an ICE, a multispeed transmission is necessary, whereas an electric traction motor having a high constant power speed ratio is well matched to the drive wheels by a single speed gearbox. This means the AEV TDS is capable of future integration into a fully integrated unit. This approach is being taken by Tesla motors, where

the power inverter, gearbox, and traction motor are combined into a single package. “Combined” is different from “integrated” in that the individual, standalone, functional modules (inverter, EM, gearbox) are in close proximity and share a common housing but are not integrated into one unit. Examples of combined traction drive units for AEVs include those developed or under development by Tesla Motors and Mitsubishi Motors (iMEV).

Note the performance metric summary in Table IV - 8 showing that the ICE has SP of 1.18 kW/kg and the AEV has SP of 1.38 kW/kg. The message is clear: today’s electric TDS can outperform best in class fossil fuel power plants.

Table IV - 7: Power electronics trends for PEVs with 120 kW traction motor.

System Parameters	Year		Comments
	2000	2005	
System voltage (V)	500	650	
Rating (kVA)	200	420	
Output current (A)	230	360	Based on 200 A class silicon trench IGBT
Mass (kg)	18	32	
Volume (L)	20	30	

Table IV - 8: Performance comparison of ICE with AEV TDS.

ICE	Engine	Trans	Metric
Power, Mass	134 kW 114 kg	6 speed 244 Nm ~80 kg	engine SP = 1.18 (kW/kg)
AEV	Electric Machine	Power Elect	Metric
Power, Mass	80 kW 58 kg	1 speed 280 Nm, 16.2 kg	E-Mtr SP = 1.38 (kW/kg)

Patents

None.

Publications

1. J. M. Miller and R. L. Smith, *Vehicle Performance Metrics Applied to Electric Drive Vehicle System Research*, ORNL/TM-2012-305, Oak Ridge National Laboratory, 2012.

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1. Philop Zuk, "High-Voltage Silicon MOSFETs, GaN, and SiC: All Have a Place," *Electronic Design News, EDN*, June 20, 2012.
2. Malikipoulos, A.A. and Aguilar, J.P., "An Optimization Framework for Driver Feedback Systems," *IEEE Transactions on Intelligent Transportation*. (in review).
3. Shinichi Matsumoto, "Advancement of Hybrid Vehicle Technology," presented at European Power Electronics Conference, EPE2005, Dresden, Germany.
4. Tim Burrell, et al., *Evaluation of the 2010 Toyota PRIUS Hybrid Synergy Drive System*, ORNL/TM-2010/253, Oak Ridge National Laboratory, March 2011.

V. Thermal Management Research and Development

V.1 Integrated Vehicle Thermal Management – Combining Fluid Loops in Electric Drive Vehicles

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Objectives

- Collaborate with industry partners to research the synergistic benefits of combining thermal management systems in vehicles with electric powertrains
- Improve vehicle range and reduce cost from combining thermal management systems
- Reduce volume and weight
- Reduce advanced power electronics and electric motor (APEEM) coolant loop temperature (less than 105°C) without requiring a dedicated system.

Approach

- Build a one-dimensional thermal model of EV thermal management systems (using KULI software)
- Identify the synergistic benefits from combining the systems
- Identify strategies for combining cooling loops
- Solve vehicle-level heat transfer problems, which will enable acceptance of vehicles with electric powertrains.

Major Accomplishments

- Improved the individual thermal models of the cabin air conditioner (A/C), cabin heater, APEEM, and energy storage system (ESS) fluid loops
- Completed a baseline EV thermal system model
- Added sophisticated controls to the A/C system and energy storage system (ESS) cooling loops
- Investigated combined cooling loop strategies
- Identified advantages of combining fluid loops.

Future Direction

- Based on the analysis results, select, build, and evaluate prototype systems in a laboratory bench test to demonstrate the benefits of an integrated thermal management system
- Collaborate with automotive manufacturers and suppliers on a vehicle-level project to test and validate combined cooling loop strategies.

◇ ◇ ◇ ◇ ◇

Technical Discussion

Introduction

Plug-in hybrid electric vehicles (PHEVs) and electric vehicles (EVs) have increased vehicle thermal management complexity (e.g., power electronics, motors, energy storage, and vehicle cabin). Multiple cooling loops may lead to reduced effectiveness of fuel-saving control strategies. The additional cooling loops increase weight, volume, aerodynamic drag, and fan/pump power, thus reducing electric range. This reduces customer acceptance of electric drive vehicles (EDVs) by increasing range anxiety, and presents a barrier for the penetration of EVs into the national vehicle fleet. Our goal is to improve vehicle performance (fuel use or EV range) and reduce cost by capturing the synergistic benefits of combining thermal management systems. The overall goal is to solve vehicle-level heat transfer problems, which will enable acceptance of vehicles with electric powertrains

The objective of this project is to research the synergistic benefits of combining thermal management

systems in vehicles with electric powertrains. Currently, EDVs typically have a separate cooling loop for the APEEM components. It would be beneficial to have an APEEM coolant loop with temperatures less than 105°C without requiring a dedicated system. Range would be increased in the winter with a combined thermal management system that maximizes the usage of waste heat from the APEEM and ESS components to minimize electrical resistive heating using battery energy. With increased focus on aerodynamics, minimizing the area and number of heat exchangers in the front end of the vehicle has the potential to reduce drag. Combining cooling loops enables the capability to thermally precondition the ESS and passenger compartment as well as the thermal management fluid loops.

Background

In the first year of the project (FY11), Visteon Corporation, a Tier 1 automotive heating, ventilation, and A/C (HVAC) component supplier, supplied detailed thermal component and system information. This included drawings, thermal and flow component data, and system performance data. National Renewable Energy Laboratory (NREL) researchers built component models in KULI using the geometry, heat transfer, and pressure drop information. The individual component models were verified to function as expected. Next we developed A/C, cabin thermal, and APEEM cooling loop models by combining the individual component models into systems. These systems were then compared to test data. This formed the basis for the complete analysis of EV thermal

systems and the assessment of combining cooling loop strategies that was performed in FY12.

Approach

The overall approach is to build a one-dimensional thermal model (using KULI software). This includes APEEM, energy storage, and passenger compartment thermal management systems. The model is used to identify the synergistic benefits from combining the systems. Once promising combined cooling loop strategies are identified, bench tests will be conducted to verify performance and identify viable hardware solutions. NREL will then collaborate with automotive manufacturers and suppliers on a vehicle-level project.

There are three main parts to the modeling process: the vehicle cost/performance model [1], the thermal model, and the battery life model. The vehicle cost/performance model simulates an EV over a drive cycle. An output of the model is the time-dependent heat generated in the APEEM and ESS components. These data are used as an input to the thermal model. KULI [2] was used to build a model of the thermal systems of an EV, including the passenger compartment, APEEM, and ESS. The thermal model calculates the temperatures of the components and the power required by the various cooling systems, including the fans, blowers, pumps, and A/C compressor. The power consumption profile is then used in the vehicle cost/performance model, and a new heat generation is calculated. If the heat generation is significantly different from the initial run, it is entered into the KULI thermal model again, and the cycle is repeated. An overview of the analysis flow is shown in Figure V - 1.

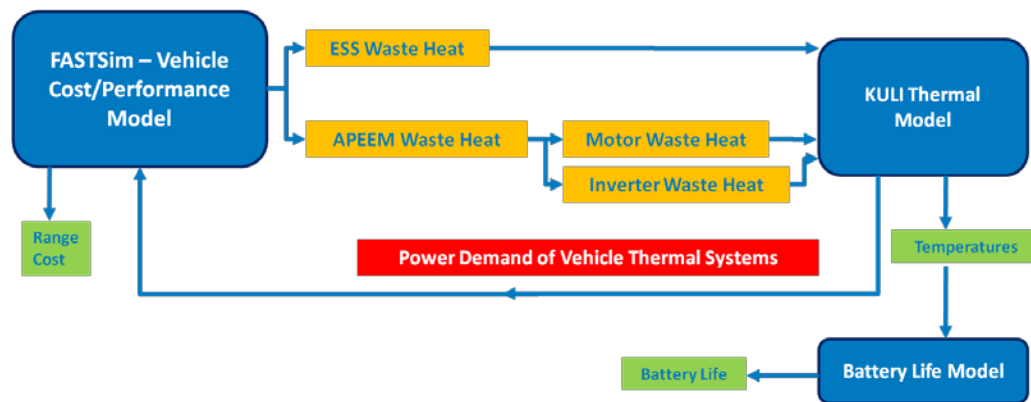


Figure V - 1: EV integrated vehicle thermal management analysis flow diagram.

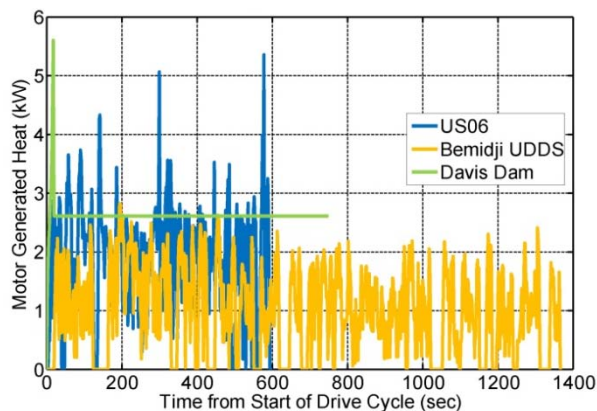
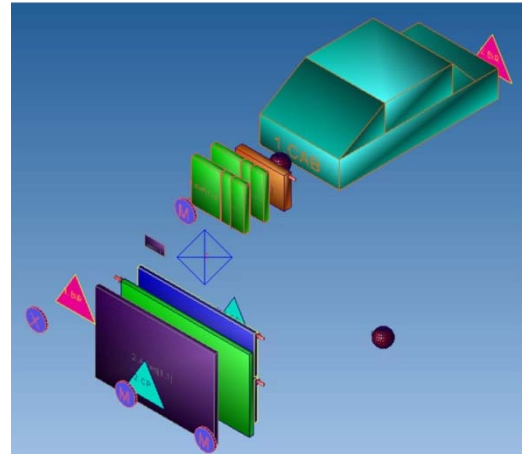
The performance of the vehicle thermal management system was evaluated over three vehicle drive profiles, and each were created to represent different driving conditions for hot and cold environments. A summary of the drive profiles and ambient thermal conditions is summarized in Table V - 1.

Table V - 1: Drive profiles and environmental conditions.

Condition	Drive Cycle Profile	Ambient Temperatures (°C)	Relative Humidity (%)
Hot soak with cooldown*	US06	43, 35, 30, 25	25
Hot soak with cooldown*	Davis Dam	43	25
Cold soak with warmup	Bemidji	-18	40

* In each of the hot soak tests, the vehicle cabin was assumed to be soaked to an initial temperature of 20°C above the ambient temperature.

The US06 drive profile [3] was selected as a standard test cycle with aggressive driving to evaluate the ability of the thermal management system to manage thermal loads over aggressive transient driving with multiple acceleration and braking events. The Davis Dam drive profile represents accelerating from a stop to 55 mph, and maintaining 55 mph up a constant 5% grade in a hot ambient environment. This profile provided a test of the thermal management system at extreme operating conditions. The Bemidji drive profile was selected to represent less aggressive driving conditions with a cold ambient temperature. The drive profile is based on the standard UDDS cycle [4]. A less aggressive drive cycle was selected to reduce the waste heat generated within the components and reduce self-heating. The intent was to provide an extreme cold weather test. A comparison of the motor heat load for each of the drive profiles is shown in Figure V - 2.

**Figure V - 2:** Comparison of drive cycles in terms of motor heat load.**Figure V - 3:** Air-side components of baseline thermal model.

The baseline electric vehicle thermal management system is illustrated in Figure V - 3 and Figure V - 4. Figure V - 4 provides a schematic of the thermal management system that enables heating and cooling of the vehicle passenger compartment or cabin, cooling for the electric drive system consisting of power electronics and an electric motor, and heating and cooling of the ESS or battery. Heating for the vehicle cabin is provided by an electric heater that heats a fluid loop and transfers heat to the cabin with a conventional heater core. Cooling for the vehicle cabin is provided by a conventional vehicle A/C system and an electric compressor. The power electronics and motor are cooled through a radiator that is located at the front of the vehicle behind the A/C condenser. The ESS or battery has multiple operating modes. Cooling is provided by two methods using either a chiller connected to the air conditioning system or a radiator at the front of the vehicle. The chiller is used for hot ambient conditions to provide chilled liquid coolant to the battery. Battery warmup can also be improved during cold conditions through the use of an electric heater to heat the liquid coolant circulating through the battery.

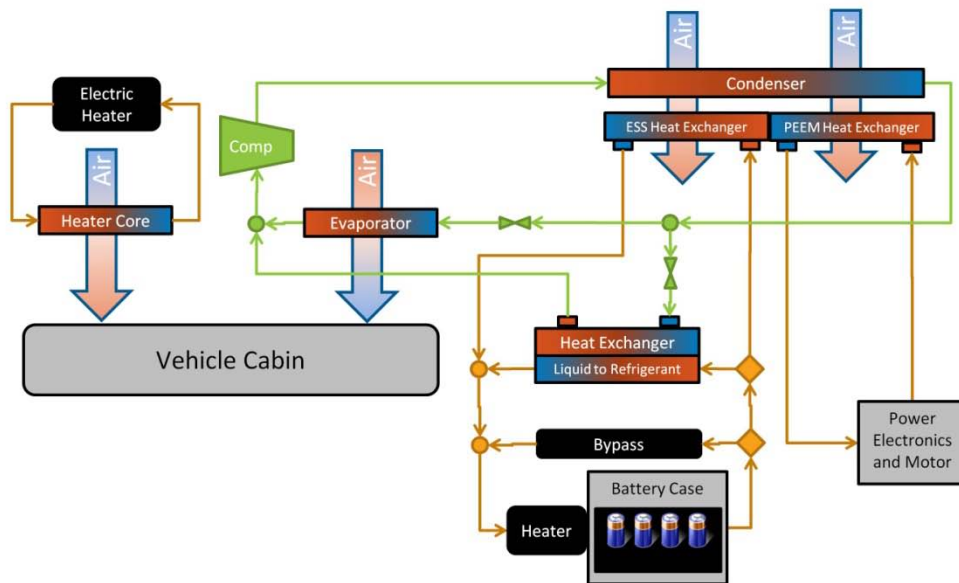


Figure V - 4: Baseline cooling system and primary components.

In addition to modeling the liquid and refrigerant loops of the vehicle thermal management system, the model also simulates the external airflow through the heat exchanger surfaces as shown in Figure V - 3. As outside air passes through upstream heat exchangers, the air is heated. For this reason, the performance of the downstream heat exchangers are impacted by the heat rejection of the upstream heat exchangers. The model is capable of capturing this interaction between heat exchanger placement and airflow.

During FY12, modeling work focused on improving the baseline vehicle thermal model and developing preliminary thermal models of alternative thermal management configurations. The improvements to the baseline vehicle thermal model were based on input from component specialists and comparisons to available thermal data. The baseline model improvements can be broken down into the following areas:

- System thermal loads
- System thermal model enhancements
- System controls.

The thermal loads for the battery, power electronics, and motor were revised based on the latest updates to the FASTSim vehicle model for a compact-sized electric car. In addition to updating the vehicle model, additional drive profiles were added to the vehicle model to evaluate the vehicle operation over more operating conditions (i.e., Davis Dam and Bemidji).

Improvements to the original baseline component and system thermal models include the addition of new system

thermal models and the improvement of existing models based on reviews with component experts. The battery cooling loop was revised to enable multiple cooling modes for cooling and heating the battery. The ability to heat the battery coolant was added to improve battery warmup during the new cold environment tests. The updated battery thermal model thermal performance and properties were reviewed with the NREL ESS group. The power electronics and motor thermal systems were improved based on input from the NREL APEEM group. The initial motor thermal model parameters were updated, and a new inverter thermal model was created based on feedback from the Electrical and Electronics Technical Team (EETT) within US DRIVE. Also, thermal models for cabin heating components were created and integrated into a working cabin heating system to enable vehicle warmup tests from cold environmental temperatures. This feature was added based on previous feedback from the DOE Annual Merit Review. Finally, the air-side positions of the vehicle heat exchangers were adjusted to more closely match current EVs with the condenser in the front.

System controls were created for the baseline thermal model to control the battery and cabin to the desired target temperatures. The cabin temperature was controlled by regulating the airflow into the cabin, activating an electric heater, and controlling the refrigerant loop compressor speed. The battery temperature was controlled by controlling the battery coolant loop pump speed, and the valves controlling the flow through the multiple fluid loop branches. When the refrigerant loop was active to cool the vehicle cabin, the controller adjusted the compressor speed

to prevent evaporator freezing. The thermal system control logic was based on a state controller with multiple operating states. The thermal management operating state was determined from the environment temperature, component temperatures, and the cooling system fluid temperatures. Each control state adjusted the control variable for the multiple actuators in the vehicle thermal system model. The control for each of the actuators was based on a proportional integrator (PI) antiwindup controller with the general logic shown in Figure V - 5.

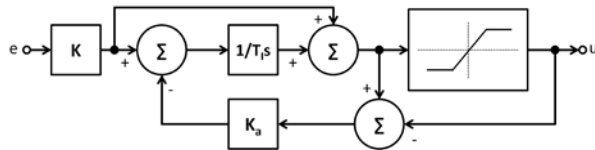


Figure V - 5: Antiwindup PI Controller [5].

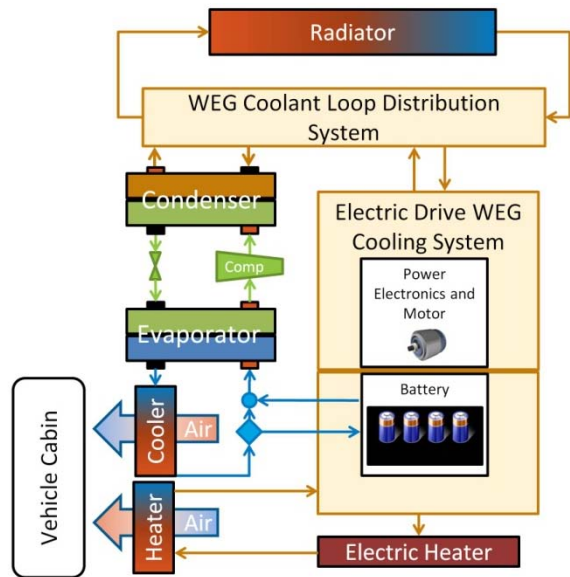


Figure V - 6: Combined system drawing.

In addition to improving the baseline thermal model, new system thermal models were developed to investigate potential combined cooling loop strategies. The overall goal of combining cooling loops was to identify the potential use of waste heat from the electric drive components, and to evaluate concepts that could reduce the number of heat exchangers at the front of the vehicle.

Figure V - 6 shows an illustration of the combined cooling system concept. The system enables the use of waste heat from the power electronics and electric motor for battery heating or cabin heating. The concept reduces front-end heat exchangers in the baseline system from three to one. The combined system uses a single chilled liquid loop for cabin and battery cooling at hot ambient temperatures that enables a compact refrigerant loop and heat pump operation.

The key features of the combined cooling system were evaluated to determine feasibility and effectiveness. The ability to utilize waste heat from the power electronics and electric motor was evaluated along with the ability to satisfy cooling demands during hot ambient conditions with a single front-end heat exchanger. Figure V - 7 shows the system schematic when operating in heating mode. The refrigerant cooling loop is off and cabin heating is provided with an electric heater, similar to the baseline thermal system. The primary difference is the connection between the electric drive cooling system, battery thermal management, and cabin. Waste heat from the electric drive system can be used to enhance the warmup of either the vehicle cabin or battery. To prevent component overheating, the radiator cooling branch can be activated as needed.

Figure V - 8 shows the schematic when operating in cooling mode for a hot ambient condition when a chiller is needed for cabin and battery cooling. The battery is cooled using a common chilled fluid that is also used for cabin cooling. For the illustrated condition, the battery is located downstream from the cabin cooling heat exchanger. For this reason, the battery coolant inlet temperature is affected by the cabin cooling airflow.

The intent of the analysis is to evaluate a worst-case condition where the cabin cooling airflow is set at the maximum value with a hot ambient temperature. The heat removed from the chilled liquid is transferred through another liquid loop that circulates through a radiator at the front of the vehicle. In addition to rejecting heat from the chilled liquid system for the air conditioning and battery, the radiator also rejects heat from the power electronics and electric motor.

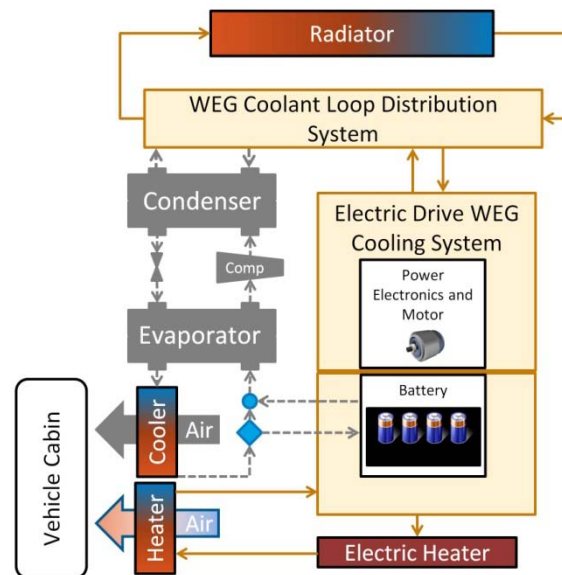


Figure V - 7: APEEM waste heat utilization for battery or cabin heating (warmup).

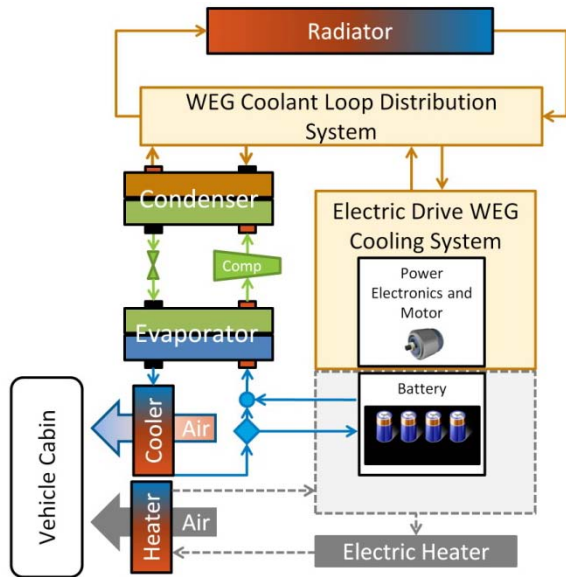


Figure V - 8: Combined radiator system and cabin/battery chiller (cooldown).

Results

The performance of the baseline thermal management system is shown in Figure V - 9–Figure V - 12 over the US06 aggressive transient drive cycle at multiple ambient temperatures. Based in NREL outdoor vehicle test data from multiple vehicles, the initial soak temperature of the vehicle cabin is assumed to be 20°C above ambient, and the initial soak temperature of the battery was assumed to be 1.6°C above ambient. The cabin target temperature was set to 25°C, and the battery cell target temperature was also set to 25°C.

The cooldown curves for the cabin in Figure V - 9 show reasonable cooldown profiles. The cooldown curves for the battery cell temperature are shown in Figure V - 10. The reason for the increasing battery cell temperature for the 25°C ambient test case is because the system controls were adjusted to force cooling through the radiator in the moderate environment.

The ability to cool the battery through the radiator and not the chiller is reflected in the reduced power needed for the thermal management system in Figure V - 11. The coolant inlet temperature to the APEEM system is shown in Figure V - 12. The coolant temperature is below the 70°C maximum inlet temperature limit [6]. Figure V - 12 also shows the interactions between the air-side heat exchanger placement and the coolant loops. For the 43°C ambient case, the A/C system is running at full power and the heat is rejected to the ambient through the condenser which subsequently warms the air entering the APEEM radiator resulting in a higher APEEM coolant temperature. For the 30°C ambient case, the cabin and battery approach the target temperature and the total vehicle thermal management power drops. The reduced cooling demand on

the condenser reduces the outlet air temperature of the condenser and reduces the inlet air temperature to the APEEM radiator.

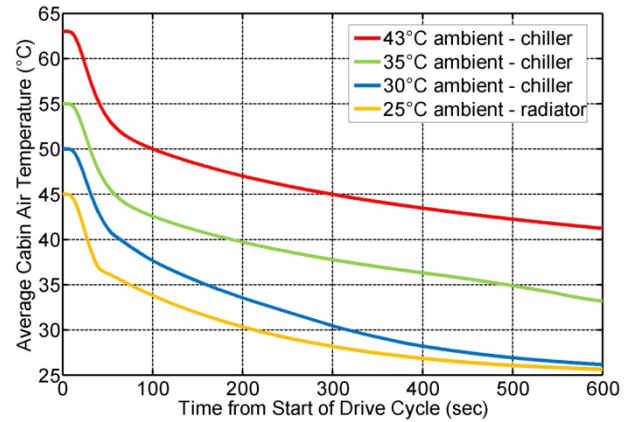


Figure V - 9: Baseline cabin air temperature over the US06 drive profile.

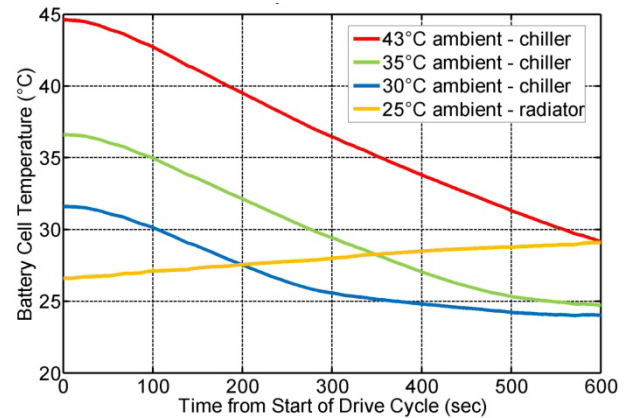


Figure V - 10. Baseline battery cell temperature over the US06 drive profile.

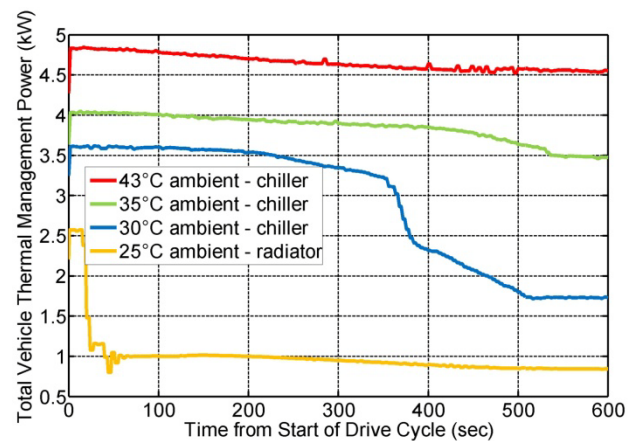


Figure V - 11: Baseline vehicle thermal management power over the US06 drive profile.

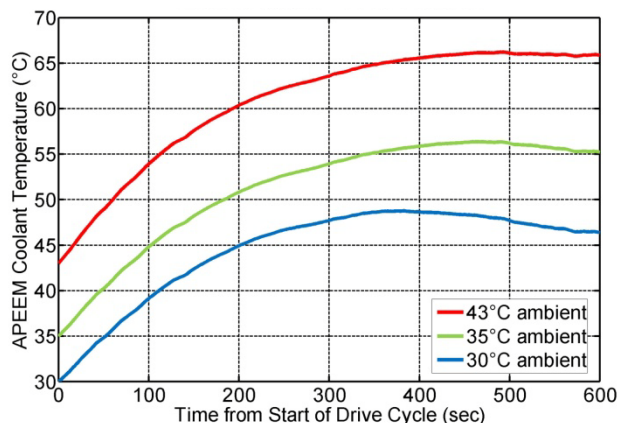


Figure V - 12: Baseline APEEM coolant inlet temperature over the US06 drive profile.

The baseline heating performance over the Bemidji test profile is shown in Figure V - 13–Figure V - 15. The baseline heating performance uses 7 kW for cabin heating and 1 kW to supplement the battery warmup. The baseline results are compared against two different combined cooling loop strategies using the APEEM waste heat (Figure V - 7). The first scenario links the APEEM cooling system with the cabin heater. The cabin heater power is reduced to 5.8 kW and the waste heat from the APEEM components is used to maintain equivalent cabin heating performance as seen in Figure V - 13. While meeting the same cooling performance, the coolant temperature to the APEEM components remains below the upper temperature limit of 70°C as seen in Figure V - 14. The second scenario links the APEEM cooling system with the ESS thermal management loop. The waste heat from the APEEM system is used to improve the warmup of the battery, and the 1 kW battery heater is off (Figure V - 15). The total vehicle thermal management power was reduced 1 to 1.2 kW with these configurations.

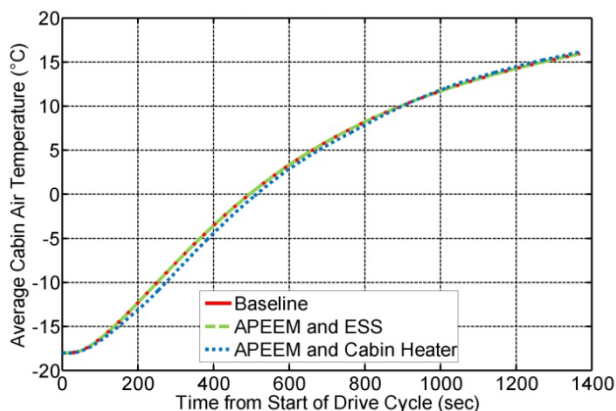


Figure V - 13: Comparison of cabin air temperature for baseline and alternative heating configurations for Bemidji -18°C condition.

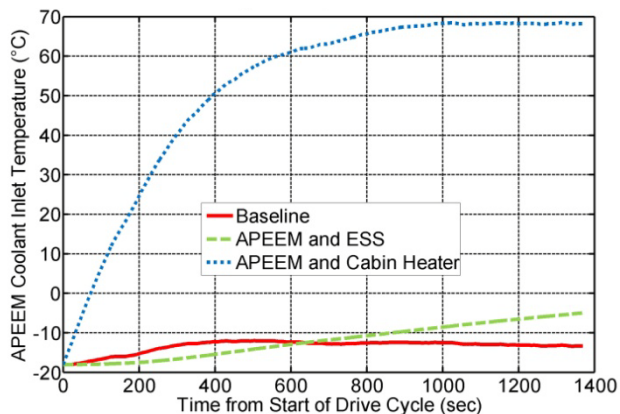


Figure V - 14: Comparison of APEEM coolant temperature for baseline and alternative heating configurations for Bemidji -18°C condition.

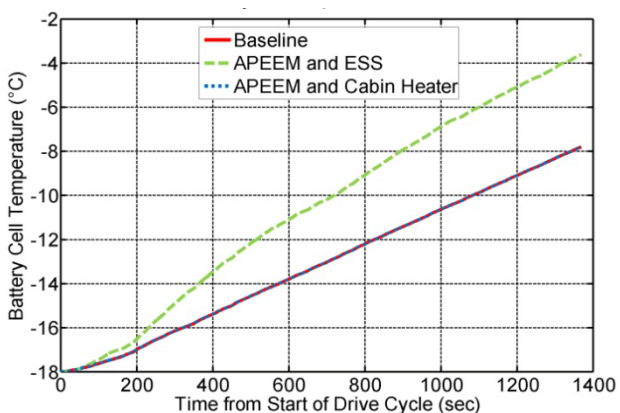


Figure V - 15: Comparison of battery cell temperature for baseline and alternative heating configurations for Bemidji -18°C condition.

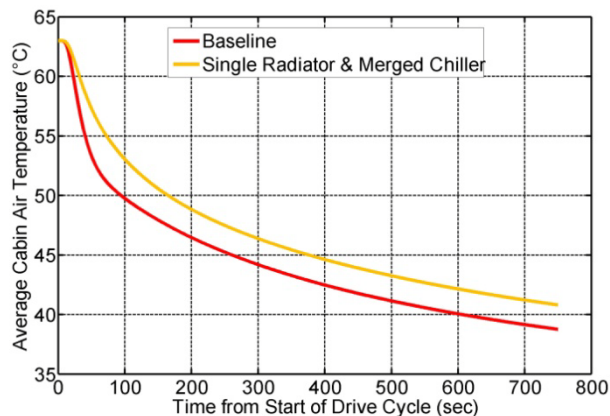


Figure V - 16: Comparison of cabin cooldown performance of baseline and combined configuration for Davis Dam 43°C condition,

Besides the alternative warmup configurations, the ability to reduce the front-end heat exchangers from three to one (as shown in Figure V - 8 was evaluated. In this configuration, the condenser, APEEM radiator, and ESS radiator are combined into a single low-temperature radiator. The air-to-refrigerant condenser and evaporator

are replaced with a liquid-to-refrigerant condenser and evaporator. The results of the combined system are compared with the baseline system in Figures 16-18. The single radiator configuration uses a radiator that is 0.71 m tall and 0.51 m wide with a maximum airflow per frontal area of $3.87 \text{ kg}/(\text{s}\cdot\text{m}^2)$. Both the size and airflow are within the range of typical automotive radiators [7,8].

Figure V - 16 compares the cabin cooldown performance and shows the combined system has slightly reduced cabin air cooling performance. This reduced cooling performance is typical for a secondary loop system. The reduced performance in cooling the battery (Figure V - 17) is because of the increased emphasis on cabin cooling in the combined cooling system. Both the cabin and battery are cooled with the same secondary loop chiller, although the battery is placed downstream of the cabin cooling heat exchanger. The impact on the battery could be mitigated by adjusting the cabin cooling airflow.

Figure V - 18 compares the coolant temperature for the APEEM system. The combined cooling configuration provides a lower coolant temperature relative to the baseline system, and eliminates the dedicated liquid loop and heat exchanger for the APEEM system. Even with the combined A/C condenser and APEEM components adding heat to the cooling fluid, the coolant temperature was lower than the baseline case because the air entering the single radiator was at ambient temperature and not pre-warmed by the A/C condenser as in the baseline case.

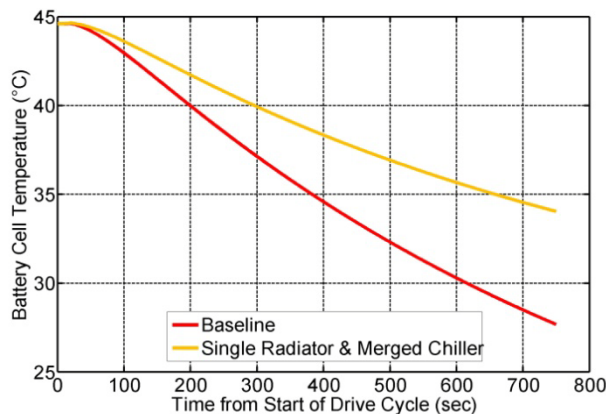


Figure V - 17: Comparison of battery cell temperature of baseline and combined configuration for Davis Dam 43°C condition.

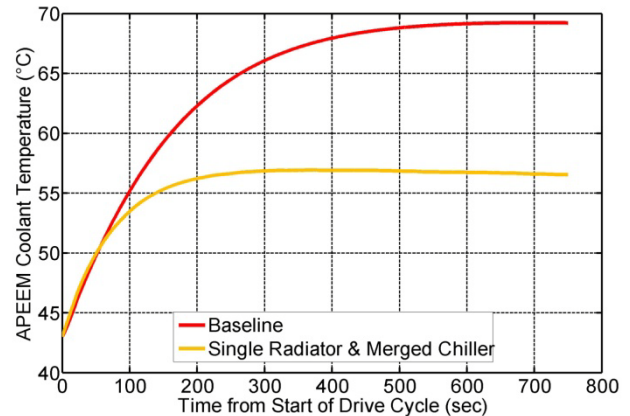


Figure V - 18: Comparison of APEEM coolant temperature of baseline and combined configurations for Davis Dam 43°C condition.

Conclusion

NREL researchers developed a modeling process to assess synergistic benefits of combining cooling loops. A KULI thermal model of a compact-sized EV was built, which produced reasonable component and fluid temperatures. This model was then used to assess combined cooling loop strategies. By using the waste heat from APEEM components, the total vehicle thermal management power was reduced. Replacing the air-to-refrigerant heat exchangers with refrigerant-to-liquid heat exchangers resulted in slightly reduced cabin air and battery cooldown performance. By adjusting component sizes and flowrates, it is likely the baseline cooldown performance could be matched.

The refrigerant to liquid heat exchanger (chiller) would enable the benefits of a secondary loop system. If a flammable refrigerant is used, the refrigerant would not enter the passenger compartment and a lower charge would be needed. Having a chilled liquid would then enable multiple cooling points without the concern of oil trapping common in dual evaporator systems and eliminate the condensation concerns and associated smells as long as the chilled liquid was maintained above 32°F. For EVs, the chilled liquid could be used for APEEM and ESS thermal management. Combining the chiller with the refrigerant to liquid heat exchanger (condenser), a heat pump system can be designed that does not reverse the flow of the refrigerant. By reversing the flow of the liquid loops, the A/C system is simplified and more efficient heating of the vehicle is possible compared to electric resistance heating. Also the opportunity to use APEEM and ESS waste heat for cabin heating is available in this type of system.

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V.2 Physics of Failure of Electrical Interconnects

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Objectives

In automotive power electronics modules, standard packaging technologies have limited the advancement of insulated gate bipolar transistor (IGBT)-based power modules toward designs that promise higher performance and reliability. Increased power densities and larger temperature swings reduce lifetimes for traditional wire bond interconnects. Replacement of wire bonds can be accomplished with a transition to ribbon bonding technology. The ribbon bond process promises a reduction in bonding time, lower loop heights and corresponding less heel fatigue, and higher current densities than wire bonds. However, as a newer technology, ribbon bond failure mechanisms are not as well understood and thus do not have an accurate lifetime estimate. The objective of this research is to investigate and improve the reliability of the ribbon bonding process using aluminum (Al) and copper/aluminum (Cu/Al)-clad ribbon material. Completion of experimental testing will highlight suitable ribbon bonding geometries that provide higher electrical and mechanical performance than wire bonding while maintaining desired reliability. The objectives for FY2012 were to:

- Collaborate with industry partners for selection of ribbon material and bonding process.
- Design and synthesize test sample substrates that represent a variety of wire and ribbon bonding geometries.
- Establish laboratory capabilities for evaluating the reliability of ribbon interconnects under a variety of

accelerated thermal, power, humidity, and vibration conditions.

- Model wire and ribbon bonding geometry using analytical and numerical methods to calculate maximum deflections and strains while under elevated thermal conditions.
- Update wire physics-of-failure (PoF) lifetime estimation models to incorporate ribbon bond geometry.

Approach

- Synthesize sample packages that incorporate ribbon interconnect technology under a variety of material and geometry selections.
- Perform mechanical tests on the ribbon bond interconnects to obtain information on initial bond strength and strength after accelerated testing conditions.
- Perform thermal elevation, thermal cycling, combination power and thermal cycling, high humidity, and vibration testing to accelerate failure mechanisms within ribbon interconnects. Perform destructive mechanical tests and cross-sectioning after completion of accelerated testing.
- Update wire bond PoF models to provide ribbon interconnect lifetime estimation.
- Provide a conclusion on the performance and reliability advantages of transitioning from wire to ribbon bond technology.

Major Accomplishments

- Designed and produced large area alumina test substrates that enable the bonding of wire and ribbon interconnects under a variety of geometry conditions.
- Completed die attach and ribbon bonding to test substrates for initial bond strength evaluation.
- Developed relationships with industry partners – Materion Technical Materials (MTM) for the ribbon materials and Orthodyne Electronics (OE) for ribbon bonding on test substrates.
- Enhanced NREL capabilities to complete accelerated testing of ribbon bond interconnects.
- Generated finite element analysis (FEA) models to predict heel stresses within wire and ribbon bonds.

Future Direction

The following activities are envisioned for this project for FY2013:

- Complete accelerated testing of ribbon interconnects technology.
- In conjunction with PoF models, obtain estimates for cycles to failure.
- Provide recommendations to industry on the incorporation of ribbon bonding into power electronic package designs.



Technical Discussion

Introduction

The drive towards reduced cost, weight, and volume of components in electric drive vehicles has led to increased performance demands on power electronics modules. The trend towards higher power densities, current levels, and operating temperatures has shown that traditional packaging designs cannot meet the industry's reliability needs. Figure V - 19 shows an example of a power electronics package with wire/ribbon bonds, silicon die (IGBT or diode), metalized substrate, and base plate components.

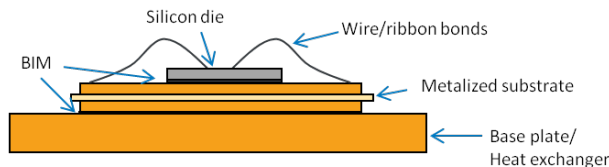


Figure V - 19: Traditional power electronics package.

Wire bonding technology is used to electrically connect dies to each other, to the top metallization layer within the substrate, or to lead frames for connections outside of the power electronics package. Gold, copper, or aluminum has traditionally been used as the material of the wire, with each having tradeoffs in cost, current carrying capability, and mechanical strength [1]. For most common applications, aluminum has replaced gold and copper due to its lower cost, but copper is still selected for power module designs with high current requirements.

In addition to material selection, the maximum current a wire can carry is dependent on its length and diameter, where wire sizes typically range between 300 and 500 μm in diameter. If the maximum current level is exceeded, ohmic self-heating will lead to fusing of the wire [2]. Heating from within the wire as well as from the silicon dies creates large temperature fluctuations during operation. These temperature variations and coefficient of thermal expansion (CTE) mismatches between the wire material and silicon dies or metalized substrates cause

failures in the heel of the wire through flexure fatigue as well as bond pad liftoff. Analytical models have been developed for both failure modes to estimate the mean number of cycles to failure. Failure modes for wire and ribbon interconnects are shown in Figure V - 20.

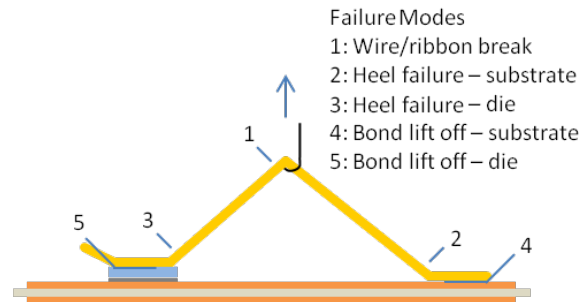


Figure V - 20: Wire and ribbon interconnect failure modes.

For high-current power modules, mechanical limitations to bonding a wire with a diameter larger than 500 μm has required multiple wires to be bonded in parallel. Adding additional parallel wires is limited by a substrate's bond pad area and increases the time and cost of bonding. These limitations have generated interest in replacing wire bonds with ribbon bonding technology, shown in Figure V - 21. Three aluminum wire bonds with diameters of 400 μm can be replaced on an equivalent electrical current basis by one ribbon bond with a cross section of 2,000 μm x 200 μm [3]. The single ribbon requires a bond width of 2 mm, while the three wire bonds require a width of 2.5 mm. Bonding times for both technologies remain the same (300 ms per bond); therefore, the ribbon bonding time for a package can be reduced. For the same span distance, a ribbon bond allows for a lower loop height than a wire bond. This helps to reduce heel stress and ultimately flexure fatigue. Minimizing heel stress is necessary as desired IGBT operating junction temperatures continue to rise to 175°C or higher [4]. However, due to the ribbon's larger geometry, higher bonding energies and forces are required and bond pad contact areas become larger. Damage initiated during the bonding process could become more likely under ribbon bonding, and coefficient of thermal expansion mismatches between the interconnect material and silicon devices or metalized substrate could cause failure under thermal cycling conditions.

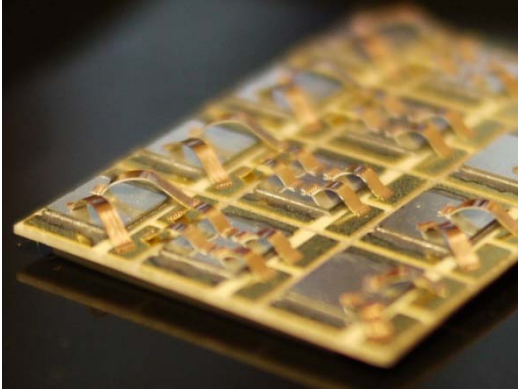


Figure V - 21: Ribbon bonds (Photo credit: Doug DeVoto, NREL).

While the performance and reliability of conventional wire bonding are well understood, lifetime uncertainties of newer interconnect technologies remain a barrier for those novel processes to be utilized by industry. NREL is focused on providing a comprehensive reliability assessment of alternative interconnect technologies to wire bonds, beginning with ribbon bonding. Ribbon bonds are attached to a substrate under a variety of materials and geometries, and then subjected to accelerated test conditions that highlight the same failure mechanisms found under normal operating conditions. Unique ideas to ribbon bonding will be evaluated, first with the selection of a Cu/Al-clad ribbon that allows the aluminum to be easily bonded to silicon die surfaces while providing the improved electrical performance of copper [5]. The ribbon's rectangular cross-section geometry makes twisting to create forced angles more difficult than with wire bonding; therefore, bonds with several forced angles will be attached to substrate samples [6]. The proposal to attach multiple ribbons over the same bond pad location will be explored as a stacked bonding technique [7]. In conjunction with accelerated testing, PoF models based on wire bond geometry will be validated for ribbon bonds.

Materials and Sample Synthesis

NREL has chosen several ribbon materials under various geometries for accelerated testing. The variations are as follows:

- Material – Al ribbon and a 1:2 ratio Cu/Al-clad ribbon.
- Ribbon cross-section – Two cross-sections suitable for current levels within a power module were chosen to be 2,000 μm x 200 μm and 1,000 μm x 100 μm .
- Ribbon span – 10-mm and 20-mm spans selected. Corresponding loop heights were set at a ratio of 1:2.2 to ribbon span.
- Number of stitches – Single and double stitches were bonded for 20-mm ribbon spans.

- Ribbon stacking – Stacking one ribbon pad above a second pad can minimize bonding area on top of a die but may create a weaker bond.
- Forced angle – Forcing a ribbon at various angles from its bond pad orientation would allow for offset pad locations, but may also create a weaker bond.
- Bond pad interfaces – One end of each ribbon will be bonded to a silicon die and the other end to a substrate's top Cu metalized surface.
- Bonding power – Two bonding powers were selected to evaluate the relationship between bond pad strength and long-term reliability.

The ribbon material and geometry variations cover a design space likely used within a power electronics unit if wire bonds were to be replaced with ribbon bonds. The ribbon bond variations are listed in Figure V - 22.

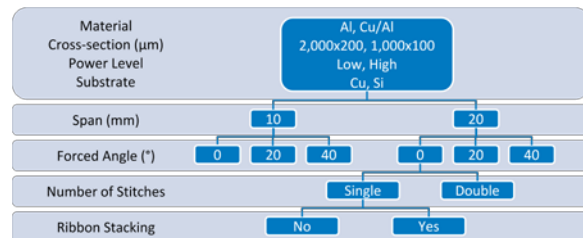


Figure V - 22: Ribbon bond variations.

Three instances of each ribbon configuration were arranged on a 140-mm x 190-mm test substrate. The substrate itself was obtained from Curamik and is constructed of a 0.635-mm-thick alumina layer sandwiched between two 0.203-mm-thick copper metallization layers. The design of the etch mask for the top copper layer configures four ribbon bonds electrically in series with multiple parallel paths. This layout was chosen for power cycling samples, but remains the same for all samples. Before the ribbon material was attached to the test substrate, Vishay 5-mm x 5-mm Schottky diodes were soldered in place. The selected diodes have a breakdown voltage of 100 V and can reach a maximum junction temperature of 175°C. The diode backside has a chromium/nickel/silver coating for good solderability, while the topside includes a 3- μm layer of aluminum (1% silicon) to be compatible with the ultrasonic bonding process. Each test substrate was imaged by acoustic microscopy to ensure that the solder attach for each diode contained minimal voiding, as shown in Figure V - 23.

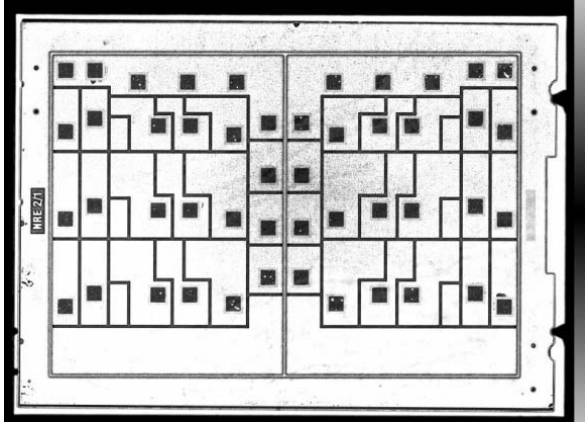


Figure V - 23: Acoustic microscopy analysis of solder attach (Photo credit: Doug DeVoto, NREL).

The first end of each ribbon interconnect was bonded to the top Cu metallization layer of the test substrate, while the second was bonded to the top surface of the diode. Both Al and Cu/Al-clad ribbon materials were obtained from MTM and were attached using an Orthodyne 3600 wedge bonder at OE. An example of a test substrate with a completed design layout is shown in Figure V - 24.

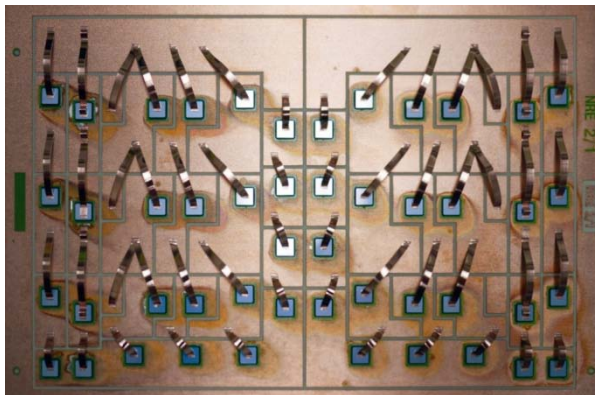


Figure V - 24: Test substrate showing ribbon layout (Photo credit: Doug DeVoto, NREL).

The four geometry variations (span, forced angle, number of stitches, and ribbon stacking) require eight ribbon bonds; repeating each variation three times brings the total number of bonds to 24, or one half of a test substrate. Including the additional ribbon selection variations (material, cross-section, and power level) requires a total of eight test substrate halves, or four test substrates. An additional test substrate is added to include 500- μm -diameter Al wire bonds as a reference to the ribbon bonds, thus requiring five test substrates for each accelerated test condition.

Ribbon Bonding Mechanical Characterization

An XYZTEC Condor 100-3 mechanical bond tester, shown in Figure V - 25, was used to measure the pull strength of the ribbon and wire bonds. As this was a

destructive evaluation, one set of test sample substrates without any prior accelerated testing was selected to measure initial bond strength through pull tests.



Figure V - 25: Mechanical bond tester (Photo credit: Doug DeVoto, NREL).

For the pull test, a hook was first positioned under the ribbon bond. At the initiation of the test, a constant velocity of 250 $\mu\text{m}/\text{s}$ was applied to the hook and maintained for a travel distance of approximately 4 mm. Sufficient force was used to maintain this velocity against the tensile strength of the ribbon material and strength of the bond pads. A test was completed when one of the five failure modes previously listed occurred, and the maximum force required for failure was recorded. An example of a ribbon pull test and its accompanying hook force data are shown in Figure V - 26.

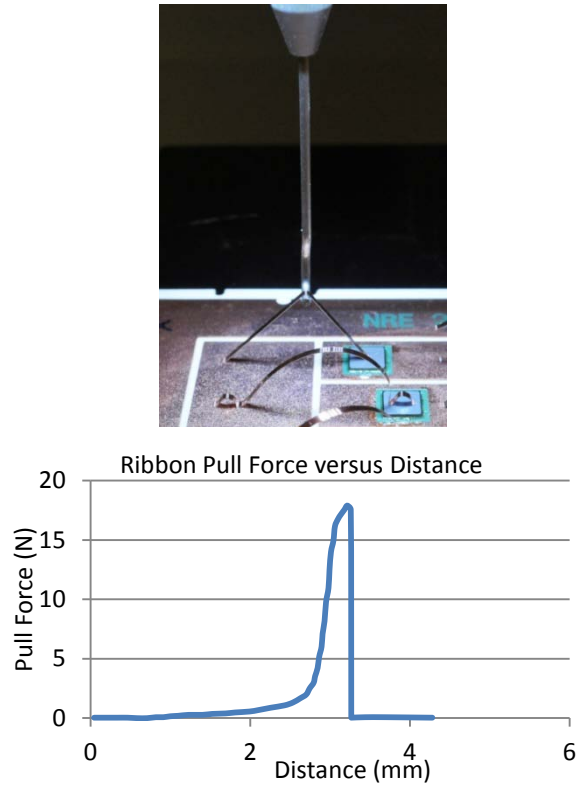


Figure V - 26: Ribbon pull test and pull force as measured from hook (Photo credit: Doug DeVoto, NREL).

In addition to recording the maximum tensile force, the failure mode was also documented. Images showing the most common modes are shown in Figure V - 27.

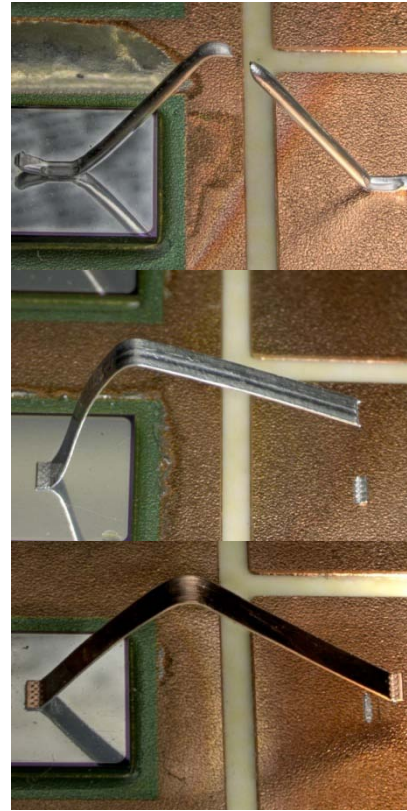


Figure V - 27: Failure modes from the left: wire break (top), heel failure from substrate (center), and bond liftoff from substrate (bottom) (Photo credit: Doug DeVoto, NREL).

Initial results from pull test data are shown in the following figures for Al wire, Cu/Al ribbon, and Al ribbon. The Al wire used has a cross-section of $500\ \mu\text{m}$ while the ribbon interconnects have $1,000\ \mu\text{m} \times 100\ \mu\text{m}$ cross-sections. The bonding power for ribbon interconnects is specified as either low or high. Three test bonds were completed for each bonding method that includes defined interconnect material, geometry, and bonding parameters. The averages of these pull strength tests with error bars indicating the standard deviations between tests are shown in Figure V - 28 between Al wire, Cu/Al ribbon, and Al ribbon.

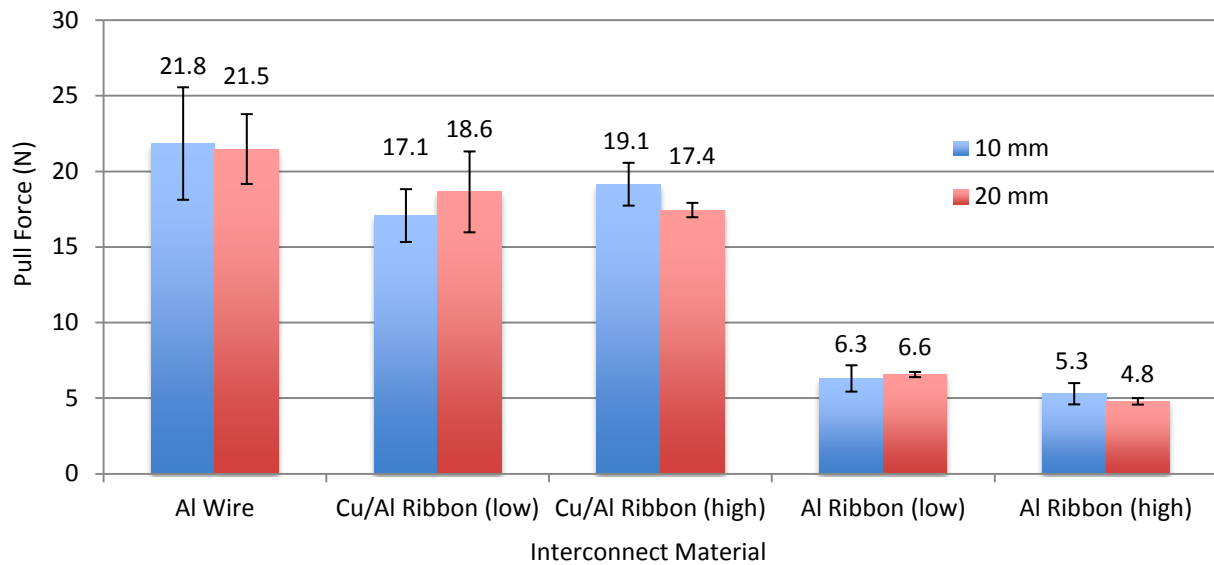


Figure V - 28: Pull force versus interconnect material.

Al wire interconnects exhibited the greatest strength from the pull tests, closely followed by Cu/Al ribbons. The strength of Al ribbon bonds was noticeably lower, but still strong enough to be considered successful. The key aspect to monitor is if the bond strength for each respective interconnect material significantly decreases after accelerated tests.

The failure mode associated with the above pull test measurements is shown in Figure V - 29. The three interconnects tested for each bonding method typically

failed by a similar method. While bond strength remained approximately the same between low and high power bonds for Cu/Al ribbons, it is interesting to note that the failure method shifted from bond pad lift-offs to heel failures. This indicates that the lower power setting for Cu/Al ribbons may not be sufficient to adequately bond the Al side of the ribbon to the metalized substrate, but accelerated testing will highlight if the lower power setting ultimately ends in a bond with longer lifetime.

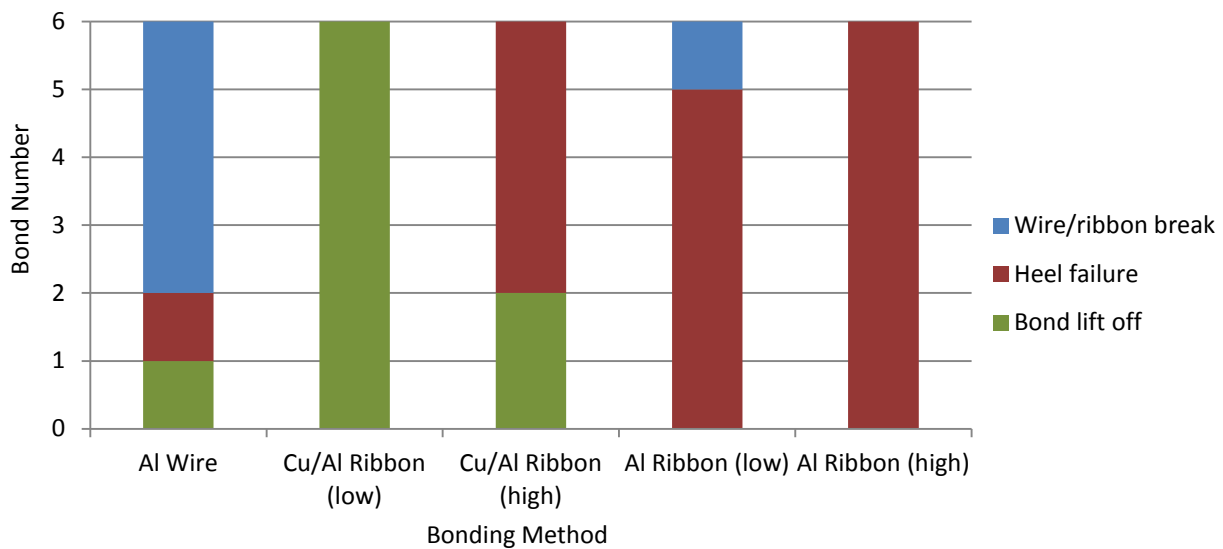


Figure V - 29: Failure modes for interconnect materials.

A similar analysis of bond strength and failure methods for Cu/Al ribbon interconnects at various forced angles was also completed. Results indicated that bond strength was reduced as a consequence of imparting a forced angle onto the ribbon bonds. The averages of these pull strength tests are shown in Figure V - 30, with error

bars indicating the standard deviations between tests. As previously apparent with Cu/Al ribbon bonds with no forced angle, increasing bonding force shifted the failure methods from bond pad lift-offs to heel failures.

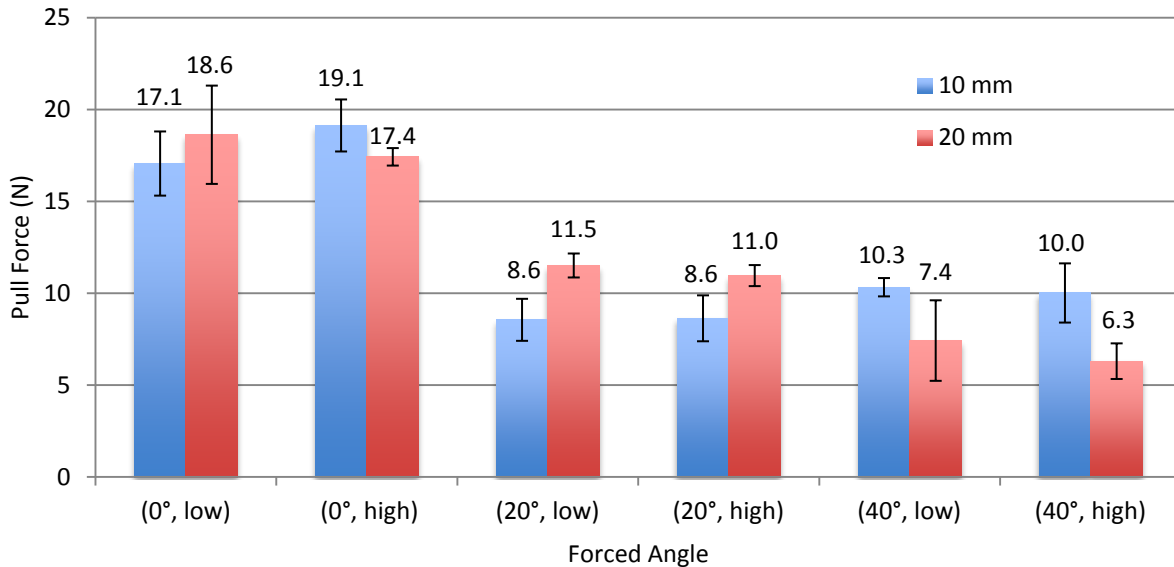


Figure V - 30: Pull force versus forced angle of Cu/Al ribbon.

The forced angle analysis was also completed for Al ribbon bonds, as shown in Figure V - 31. The bond strength is slightly reduced when incorporating forced

angle geometries, but the failure modes consistently were heel failures on either the die or substrate side of the ribbon.

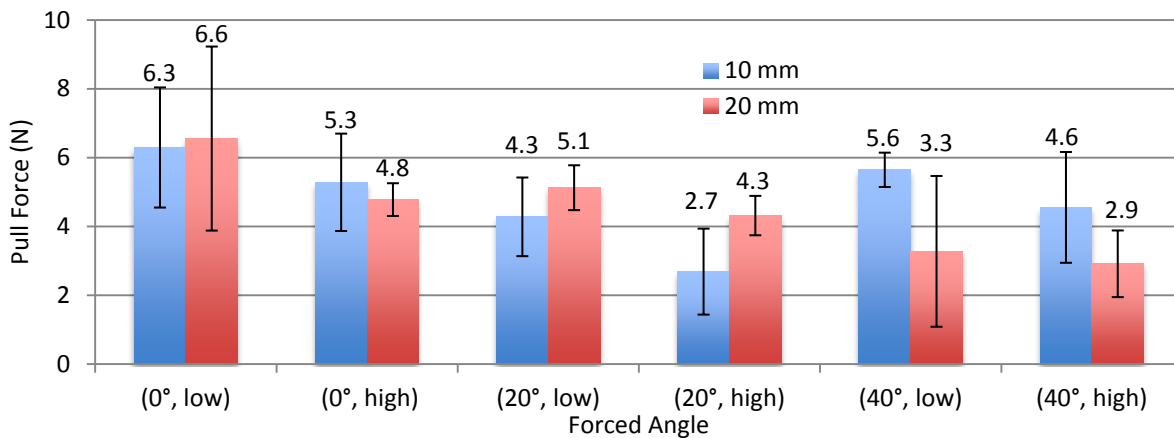


Figure V - 31: Pull force versus forced angle of Al ribbon.

Mechanical tests will be conducted on samples after they have completed their designated accelerated testing procedure. In addition to mechanical evaluation, cross sections of ribbon bond pads will provide a qualitative way to determine if the grain structure has changed after

accelerated testing. Bonding of dissimilar metals between the ribbon and pad causes intermetallic formation and Kirkendall voiding under high-temperature storage tests. Visual analysis will also monitor signs of corrosion development.

Accelerated Testing

Subjecting a component to accelerated conditions will identify its failure mechanisms in a reduced amount of time relative to normal operating stress conditions. Various

Table V - 2. Test procedures are based on standards developed by the JEDEC Solid State Technology Association [8].

accelerated tests have been selected to evaluate likely failure mechanisms within ribbon interconnects and are shown in

Table V - 2: Accelerated Testing Procedures.

Accelerated Test	Testing condition	Duration
Temperature Elevation	150°C	1,000 hours
	200°C	96 hours
Temperature Cycling	-40°C to 150°C, 10 minute dwell, 10°C/min ramp rates	2,000 cycles
Corrosion Testing	85°C, 85% relative humidity, cycled DC bias	1,000 hours
	121°C, 100% relative humidity	96 hours
Power Cycling	-40°C to 125°C, 10 minute dwell, 10°C/min ramp rates, cycled DC bias	1,500 temperature cycles
Vibration Testing	Highly accelerated life test (HALT)	Until interconnect fails

Accelerated test methods—humidity, thermal, power, vibration, or a mixture of the four—are designed to highlight a particular interconnect’s failure mode.

- Samples subjected to high-temperature storage testing will highlight thermally activated failure mechanisms. Ribbon bonds will be stored under two separate test conditions, at 150°C for 1,000 hours and at 200°C for 96 hours.
- Alternating temperature extremes will test the ability of interconnects to withstand thermally induced mechanical stresses. Samples will be cycled from -40°C to 150°C for 2,000 cycles, with ramp rates of 10°C/minute and dwell/soak times of 10 minutes.
- Two humidity-based tests will evaluate the corrosion resistance of the ribbons and their bond pads. Under a humidity bias test, ribbon interconnects will be placed in an 85°C, 85% relative humidity environment for 1,000 hours. A DC bias will be applied during the test. Under a second humidity test, samples will be subjected to a 121°C, 100% relative humidity environment for 96 hours with no electrical bias. This is considered a destructive test.
- Under combined power and thermal cycling, interconnects will be subjected to a periodically applied operating bias while they experience high and low temperature extremes. Samples will be cycled from -40°C to 125°C for 1,500 cycles, with ramp rates of 5°C/minute and dwell/soak times of 10 minutes.
- Random six-degree-of-freedom vibration and rapid thermal cycling will stress the ribbon bonds beyond

their design specifications to quickly highlight predominant failure mechanisms.

Physics of Failure Models

Under temperature cyclic loads, the CTE mismatch between the ribbon material and the silicon die or metalized substrate results in stress/strain reversals in the heel of the ribbon interconnect, gradually leading to its failure. PoF models identify the root cause of this failure and then provide lifetime estimation based on material properties, geometry, and environmental conditions [9]. Using the theory of curved beams, the strain prediction on the upper side of the ribbon bond can be approximated using the equation,

$$\epsilon = \frac{r(\rho_f - \rho_i)}{\rho_i \rho_f} = r(k_i - k_f) \tag{1}$$

where

- ϵ is strain induced,
- r is half the thickness of the ribbon,
- ρ_f is the radius of curvature of the ribbon heel after heating,
- ρ_i is radius of curvature of the ribbon heel before heating,
- k_f is curvature at the heel of the ribbon after heating,
- k_i is curvature at the heel of the ribbon before heating.

From the above equation, it can be seen that the strain induced in the lower side ($[\rho_i/\rho_f]+2r$) will be lower compared to the strain in the upper side of the ribbon. Once the strain is calculated, the number of cycles to failure, N_f , can be determined using the Coffin-Manson equation

$$N_f = C_r \varepsilon^{-m_r} \quad (2)$$

where C_r and m_r are fatigue properties found through material tensile tests.

As the loop geometry plays a significant role in the prediction of strain values, the ribbon should be in a state of minimum potential energy. An energy-based cubic spline model is used to determine the geometry of the loop that achieves a minimum potential energy [9]. For a given span, the loop height is varied to find the least energy state, by

$$d = \frac{Dh}{H} \left[1 - \sqrt{1 - \frac{H}{h}} \right] \quad (3)$$

where

d is half the span,

h is loop height,

D is total span of the ribbon,

H is the height offset.

This calculation was used to determine the least energy state for a ribbon interconnect to have a ratio of 1:2.2 loop height to span length.

A FEA model was developed to find the stress and strain values induced in an Al ribbon bond with a 10-mm span. The model geometry of a sample ribbon interconnect was created in SolidWorks and imported into ANSYS Workbench. A cross-section image of the sample ribbon was experimentally measured using a microscope to create a spline fit profile that could be imported into the FEA model. The plasticity model was specified as a multi-linear kinematic hardening model to properly define the plastic behavior of the Al material, with stress-strain values at room temperature obtained from corresponding curves from literature [10]. A test case was run with a temperature cycle profile from 20°C to 160°C at a ramp rate of 5°C/min. A maximum deflection of 33.8 μm was observed at the center of the profile at the highest region. Maximum von Mises stress values of 193.87 MPa and 183.07 MPa were found to be at the heel for the first and second bond pads, respectively. The maximum deflection result from the model will be compared against experimentally obtained deflection results to validate the FEA model.

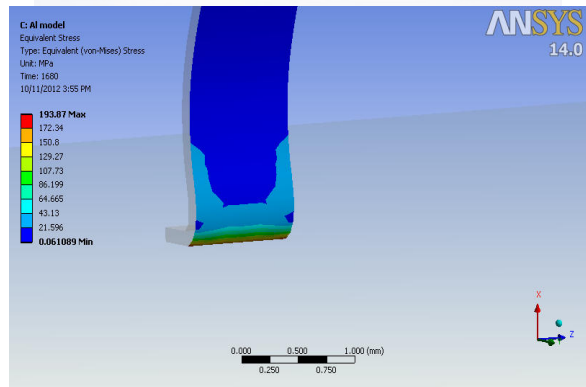
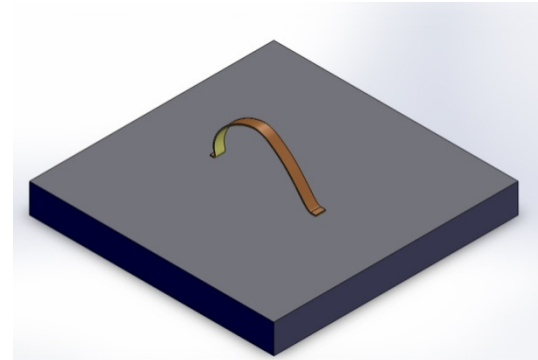


Figure V - 32: FEA model of 1,000 μm x 100 μm Al ribbon with 10-mm span (top) and maximum stress shown at heel location near second bond pad (bottom).

Future modeling results will be improved by including temperature-dependent material properties for Cu and Al, and will be expanded to include Cu/Al-clad ribbon geometries. Deflection, von Mises stress, and strain results will be compared to the failure modes observed in the experimental accelerated tests. Analytical and FEA results will be incorporated into the Coffin-Manson relation to predict the number of cycles to failure, and validated with experimental test results for cycles to failure.

Conclusion

The work accomplished in FY2012 establishes the foundation for a comprehensive evaluation of the reliability of ribbon bond interconnects. A variety of materials and geometries will be tested under various accelerated testing conditions to highlight failure mechanisms. Combining experimental results with lifetime-to-failure models will enable reliability predictions for ribbon interconnects.

Acknowledgments

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V.3 Thermal Performance and Reliability of Bonded Interfaces

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Objectives

In automotive power electronics packages, conventional thermal interface materials (TIMs) pose a bottleneck to heat removal. Due to advantages from heat transfer and packaging standpoints, there is an industry trend towards high-thermal-performance bonded interfaces. However, due to coefficient of thermal expansion (CTE) mismatches between materials/layers and the resultant thermomechanical stresses, these interfaces are susceptible to fatigue, resulting in defects that pose a problem from a reliability standpoint. These defects, such as cracks, voids, or delaminations, manifest themselves in increased thermal resistance in the package, which again is a bottleneck to heat removal. Hence, the overall objective of this project is to investigate and improve the thermal performance and reliability of emerging bonded interface materials (BIMs) for power electronics packaging applications. Specifically, the objectives for FY2012 were as follows:

- In conjunction with partners, synthesize large-area bonded interfaces between metalized substrates and copper (Cu) base plates for BIMs based on lead-based solder, thermoplastics with embedded carbon fibers, and sintered silver materials.
- Subject BIMs to accelerated thermal cycling conditions and monitor their reliability using nondestructive techniques.
- Continue finite element modeling of strain energy density in the lead-based solder BIM with the intent of establishing experimental cycles-to-failure versus strain energy density correlation.

Approach

- Establish various bonded interfaces between 50.8 mm x 50.8 mm cross-sectional area substrate and copper base plate samples. These interfaces are based on lead-based solder (as a baseline), sintered silver (based on micrometer-sized particles), and thermoplastics with embedded carbon fibers.
- Perform thermal shock and thermal cycling on these samples (going from -40°C to 150°C) according to the Joint Electron Devices Engineering Council (JEDEC) standards for up to 2,000 cycles as an upper limit. Monitor their reliability through acoustic microscopy and high-potential (hipot) tests on these samples after a select number of thermal cycles.
- Perform mechanical tests on the select bonded interface samples to obtain information on stress versus strain relationship for the bonded material. In conjunction with modeling, this will ultimately help in establishing strain energy density versus cycles-to-failure correlations for the different bonded interfaces.
- Change synthesis parameters to obtain improved thermal performance and reliability for the emerging/novel bonded interfaces under investigation.

Major Accomplishments

- Bonded interfaces were established between 50.8 mm x 50.8 mm cross-sectional area metalized substrate and copper base plate samples for lead-based solder, thermoplastics with embedded carbon fibers, and sintered silver materials.
- Samples were subjected to accelerated thermal cycling between temperatures of -40°C and 150°C, and the degradation of the bonded interface was imaged every 100 cycles using a C-mode scanning acoustic microscope (C-SAM). Results were obtained for lead-based solder samples up to 500 cycles, and thermoplastics with embedded carbon fibers and sintered silver samples up to 1,500 cycles.
- Finite element analysis (FEA) modeling of the lead-based solder BIM was used to establish the relationship between strain energy density and the corner radius of the BIM.

Future Direction

The following activities are envisioned for this project for FY2013:

- Complete 2,000 accelerated thermal cycles for lead-based solder, thermoplastics with embedded carbon fibers, and sintered silver materials and report on their reliability.
- Expand reliability testing of sintered silver BIMs by evaluating commercially available materials under accelerated thermal cycling conditions.
- In conjunction with partners, focus on development of a sintered silver that can achieve reliable bonds with lower pressure and temperature synthesis conditions.
- Establish the shear strength and stress-strain constitutive relations for the three BIMs.
- Establish the relationship between calculated strain energy density and experimental cycles-to-failure for the lead-based solder BIM.



Technical Discussion

Introduction

In a power electronics module, a semiconductor chip/die is typically attached by a BIM such as solder to a metalized substrate. The substrate is composed of a ceramic bounded by copper layers on either side and provides electrical isolation. This substrate is then mounted on to a base plate or directly to a heat exchanger, typically made of copper or aluminum, via another BIM. A cross-section of a typical power electronics package is shown in Figure V - 33.

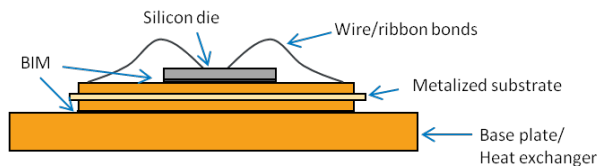


Figure V - 33: Traditional power electronics package.

A CTE mismatch between the ceramic substrate and the copper base plate can cause crack initiation and propagation in the joining solder layer. Lead-based solders have predominantly been used in the electronics packaging industry; however, the Restriction of Hazardous Substances Directive (RoHS) [1] necessitates the need for lead-free solutions. Initially, the industry focused on various SAC (tin, silver, and copper) compositions as a suitable lead-free alternative, with Innolot (SnAg3.8Cu0.7Bi3.0Sb1.4Ni0.2) proving to be a promising solution [2-4]. Research found that varying the composition of silver and copper content in the solders would help minimize creep strain. Overall, reliability under temperature cycling continues to be a concern with lead-free solders. To provide greater thermomechanical reliability under temperature cycling and to allow for

higher temperature applications, sintered silver material has also emerged as a promising bonding solution in power electronics packages [5, 6]. However, to reduce processing/synthesis temperatures to below 300°C, up to 40 MPa of pressure must be applied to the package, causing a higher complexity in the production process and more stringent flatness specifications of the substrates. Hence, alternative bonding techniques are being developed to increase the thermomechanical reliability of this joint through the use of newer materials, such as thermoplastics with embedded micrometer-sized carbon fibers. Little information is available on the thermal performance and reliability of large-area attaches based on the more recently developed thermoplastic materials.

Prior work at NREL [2, 7] focused on establishing a consistent and high-accuracy database, via the ASTM steady-state approach [8], on the thermal performance of conventional as well as emerging TIMs. The conventional materials included greases, gels, phase-change materials, and filler pads. It was concluded that the tested conventional materials could not meet the thermal performance specification of 5-mm²K/W thermal resistance for a 100-μm bond line thickness. For a number of power electronics packaging stack-ups, the TIM stops being a bottleneck to heat removal when its resistance is on the order of 5 mm²K/W, which is the reason why it is a target. In addition, practical power electronics packaging configurations and manufacturing constraints dictate that the TIM has to fill gaps on the order of 100 μm.

Due to the promise of BIMs [9-13], work at NREL has been focused on assessing their thermal performance and reliability. Conclusions on thermal performance and reliability from this effort are intended to directly assist the incorporation of these materials into automotive power electronic designs. This report focuses on thermoplastic (polyamide) adhesive with embedded near-vertical aligned carbon fibers (8- to 10-μm diameter), sintered silver based on micrometer-sized silver particles, and lead-based solder as a baseline. The sample synthesis, characterization plan, and results are described below.

Materials and Sample Synthesis

The assembly consists of a 5-mm-thick copper base plate attached to a 0.72-mm-thick active metal bonding substrate [0.32-mm-thick silicon nitride (Si₃N₄) with 0.2-mm-thick Cu foil on either side of Si₃N₄, 50.8 mm x 50.8 mm cross-sectional area footprint] via the bonding material. Before assembly, the Cu metallization layers in the substrate were finished with 4 μm of electroless nickel-phosphorus (NiP), 1 μm of palladium (Pd), and 0.3 μm of silver (Ag) to improve adhesion with the bonding material. The Cu base plate was electroplated with 5 μm of Ag. An assembled sample is shown in Figure V - 34.



Figure V - 34: Representative metalized substrate/base plate assembly (Photo credit: Doug DeVoto, NREL).

A tabletop hot press was developed for synthesizing test samples requiring both temperature and pressure bonding parameters. Two hot plates were positioned on either side of the sample to be bonded and were embedded with five 250-W cartridge heaters. Three heaters were inserted in the top hot plate and two in the bottom hot plate. A temperature controller adjusted the power of the heaters based upon the temperature measurement by a thermocouple located in the bottom hot plate. The test sample and hot plates were placed between layers of mica and cold plates, and then inserted into an arbor press [14]. Glycol-water (50%–50% mixture by volume) coolant was circulated within the cold plates to isolate the high bonding temperatures from the hydraulic piston and fluid. A screw

jack was also placed between the hydraulic piston and top cold plate to provide fine adjustment to the applied bonding pressure. The pressure of the hydraulic fluid was electronically monitored to determine the force applied to the sample under bonding.

The HM-2 material, manufactured by Btech Corporation, is a composite structure consisting of 8- to 10- μm -diameter carbon fibers embedded in a polyamide/thermoplastic adhesive. The HM-2 was placed between the substrate/base plate assembly and subjected to a pressure of 689.5 kPa and a temperature of 190°C. Once the temperature was reached, the assembly was allowed to cool down to room temperature while maintaining the pressure.

Bonded interfaces based on sintered silver particles were synthesized by Semikron. Corners of the Si_3N_4 substrate were rounded off to match the 2 mm radius of the copper layers. The sample assembly was placed in a hot press and raised to its processing temperature, after which pressure was applied.

As a baseline, a lead-based (Sn63Pb37) bond was also synthesized between the substrate/base plate assembly. A 127- μm -thick stainless steel stencil with 9-mm x 9-mm square openings and 1-mm separation was used to evenly apply solder to the substrate and base plate surfaces. After the solder was applied, the assembled sample was placed in a vacuum solder reflow oven. The reflow profile, shown in Figure V - 35, ensured that flux was removed from the bond and that voiding remained under 2%.

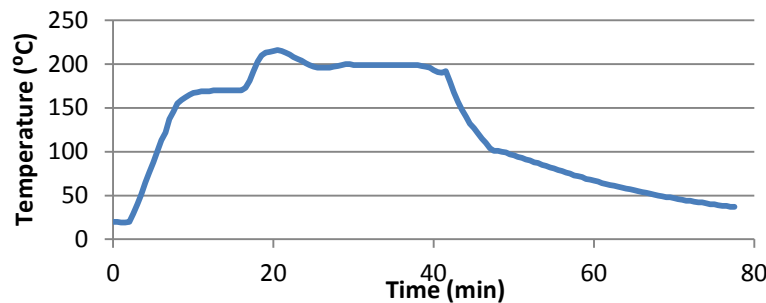


Figure V - 35: Reflow profile for lead-based solder.

Initial Bonded Interface Material Characterization

Degradation (e.g., cracks, voids, and delaminations) of the bonded interface can be non-destructively detected by acoustic microscopy. After defect initiation, the thermal and electrical performance of the sample assembly degrades. A C-mode acoustic microscope (C-SAM) emits ultrasound waves with frequencies ranging from 5 MHz to 400 MHz into a sample suspended in water. The strength of the signal reflected back to the microscope's transducer from an interface within a sample depends on the relationship between the acoustic impedances of the two

materials forming the interface. A crack, void, or delamination will create a solid-to-air interface, the presence of which will cause a strong reflection to be detected by the microscope's transducer. Samples were measured for their initial bonding condition and then subsequently tested every 100 thermal cycles. Images showing the bonded interface within samples before accelerated thermal testing are shown in Figure V - 36. Circular bandings visible in each sample are artifacts of the C-SAM representing top surface curvatures as 2-D images and are not indicators of bond quality. The lead-based solder, Btech HM-2, and sintered silver all exhibited

uniform bonds between the base plate and substrate samples.

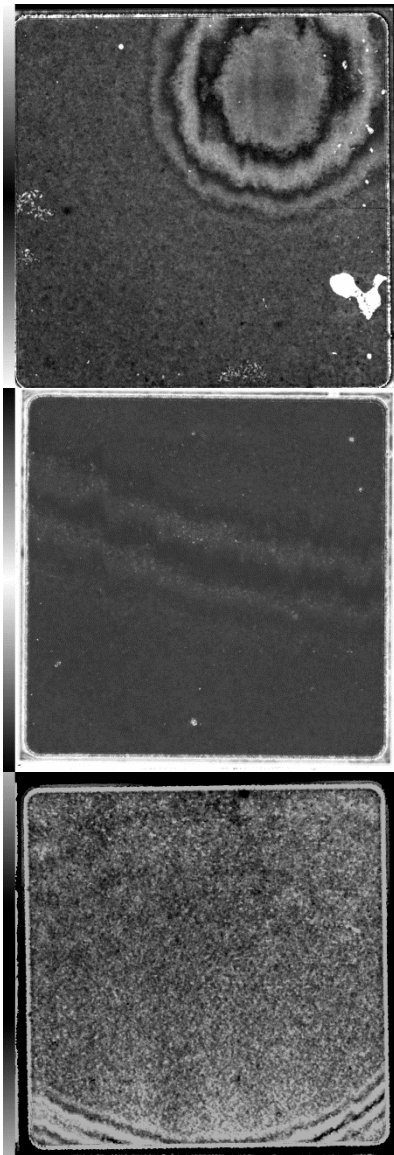


Figure V - 36: C-SAM images showing initial bond quality in lead-based solder (top), Btech HM-2 (middle), and sintered silver (bottom) (Photo credit: Doug DeVoto, NREL).

In addition to acoustic microscopy, the electrical resistance of the Si_3N_4 insulation layer was also measured. In a hipot test, a high voltage is applied to an electronic device's current-carrying components. The quality of the insulation in the device is determined by measuring the presence of a leakage current. Leakage current indicates that dielectric breakdown in the insulation layer has occurred [15]. A dielectric resistance tester was previously constructed based on the hipot testing process to detect when a crack in the Si_3N_4 has developed. A custom fixture contacts the top and bottom sides of a test sample and applies a test voltage of 2.0 kV for 20 seconds, which is sufficient voltage to cause an arc in the air through a defect/crack in the 0.32-mm-thick Si_3N_4 layer. Measurement of the leakage current from an arc indicates that damage has occurred within the Si_3N_4 layer in the sample. The sample successfully passed the test if no current was measured over the analysis period. The results correlated with acoustic microscopy images, indicating that all initial samples exhibited no defects within the Si_3N_4 layer.

CTE mismatches within the samples cause package deformation and stresses to build up in the Si_3N_4 layer during the cool down from the synthesis temperature to room temperature. These stresses can be sufficient to cause crack initiation and propagation within the Si_3N_4 , leading to failure of the layer's electrical insulating properties. Representative CTE parameters for materials common within a power electronics package and examples of package deformation conditions are shown in Figure V - 37. As a package cools from a stress-free temperature, the copper base plate's higher CTE relative to the substrate and silicon die causes it to contract more and induce a bow into the package. Heating will conversely cause the base plate to expand more quickly than the rest of the package and create a bow in the opposite direction.

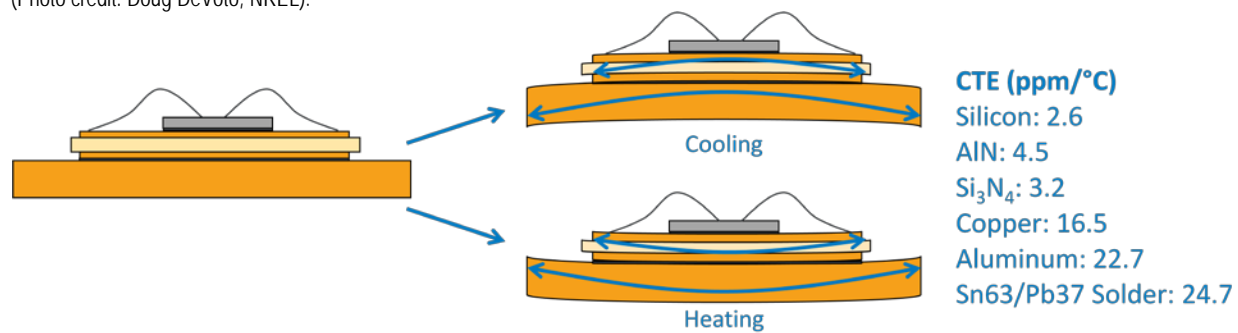


Figure V - 37: Power electronics package deformation due to CTE mismatch under cooling and heating conditions.

The high pressure and temperature synthesis requirements for sintered silver did not cause crack initiation within the Si_3N_4 substrate; however, package deformation was evident when samples were at room temperature. A laser profilometer was used to scan the top and bottom surfaces of silver sintered samples for accurate measurements of these deformations. Figure V - 38 shows

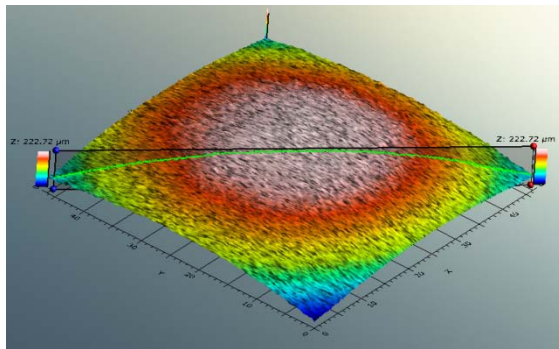
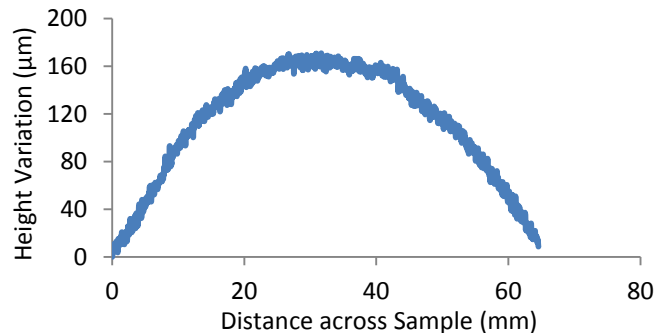


Figure V - 38: Surface profile of sintered silver sample at room temperature.

the top surface profile of one sintered silver sample as well as a cross-section profile between two of the sample's corners. The height variation across the sample was measured to be 166 μm . Surface profile measurements were also taken for lead-based solder and thermoplastic samples, but no significant package deformations were found.



Bonded Interface Material Condition after Thermal Cycling

After initial characterization of the test samples, conditions must be applied to create thermally induced stresses, leading to cracking, voiding, or delamination

failures. Generally, there are three types of thermal duty cycles that can be used to create thermally induced stresses: a temperature cycle, a thermal shock cycle, and a power cycle. A temperature cycle specifies the temperatures to which a sample under test will be exposed, the durations of exposure, and the rate of change of temperature when the sample under test is brought to a new temperature set point. A thermal shock cycle is similar to a temperature cycle, but consists of rapid changes in the ambient temperature. Finally, a power cycle is created by heat dissipation in an actual electronic device to create realistic heat flow patterns and temperature distributions in a sample under test. Because the lifetimes of samples are too long to be tested in real time, an accelerated temperature cycling test procedure is employed to bring testing times down to a reasonable duration.

Samples were cycled between -40°C and 150°C , a common temperature range for electronics testing, to evaluate the quality of the bonded interfaces [16-19]. A soak, or dwell, time of 10 minutes at the maximum and minimum temperatures was chosen to highlight lead-based solder fatigue and creep [16]. Ramp rates for thermal cycling must be sufficiently low to avoid transient thermal gradients in the test samples; therefore, ramp rates were in the $5^\circ\text{C}/\text{min}$ range. Each sample will be cycled up to 2,000

thermal cycles, or until degradation propagates to sufficient levels to consider the sample failed. A failure is defined as a crack in the Si_3N_4 substrate, a cohesive fracture within the BIM, or an adhesive/interfacial fracture between the BIM and either the substrate or base plate surface. A crack in the Si_3N_4 substrate would indicate loss of electrical insulation capabilities and the sample would immediately be considered failed. Cohesive or adhesive/interfacial fractures in the BIM would increase the thermal resistance of the power electronics package, eventually creating a thermal bottleneck that would elevate the operating temperature of a die above its maximum limit. For testing purposes, fractures leading to 15% area delamination of the BIM will be defined as a failure.

Thermoplastic HM-2 samples have undergone 1,500 temperature cycles and have shown no initiation of defects in the Si_3N_4 substrate or the BIM. Figure V - 39 shows C-SAM images highlighting the corner regions of the Btech HM-2 interfaces before cycling, after 700 temperature cycles, and after 1,500 temperature cycles.

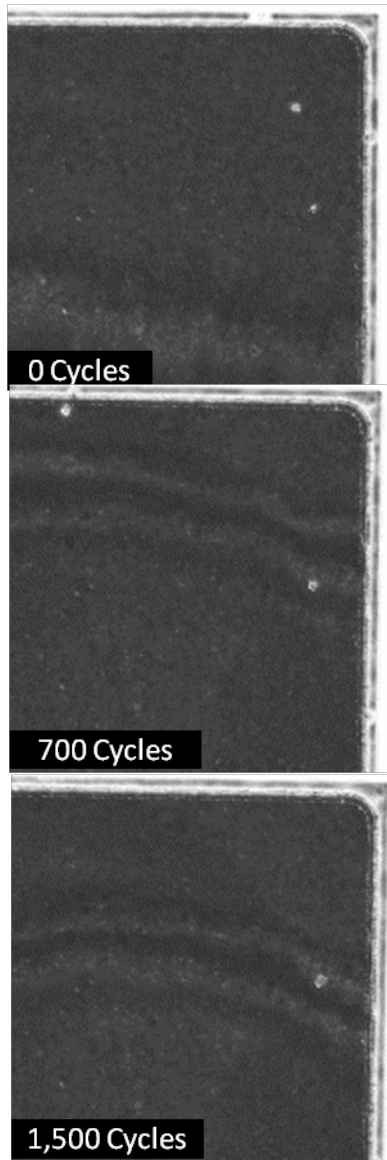


Figure V - 39: C-SAM images of Btech HM-2 thermoplastic material before and during thermal cycling (Photo credit: Doug DeVoto, NREL).

Sintered silver samples have also undergone 1,500 temperature cycles but have shown progressively increasing delamination of the BIM going from 0 cycles (pre cycling), after 700 temperature cycles, and after 1,500 temperature cycles, as shown in Figure V - 40.

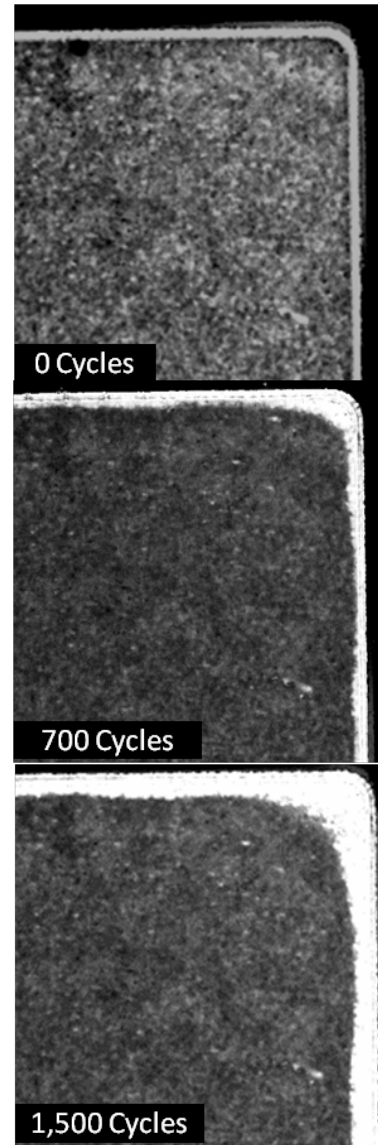


Figure V - 40: C-SAM images of sintered silver material before and during thermal cycling (Photo credit: Doug DeVoto, NREL).

Measurements of the delamination percentage within the sintered silver BIM were taken every 100 cycles from C-SAM imagery. Depending on the sample, this perimeter delamination increased to 6%–13% of initial bonded area after undergoing 1,500 cycles, as shown in Figure V - 41.

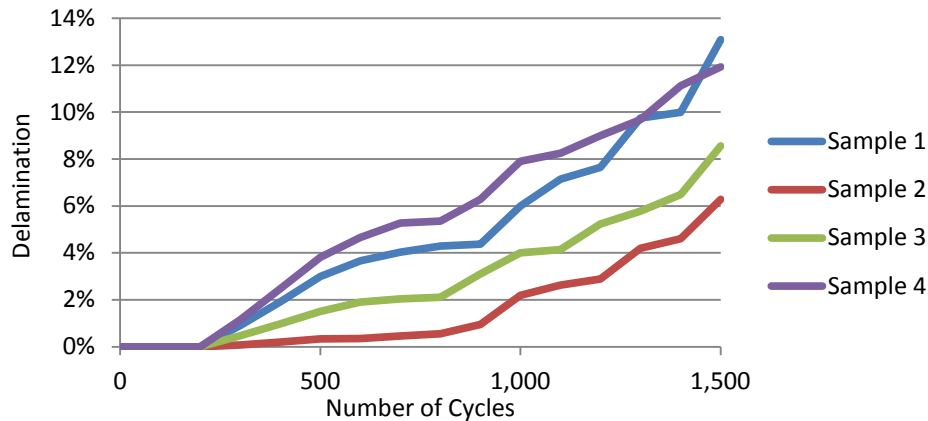


Figure V - 41: Perimeter delamination of sintered silver BIM as a function of number of thermal cycles.

Accelerated thermal testing will continue for all samples to 2,000 cycles, or until failure of the Si_3N_4 substrate or BIM.

Modeling of Strain Energy Density in Lead-Based Solder

The BIM reliability modeling approach involves first calculating the accumulated viscoplastic strain energy density per cycle using FEA modeling. Results are then implemented into a fatigue model to obtain a correlation with experimentally determined number of thermal cycles to BIM failure. ANSYS Mechanical was selected for the FEA because of its established accuracy by other researchers in this field [20-24].

An ANSYS Parametric Design Language (APDL) code was developed that includes model pre-processing, solver, and post-processing stages. The model geometry matches the experimental test sample geometry and consists of a 50.8-mm x 50.8-mm cross-sectional area composed of a copper base plate, lead-based solder (63Sn-37Pb) BIM, and a Si_3N_4 substrate. A quarter symmetry of the package was utilized in the modeling to save computational space and time, shown in Figure V - 42.

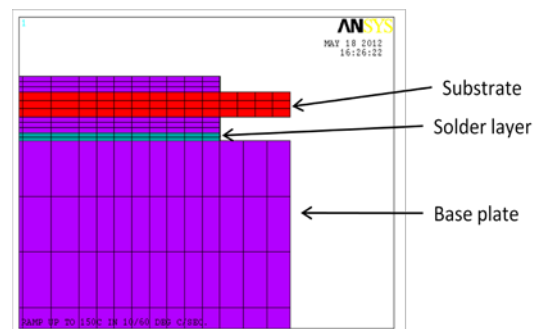
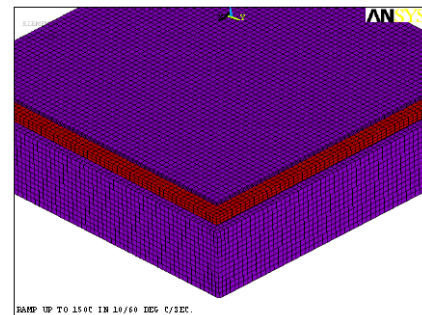


Figure V - 42: Quarter symmetry model (top) and layers in the bonded assembly (bottom).

After the geometry was constructed, material properties were assigned to the various layers within the package. The Anand constitutive model was used to define the viscoplastic nature of the solder joint while temperature dependent, elastic properties were applied to the base plate and substrate [25-26]. Nine parameters in the Anand model were obtained from published literature. Various mesh controls, including element sizing, edge sizing, and meshing technique were then used to create a structured mesh that increases in density at the joint layer. Furthermore, these controls ensured that no mesh mismatch occurred between the different layers in the model. The model was then subjected to a temperature cyclic load with maximum and minimum temperatures of

150°C and -40°C, respectively, and a ramp rate of 5°C/min and dwell time of 10 minutes. Four such cycles were simulated to study the plastic behavior of the solder joint. Results indicated that the maximum strain energy distribution occurred at the solder's corner region, at the interfacial joint with the copper base plate.

The package design was modified to create a fillet at the corner region to reduce the maximum strain energy distribution. The fillet was created both for the solder layer and for the copper metallization layers in the substrate. The geometry construction and the meshing sections of the APDL code were significantly modified to incorporate the fillet at the corner region. Separate control over the mesh in the fillet region was achieved in the modified code. This was important for minimizing computational time and mesh size, as mesh density could then be increased in the solder fillet region independently of the solder inner region. Model variations with a fillet radius of 1.5 mm and 2 mm were analyzed as the application of a fillet onto a substrate's metalized layers is a common technique to increase the reliability of the solder layer in the corner region.

Figure V - 43 shows the temperature profile and development of shear strain within the solder joint's corner region as a function of time. Calculations of strain levels within the solder joint are critical to develop relationships with fatigue failures within the interface material. As the temperature ramps up from room temperature to 150°C, strain within the solder develops and reaches a maximum value at the end of the elevated dwell period. During the subsequent ramp down, strain decreases and minimizes at the end of the low dwell period. A cyclic pattern is also seen for shear stress, where the stress level first increases with temperature during the ramping up period. Stress relaxation is then observed during the last portion of ramping up and continues to relax through the elevated dwell period. Negative shear stress levels develop during ramp down and reach a minimum at the low dwell, where some stress relaxation is then observed. This model confirms that for lead-based solder, creep effects accelerate at elevated temperatures.

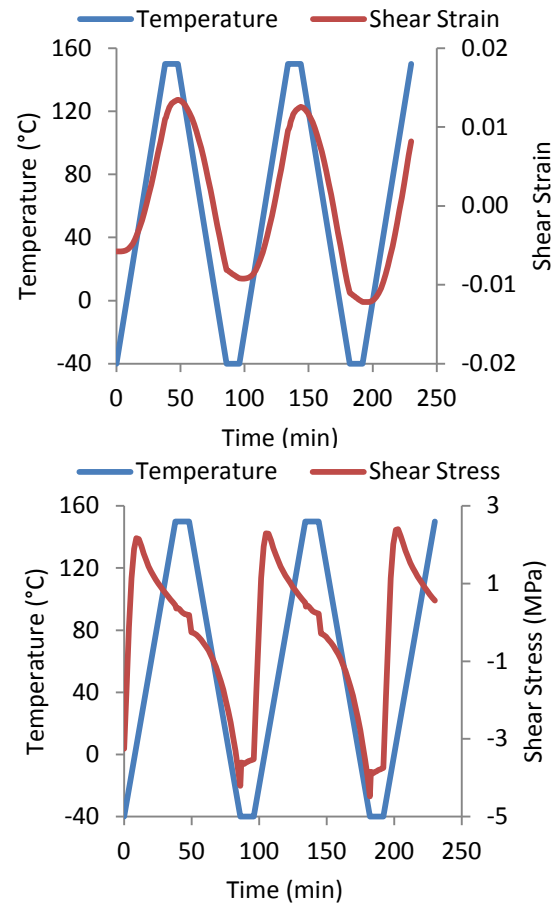


Figure V - 43: Temperature and shear strain versus time (top) and temperature and shear stress versus time (bottom).

Analysis of stress-strain hysteresis loops helps to understand the inelastic behavior exhibited by the joint and combines the effect of stress and strain into a single parameter: the strain energy density. On completion of a simulation, the node with the maximum equivalent strain was selected and its stress and strain values were obtained through time history post-processing. The inelastic behavior of the solder joint under varying thermomechanical loads during a temperature cycle is illustrated in Figure V - 44. The temperature cycle is segmented into four different cases, high dwell at 150°C, ramp down to -40°C, low dwell at -40°C, and then ramp up back to 150°C. Beginning at the 150°C high dwell, shear stress slightly decreases as shear strain increases, with creep strain playing a predominant role. The ramp down segment causes both stress and strain values to decrease until the low dwell at -40°C, at which point stress levels increase slightly while strain values continue to decrease. As the temperature increases during ramp up to 150°C, stress levels increase until approximately room temperature, at which point stress decreases and strain values begin to increase due to temperature-dependent creep effects.

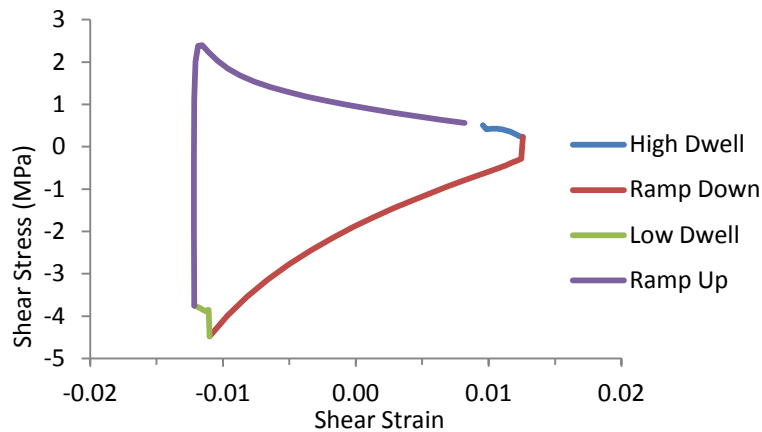


Figure V - 44: Hysteresis loop from a solder joint's 2-mm fillet region.

Figure V - 45 shows a comparison of stress-strain values between solder joints with 1.5-mm and 2-mm fillet corners. Separate simulations were run to obtain the results. It can be seen that under the same temperature loading conditions, an equivalent amount of stress was induced but the maximum strain values were reduced in the 2-mm fillet geometry. Energy stored in the solder joint region due to deformation during the temperature loading conditions is referred to as the strain energy. The strain

energy density is the strain energy per unit volume and is determined by calculating the area within the stress-strain hysteresis loop for a given temperature cycle. The strain energy density values calculated over the fillet regions for 1.5-mm and 2-mm fillet corners were 11.3 MPa and 11.2 MPa, respectively. These strain energy density values will be correlated with experimentally determined number of thermal cycles to lead-based solder BIM failure.

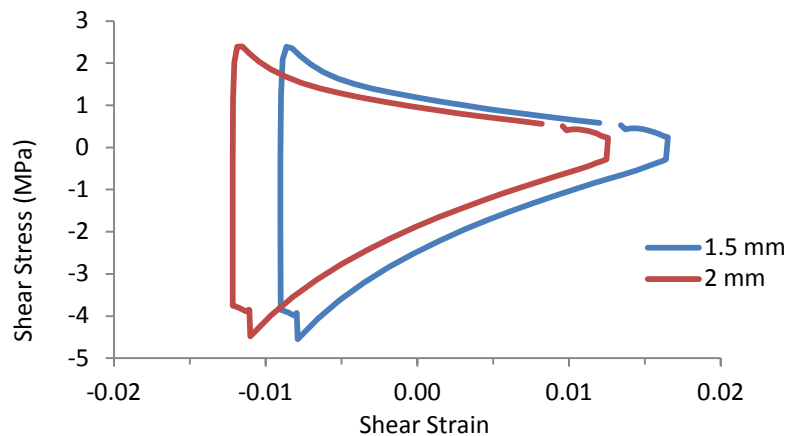


Figure V - 45: Stress-strain hysteresis loop comparison.

Conclusion

A consistent framework has been implemented to establish the thermal performance and reliability of large-area bonded joints based on novel/emerging materials such as thermoplastics with embedded carbon fibers and sintered silver materials as compared to lead-based solder. These large-area attachments are currently being considered in state-of-the-art power electronics packages

for hybrid and electric vehicle applications. Initial results for bond quality suggest that thermoplastics with embedded fibers could be a promising alternative to lead-based solders. Future work with sintered silver material will focus on minimizing the occurrence of adhesive fracturing by optimizing processing conditions.

Modeling of strain energy density for the lead-based solder BIM bonded between the metalized substrate and copper base plate was performed using the Anand model

parameters for the solder BIM from the literature. The results will be leveraged in the efforts to generate experimental cycles-to-failure versus strain energy density (obtained from modeling) curves for different BIMs of interest.

Publications

1. Narumanchi, S., DeVoto, D., Mihalic, M., Popp, T., and McCluskey, P. (2011). "Thermal performance and reliability of large-area bonded interfaces in power electronics packages," IMECE2011-65399, *Proceedings of the 2011 ASME Mechanical Engineering Congress & Exposition*, November 2011, Denver, CO.

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V.4 Light-Weight, Single-Phase, Liquid-Cooled Heat Exchanger

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Objectives

The goal of the project is to design, fabricate, and experimentally demonstrate a light-weight, low-cost, high-thermal-performance, single-phase, water-ethylene glycol (WEG) liquid-cooled heat exchanger. This demonstration is being done within the framework of a commercial (UQM Technologies Inc.) inverter. The bulk of the heat exchanger is made of plastic material because the cooling is provided by the jets impinging directly on the back side of the power module base plates. Micro-structured surfaces fabricated on the copper base plates will be employed as a simple, passive means of enhancing heat transfer. This cooling approach of impinging jets on the base plate is compared to the baseline channel flow cooling approach typical of automotive heat exchangers.

The objectives for FY2012 were:

- Fabricate prototype jet-based plastic heat exchangers and experimentally characterize thermal performance.
- Characterize reliability of jet impingement on microfinned surfaces.

Approach

- Using computational fluid dynamics (CFD) modeling, design a heat exchanger based on impinging jets of WEG in conjunction with microfinned surfaces and a fluid-manifold made of automotive-grade glass-fiber-reinforced nylon plastic. Through modeling, demonstrate improvements in thermal performance for the new heat exchangers as compared to the baseline channel-flow-based heat exchanger.

- Fabricate the prototype and show it is amenable to mass manufacturing techniques (e.g., casting, injection molding).
- Characterize the thermal performance of the new heat exchangers (one based on impingement on a plain surface and another based on impingement on a microfinned surface) using the transient thermal tester, which helps simulate steady-state heating of the insulated-gate-bipolar transistors and diodes. Compare and demonstrate improvements in performance for the new heat exchangers with respect to the baseline and also compare experimental data to results previously obtained through modeling.
- Characterize thermal performance of the heat exchangers using a dynamometer to simulate a real-world thermal load profile. Compare thermal performance of the new heat exchangers with the baseline.
- Comprehensively characterize the reliability of long-term WEG jet impingement on microfinned surfaces, as well as impingement on direct-bond-copper (DBC) and direct-bond-aluminum (DBA) with nickel and gold coatings.

For this project, NREL established collaborations with UQM Technologies Inc. and Wolverine Tube Inc.

Major Accomplishments

- A new light-weight heat exchanger was designed for the UQM inverter. The heat exchanger was made from inexpensive and light-weight plastic materials (i.e., glass fiber-reinforced nylon) and was fabricated using a selective-laser-sintering rapid prototyping technique. The heat exchanger utilizes a jet impingement cooling approach and eliminates the use of thermal interface materials to improve thermal performance. Experiments demonstrated that the new design can reduce the thermal resistance by 10% and increase the specific power by 33% as compared to the baseline, channel-flow-based heat exchanger.
- Experiments were conducted to evaluate the long-term reliability of the Wolverine MicroCool microfinned surface. The MicroCool microfinned surface, when exposed to near-continuous impingement by a 7-m/s WEG jet for 1 year, was found to have a 30% reduction in thermal performance at the end of the year. Oxidation and a white film deposited on the enhanced surfaces are believed to be the cause of the performance degradation. Modifications will be made to the

reliability experiments going forward to address issues related to oxidation/corrosion.

Future Direction

- Comprehensive CFD analyses will be performed to further optimize and improve heat transfer and reduce pressure drop and design the second version of the light-weight heat exchanger. Additionally, the use of the MicroCool enhanced surfaces will be incorporated into the new design to further improve thermal performance. The new, improved designs will be fabricated and tests will be conducted to characterize their performance.
- Additional experiments are planned to evaluate the long-term reliability of enhanced surfaces and ceramic substrates (direct-bond copper and direct-bond aluminum) subjected to WEG jets. Unlike the prior tests, these experiments will utilize automotive grade coolant (i.e., WEG with corrosion inhibitors) at coolant temperatures used in automotive power electronics applications (70°C). To minimize/eliminate oxidation and corrosion, the enhanced surfaces will be nickel plated. The effect of the impinging jets on the thermal performance of the enhanced surface and the integrity of the ceramic substrate will be evaluated over a one-year period.



Technical Discussion

Light-Weight Heat Exchanger Design and Experimental Results

A prototype heat exchanger utilizing a jet-impingement cooling approach and a light-weight plastic material was designed using CFD modeling and fabricated using a selective-laser-sintering rapid prototyping process. The heat exchanger, shown in Figure V - 46, was designed to cool a commercially available UQM inverter. The new heat exchanger design implements a light-weight manifold that incorporates liquid jets directly impinging on the power module base plates. An image of the jet nozzles is provided in Figure V - 47. This cooling approach eliminates the use of thermal interface material between the base plate and the heat sink/cold plate, and therefore is expected to improve thermal performance. Further details on the CFD modeling and design are given in [1].

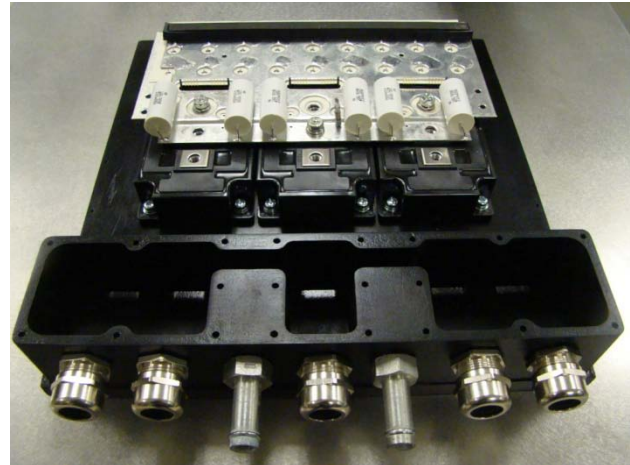


Figure V - 46: Light-weight, inverter-scale plastic heat exchanger (Photo credit: Mark Mihalic, NREL).

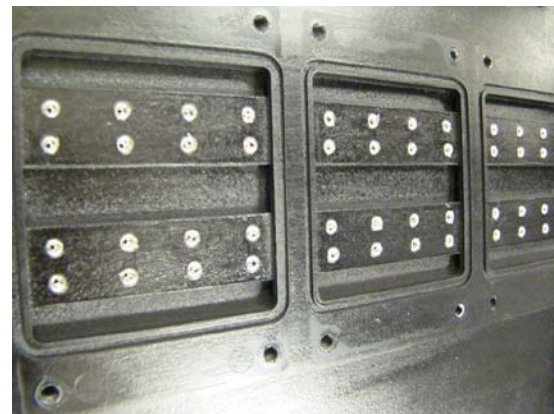


Figure V - 47: Picture of the heat exchanger jet nozzles (Photo credit: Doug DeVoto, NREL).

Experiments were conducted to characterize the performance of the new heat exchanger as well as the baseline channel-flow-based aluminum heat exchanger. The tests were carried out using WEG (50%–50% mixture by volume) as the coolant at a temperature of 70°C. For these experiments, the diodes on one power module were powered and their temperature was measured using a transient thermal tester. Based on the information of diode junction temperature as well as the total power dissipated in the diodes, the total thermal resistance was computed. At an industry-standard flow rate of 10 liters per minute ($1.67 \times 10^{-4} \text{ m}^3/\text{s}$), the new jet-impingement-based heat exchanger yielded junction-to-fluid thermal resistance that was 10% lower as compared to the baseline channel-flow-based heat exchanger (see Table V - 3). These enhancements were achieved without the use of surface enhancement techniques that should further improve performance (i.e., reduce the thermal resistance). Additionally, the light-weight construction of the new heat exchanger reduced the weight of the heat exchanger by 47%. This reduction in weight and thermal resistance

translates to a 33% increase in specific power (kW/kg) with respect to the baseline inverter heat exchanger configuration. The use of plastics as a heat exchanger material may also provide additional cost savings associated with inexpensive materials and cost-effective manufacturing techniques.

Table V - 3: Experimental results with the first heat exchanger prototype.

Parameter	Baseline (channel flow)	Jets impinging on plain surface
$R_{th,ja}$ (K/W)	0.142	0.128
Heat Exchanger Mass (kg)	5.7	3.0
Total Inverter Mass (kg)	16.0	13.3

Future work will focus on improving the design of the heat exchanger to obtain further enhancements in heat transfer as predicted by the CFD modeling. In addition, the performance of jets impinging on Wolverine's MicroCool enhanced surfaces will also be characterized experimentally.

Long-term Reliability of Micro-Structured Surfaces

Experiments were conducted to evaluate the long-term reliability of Wolverine's MicroCool enhanced surfaces (Figure V - 48). This enhanced surface has demonstrated significant heat transfer enhancement [2] and thus will be utilized in future heat exchanger designs. However, its long-term reliability under impinging jet configurations is unknown and requires investigation.

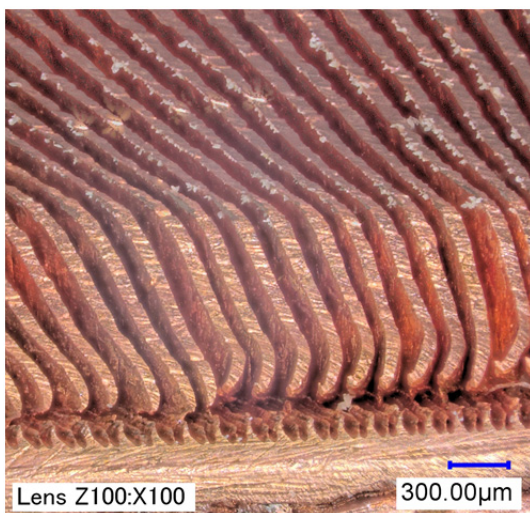


Figure V - 48: Wolverine Tube MicroCool finned surface technology significantly increases jet-impingement heat transfer (Photo credit: Gilbert Moreno, NREL).

Reliability of the MicroCool surface was evaluated by subjecting test samples to an impinging WEG jet (50%/50% mixture by volume) for one year. The samples were blocks machined out of copper. Wolverine Tube, Inc. fabricated the MicroCool micro-finned surface on the top surfaces of the copper blocks. In the experiments, WEG jets at 35°C temperature were impinging normal to the target surfaces. The impact of near-continuous WEG jet impingement on the MicroCool surface thermal performance was evaluated. Two MicroCool samples were tested, sample W1 and sample W2. The mean jet velocities for sample W1 and sample W2 were 7 m/s and 2 m/s, respectively. Images of both samples initially and after one year of jet impingement are shown in Figure V - 49. As seen in the figure, both samples oxidized and a thin white film was found to be deposited on the sample's finned surfaces.

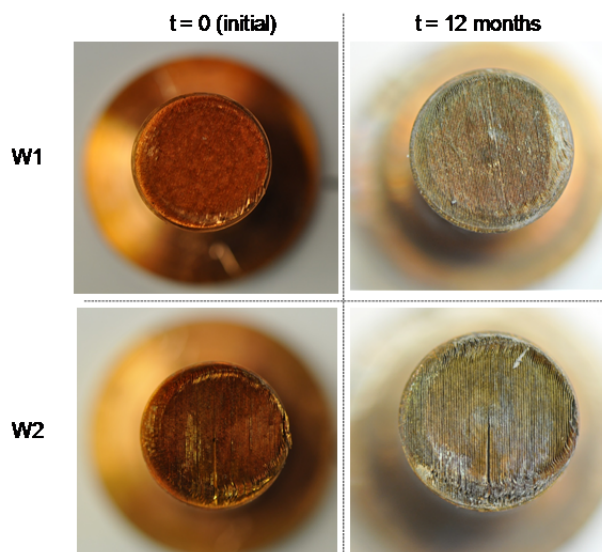


Figure V - 49: Images of the two MicroCool samples before and after one year of near-continuous jet impingement (Photo credit: Gilbert Moreno, NREL).

At various stages during the long-term jet impingement reliability experiments, the samples were temporarily removed from the experiments and tests were conducted to measure the thermal performance of the MicroCool samples. Submerged-jet impingement heat transfer experiments with pure water were conducted to measure the thermal performance (i.e., heat transfer coefficients) of the two sample surfaces. Heat transfer coefficient results at jet velocities of 2 m/s and 12 m/s are shown in Figure V - 50. The results were obtained initially and at the 1-, 2-, 3-, 6-, and 12-month time periods. The error bars provided at each data point represent the 95% confidence intervals (CI) calculated as

$$CI = \pm \frac{t s}{\sqrt{n}}$$

where t is the Student t-distribution, s is the sample standard deviation, and n is the number of tests performed (typically 3 to 5 tests). As shown in the figure, after 12 months of near-continuous jet impingement, both samples showed some degradation in performance. However, only sample W1, which was subjected to a higher jet velocity, demonstrated statistically significant degradation, considering its CI at 12 months did not overlap the CIs for prior months. For sample 1, the heat transfer coefficient at 12 m/s was almost 30% lower than the initial heat transfer coefficient value. Interestingly, degradation for this sample was only about 13% for the 2-m/s heat transfer test. The measured decreases in performance may be due to both oxidation and the white film deposited on the MicroCool finned surfaces (Figure V - 48), which may have restricted flow within the finned structures, especially at elevated velocities (i.e., 12 m/s case).

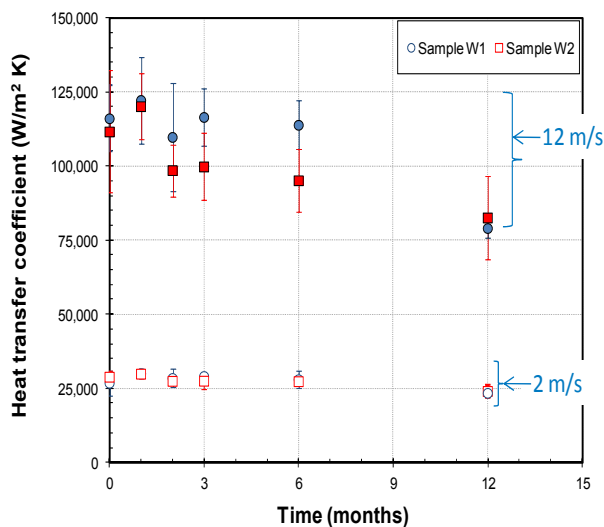


Figure V - 50: Heat transfer coefficient versus time for both samples W1 and W2.

Since oxidation may have played a role in the observed performance degradation, future jet impingement reliability experiments are planned using automotive-grade coolant/antifreeze (i.e., WEG coolant with corrosion inhibitors) and nickel-plated MicroCool surfaces. These experiments will be carried out at 70°C fluid temperatures, which is a representative automotive power electronics coolant temperature. These modifications to the reliability tests would better simulate actual automotive conditions and may eliminate the observed performance degradation.

Nozzle wear/erosion was also evaluated during these year-long experiments. The nozzles used in these experiments were simple orifice-plate nozzles fabricated from 6061 aluminum. Nozzle wear was quantified by measuring the inner diameter (i.e., inlet of the nozzle plate) of the nozzle orifices using a microscope. As was the case with the MicroCool samples, nozzle-wear measurements were taken at various times during the year-long

experiments. Figure V - 51 shows the measured nozzle diameters at various times during the experiment. The velocities through each nozzle were 2 m/s and 7 m/s for Nozzle 2 and Nozzle 1, respectively. The data show minimal change in the nozzle orifice diameters for both nozzles, indicating negligible nozzle wear.

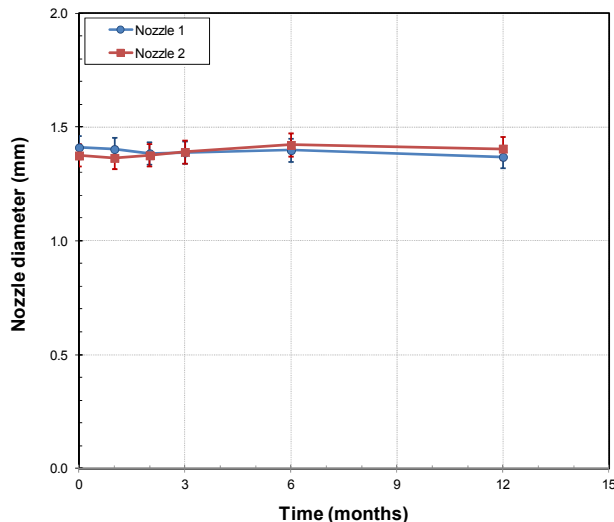


Figure V - 51: Jet nozzle orifice diameter versus time for nozzles 1 and 2.

Conclusions

- A new light-weight heat exchanger designed to cool a commercially available inverter was fabricated. Experiments demonstrate that the new heat exchanger can reduce the thermal resistance by 10% and improve specific power by 33% as compared with the baseline, channel-flow-based heat exchanger design. Additionally, the fabrication of the new heat exchanger out of light-weight plastic may also provide additional cost savings associated with inexpensive materials and cost-effective manufacturing techniques.
- Experiments were conducted to evaluate the reliability of the Wolverine MicroCool enhanced surfaces when subjected to near-continuous impinging WEG jets for one year. Results showed some decrease in performance. The MicroCool sample subjected to a 7-m/s continuously impinging jet was found to provide heat transfer coefficients as much as 30% lower than the initial heat transfer coefficients. Oxidation and a white film residue deposited on the surfaces could potentially have restricted fluid flow on to the finned surfaces and thus degraded performance.

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Publications

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2. Narumanchi, S., Mihalic, M., Moreno, G., and Bennion, K., 2012, "Design of light-weight, single-phase, liquid-cooled, jet-based heat exchanger for an automotive inverter," Proceedings of the 2012 ITherm conference, San Diego, CA, May 2012.

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V.5 Two-Phase Cooling Technology for Power Electronics

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Objectives

The overall project goal is to enable the DOE's Advanced Power Electronics and Electric Motors (APEEM)-specific power, power density, and cost targets to be achieved through the use of two-phase cooling technology. The high heat transfer rates and near isothermal characteristics of two-phase heat transfer can enable greater power densities, which would allow for less silicon (e.g., insulated gate bipolar transistors) and thus, reduce power electronics system size and cost. This project will focus on efficient, passive (i.e., no pumps or compressors) two-phase cooling strategies. Thus, in addition to potential reductions to power electronics cost and size, there is also potential to increase system efficiency.

Approach

This project conducts both fundamental and system-level research to evaluate two-phase (boiling/evaporation) heat transfer as a potential power electronics cooling approach. The fundamental study is focused on characterizing the pool boiling performance of novel coolants/refrigerants as well as investigating promising boiling enhancement techniques. Fundamental research results then feed into the design of the system-level components. The system-level study is focused on developing a prototype passive two-phase cooling system capable of dissipating automotive power electronic heat loads. Work is currently underway to design and fabricate a passive, two-phase cooling system for Delphi's discrete power modules. The intent is to demonstrate superior thermal performance, increased efficiency, and reduce cost

with the two-phase cooling system(s) developed. Air-cooled, passive (pump-less) two-phase systems will be considered due to their inherent efficiency and lower cost.

For this project, NREL has collaborated with companies including Delphi, 3M, DuPont, General Electric and universities including University of Colorado at Boulder, Iowa State University, and University of Illinois at Chicago.

Major Accomplishments

- The team characterized the two-phase (i.e., pool boiling) performance of R-245fa up to the critical heat flux (CHF) condition. We conducted experiments to evaluate the effects of a boiling enhancement coating and system temperature on performance. The boiling enhancement microporous coating was found to significantly enhance heat transfer coefficients and CHF by as much as 400% and 50%, respectively. Compared to HFO-1234yf, R-245fa produced lower heat transfer rates with a plain surface, but provided higher heat transfer rates with the microporous coated surface. R-245fa and HFO-1234yf each offer advantages as refrigerants in a two-phase cooling system. Future experiments with two-phase power electronic cooling systems will be carried out with both refrigerants.
- We fabricated and tested a low-pressure passive, two-phase cooling system (i.e., condenser and evaporator). Experiments combined with finite element modeling indicate that an indirect, passive two-phase cooling scheme can decrease the junction to liquid thermal resistance by 43% and increase power density by 75% as compared to conventional automotive cooling schemes. Moreover, experiments indicated that it may only require a small quantify of refrigerant (≤250 mL) to dissipate automotive power electronic heat loads (3.5 kW).
- We designed passive, two-phase cooling systems to cool Delphi's discrete power modules. These two-phase cooling systems consist of an evaporator and air-cooled condenser and can operate at higher pressures to allow for testing with R-245fa and HFO-1234yf. We used experimental research and finite element simulations to aid in the design of the systems. Extensive testing is planned with these systems to demonstrate the advantages of two-phase based power electronics cooling systems.

Future Direction

- Demonstrate a passive, two-phase cooling solution for Delphi’s advanced discrete power modules/switches. Three two-phase systems have been designed and will be tested. We will compare the performance, size, weight, and efficiency of these systems to that of a representative conventional, automotive single-phase cooling system. The performance of the two-phase cooling systems will be characterized using both HFO-1234yf and R-245fa. The following is a more detailed description on the experiments planned.
 - Measure the total thermal resistance (junction to air) and maximum power dissipated by the two-phase cooling system(s).
 - Investigate the effects of orientation on system performance.
 - Characterize the performance of the two-phase cooling system under transient heat loads by imposing a drive cycle power electronics heating profile.
- Report on the long-term reliability of boiling enhancement coatings subjected to power cycling boiling operation.

Table V - 4 and Table V - 5, respectively.

Table V - 4: R-245fa Saturated Properties.

T (°C)	P (MPa) ¹	P _r (P/P _c)	ρ _l (kg/m ³) ¹	ρ _v (kg/m ³) ¹	h _{lv} (kJ/kg) ¹	σ (mN/m) ¹	μ (mPa·s) ¹	C _p (J/kg·K) ¹
20	0.124	0.03	1,352	7.2	193.8	14.69	0.432	1,328
30	0.179	0.05	1,325	10.2	187.9	13.41	0.381	1,350
40	0.252	0.07	1,297	14.1	181.7	12.13	0.337	1,373
50	0.345	0.09	1,268	19.1	175.3	10.86	0.299	1,399
60	0.464	0.13	1,237	25.5	168.4	9.59	0.266	1,428
T _c (°C)	154.1 ¹						P _c (MPa)	3.64 ¹

¹ National Institute of Standards and Technology [2]

Table V - 5: HFO-1234yf Saturated Properties.

T (°C)	P (MPa) ¹	P _r (P/P _c)	ρ _l (kg/m ³) ¹	ρ _v (kg/m ³) ¹	h _{lv} (kJ/kg) ¹	σ (mN/m) ²	μ (mPa·s) ³	C _p (J/kg·K) ⁴
20	0.590	0.17	1,112	33.0	148.7	6.77	0.167	1,470
30	0.782	0.23	1,075	44.1	140.3	5.56	0.149	1,512
40	1.018	0.30	1,035	58.4	131.0	4.42	0.133	1,565
50	1.302	0.39	991	76.9	120.5	3.35	0.120	1,637
60	1.642	0.49	941	101.2	108.5	2.37	0.108	1,736
T _c (°C)	94.7 ^{1,2}						P _c (MPa)	3.375 ¹

¹ Leck [3]

² Tanaka and Higashi [4]

³ Brown et al. [5]

⁴ Tanaka [6]

A schematic of the experimental apparatus used for these tests is shown in Figure V - 52. The high-pressure system has a maximum operating pressure of 2 MPa and

◇ ◇ ◇ ◇ ◇

Technical Discussion

Two-Phase Performance of R-245fa on Plain and Enhanced Surfaces

We have conducted experiments to characterize the two-phase (i.e., pool boiling) performance of R-245fa on plain and microporous-enhanced surfaces. This data is important because it is not available in the open literature and because it allows us to compare the performance of R-245fa to that of HFO-1234yf. R-245fa is a fairly new refrigerant that operates at lower pressures (as compared with HFO-1234yf and R134a), is non-flammable, has excellent thermal properties (high latent heat and critical temperature), and has been identified as a viable refrigerant for two-phase cooling of power electronics [1]. The pool boiling performance of HFO-1234yf was characterized last year at NREL. Both R-245fa and HFO-1234yf are being considered as refrigerants for use in automotive power electronic two-phase cooling systems; therefore it is important to characterize and compare the performance of the two candidate refrigerants. Relevant saturated properties for R-245fa and HFO-1234yf are provided in

was fabricated from materials compatible with a variety of refrigerants. The system was designed for both pool and forced convection boiling experiments. System

components include a test section, flat-plate heat exchangers, gear pump, mass flow meter, vacuum pump (not shown), and a pneumatic compressor (not shown). Pool boiling experiments were conducted within the test section using horizontally-oriented heat sources. A schematic of the heated test article is provided in Figure V - 52. The test article consisted of a $10 \times 10 \times 3$ mm oxygen-free copper block, a 50-ohm film resistor, and a polytetrafluoroethylene (PTFE) substrate. Test article temperature measurements were taken using a calibrated K-type thermocouple that was embedded 1.5 mm below the heated surface in the copper block. Test article wall temperatures (T_{wall}) were then calculated assuming one-dimensional, steady-state heat transfer through the copper

block. Pool boiling experiments were controlled and monitored using a program created in LabVIEW. The program controlled a data acquisition system and power supply to generate heat-flux-controlled boiling curves.

R-245fa pool boiling experiments were conducted at 25°C , 40°C , 50°C , and 60°C saturation temperatures (T_{sat}) to measure heat transfer coefficients and CHF. This temperature range is intended to encompass potential operating temperatures for an automotive two-phase power electronics cooling system. Plain/smooth surface heat transfer coefficients and CHF values for R-245fa and HFO-1234yf are provided in Figure V - 53.

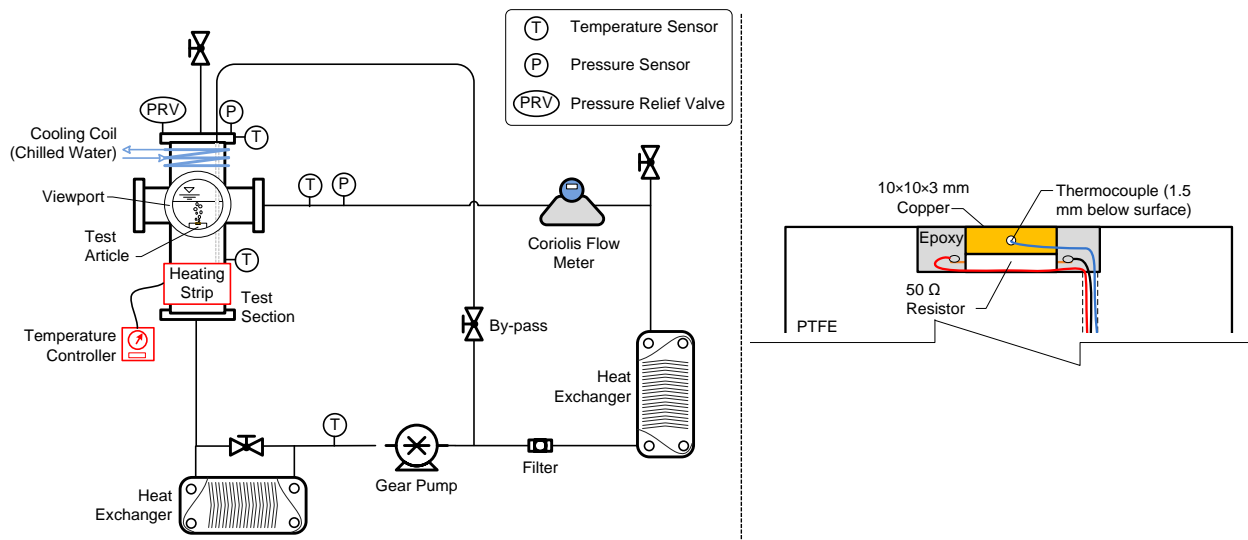


Figure V - 52: High-pressure apparatus/flow loop (left) and test article (right) schematics.

The heat transfer coefficients of R-245fa and HFO-1234yf obtained at $T_{sat} = 60^\circ\text{C}$ are plotted in Figure V - 53a. With the plain surface, R-245fa was found to provide lower heat transfer coefficients as compared to HFO-1234yf. A reason for R-245fa's lower heat transfer is that it operates at a lower reduced pressure ($P_r = P_{system} / P_{critical}$) as compared with HFO-1234yf at the same saturation temperature (see Table V - 4 and Table V - 5). It is well known that operating at higher pressures (i.e., reduced pressure) will provide higher heat transfer [7, 8]. This may explain why HFO-1234yf produced higher heat

transfer. Therefore, comparing the two refrigerants on an equivalent reduced pressure basis may provide different results. However, in real applications, ambient temperatures and imposed heat will determine the operating system temperatures. The system temperatures will then dictate operating pressures. For this reason, the comparisons for this study were made on the basis of an equivalent system (i.e., saturation) temperature.

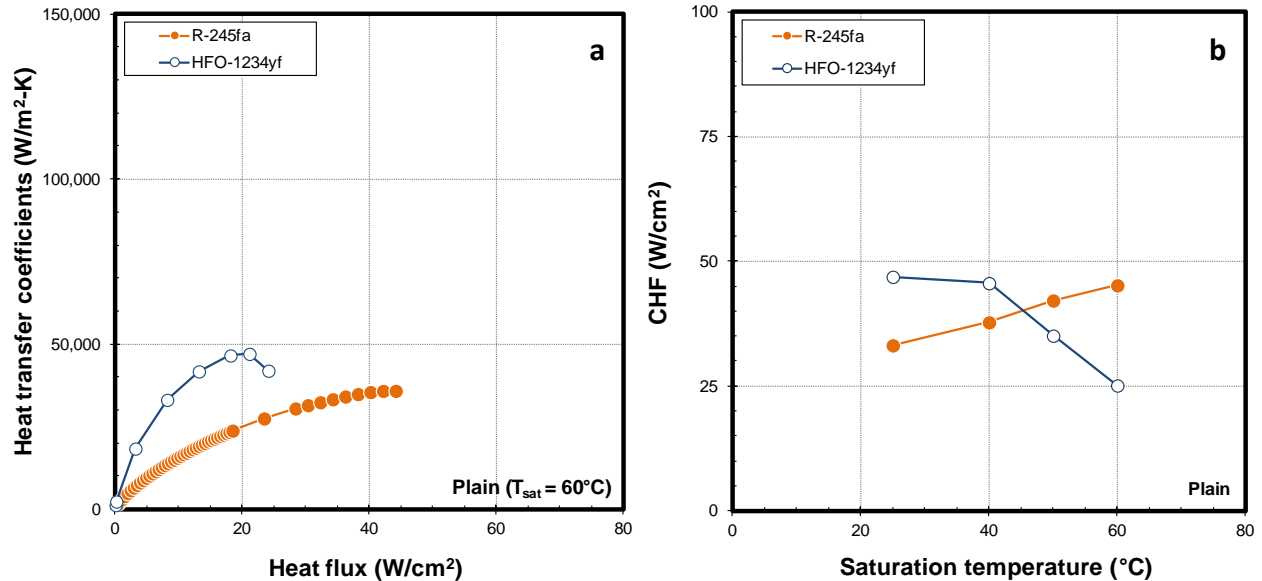


Figure V - 53: R-245fa and HFO-1234yf two-phase heat transfer coefficients (a) and CHF (b) for a plain surface.

Plain surface CHF values for R-245fa and HFO-1234yf at 25°C—60°C saturation temperatures are provided in Figure V - 53b. As shown in the figure, R-245fa CHF increases from 34 W/cm² at T_{sat} = 25°C to 46 W/cm² at T_{sat} = 60°C. Compared to HFO-1234yf, R-245fa provides lower CHF (27% lower at T_{sat} = 25°C) at lower saturation temperatures, but provides higher CHF (84% greater at T_{sat} = 60°C) at higher saturation temperatures. Thus, within this temperature range, the R-245fa CHF increases while the HFO-1234yf CHF decreases. The observed CHF versus saturation temperature trend can be explained in terms of the reduced pressure. Studies [9, 10] have demonstrated that CHF will increase with increasing pressure, achieving a maximum at about $P_r = \frac{1}{3}$ after which it decreases. As pressure increases, vapor buoyancy ($\rho_l - \rho_v$), latent heat, and surface tension will decrease. The combination of these effects dictates the CHF versus pressure behavior [11]. At the higher temperature range tested (T_{sat} ≥ 50°C), HFO-1234yf's $P_r > \frac{1}{3}$ and thus its CHF is in a declining trend. Conversely, within the temperature range tested, R-245's $P_r < \frac{1}{3}$ and thus its CHF should continue to increase with increasing saturation temperature achieving a maximum near T_{sat} ≈ 98°C (i.e., $P_r = \frac{1}{3}$).

We also conducted experiments to study the effect of 3M's microporous coating on R-245fa pool boiling performance. The microporous coating was developed by 3M and is a passive means of enhancing boiling heat transfer. A scanning electron microscope (SEM) image of 3M's microporous coating is provided in Figure V - 54.

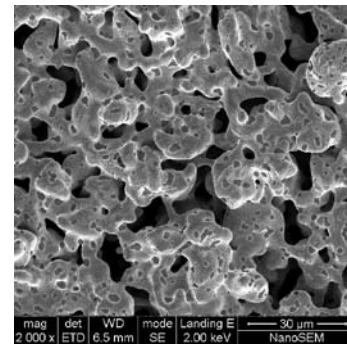


Figure V - 54: SEM image of the 3M microporous coating.

R-245fa pool boiling experiments, with the microporous coating, were conducted at T_{sat} = 40°C, 50°C, and 60°C. The ratios (microporous over plain) of the heat transfer coefficients and CHF values at various saturation temperatures are shown in Figure V - 55a and Figure V - 55b, respectively. The coating is found to increase heat transfer coefficients by as much as 400% and achieve values as high as 130,000 W/m²-K. Additionally, the coating is found to increase CHF by as much as 50% and provide values as high as 68 W/cm². The passive fluid transport, provided via capillary wicking within the porous coating, combined with increased nucleation site density and increased surface area are the mechanisms believed responsible for the enhancements. The increased heat transfer dissipation provided by the coating would allow for increased device power densities and smaller cooling systems. These results show that R-245fa provides good thermal performance and thus should be considered for two-phase cooling of automotive power electronic systems.

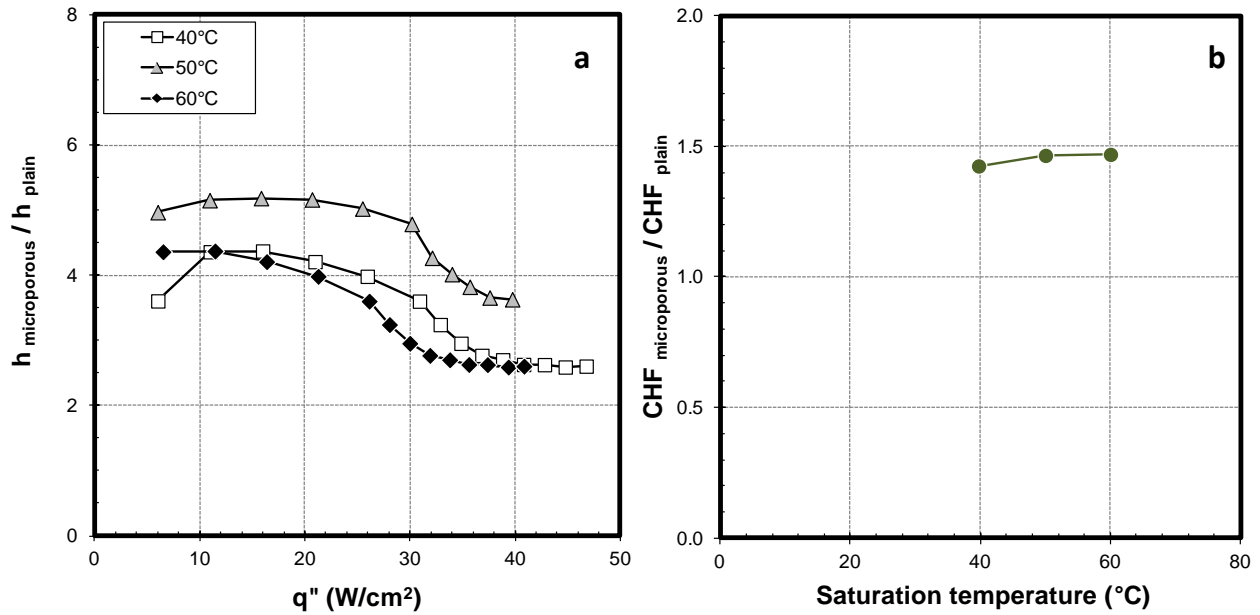


Figure V - 55: Ratio (microporous over plain) of the heat transfer coefficients (a) and CHF (b).

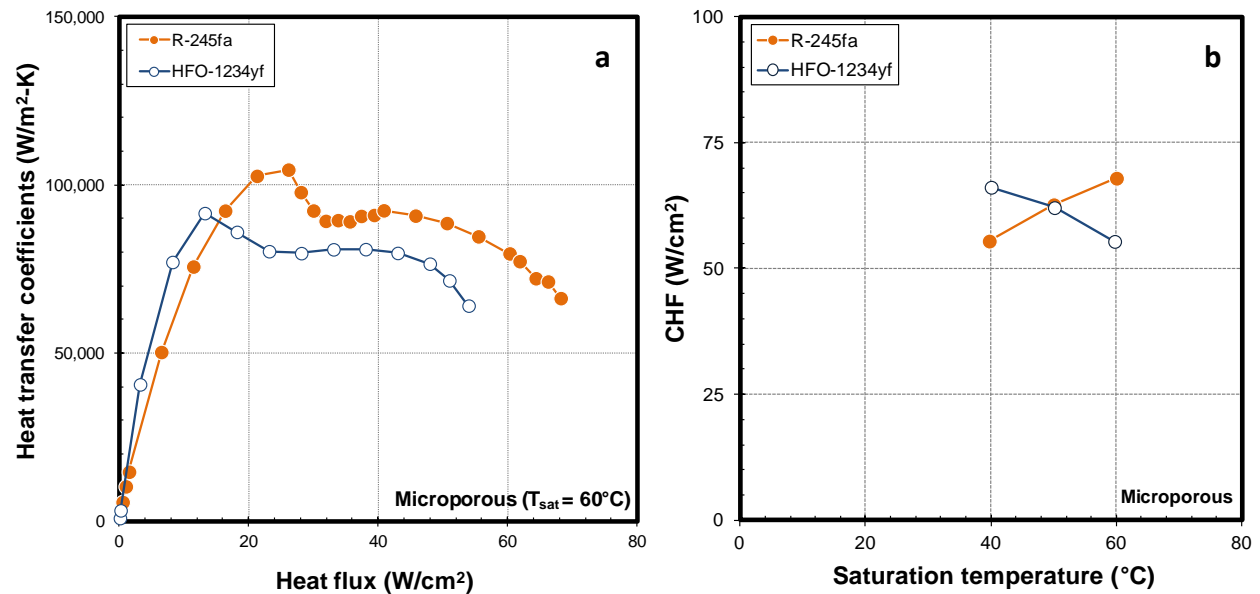


Figure V - 56: R-245fa and HFO-1234yf two-phase heat transfer coefficients (a) and CHF (b) for a microporous-coated surface.

The R-245fa and HFO-1234yf heat transfer coefficients for a microporous coated surface at $T_{\text{sat}} = 60^\circ\text{C}$ are plotted in Figure V - 56a. With the microporous coating, R-245fa can provide heat transfer coefficients greater than those provided with HFO-1234yf. This is the case at higher heat fluxes ($> 20 \text{ W/cm}^2$) and is also the case at the other saturation temperatures tested. This finding is contrary to the plain surface results in which R-245fa always provided lower heat transfer coefficients. CHF versus temperature trends (Figure V - 56b) for the two

refrigerants on microporous coated surfaces are nearly identical to the CHF versus temperature trends on plain surfaces. As in the case with the plain surface, with a microporous coated surface R-245fa CHF increases with increasing temperature, while HFO-1234yf CHF decreases with increasing temperature. These trends can be attributed to the respective P_r range that each refrigerant operates within. Compared to HFO-1234yf, the CHF for R-245fa is found to be 16% lower at $T_{\text{sat}} = 40^\circ\text{C}$ and 23% higher at $T_{\text{sat}} = 60^\circ\text{C}$.

Long-term Reliability of Boiling Enhancement Coatings

The micrometer features of boiling enhancement coatings have raised concerns regarding their long-term performance. To address this issue, we have designed an experimental system consisting of a pressure vessel, data acquisition system, and computer to test the long-term reliability of the coatings. A picture of the system test vessel with samples is provided in Figure V - 57. The system will stress multiple coated samples by subjecting them to two-phase (boiling) operation for an extended period of time (1 year). The coated samples will be power cycled (up to 50% CHF). Simultaneously, the system will measure the thermal enhancement properties of the coating and in this manner record the performance of the samples over time.

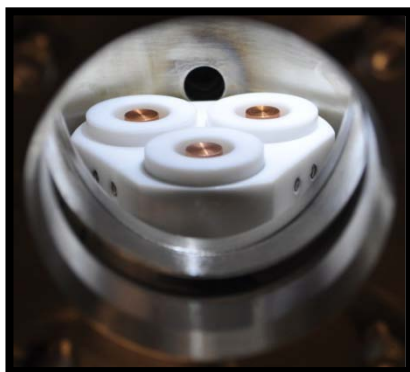


Figure V - 57: Picture of the reliability vessel with test samples.

Implications for Two-Phase Cooling of Power Electronics

This section discusses work conducted to characterize, understand, and improve performance of passive, two-phase cooling systems (thermosyphon) to evaluate their potential use for power electronics cooling. Two-phase systems consist of an evaporator and a condenser and do not require a pump or compressor to circulate refrigerant. Due to reliability concerns associated with direct two-phase cooling (i.e., electronics submerged in dielectric refrigerants), this project will focus on an indirect two-phase cooling approach.

We fabricated a passive, two-phase (thermosyphon) cooling system using an indirect cooling scheme and carried out tests to characterize and improve performance as well as to establish refrigerant quantity requirements (e.g., volume of refrigerant per kW of heat dissipated). The system consists of an evaporator and a condenser. A schematic of the system is provided in Figure V - 58.

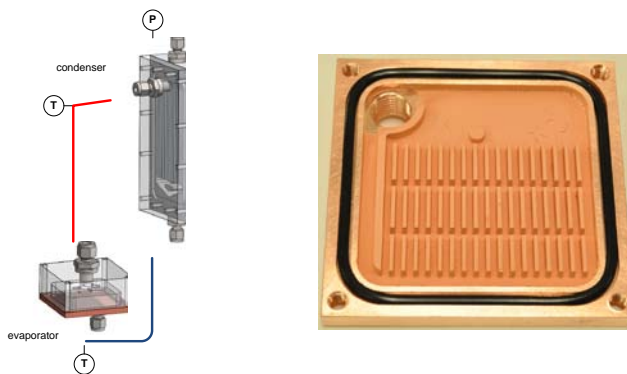


Figure V - 58: Schematic of the passive two-phase cooling system (left) and evaporator cold plate (right).

We conducted experiments with evaporator modules of various designs. A picture of a finned evaporator with boiling enhancement coating is shown in Figure V - 58. The evaporator is essentially a two-phase-based cold-plate. Tests were conducted to measure the thermal resistance of the various evaporator modules to evaluate the effects of finned surfaces and boiling enhancement coatings. The boiling enhancement coating used was the 3M microporous coating shown in Figure V - 54. The thermal resistance of the evaporator includes the resistance of boiling heat transfer at the liquid-solid interface within the evaporator and conduction-spreading through the evaporator copper cold plate (Figure V - 59). Saturated HFE-7100 was the refrigerant used for these experiments. HFE-7100 was used here because it operates at lower pressure, and thus, allows for visualization of the fluid-vapor through the use of lower strength transparent thermosyphon components (e.g., polycarbonate). Visualization aided in understanding fluid-vapor flow patterns and improving performance. Although HFE-7100 was used for these experiments, the conclusions reached should also apply for R-245fa and HFO-1234yf. Results and knowledge gained from this study will be used in designing future two-phase based cooling system.

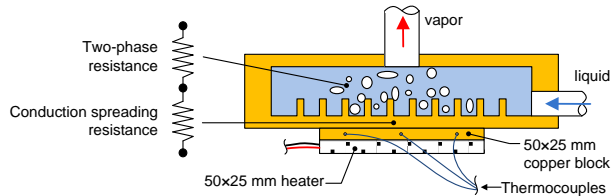


Figure V - 59: Schematic of the evaporator.

The performance of the thermosyphon evaporator is plotted in Figure V - 60. This figure plots the unit thermal resistance (R''_{th}) as a function of the heat dissipated for the plain/smooth and microporous-coated evaporator. The unit thermal resistance is the thermal resistance of the evaporator multiplied by the area that is cooled (i.e., 50×25 mm). As shown in Figure V - 60, the use of the microporous coating decreases the evaporator thermal

resistance by over 50%, as compared to the plain evaporator and provides unit thermal resistance values as low as about $30 \text{ mm}^2\text{-K/W}$. A small increase in the thermal resistance is observed at high power levels ($\geq 700 \text{ W}$) for the microporous coated evaporator. This increase is believed to be associated with localized dry-out occurring within the evaporator at elevated power levels.

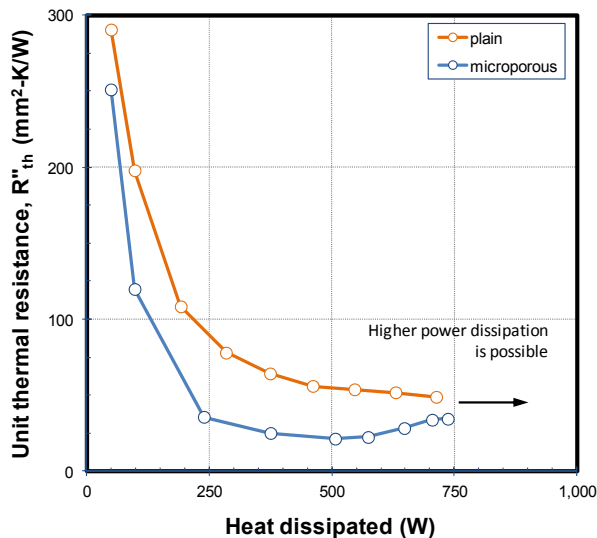


Figure V - 60: Thermal resistance of the plain and microporous-coated evaporator in the thermosyphon configuration.

We then imposed these experimentally obtained thermal resistance values as boundary conditions in three-dimensional finite element simulations of a power module to estimate the benefits of this cooling approach compared to conventional automotive cooling schemes. The results from this analysis indicate that employing an indirect, passive two-phase cooling strategy can reduce the total thermal resistance of the power module (junction to liquid) by approximately 43%, as compared to the conventional single-phase, forced-convection liquid cooling approach. This reduction in the thermal resistance may translate to a 75% increase in power density. In addition to the thermal benefits, this passive cooling approach does not require a pump or compressor, leading to increased efficiency. Note that the system can dissipate higher heat loads beyond those tested; however, the system pressure capacity limited the amount of power imposed. A key finding from these tests is that only a small quantity of refrigerant ($\leq 250 \text{ mL}$) may be required to dissipate automotive power electronic heat loads (3.5 kW). Smaller refrigerant requirements translate to lower system cost, size, and weight.

Two-Phase Power Electronics Cooling System Design

We designed a two-phase cooling system to cool Delphi's advanced discrete power modules/switches. This work is an attempt to demonstrate a viable power electronics two-phase cooling solution using advanced

automotive power modules. The system uses a passive and indirect cooling approach. Unlike the prior two-phase system (Figure V - 58), this system is designed to cool Delphi's discrete power modules, use an air-cooled condenser, and operate with higher pressure refrigerants (i.e., HFO-1234yf and R-245fa). To allow operation with higher pressure refrigerants, the system was designed with a maximum operating pressure of 1 MPa. Finite element structural and thermal analysis was used to aid in the design of the system.

This system will allow us to characterize the total thermal resistance (junction to air) of the two-phase cooling system. Three systems have designed and are currently in the process of being assembled. Once fabricated, these two-phase systems will be tested and their performance, size, weight, and efficiency will be compared to that of a representative, automotive single-phase cooling system.

Conclusion

- Our team characterized the pool boiling performance of R-245fa. Heat transfer coefficients and CHF values were obtained at different temperatures with plain and microporous-enhanced surfaces. With microporous coatings, R-245fa provides heat transfer coefficients and CHF values as high as $130,000 \text{ W/m}^2\text{-K}$ and 68 W/cm^2 , respectively. Based on its thermal performance, R-245fa is a viable refrigerant for two-phase cooling of power electronics.
- Experimental results combined with finite element simulations reveal that employing an indirect, passive two-phase cooling scheme can decrease power module thermal resistance by 43% and increase power density by 75%, as compared to conventional automotive cooling strategies. Additionally, experiments show that only $\leq 250 \text{ mL}$ of refrigerant may be required to dissipate automotive heat loads (3.5 kW).
- We have designed passive, two-phase cooling systems to cool Delphi's discrete power modules. The cooling systems employ an indirect cooling approach and have an air-cooled condenser. Experiments are planned to characterize the performance of these cooling systems using refrigerants HFO-1234yf and R-245fa. Extensive testing is planned with these systems to demonstrate the advantages of two-phase based power electronics cooling system.
- We have designed and fabricated an experimental system to test the long-term reliability of boiling enhancement coatings.

Publications

1. Moreno, G., Narumanchi, S., and King, C., 2012, "Pool Boiling Heat Transfer Characteristics of HFO-1234yf on Plain and Microporous-Enhanced Surfaces," ASME Journal Heat Transfer (submitted).
2. Moreno, G., Narumanchi, S., and King, C., 2011, "Pool Boiling Heat Transfer Characteristics of HFO-1234yf with and without Microporous Enhanced Surfaces," Proceedings ASME 2011 International Mechanical Engineering Congress & Exposition, Denver, CO, USA.
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V.6 Air-Cooling Technology for Power Electronics Thermal Management

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Objectives

The overall project objective is to develop and apply air-cooling technology to improve power electronics thermal control design and influence industry, enhancing system performance to meet DOE's 2015 technical targets for weight, volume, cost, and reliability by 2014. This overall objective includes the following:

- Develop and demonstrate commercially viable, low-cost air-cooling solutions for a range of vehicle applications and assess their potential for reducing the cost and complexity of the power electronics cooling system.
- Enable heat rejection directly to ambient air, simplifying the system by eliminating liquid coolant loops, thereby improving weight, volume, cost, and reliability.
- Collaborate with Oak Ridge National Laboratory (ORNL) to demonstrate the feasibility of using a high-temperature air-cooled inverter to achieve DOE's 2015 technical targets by 2014.
- FY 12 objectives included:
 - Determine the feasibility of high-temperature air-cooled inverter
 - Build a system-level test bench and begin investigation of balance-of-system components
 - Begin thermal design optimization to ensure that effective designs are being used to determine the bounds of air-cooled inverter design space.

Approach

- Use a system-level approach that addresses the cooling technology, package mechanical design, balance-of-system, and vehicle application requirements.
- Research each of these areas in depth and apply findings to develop effective system-level designs.
- Develop experimental and analytical/numerical tools and processes that facilitate high-quality and rapid research results.
- Investigate the effect high temperature power semiconductor devices have on air-cooled inverter design.
- Work closely with industry, university, and national laboratory partners to ensure relevant and viable solutions.

Major Accomplishments

- Worked with ORNL to determine thermal requirements for high temperature air-cooled inverter.
- Through modeling and validation experiments, showed the heat transfer feasibility of a high-temperature air-cooled inverter. Predicted 3.5 kW of heat rejection, surpassing the conservative target of 3.2 kW, using 150 CFM of air. This predicted flow rate and pressure drop could be provided by a 50-W fan. This flow rate is less than that used by a typical automotive climate control system. Additional balance-of-system issues and losses still need to be addressed in a more detailed design phase.
- Experimentally measured the baseline fin performance and used data to validate computational fluid dynamics (CFD) model to within 6.5% error for heat dissipation, pressure drop, and outlet temperature.
- Began the thermal design phase of the project, using CFD to establish the baseline fin performance and found an improved design that reduces fluid power, volume, and weight.
- Developed air-cooling system-level test bench for balance-of-system evaluation. Determined accuracy and repeatability of test bench. Used bench to complete initial fan tests and began to baseline commercial automotive air ducting approaches.

Future Direction

- Prototype and test optimized and advanced fin designs. Improve models based on test results. Down select best design for prototype module.
- Test balance-of-system components (fans and ducting). Incorporate results into system-level model. Develop initial high temperature air-cooled inverter balance-of-system design. Demonstrate operation of thermal system design.
- Test optimized module design for thermal performance and in combination with high temperature electronics from ORNL. Results will feed into improved design and future high temperature air-cooled inverter demonstration with ORNL.



Technical Discussion

Approach

The objective of NREL’s Air-Cooling Technology for Power Electronics Thermal Management project is to assess, develop, and apply air-cooling technology to improve power electronics thermal control design and influence industry’s products, thereby enhancing system performance to meet DOE technical targets for weight, volume, cost, and reliability. With the notable exception of the low-power Honda Insight, commercially available hybrid vehicles use liquid-cooled power electronic systems. All the heat from a vehicle, however, must ultimately be rejected to air. For liquid-cooled systems, heat from the power electronics is transferred to a water-ethylene glycol coolant via a heat exchanger and then pumped to a separate, remote liquid-to-air heat exchanger where the heat is rejected to air. This research effort seeks to develop the necessary heat transfer technology and system-level understanding to eliminate the intermediate liquid-cooling loop and transfer heat directly to the air. The relative merits of air-cooled, high-heat-flux

automotive power electronic thermal management systems and the influence of high-temperature, wide bandgap semiconductors on this design space will be quantified, evaluated, and demonstrated under steady state and transient conditions.

Effectively and viably accomplishing these goals requires an air-cooled system thermal design understanding and approach. As shown in Figure V - 61, this project will use modeling and experimentation to address each aspect of the system: heat transfer cooling technology, power electronics package thermal design, balance-of-system (prime movers, ducting, etc.), and their interconnected interactions. It is also critical to account for and understand the effects of constraints and inputs into the air-cooled thermal management system: thermal environment, device type, and vehicle context. The thermal environment constraints have a direct impact on the driving temperature difference available for air-cooled heat transfer and can vary depending on design targets and system location in a vehicle. Under-hood temperatures are approximately 100°C –140°C and are therefore unsuitable for cooling. External ambient air at 30°C –45°C is highly suitable for cooling, and some additional benefit can be gained from using cabin air, but it must be balanced with the added parasitic load on the air conditioning system. The device type will determine both the maximum junction temperature and efficiency and thus influences the maximum allowable package surface temperature and heat load. Advanced power semiconductors, such as silicon carbide and gallium nitride, have the potential to greatly expand the air-cooling feasibility range by increasing the allowable junction temperature from 125°C to 200°C or higher while possibly improving efficiency. Vehicle context determines the power electronics duty cycle, affecting the total heat rejection needs and also imposing constraints on the system volume and weight. Understanding the in-vehicle demands on the power electronics systems will allow for modulated designs to meet cooling needs, reducing system overdesign and minimizing parasitic losses.

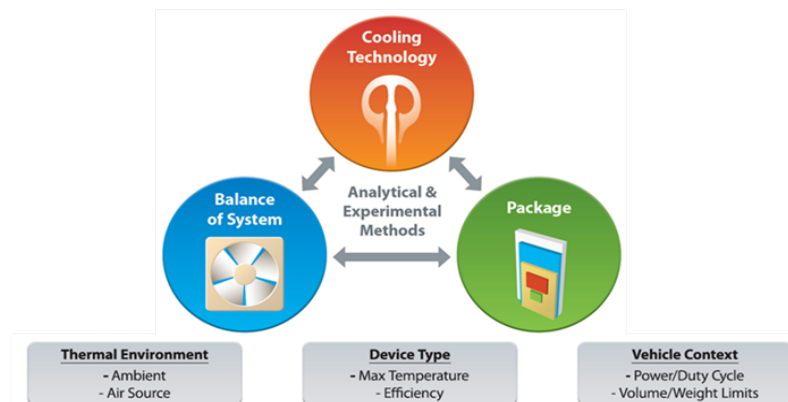


Figure V - 61: Power electronics air-cooled thermal management system research and design approach.

To move ideas from concept to implementation, four levels of research, development, and demonstration will be used: novel cooling technology fundamental heat transfer, system-level heat transfer and balance-of-system, inverter-level application, and vehicle-level demonstration with

partners (Figure V - 62). This process will both ensure that each level of complexity assists in achieving the overall objectives and will serve to screen ideas so that only the best approaches pass to the next level.

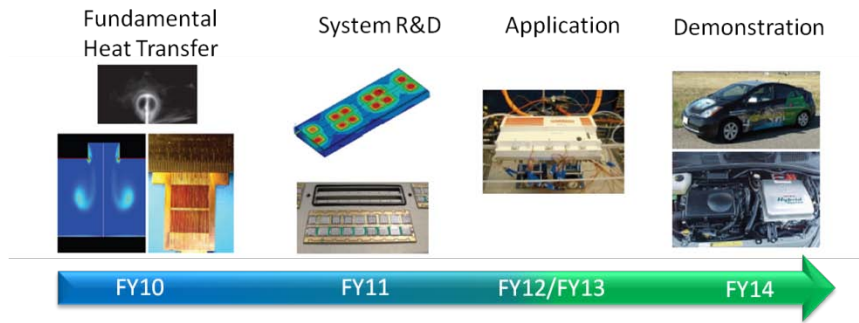


Figure V - 62: Air-cooling system research, development, and demonstration approach.

In FY11, NREL completed a proof-of-principle analysis using a system-level approach (Figure V - 63) [1]. In this analysis, as expected, the baseline liquid-cooled system significantly outperforms the air-cooled system. The relative performance of the air-cooled system improves with increasing allowable junction temperature and/or use of the improved concept spreader. At an allowable junction temperature of 200°C or 150°C plus the use of the advanced spreader, the air-cooled system is able to match the power density of the liquid-cooled approach

(Figure V - 63a). Insufficient information is available about this system to directly estimate cost; however, the power per silicon area can be a good indicator for cost. Figure V - 63b shows that the air-cooled system using advanced technology can meet or exceed the power per total insulated-gate bipolar transistor (IGBT) area of the liquid-cooled system. This analysis indicated that a high-temperature air-cooled system held significant promise and should be pursued in more depth.

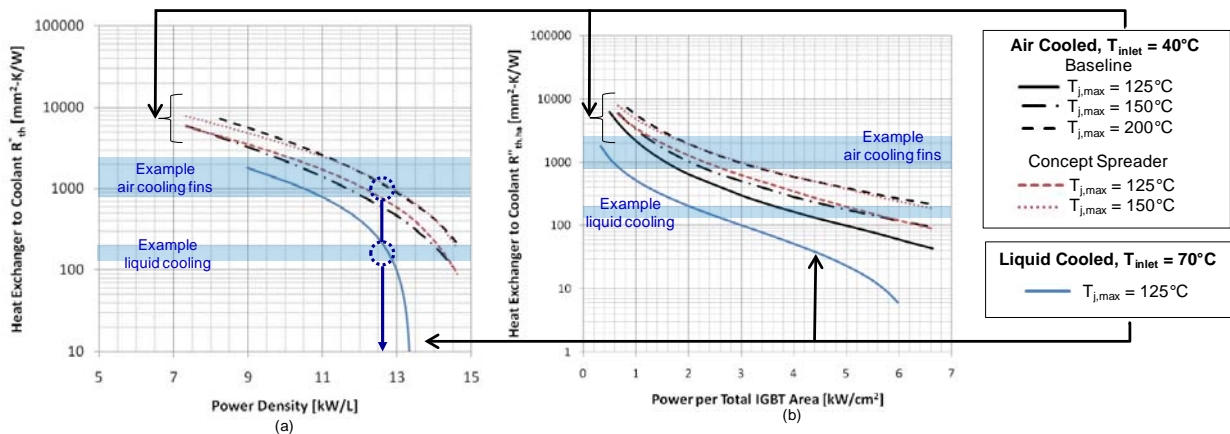


Figure V - 63: Air-cooled and liquid-cooled inverter performance: (a) power density (b) power per total IGBT (silicon) area.

Based on these results, NREL established a high-temperature air-cooled inverter collaboration with ORNL. The goal of this project is to demonstrate the feasibility of meeting DOE’s 2015 technical targets by 2014 using a high-temperature air-cooled inverter. ORNL is leading the advanced wide bandgap device evaluation and selection and electrical topology design. NREL is leading the thermal management design and evaluation at both the module- and system-level. The thermal system design approach for this collaboration is shown in Figure V - 64.

This is an iterative process between NREL and ORNL that involves other industry partners at various stages. In FY12, electrical design information was passed from ORNL to NREL, which then converted the information into thermal design targets. Based on this information, a feasibility/trade-off study was conducted using CFD modeling and experimental validation. After determining the feasibility, NREL applied modeling and experimental tools to begin a detailed thermal design to ensure an optimized prototype. In FY13, the optimized module

design will be completed, prototyped and tested. This will be combined with the module electronics from ORNL and tested as an operational unit. The full system thermal feasibility will also be determined. In FY14, a second pass through this process will be completed to design, build, and demonstrate an operational high temperature air-cooled inverter.

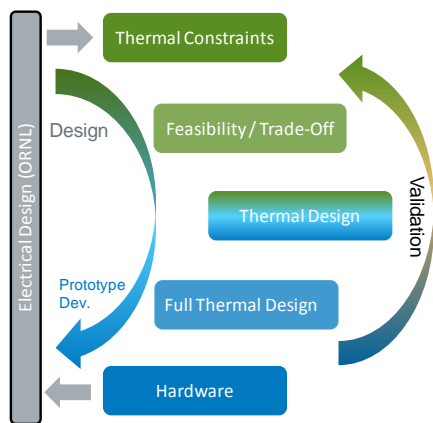


Figure V - 64: High temperature air-cooled inverter thermal design approach.

Experimental Methods

The Air Cooling Technology Characterization Platform, shown in Figure V - 65 was updated and used for

testing fin subsections in FY12. Compressed air was supplied to a desiccant dryer to remove moisture. The air was dried to a dew point of -20°C or lower. It was then passed through a 5-µm particulate filter and regulated to a constant 68 to 137 kPa. This regulated pressure served as the source air for a mass flow controller, Sierra model C100L, which provided a range of flow from 3.3 cm³/s to 166 cm³/s. Next, a laminar flow element, CME model 10 (0-166 cm³/s), was used for more accurate measurement of the actual air flow rate. This more accurate measurement was then used to adjust the upstream mass flow controller set point. The air then passed through a plate heat exchanger for optional temperature control. It then entered the flow channel fin test section (Figure V - 66a.). Air first flows through the entrance flow development section prior to reaching the fins under test. A guarded heater was placed on the back side of the fin section base. Indium was melted between the heater and fin base to minimize contact resistance. Air flow exiting the fin section passed through porous aluminum foam to mix the air and get an accurate bulk air exit temperature. The test section was wrapped in insulation and placed in a Plexiglas enclosure to minimize the effect of ambient air motion in the laboratory. Heat transfer measurements were fully automated and controlled by a computer and a National Instruments data acquisition system.

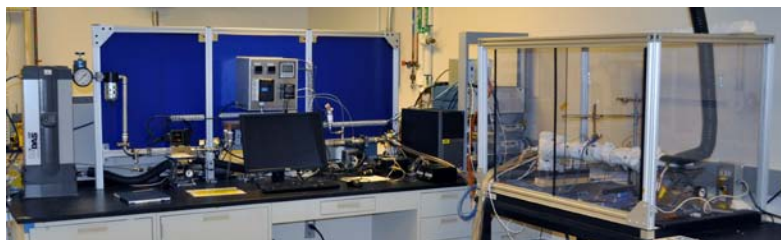


Figure V - 65: Photograph (left) and schematic (right) of the channel flow experimental setup: (1) compressed air, (2) desiccant dryer, (3) filter/regulator, (4) mass flow controller, (5) laminar flow element, (6) plate heat exchanger, (7) temperature control bath, (8) fin test section, (9) guarded heater, and (10) isolation box.

The guarded heater assembly (Figure V - 66b) had a copper base plate in contact with the fin section. Small grooves were machined to allow thermocouple placement. Above this copper base plate were the main heater, another copper plate with thermocouples, a mica thermal separator, another copper plate, and then the guard heater. The mica

separator provided thermal resistance. The guard heater was controlled to drive the temperature difference across the mica separator to zero, eliminating heat loss from the back of the main heater. The channel flow experimental uncertainty was calculated in accordance with ASME standard PTC 19.1-2005 [2].

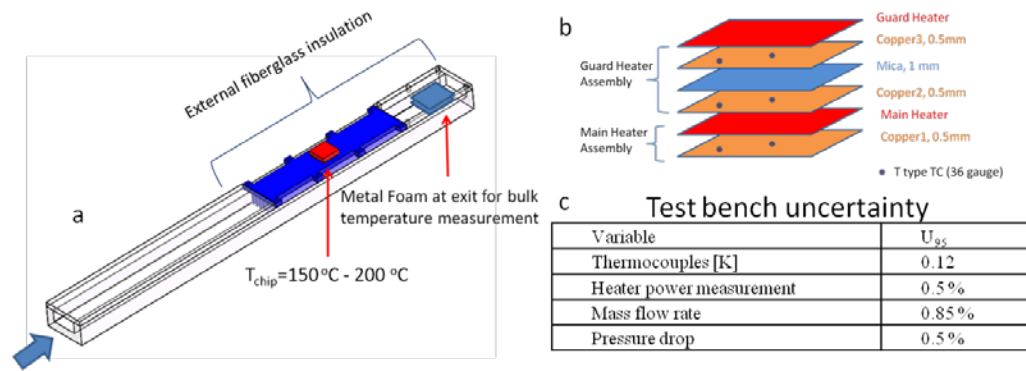


Figure V - 66: Channel flow experimental setup: a. channel flow section, b. guarded heater assembly, c. test bench uncertainty analysis.

In FY12 an air-cooling system-level test bench was completed (Figure V - 67). This test bench is intended for fan performance characterization, duct and plenum measurement, inverter module-level testing, and system-level demonstration. The air flow measurement section of the test bench follows ANSI/AMCA Standard 210-07 [3]. By using a series of nozzles, the flow chamber can maintain high accuracy measurements over a 5–500 CFM range. In the current configuration, air enters the chamber at plane 1, passing through the device under test (fan

currently), and through plane 2 entering the larger chamber. Using a combination of the variable exhaust fan and blast gate controls, the pressure at plane 7 is controlled for back pressure on the fan. The air then passes through settling screens and across the nozzle plate. Pressure drop across the nozzles, plane 5 to plane 6, is used to determine flow rate. The air then passes through additional settling screens and exits through the blast gate and variable exhaust blower.



Figure V - 67: System-level air-cooling test bench: a. picture b. schematic.

The test bench was checked for repeatability, transducer hysteresis, and instrument impedance effects, all of which had negligible errors. An optical fan speed sensor was used to measure fan speed. Uncertainty and propagation of error analysis, per ASME standard PTC 19.1-2005 [2], determined an average U_{95} flow uncertainty of $\pm 1.2\%$ and an average pressure uncertainty of $\pm 0.94\%$.

Numerical Methods

CFD models were created in ANSYS Fluent software for several stages of this project. For most of these models, convergence criteria were 1×10^{-3} for all residuals except energy and continuity, in which case the convergence criteria were tighter. More stringent convergence criteria were tested with minimal impact on results. Velocity and pressure residuals were also monitored. When needed, a $k-\epsilon$ turbulence model with enhanced wall treatments was

utilized. For each model, the results were confirmed to be mesh independent. To reduce computational expenses for the parametric optimization study, a full mesh sensitivity study was completed (Figure V - 68). It can be seen that as the mesh size increases, the time to converge increases, and the relative error decreases. There comes a point where increasing the mesh size does not have a significant benefit and increases computational time. The circled point was selected for the parametric simulations to balance run time and accuracy. Simulations were run on a high-performance computer, using up to 32 computational cores in parallel.

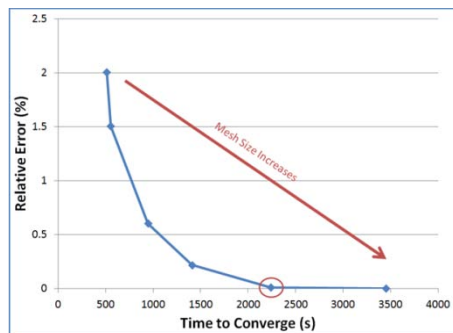


Figure V - 68: Mesh sensitivity plot for parametric optimization study. The circled point was selected.

Results

Thermal constraints

To determine the thermal constraints, NREL applied analytical and device switching level models to estimate the heat generation loads based on operating conditions provided by ORNL. The analytical model followed methods found in the literature for calculating conduction and switching losses for pulse-width modulation (PWM) inverters [4, 5]. The switching level model included an inverter model developed within Simulink to calculate conduction and switching losses of an operating inverter. Both the analytical model and Simulink inverter model relied on device data provided by ORNL. ORNL provided experimental data for high-temperature semiconductor device parameters collected as part of its wide bandgap

benchmarking efforts. Data included device voltage as a function of temperature and current, turn-on energy losses, turn-off energy losses, and reverse recovery losses. Using the data provided, the transistor conduction loss, diode conduction loss, transistor switching loss, and diode switching loss were calculated over a range of operating conditions. These results were checked for consistency and also compared with overall inverter efficiency estimations. From this analysis, and allowing for significant safety margins, a design target of 3.2kW of heat removal was determined. Maximum junction temperatures ranging from 150°C to 200°C were selected to represent a range of near-to mid-term technologies. Future studies may allow for higher junction temperatures to investigate the impact of longer term wide bandgap materials and package designs.

Feasibility

To determine the feasibility of meeting the thermal constraints of 3.2kW and 175°C, a CFD model of one flow channel from the inverter module was developed in ANSYS Fluent (Figure V - 69). This baseline module design concept was developed by ORNL. The yellow box in Figure V - 69a defines the model domain. This smaller domain was chosen to facilitate rapid feasibility analysis while capturing the heat transfer behavior. Air enters the model on the left of the figure at 40°C and exits on the right. The device temperatures were varied from 150°C–200°C. Symmetry boundary conditions were used on the left and right side of the model domain.

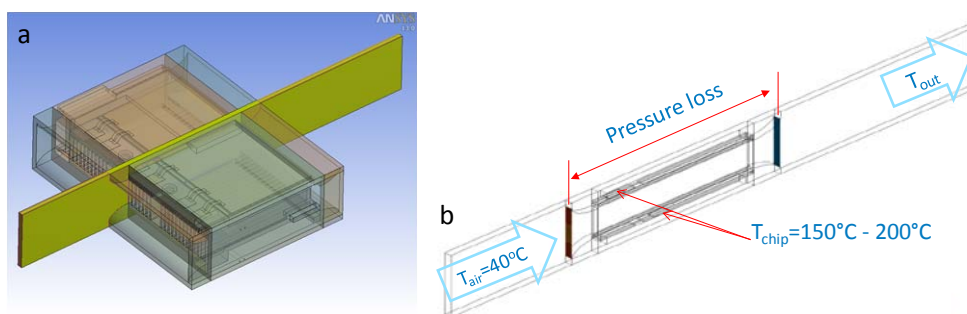


Figure V - 69: Single channel computational fluid dynamics model.

The results from this model were then scaled to investigate system-level performance using nine modules. Two system configurations were investigated (Figure V - 70): three parallel flow paths with three modules in series for each path (3x3) and all nine modules in parallel flow (9x1). By arranging the modules in the 3x3 arrangement, the volumetric flow required is reduced but

at the cost of additional pressure loss. The 9x1 arrangement conversely minimizes pressure loss but at the cost of additional volumetric flow. Both configurations were able to meet the 3.2-kW maximum heat rejection target at reasonable flow rate ranges. Even the higher 150 CFM flow rates are significantly smaller than flow rates in a typical automotive air conditioning system.

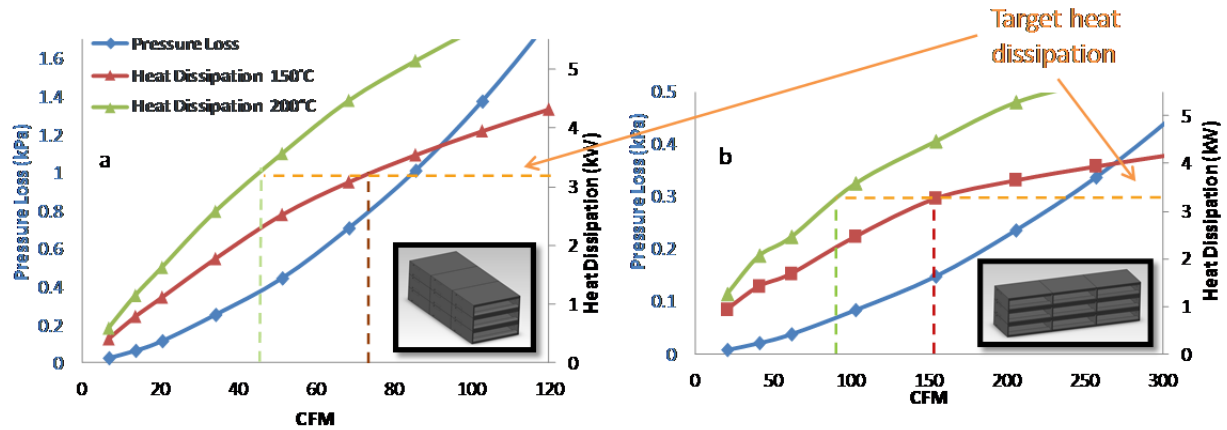


Figure V - 70: Extrapolated thermal performance of system arrangements: a. 3x3 modules b. 9x1 modules.

Figure V - 71 shows the predicted performance of the 9x1 arrangement with 175°C junction temperature in more detail. The example fan curve is from a manufacturer performance data sheet. The intersection of this fan curve

and the predicted 9x1 inverter fin pressure loss, results in a 150 CFM flow rate. The heat dissipation can then be found at the 150 CFM flow rate, in this case 3.5 kW, which exceeds the conservative 3.2-kW target.

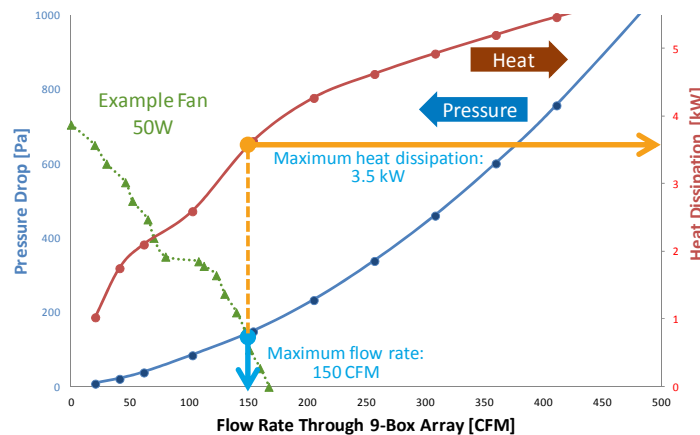


Figure V - 71: Feasibility analysis, 9x1 array, 175°C.

For the initial feasibility analysis, the air distribution plenum and ducting pressure losses have not been fully accounted for. These will be included in the more detailed Thermal Design phase and will increase the pressure loss requirements on the fan.

In order to validate the CFD modeling approach, similar methods and assumptions were used to compare the model to experimental data. For this process, however, a larger model domain (Figure V - 72a) was used to match the experimental domain (Figure V - 72b). This domain

included the air entrance region, all the fins for one device, and the exit region. To account for non-ideal contact between the heater and the base fin, a contact area of 70% was estimated for the model. This estimation was based on observed voiding in the indium when melted and was supported by experimental temperature measurements. Comparison between the model and experimental data was done for 150°C, 175°C, and 200°C. For heat dissipation, pressure loss, and outlet temperature, less than 6.5% error was found between the model and experiment.

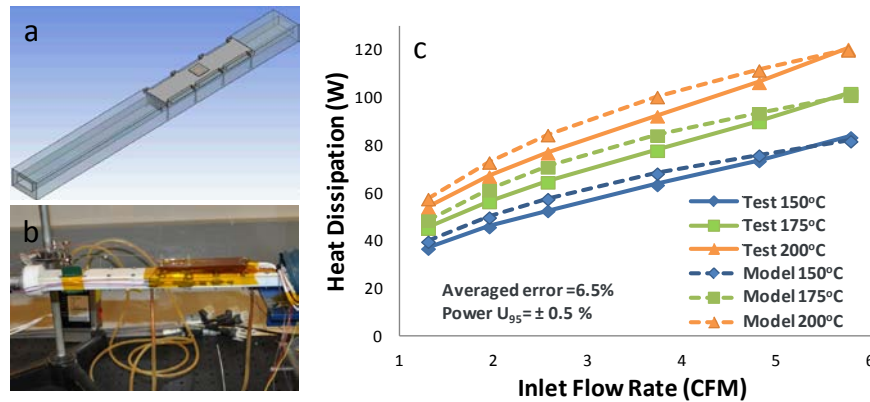


Figure V - 72: Validation of CFD model to experimental results, a. model domain, b. experimental setup, c. heat dissipation comparison.

Thermal Design

Once feasibility was established, the next step was to optimize the thermal design to make sure that an effective design was being used to investigate the air-cooled design space. This optimization was done with ANSYS Fluent and an NREL developed “ANSYS Driver” tool to control the optimization process. The NREL tool controls the simulation parameter selection and allows for sub-design point iteration. It is described in more detail in the Integrated Module Heat Exchanger annual report section [6]. For fin design optimization, the computational domain was expanded further to account for asymmetrical device locations (Figure V - 73). Each semiconductor device was assumed to have a fixed volumetric heat generation based on the thermal constraint specification previously discussed. For each design point, a sub-design point iteration was conducted by varying air flow rate until the maximum device temperature of $175^{\circ}\text{C} \pm 1^{\circ}\text{C}$ was achieved. This allowed the designs to be compared on an equal heat transfer performance basis and ensured that they would all meet the thermal requirements if allowed sufficient air flow rate.

This approach ensured all simulations would meet the thermal requirements at some flow rate, so the goal of the fin optimization was then to decrease fluid power, weight, and volume. Fluid power is defined as volumetric flow rate multiplied by pressure drop and will be related to parasitic losses through the prime mover efficiency. It should be noted that reducing fluid power, weight, and volume can be competing optimization goals.

The following geometric parameters for the baseline rectangular fin design were parametrically studied: semiconductor device location (top and bottom), fin height, fin length, baseplate thickness, fin thickness, and channel width. In order to reduce the design space, the

optimal device location was studied first. The optimal device location was found to be predominantly dependent on length, so an optimal location model as a function of length was developed for both devices. The top and bottom device locations were then adjusted with length to remain in their optimal positions. A three-level full factorial study was then conducted with fin height, fin length, and fin thickness. Within the parameter range studied, it was found that fluid power decreases as fin thickness decreases. This indicated that fin thickness should be set at cost-effective lower manufacturing limits. A more refined three-level full factorial study was then conducted adding in baseplate thickness and channel width, along with fin height and fin length. Based on these results, additional simulations were conducted in promising design regions. Figure V - 74 shows a subset of these combined results in the design region of interest. The blue region in Figure V - 74 indicates improvement from the baseline. For the design parameters studied, weight and volume tracked closely. Adjusting baseplate thickness and channel width within manufacturing constraints did not improve the optimal design. A curved front can be seen in the blue improved design region on both the volume and weight graphs in Figure V - 74.

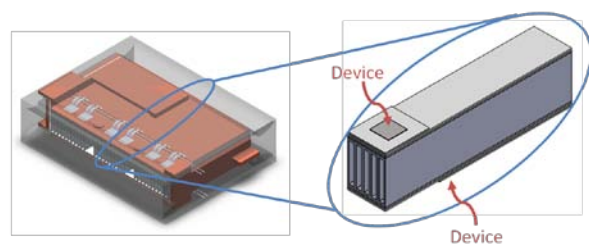


Figure V - 73: CFD model domain for fin optimization.

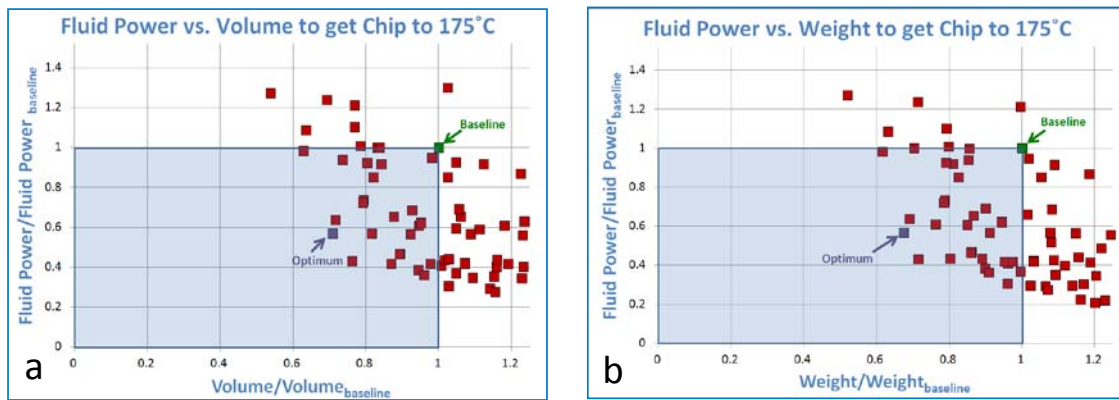


Figure V - 74: Design optimization results (subset of full results): (a) normalized fluid power versus normalized volume, and (b) normalized fluid power versus normalized weight. The baseline design is shown in green, and the initial optimum design is shown in purple.

Closer examination of this curved front found the behavior was predominately due to fin height and length. Figure V - 75 shows constant height and constant length contour lines that were developed from these results. This figure clearly shows the relationship between height, length, and fluid power. At this point in the optimization, design decisions must be made about how to weight the competing performance requirements. To optimize for fluid power and volume equally, a design on the green line should be developed, and to optimize for fluid power and weight equally, a design on the blue line should be

developed. The initial optimum design, therefore, will be at approximately $h/h_b = 1.4$ and $l/l_b = 0.54$. At this location, fluid power, volume and weight are all reduced in almost equal amounts. This optimal design point can also be seen on Figure V - 74. Once this design has been validated experimentally, computational and experimental results will be used to find more optimal designs. Future design decision will ultimately be determined by weight and volume constraints to meet DOE’s APEEM technical targets.

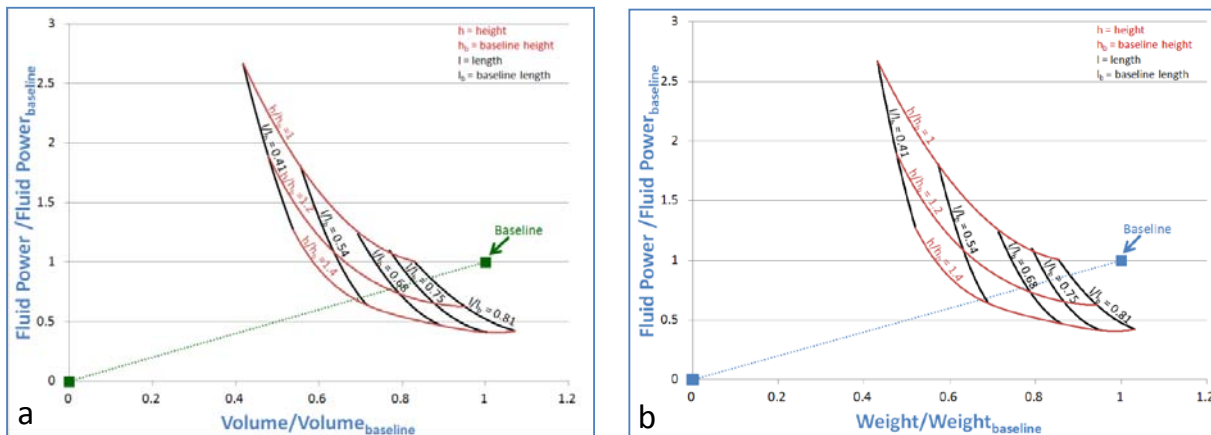


Figure V - 75: Contour plot showing (a) normalized fluid power versus normalized volume and (b) normalized fluid power versus normalized weight. The red lines indicate constant height, and the black lines indicate constant length. The baseline design is also shown in (a) green and (b) blue.

The next step in design optimization is experimental design evaluation. A new Air-Cooling Characterization Platform attachment was designed to evaluate module subsections with two heat sources. NREL will work with Sapa to prototype and test baseline and optimized designs. NREL is also currently applying this optimization process to several advanced fin concepts in collaboration with Sapa.

In parallel to the fin and module design optimization work, NREL is using its air-cooling system-level test

bench to research balance-of-system components, including fans and ducting. Figure V - 76a shows flow performance results for three example fans operating at their rated speeds. Figure V - 76b shows the variation in fan efficiency, defined as measured power divided by fluid power, under these same operational conditions. This chart shows the efficiency peak and behavior can vary between fan models.

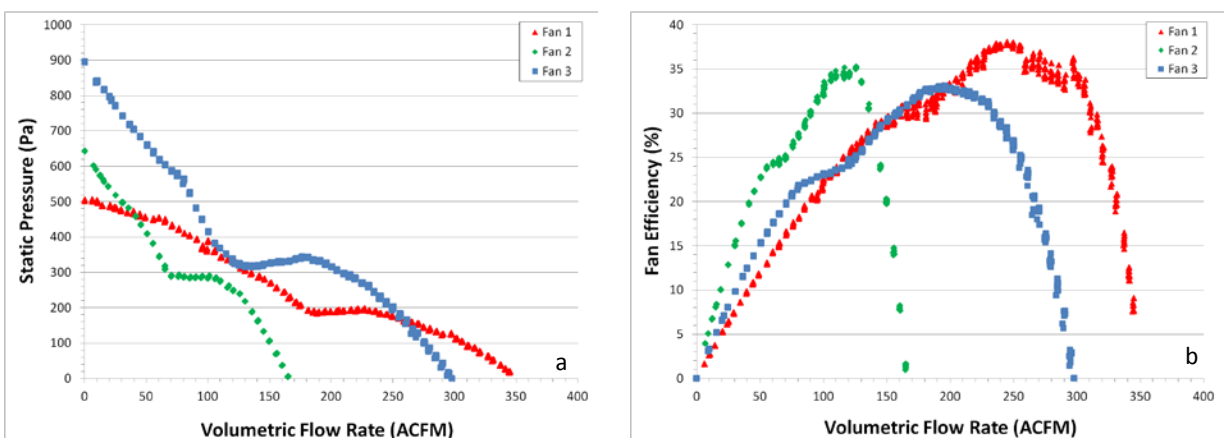


Figure V - 76: Example fan testing results: a. fan flow performance, and b. fan efficiency.

These three fans can also be pulse-width modulated to adjust blade speed and the resulting pressure, flow and efficiency performance. In Figure V - 77a, for example, “Fan 3” from Figure V - 76 was tested over the allowable range of operation. Adjusting the fan speed expands the potential operation range. The optimal operational zone for the three fans, shown in Figure V - 77b, was determined by

setting a lower efficiency limit of 25%. Therefore, any operation point in the bounded region will be above this efficiency. Combining these optimal fan operation zones with the module- and system-level pressure losses and flow requirements will ensure fans are properly selected to minimize parasitic losses while maximizing heat transfer performance.

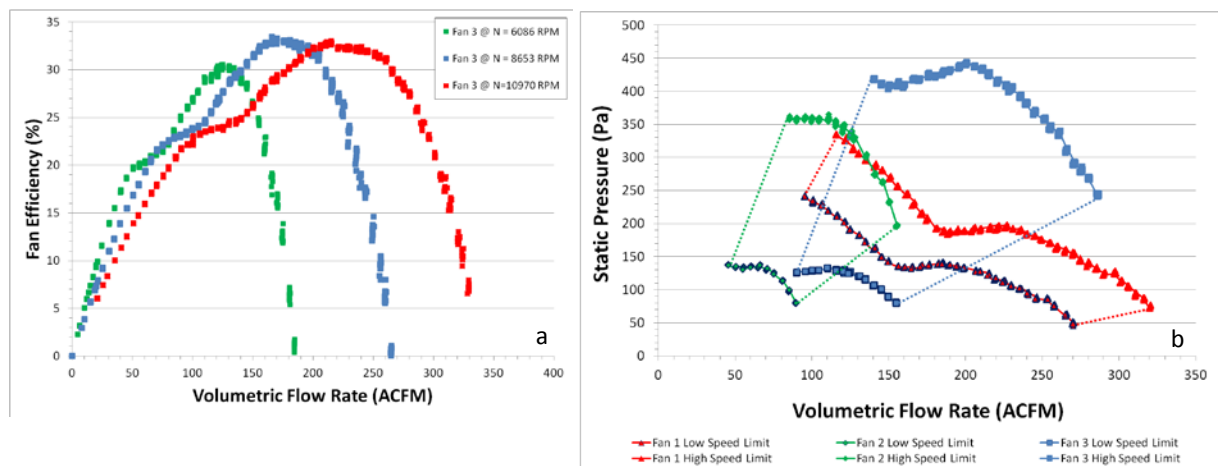


Figure V - 77: Fan efficiency: a. Fan 3 efficiency operation range b. optimal fan operation zone, area inside contours above 25% efficiency.

To address ducting and plenum design considerations, NREL is currently experimentally benchmarking production vehicle air duct performance. This will be used as an initial starting point for duct pressure loss estimation and design. By learning from existing air handling systems, effective production-viable solutions will be developed specifically for the air-cooled inverter designs.

Conclusion

Significant progress was made toward the project’s objective to develop and apply air-cooling technology to improve power electronics thermal management design and influence industry, thereby enhancing system

performance to meet DOE technical targets for weight, volume, cost, and reliability. To this end, NREL worked with ORNL to establish a high-temperature air-cooled inverter collaboration with the objective of meeting DOE’s 2015 technical targets by 2014.

NREL and ORNL worked together, using experimental data and models to establish a 3.2-kW heat rejection requirement for the high temperature inverter design. NREL then developed a CFD model that showed the feasibility of rejecting 3.5 kW with 150 CFM and 175°C junction temperature. This is less than the flow needed for a typical automotive air conditioning system. This flow rate and pressure drop could potentially be achieved using a 50W commercial fan. CFD models were

then validated with experimental data to within 6.5% error for heat dissipation, pressure drop, and outlet temperature. While there are still significant balance-of-system and design details to address in the Thermal Design phase, this analysis showed the potential heat transfer feasibility of a high-temperature air-cooled inverter.

Based on this success, NREL used CFD models to explore the design space and optimize the baseline design, improving predicted performance. These results created an understanding of the design trade-offs and the ability to adjust optimization priority between fluid power, volume, and weight. NREL is working with Sapa to prototype these and other advanced fin concepts that will be tested and used for model validation and improvement. The best of these designs will then be down selected and used for a module-level prototype evaluation.

NREL also completed an air-cooling system-level test bench. The test bench was determined to be highly repeatable and have insignificant hysteresis, meeting design objectives. Initial fan tests were completed, providing fan selection and efficiency information for system-level decisions. Commercial automotive ducting is currently being evaluated, and design options are being considered.

The significant progress this year has laid a strong foundation for developing and demonstrating a high-temperature air-cooled inverter that will meet DOE's 2015 technical targets by 2014.

Publications

1. He, X., Lustbader, J., Arik, M., Sharma, R. "Characteristics of Low Reynolds Number Steady Jet Impingement Heat Transfer Over Vertical Flat Surfaces." ITherm 2012. San Diego, CA. May 20 – June 1, 2012.
2. Arik, M., Sharma, R., Lustbader, J., He, X. "Comparison of Synthetic and Steady Jets for Impingement Heat Transfer Over Vertical Surfaces." ITherm 2012. San Diego, CA. May 20 – June 1, 2012.
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- Photo credits: Figure V - 62 - a. Charlie King, b-c. Mark Mihalic, d. NREL PIX 15141; Figure V - 65 - Jason Lustbader; Figure V - 67 - Casey Smith; Figure V - 72- Xin He

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V.7 Integrated Module Heat Exchanger

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Objectives

A cost-effective, compact, efficient, and reliable electric traction drive is a key enabling technology for the electrification of vehicle propulsion systems. Heat dissipation has a significant impact on the power capability of power electronics, which leads to increased device cost and package volume or size. The optimal thermal performance is a function of the power electronics packaging and the heat exchanger design. To reach the desired cost and performance objectives, a solution that integrates commercially available packages with low-cost cooling technologies is needed. The NREL team has developed a concept for an integrated power electronics module heat exchanger to reduce cost by improving the power per die area. The primary objectives are to:

- Improve power per die area by 100% over existing commercial power electronics thermal management systems
- Maintain best-in-class power density capabilities as compared to existing systems
- Enable a modular or scalable thermal approach to reduce the need for custom heat exchanger redesigns as applications scale in power
- Eliminate internal fluid seals commonly found on existing integrated cooling concepts to reduce leaking induced failure modes
- Reduce parasitic power requirements for the cooling system.

Approach

The team's approach was to:

- Select baseline package configurations for performance benchmarking
- Perform thermal finite element analysis (FEA) design optimization of heat spreader structure to investigate the thermal structure design and material selection
- Identify convective cooling performance targets
- Pass through go/no-go decision point to determine design feasibility of meeting performance objectives
- Evaluate cooling surface enhancement designs using computational fluid dynamics (CFD) modeling tools and confirm ability to develop the heat exchanger surface that meets the minimum convective cooling performance requirements
- Perform full system thermal and fluid simulations to revise the heat spreader design and the convective cooling heat exchanger surface, enabling cost reductions
- Design and develop prototype hardware for testing
- Design experimental test setup for prototype testing.

Major Accomplishments

The team has achieved the following:

- Selected and analyzed baseline thermal stack configurations for performance benchmarking
- Compared performance of alternative designs at targeted cooling performance region against baseline configurations
- Performed parametric design study and selected preliminary design for CFD analysis and design refinement
- Developed CFD model of convective cooling interface and full integrated thermal system with power electronics package and heat exchanger
- Completed design iterations to reduce manufacturing cost
- Designed test heater package to represent power semiconductor package for prototype testing
- Designed and modeled the test setup to improve accuracy of experimental results and correlation to model results.

Future Direction

- Complete prototype fabrication and compare experimental results against modeling expectations
- If prototype hardware matches design expectations, integrate the design with a power electronics package
- Investigate new design as applied to a half bridge inverter module instead of a single switch
- Explore application to alternative coolants with reduced heat transfer potential such as air or transmission oil.



Technical Discussion

Improving the ability to remove heat from power electronics semiconductor packages is significant in reducing the cost and size of semiconductor devices [1]. For this reason, new and improved thermal management approaches are needed for power electronics systems. The overall thermal performance of the power electronics system depends on both the thermal packaging of the semiconductor devices and the design of the cooling interface. As shown in previous work, the cooling performance must be matched to the package design to get the optimal integrated solution [2–4].

Existing State of the Art

The heat dissipation limitations of a conventional power electronics package, as shown in Figure V - 78, are well known and described in the literature. The thermal limitations of the thermal interface material between the heat spreader and the heat exchanger have led to efforts to improve the thermal interface [5] or remove interface materials through direct cooling.

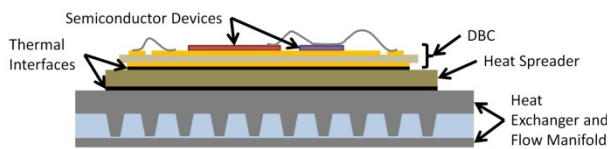


Figure V - 78: Conventional power electronics semiconductor thermal stack with heat spreader and thermal interface material between the heat spreader and the heat exchanger surface.

Direct cooling of the power semiconductor package can take multiple forms, but generally involves removing intermediate layers between the semiconductor device and the cooling fluid. Two common approaches involve direct cooling of the heat spreader, as shown in Figure V - 79 or direct cooling of the substrate metallization layer. Examples include direct bond copper (DBC) or direct bond aluminum, as shown in Figure V - 80. Often, the direct cooling is combined with aggressive cooling mechanisms. Examples include fluid jets that impinge on the heat spreader or DBC directly [6–8], microchannels [9], pin

fins [10–13], or other fin structures such as folded fins attached to the heat spreader [14].

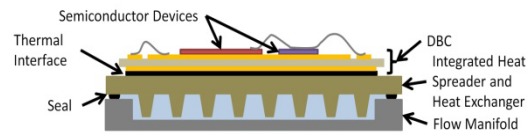


Figure V - 79: Example package with a direct-cooled heat spreader.

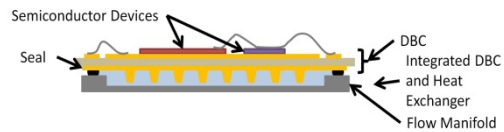


Figure V - 80: Example package with direct-cooled metallization layer such as direct bond copper (DBC).

In addition to improving the thermal performance through reducing the thermal stack resistance and more aggressive cooling, others have proposed methods to remove heat from both sides of the power semiconductor device (also known as double-sided-cooling) [1], [15], [16]. A commercial example is the 2008 Lexus LS 600H hybrid electric vehicle, which is summarized in a report by Burress [17] and achieved the highest power density of the commercial devices benchmarked through the Department of Energy’s Vehicle Technologies Program. A schematic of the cooling and thermal package structure is provided in Figure V - 81.

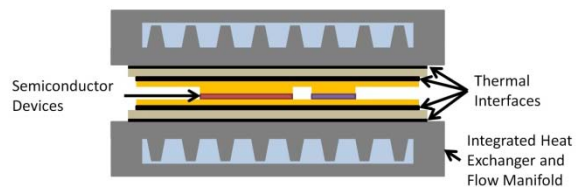


Figure V - 81: Example package enabling cooling on both sides of the power semiconductor device (double-sided cooling).

While the approaches discussed previously are effective at improving the ability to remove heat from the semiconductor devices, they face challenges regarding implementation. All of the cooling approaches highlighted above are dominated by planar heat removal structures that focus on one-dimensional heat transfer out of the power semiconductor package through the top or bottom of the package. The heat spreader does allow for some thermal spreading, but the cooling is applied to a single surface of the package. When the heat spreader is removed and the coolant fluid is directly applied to the DBC, the reduced heat spreading requires more aggressive cooling to maintain the same performance as illustrated by Bennion and Moreno [3]. The drive to more aggressive cooling leads to concerns related to fluid channel size, parasitic power, reliability, construction, and cost. To enable less aggressive convective cooling technologies, the heat

spreading characteristics of the thermal package must be matched to the convective cooling performance. The removal of layers within the semiconductor package also reduces the thermal capacitance of the structure, making the semiconductor more susceptible to transient loading effects, which impact reliability. Also, the direct-cooling approaches illustrated in Figure V - 79 and Figure V - 80 often require seals to prevent coolant from leaking into the electronics, which can lead to issues related to performance and reliability [10].

Proposed Concept

NREL's proposed cooling approach attempts to emphasize the use of the heat spreader to enable high cooling performance with less aggressive convective cooling methods. The approach integrates the heat spreader with the heat exchanger to provide multiple heat transfer paths within the heat spreader. Improving the heat spreading characteristics of the package provides an opportunity to increase the available surface area in contact with the coolant and does not rely on aggressive convective cooling methods or small fluid channel passages. Instead of relying on a planar thermal stack dominated by one dimensional heat transfer (Figure V - 82a), the concept design attempts to use the available space around the package to spread and remove heat along multiple paths, as illustrated in Figure V - 82b.

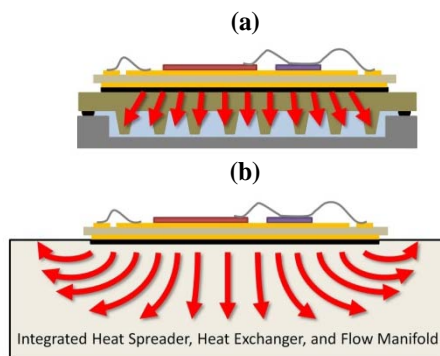


Figure V - 82: Schematic of conventional and design heat flow paths; (a) Conventional system with one-dimensional dominated heat flow path; (b) Conceptual drawing of integrated heat spreader and heat exchanger system to enhance heat spreading and cooling performance.

In addition to improving the thermal performance, the concept features other important characteristics not directly related to heat transfer. The design enables a modular, or scalable, approach to the cooling of power semiconductor devices that builds upon high-volume manufacturing methods already accepted by the automotive industry. Examples include thin-film folded fins used in brazed automotive heat exchangers and extruded aluminum materials used in a wide range of applications. The concept also eliminates the internal seals shown in Figure V - 79 and Figure V - 80. The seals are moved to external locations to reduce the risk of coolant

interfering with the electrical components. Additionally, the parasitic power requirements for the cooling system are reduced.

Approach

The initial approach of the project was to prove the potential of the cooling concept and refine the design that would lead to a hardware prototype for validation of the model results. Our work during FY12 focused on modeling and analysis to prove-out the concept and design a prototype heat exchanger that met the project objectives. The analysis work focused on the following three activities:

- Performing thermal FEA design optimization of the heat spreader structure to investigate the thermal structure design, select heat spreader materials, and identify convective cooling performance targets
- Evaluating cooling surface enhancement designs using CFD modeling tools and confirming the ability to develop the heat exchanger surface that meets the minimum convective cooling performance requirements
- Simulating the full system to iterate on the heat spreader design and the convective cooling heat exchanger surface to enable lower cost manufacturing.

To perform the FEA and CFD analysis, NREL developed a tool to enable control over the software applications required for the analysis. The tool was developed as a MATLAB graphical user interface (GUI) that interfaced with ANSYS Workbench, ANSYS Mechanical, ANSYS Fluent, and computer aided design (CAD) software (Figure V - 83). The tool enabled parametric studies of a large design space, including a range of geometrical parameters, material properties, heat loads, temperature limitations, and cooling parameters. Using custom-developed MATLAB codes, the tool was able to control the iteration of sequential simulations to converge on targeted solution results. Examples include an insulated gate bipolar transistor (IGBT) temperature, fluid flow rate, or coolant parasitic power value. Thousands of design iterations were performed through the use of NREL's parallel computing resources. The results are summarized below.

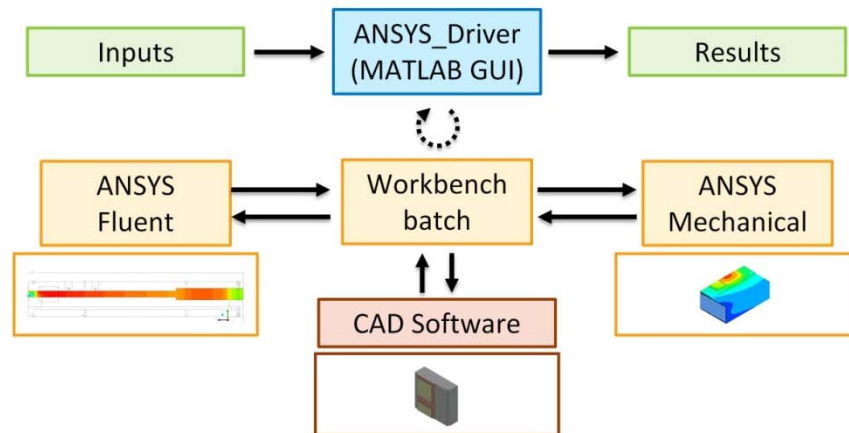


Figure V - 83: Modeling approach and tool development to link multiple simulation design software programs to enable large-scale parametric studies on NREL's parallel computing cluster.

Results

The first step in our analysis was to select packages for baseline comparison. The team selected the Lexus LS 600H thermal system as the primary baseline because of the documented high performance of the system. The design goals were to improve the power per die area by 100% while maintaining the best-in-class power density of the Lexus system. We also selected a second theoretical baseline to provide a more stringent baseline. The theoretical baseline was based on a direct-cooled system in which the heat spreader was cooled directly, as shown in Figure V - 79. In comparing the design concept performance against the theoretical direct heat spreader cooled baseline, all of the package interface and material properties were kept consistent. The direct-cooled heat spreader configuration was selected based on analysis of direct-cooled heat spreader and direct-cooled DBC (Figure V - 80) cooling configurations. The goal of the research was to enable less aggressive cooling technologies, and the direct cooled heat spreader configuration outperformed the direct-cooled DBC configuration in the targeted heat exchanger performance range.

Once the baseline systems were selected, the next step in the analysis was to perform a feasibility study using thermal FEA tools. The objective was to evaluate design alternatives related to the geometry of the heat spreader and material. An example of the design exploration is highlighted in Figure V - 84. The goals of the design were to improve the power per die area while maintaining power density at an acceptable level. The heat flux through the IGBT was selected as a metric for the power per die area objective. Two metrics were selected for quantifying impacts on the system size. The first focused on the package volume, while the second looked at the system

footprint area. Figure V - 84 compares a selection of designs by calculating their ranking relative to other designs. The graphs compare the IGBT heat flux percentile ranking against the percentile rankings for volume and footprint area. For each of the metrics, a number closer to one represents a design that outperforms the other designs in terms of power and size. The design objective was to find possible designs that would show a significant improvement in the IGBT heat flux percentile ranking while maintaining at least an average ranking for volume and footprint area. The results shown in Figure V - 84, while not a complete picture of the full design space, illustrate the process to identify design features that supported the overall project objectives. When combined with additional analysis and constraints, the design features were narrowed down to a preliminary design. The preliminary selected design is highlighted by the red circle in Figure V - 84a and Figure V - 84b.

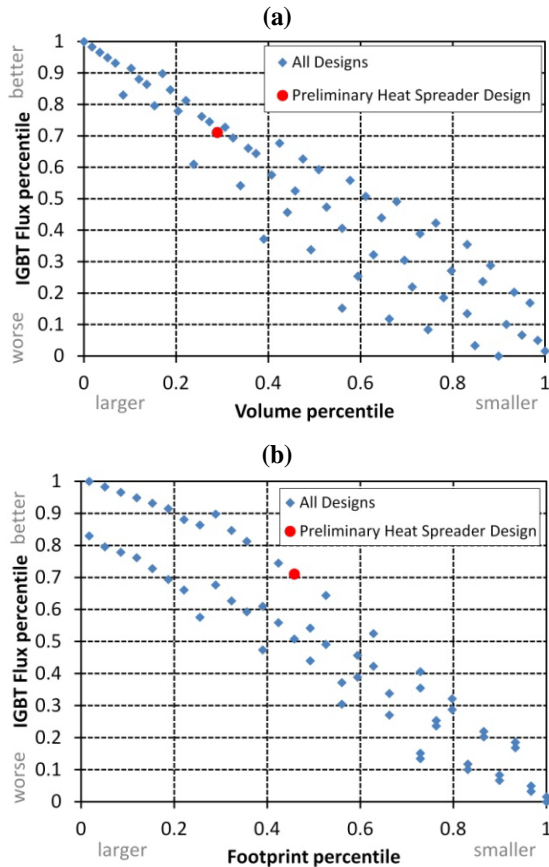


Figure V - 84: Parametric geometry parameter study comparing metrics for power per die area and package size: (a) IGBT heat flux versus package heat density, (b) IGBT heat flux versus package footprint area.

The performance of the preliminary heat spreader design was compared against the baseline configurations in Figure V - 85. The figure shows the relative improvement against the Lexus baseline in IGBT heat flux over a range of heat exchanger cooling performance values. The results satisfied an initial go/no-go decision point early in the project to determine the feasibility of meeting the design objectives. The results showed that an 87% to 98% improvement was possible over the targeted cooling operating region, as highlighted in Figure V - 85. The targeted operating region of the heat exchanger is shown in the figure as an effective area weighted resistance. The effective resistance was based on the effectiveness-NTU (number of transfer units) method for heat exchanger analysis and accounted for the convection coefficient, area enhancement, fluid properties, and mass flow rate of the fluid [4]. The targeted convective cooling operating region for the design was between 80 and 250 mm²-K/W.

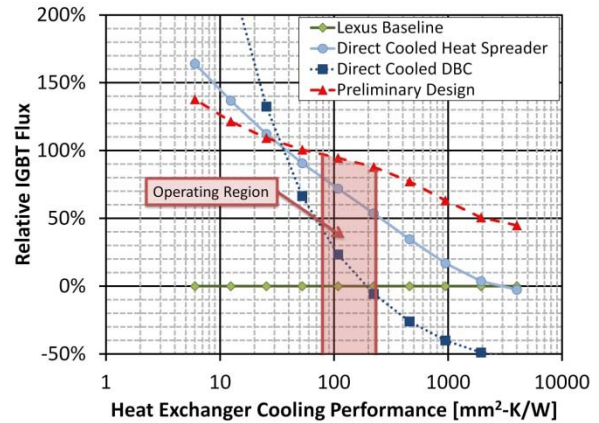


Figure V - 85: IGBT heat flux comparison of preliminary heat spreader design and target heat exchanger performance region.

The design showed a slight knee in the curve at 222 mm²-K/W, which is a result of attempts to enhance the heat spreading characteristics of the package. The initial preliminary heat spreader design was optimized for an effective heat exchanger cooling performance of 222 mm²-K/W. The knee in the curve of the preliminary design enables improved heat rejection over the targeted operating region. The performance of the design improves relative to the Lexus system as the heat exchanger performance increases, while the relative improvement is less as the heat exchanger performance decreases. The design is based on a heat spreader with the thermal conductivity equivalent to aluminum, while the Lexus package uses copper. Because copper has a higher thermal conductivity, it will provide better heat spreading with a less aggressive heat exchanger or higher heat exchanger thermal resistance. The reason for selecting aluminum was based on industry input and efforts to reduce cost. The performance of the design relative to the direct cooled heat spreader baseline decreases as the heat exchanger performance improves, or as the heat exchanger thermal resistance decreases. When the heat exchanger effective resistance decreases below 40 mm²-W/K, the curves cross and the baseline direct-cooled heat spreader shows better performance. For comparison, the figure also shows the relative performance of the direct-cooled DBC configuration, illustrating how it underperforms the direct-cooled heat spreader over the targeted operating region. For this reason, the direct-cooled heat spreader was selected as a more aggressive baseline configuration for comparison in the following analysis.

Figure V - 86 compares the performance measures for power per die area and power density of the preliminary heat spreader design against the two selected baseline configurations. IGBT heat flux was used as a metric for power per die area, and the volumetric package heat density was used as a metric for power density. The volumetric package heat density was calculated by dividing the total package heat by the total package

volume. The package heat was determined by solving for the heat generation that would result in a target IGBT temperature. The maximum allowable IGBT temperature was kept at 150°C for the results shown in this report. The results in Figure V - 86 were normalized by the Lexus package performance to illustrate the performance benefit. The performance of the Lexus package was based on previous work by Bennion and Kelly [4]. To be consistent, all of the results displayed were for a single-sided package, and the Lexus performance results were based on the average performance for a single cooling surface. The results in Figure V - 86 showed that single-sided cooling of the design achieved almost the same performance with a smaller size as the double-sided cooling of the Lexus baseline package. The design was made to be compatible with double-sided cooling, so the performance benefit would increase if double-sided cooling was applied. The preliminary design exceeds the IGBT heat flux performance of the direct-cooled heat spreader baseline with a slightly smaller package heat density. The results shown in Figure V - 86 confirmed the design's ability to almost double the power per die area, as compared to the Lexus baseline, while maintaining equal or better power density, and satisfied the initial project go/no-go decision point.

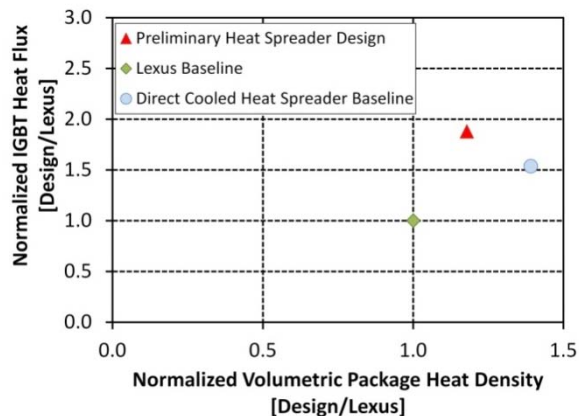


Figure V - 86: Performance comparison at a heat exchanger cooling performance of 222 mm²-K/W.

Once the target operating region of the heat exchanger was known the next step was the evaluation of potential cooling surface enhancement designs using computational fluid dynamics (CFD) modeling tools. The cooling performance of the heat exchanger surface was converted into an effective area-weighted thermal resistance, as discussed previously. The performance of the heat exchanger surface was evaluated over a range of flow rates, two of which are illustrated in Figure V - 87. In Figure V - 87a, the total system flow is divided into six parallel branches, while in Figure V - 87: b the full flow passes through each module represented by the blue rectangle. Figure V - 88 summarizes some of the results to illustrate the design process. Figure V - 88 compares the

heat exchanger performance against the system pressure drop for the flow configuration shown in Figure V - 87a with a total system flow rate of 10 L/min (1.67e-4 m³/s). The results uncovered a range of designs capable of achieving the desired performance between 100 and 220 mm²-K/W. All of the evaluated designs met the criterion of being able to pass a 1-mm particle in the fluid stream. However, for the initial prototype, a larger channel size capable of passing a 2-mm size particle was selected. The larger channel size was chosen to reduce manufacturing cost and provide a more conservative heat exchanger performance. Future work will revisit the manufacturing costs and investigate opportunities to reduce channel size, leading to increased thermal performance.

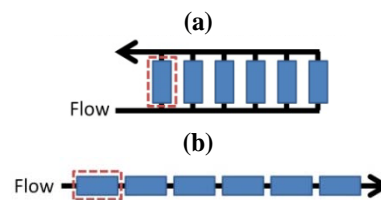


Figure V - 87: Example design flow rate configurations: (a) The total system flow is divided equally between six branches, (b) The total system flow passes through each module in series.

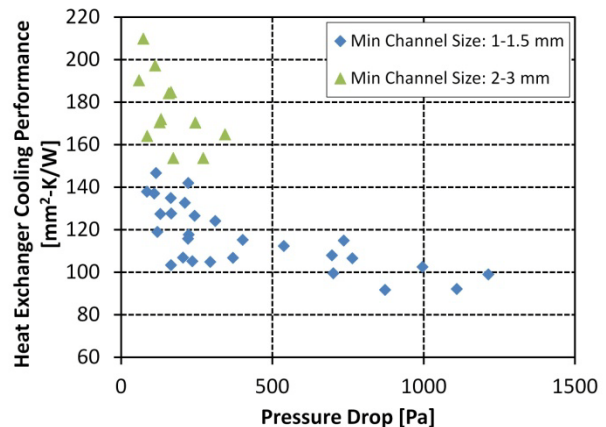


Figure V - 88: Sample comparison of heat exchanger surface geometry designs highlighting the ability to meet the targeted heat exchanger operating region.

The results shown in Figure V - 88 provided preliminary guidance on the heat exchanger surface design for the heat spreader. A full model was developed of the heat exchanger surface, heat spreader and semiconductor package to evaluate the combined thermal and fluid performance of the design. Using the full system CFD model additional modifications were evaluated to the heat exchanger design to reduce manufacturing cost. The model also enabled another design iteration of the heat spreader geometry to improve the overall thermal performance. The performance of the revised heat exchanger and heat spreader design was evaluated at the mass flow rate equivalent to one side of the Lexus LS 600H

system ($8.6e-3$ kg/s or $4.17e-6$ m³/s) [1], [4]. As shown in Figure V - 89a, the design outperformed the two baseline configurations in terms of the IGBT heat flux. The design outperformed the Lexus baseline system in terms of the volumetric heat density, but the direct-cooled heat spreader baseline showed the best volumetric heat density. The design at the Lexus equivalent flow rate improved the IGBT heat flux by almost a factor of two. Figure V - 89b compares the pressure drop of the different configurations. The pressure drop of the Lexus system is based on past analysis [4]. The design showed an 83% reduction in the pressure drop of the heat exchanger relative to the Lexus system at the same mass flow rate. The design also showed a 41% reduction in pressure drop as compared to the direct cooled heat spreader baseline for the same flow rate.

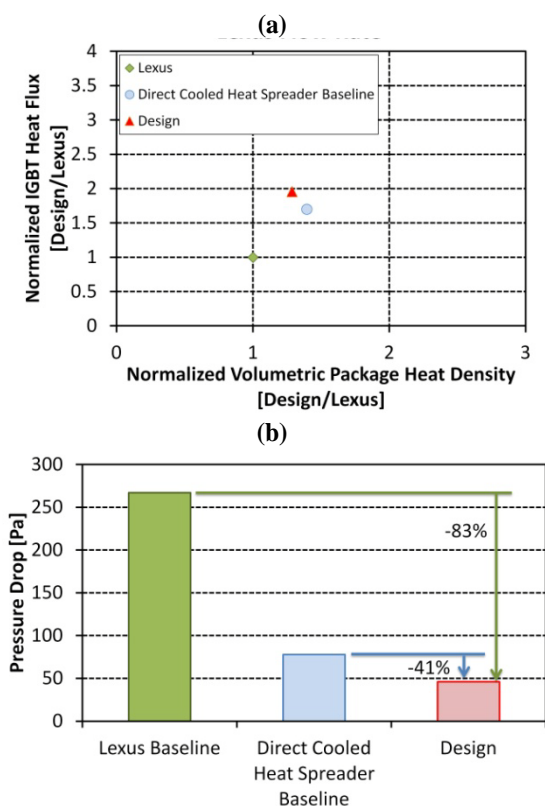


Figure V - 89: Performance of the design, Lexus system, and direct-cooled heat spreader baseline at the Lexus flow rate: (a) performance metrics for heat flux and heat density, (b) pressure drop.

The team also compared the performance of the design against the direct-cooled heat spreader baseline at increased flow rates. Figure V - 90 compares the performance of the design at a system flow rate of 10 L/min ($1.67e-4$ m³/s) with six modules placed in parallel branches, as shown in Figure V - 87a. The pressure drop was for one module, as highlighted in the dotted red line in Figure V - 87a. The pressure drop of the design was roughly equivalent to the Lexus system at the Lexus flow rate shown in Figure V - 89. The design heat flux and heat

density exceed the baseline Lexus system, but the design now exceeds both the heat flux and heat density of the direct-cooled heat spreader baselines. The design pressure drop is 20% below the direct-cooled heat spreader baseline pressure drop at the same parasitic power (0.00688 W). At the same flow rate, the difference in pressure drop would be larger.

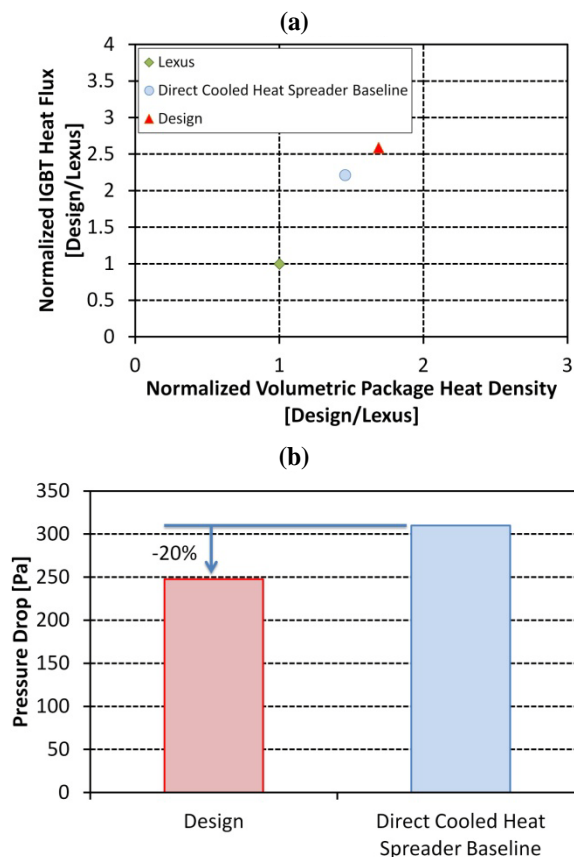


Figure V - 90: Performance comparison of the design assuming six parallel flow branches and the direct-cooled heat spreader baseline at the equivalent parasitic power: (a) heat flux and heat density performance, (b) pressure drop.

While the design heat exchanger was intended to operate as shown in Figure V - 87a, Figure V - 91 compares the performance at the flow rate of 10 L/min ($1.67e-4$ m³/s) with all of the modules placed in series, as shown in Figure V - 87: b. The pressure drop was for one module, as highlighted in the dotted red line in Figure V - 87b. The design heat flux and heat density significantly outperformed the original Lexus performance, and it also outperformed the direct-cooled heat spreader baseline at the same parasitic power (0.623 W). The reduced improvement in IGBT heat flux over the direct cooled heat spreader can be explained by Figure V - 85. At the higher flow rate the convective cooling increases, resulting in a lower thermal resistance, which reduces the performance benefit of the design. The design heat exchanger pressure drop is 21% below the

direct-cooled heat spreader baseline pressure drop at the same parasitic power, as shown in Figure V - 91b. Because the pressure drop comparison is at the same parasitic power, the difference in pressure drop would be larger if the two systems were compared at the same fluid flow rate.

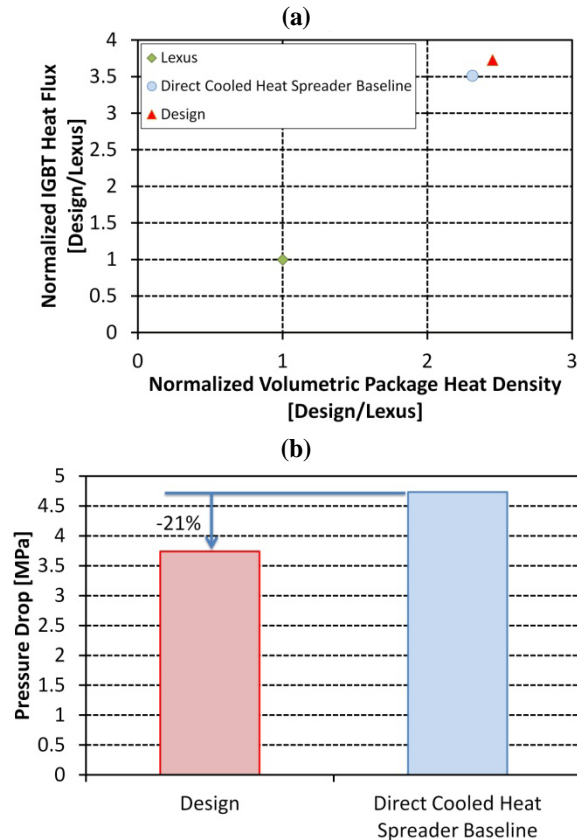


Figure V - 91: Performance comparison of the design assuming one-way flow in series and the direct-cooled heat spreader baseline at the equivalent parasitic power; (a) heat flux and heat density performance, (b) pressure drop.

Conclusion

During FY12, NREL achieved the goal of designing an integrated heat exchanger that met the project objectives. Our work in FY12 focused on the design of an integrated heat exchanger that provided direct cooling to a power semiconductor package. The design was refined through thermal FEA analysis of the heat spreader, CFD analysis of the heat exchanger surface, and combined CFD and thermal analysis of the full integrated system. We placed emphasis on developing an initial prototype that could reduce manufacturing costs. Finally, we initiated work to build the prototype hardware and necessary experimental setup. The model validation work is scheduled to proceed into next year.

In summary, our heat exchanger design improved the power per die area by almost 100% over existing high-performance commercial power electronics thermal

management systems, and it outperformed other more aggressive direct-cooled baseline configurations. The design exceeded the best-in-class power density capabilities, as compared to existing commercial systems. In addition to meeting the hard performance metrics, the prototype design enables a modular or scalable thermal approach to reduce the need for custom heat exchanger redesigns as applications scale in power. The concept was envisioned to eliminate internal fluid seals commonly found on existing integrated cooling concepts to reduce leak-induced failure modes. Finally, the design reduces the parasitic power requirements of the cooling system.

The project is scheduled to proceed into FY13 with an emphasis on experimental results. The initial prototype fabrication will be completed and tested to compare against the modeling expectations. If the prototype hardware matches the design expectations, we will proceed with work to integrate the design with a power electronics package and investigate the potential for other applications.

Acknowledgments

- DOE APEEM Technology Development Managers: Susan Rogers and Steven Boyd
- Co-PI: Jason Lustbader; Team Members: Justin Cousineau and Charlie King

Patents

1. K. Bennion, J. Lustbader, "Integrated Three-Dimensional Module Heat Exchanger for Power Electronics Cooling." Non-provisional patent application filed September 30, 2011.

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V.8 Electric Motor Thermal Management

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Objectives

With the push to reduce component volumes, lower costs, and reduce weight without sacrificing performance or reliability, the challenges associated with thermal management increase for power electronics and electric motors. Thermal management for electric motors will become more important as the automotive industry continues the transition to more electrically dominant vehicle propulsion systems. Thermal constraints place significant limitations on how electric motors ultimately perform, and as thermal management improves, there will be a direct trade-off between motor performance, efficiency, cost, and the sizing of electric motors to operate within the thermal constraints.

The goal of this research project is to characterize the current state of thermal management technologies for electric traction-drive motors and quantify the impact of thermal management on the performance of electric motors. The ultimate goal is to identify areas for improvement and knowledge gaps that would benefit from additional research, leading to focused efforts within the

identified areas. The research objectives are summarized as follows:

- Establish a foundation on which to evaluate potential improvements to electric motor thermal management
- Quantify opportunities for improving cooling technologies for electric motors
- Link thermal improvements to their impact on APEEM targets to prioritize future research
- Increase available information to support thermal management of electric motors in the public domain.

Approach

The approach for FY12, illustrated in Figure V - 92, emphasized three key areas. The passive thermal design refers to the geometrical layout, material selection, and thermal interfaces that affect the heat spreading capabilities within the motor. The cooling technology selection focuses on the convective cooling mechanism that is employed to transfer heat away from the motor through some form of cooling. The cooling mechanism could involve single-phase liquids, air, or two-phase liquids. The emphasis during FY12 was on single-phase liquids, such as transmission oil and water-ethylene glycol mixtures. The combined or integrated thermal performance depends on the interactions between the passive thermal design and the cooling technology selection. For this reason, the third focus area for FY12 looked at the integrated thermal impacts of improvements to the passive thermal design and the cooling technology selection. The work during FY12 built upon previous efforts and results. Past work generated preliminary thermal data for materials and key thermal interfaces within the electric motor. The thermal data were incorporated into a parametric thermal model using finite element analysis (FEA) for a distributed winding motor stator. The model results were compared against experimental data and led to the ultimate objective of completing a sensitivity analysis of the passive thermal design and cooling technologies.

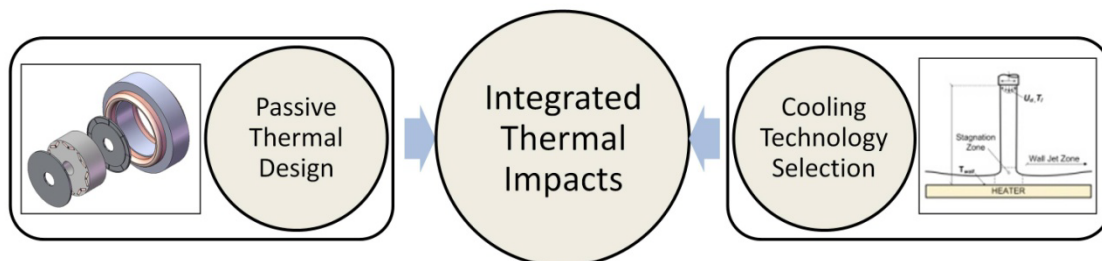


Figure V - 92: Approach.

The work performed during FY12 expanded on the conclusions from the previous stator thermal sensitivity analysis. A second motor configuration with a distributed winding stator and interior permanent magnet (IPM) rotor was selected, and the model was validated against experimental data provided by Oak Ridge National Laboratory (ORNL) through its benchmarking activities. The IPM motor was selected because the winding and core thermal benefits could be applicable to other motor configurations such as induction or switched reluctance motors. In addition, it also included results specific to the rotor and magnets of the IPM motor. A significant cost of the permanent magnets is due to rare-earth materials such as dysprosium to enhance the capability of the magnet to operate at higher temperatures. Improving the cooling of the magnet material has a recognized impact on motor cost and rare-earth materials because it reduces the quantities of dysprosium in the magnet. In addition, NREL continued its partnership with the University of Wisconsin – Madison to investigate the thermal characteristics of a concentrated winding stator motor. In addition to the integrated thermal sensitivity analyses on multiple motor configurations, more experimental and analytical emphasis was put into the areas of passive thermal design and cooling technology selection related to lamination materials, thermal contact resistances, slot windings, oil cooling, and insulation reliability. In summary, the approach for FY12 included:

- Complete thermal sensitivity analysis of second distributed winding motor configuration with distributed winding stator and IPM rotor.
- Complete characterization of initial materials and thermal interfaces to quantify thermal contact resistance between steel laminations in stator and rotor core.
- Complete phase one of collaboration with the University of Wisconsin – Madison to:
 - Develop methods for accurate but fast transient simulation of thermal cycles experienced by electric motors in electric traction drive applications
 - Identify thermal bottlenecks and hot spots that limit performance of electric motors
 - Investigate the thermal characteristics of a concentrated winding stator motor
 - Develop methods for improving the heat spreading inside the electric motor to improve the passive thermal design.

Major Accomplishments

- Completed thermal sensitivity analysis of IPM motor configuration incorporating stator and rotor with

baseline model results validated against experimental data

- Included multiple loss distributions or operating points
- Included heat transfer coefficients, cooling locations, material orthotropic thermal conductivity values, and interface contact resistances
- Demonstrated that improvements to both internal heat spreading within the passive thermal design and improved convective heat transfer can significantly improve the output power capability of electric motors
- Completed bulk thermal conductivity measurements of motor steel lamination materials
- Completed measurements of specific heat for selected lamination materials
- Quantified thermal contact resistance between laminations over a range of stack pressures
- Completed phase one of partnership with the University of Wisconsin – Madison, which covered the following topics
 - Carried out state-of-the-art review of thermal analysis and cooling techniques for motors with an emphasis on electric traction drive applications
 - Developed a computationally efficient technique for segregating and estimating the loss components in IPM motors as a function of the motor's operating point
 - Developed a 3D thermal finite element thermal model for a concentrated winding stator motor configuration and characterized thermal bottlenecks and thermal hot spots
 - Developed a thermal equivalent circuit model for an IPM concentrated winding motor with impedance values that can be conveniently extracted from FEA results
 - Initiated investigation into methods to improve internal heat spreading within the motor.

Future Direction

The current project is scheduled to be completed next year. The emphasis during FY13 will be generating experimental data related to the passive thermal design and cooling technology performance. The object is to develop data that will serve as a baseline for evaluating future motor thermal technology improvements. The efforts in FY13 will include the following

- Oil impingement heat transfer performance and reliability characterization

- Measure jet/spray convective cooling performance
- Measure wire insulation degradation effects of oil impingement
- Thermal interface mitigation strategies
 - Enhance material thermal performance
 - Develop and apply cooling methods to reduce impact of thermal interfaces
- Motor winding thermal improvements
 - Perform experimental tests of winding structures
 - Evaluate alternative wire or winding methods such as twisted wire
- Enhanced internal heat spreading
 - Reduce the rotor thermal bottleneck by improving axial heat flow in the rotor core.



Technical Discussion

The technical discussion in this summary report highlights the approach and results from the motor thermal sensitivity analysis and the material property tests. In addition, NREL partnered with the University of Wisconsin – Madison to support thermal and loss analysis for automotive electric traction drive motors, and a brief summary of the collaborative effort is included below.

University of Wisconsin – Madison Collaboration

The University of Wisconsin – Madison completed phase one of the collaborative effort during FY12. Specific activities completed within the partnership during FY12 include the development of a 3D thermal FEA model for a concentrated winding stator motor and the development of a thermal equivalent circuit (TEC) model of a concentrated winding motor. The model parameters or thermal impedance values were extracted from the FEA results. A comparison between the FEA model results and the lumped parameter TEC model is shown in Figure V - 93. The agreement between the FEA and TEC predictions are good in the machine sections with low spatial temperature gradients. In regions with higher gradients, the TEC provides approximate results between the maximum and minimum component temperatures. Future work for phase two of the collaboration is scheduled to include experimental validation of the thermal modeling work, and investigations into methods to improve internal heat spreading within the motor.

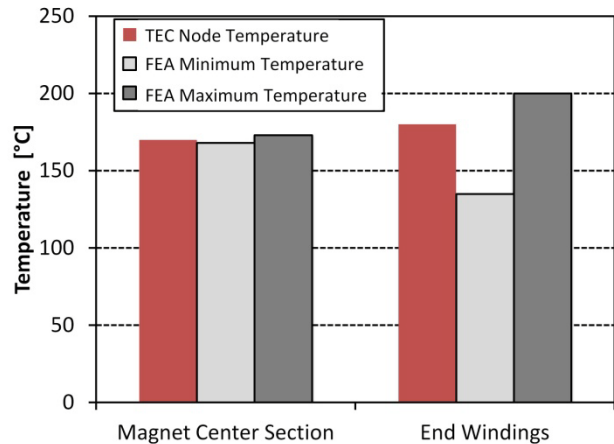


Figure V - 93: Sample of TEC predictions compared to FEA component temperature ranges.

Motor Thermal Sensitivity Analysis

Thermal analysis of electric motors is a challenging task because of the number of design variables that affect heat transfer. A few of the significant challenges include: 1) the variation in potential motor configurations or designs, 2) the heat generation distribution and variation based on operating conditions, and 3) uncertainty in material thermal properties or critical thermal contact interfaces. The selected research approach focused on addressing these challenges. The following results are a summary of work published in 2012 by Bennion and Cousineau [1].

Motor Thermal Sensitivity Analysis Approach

During FY11, a thermal sensitivity analysis was completed for a distributed winding stator, and the analysis was extended to a second motor configuration in FY12 incorporating not only a distributed winding stator but also an IPM rotor. Performing the analysis on a second motor design enabled validation of the modeling approaches and provided insight into common thermal improvements not specific to a single motor design. The variation in heat distribution was incorporated into the analysis by including a range of loss distributions broken down by motor components (windings, stator core, and rotor core). Finally, the material thermal properties used within the models were based on data available in the published literature. Preliminary internally measured thermal property data were used in cases where no published literature was available.

Prior to performing the thermal sensitivity analysis, the results of the baseline thermal FEA models were compared against available test data. Once confidence was established in the motor FEA thermal model, we initiated sensitivity studies to identify areas impacting the overall motor heat transfer. The factors included heat transfer coefficients, cooling locations, material orthotropic thermal conductivity values, heat load distributions, and

interface contact resistances. Due to the large number of parameters, a MATLAB script and graphical user interface (GUI) were created to drive batch runs of ANSYS. The script enabled quick setup and unattended runs of multiple simulations. The program also included the capability to run simulations iteratively to solve for an input parameter that satisfied an output solution target. For example, the program was used to find the heat generation necessary to produce a desired maximum component temperature. The program is summarized in Figure V - 94, showing the ability to interface with not only FEA models in ANSYS Mechanical, but also computational fluid dynamics codes (Fluent) and computer-aided design (CAD) programs.

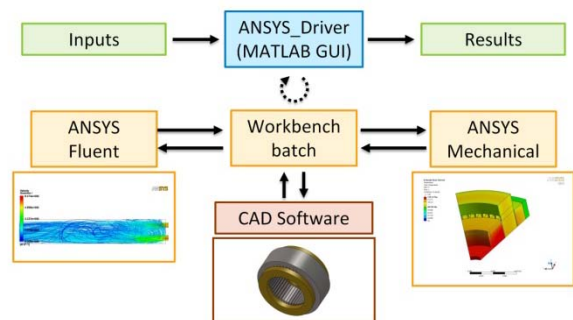


Figure V - 94: Modeling approach and tool development to link multiple simulation design software programs to enable large-scale parametric studies.

The model did not include the individual wires within the slot and end windings. Instead of modeling the individual wires, a similar approach to [2] was used in which a simplified model of the slot and end winding was used with equivalent effective thermal properties. The equivalent thermal conductivity of the slot windings and end windings were determined from analytical estimates and FEA models following and expanding on methods used in [2] and [3]. The material properties applied to the model are summarized in Table V - 6. The listed axial direction is aligned with the rotating axis of the motor, while the angular and radial directions form a plane perpendicular to the motor’s rotating axis. The air gap thermal resistance was estimated from [4], which accounts for variation in motor speed. A fixed value equivalent to the average conductivity over a wide speed range was used in the analysis. Future work could adjust the air gap effective thermal conductivity as a function of motor speed.

Table V - 6: Material thermal properties applied to baseline model.

Material	Thermal Conductivity (W/m-K)	Source
Insulation paper liner	0.144	[2]
Case	230	[5]
Yoke to case thermal contact	1.17	[5]*
Stator: Radial/Angular/Axial	22.2/22.2/2.0	Preliminary Measurements at NREL.
Slot Winding: Radial/Angular/Axial	1.2/1.2/302	Analytical and FEA model approximation
End Winding: Radial/Angular/Axial	0.76/202/102	Analytical approximation
Magnet	7	NeFeB [5]
Rotor Hub	55	Carbon Steel
Rotor End Plate	154	Aluminum Alloy
Air Gap	0.063	Estimated from [4]

* A 1-mm-thick section was used to approximate the equivalent contact resistance because contact resistances cannot be parameterized in ANSYS

The second motor model represented an IPM motor. The model was constructed from information provided by ORNL researchers for the 2007 Camry Hybrid traction motor [6] as part of their benchmarking work supported by the U.S. Department of Energy APEEM Program. The model incorporated both stator and rotor elements. ORNL researchers provided the total losses from their benchmarking work, and the component losses were extracted from the provided data. The copper winding losses were calculated from the root-mean-square (RMS) current and phase resistance provided by ORNL researchers. The reference phase resistance (R1) corresponded to a set reference temperature (T1). To calculate the winding losses, the winding resistance was adjusted to represent the test phase resistance (R2) at the measured test temperature (T2) using Equation (1) below with the coefficient k (temperature constant) equal to 234.5 for copper [7]. The revised estimate for winding resistance was used when calculating the copper winding losses. The core losses were calculated by subtracting the winding losses from the total measured losses. The core losses were further divided among the stator yoke, stator teeth, rotor laminations, and magnets from approximations based on current and speed.

$$R_2 = R_1 \left(\frac{T_2 + k}{T_1 + k} \right) \tag{1}$$

The components of the IPM motor model are shown in Figure V - 95a. The primary additions to the IPM motor over past work included the rotor and additional convection boundary conditions shown in Figure V - 95b to enable cooling from the case, rotor end surfaces, and end windings. The IPM motor model results were compared against the eight different experimental tests

shown in Table V - 7, which were provided by ORNL. The component temperatures resulting from tests 1 and 5 in Table V - 7 were used to estimate the convection boundary conditions for the model, while the other datasets were used for additional model validation. The temperatures within the motor and magnet materials were also compared against other reported results for IPM motors [8].

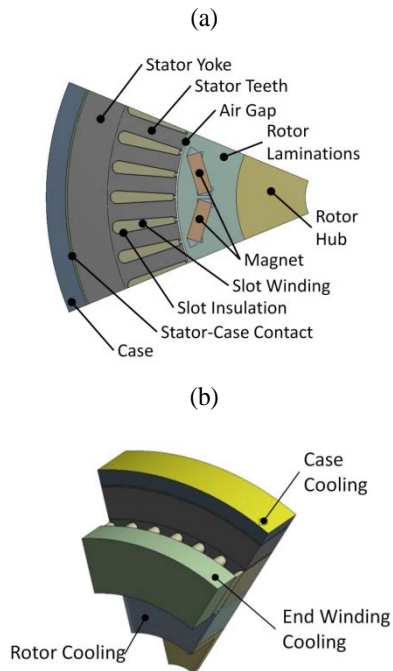


Figure V - 95: (a) Interior permanent magnet thermal model geometry, (b) Convection heat transfer boundary conditions.

Table V - 7: Thermal model validation test data for IPM motor.

Test	Speed (Revolutions per Minute or RPM)	Torque (Nm)	Loss Distribution		
			Winding Loss	Core Loss	
				Stator	Rotor
1	5,000	47.75	13%	78%	9%
2	3,000	106.6	30%	65%	4%
3	3,000	106.6	30%	66%	4%
4	5,000	63.03	17%	75%	9%
5	5,000	63.03	17%	74%	9%
6	7,000	45.70	15%	68%	17%
7	5,000	95.49	24%	68%	8%
8	5,000	95.49	24%	68%	8%

Motor Thermal Sensitivity Analysis Results

Figure V - 96 compares the steady-state FEA thermal model results with the provided experimental data. As seen in Figure V - 96, the shorter duration tests show a larger deviation between the model and experimental results. The larger temperature deviation at shorter test durations is caused by the transient effects in the tests. The shorter duration tests do not allow all of the motor components to reach steady-state temperatures. The temperature deviation

is more pronounced for items with large thermal mass such as the motor case (Figure V - 96b), which take a significant amount of time to reach steady-state temperatures. For this reason the test temperatures for the case were lower than the model results.

Once the model validation was complete, the next step was to perform a sensitivity analysis with FEA of the cooling parameters. Figure V - 97 shows the effect of varying the effective cooling performance applied to the motor. Two different thermal limitations are shown based on a peak winding temperature of 180°C (class H insulation) [7], [9], [10] and a peak magnet temperature of 180°C (neodymium-iron-boron) [7], [9]. The cooling performance is shown in Figure V - 97 as the effective thermal resistance between the cooled motor surface (winding, rotor end surface, and case) and the coolant (water-ethylene glycol and oil). The cooling performance was swept over a large range to see how much heat could be rejected at the listed maximum component temperatures. The vertical band represents the baseline cooling performance applied to the model for the model validation. The primary highlight in Figure V - 97 is the impact of improved cooling or reduced cooling thermal resistance. A significant increase in heat rejection capability is possible before the curves level off as the cooling thermal resistance decreases. The increased heat rejection directly relates to increased power output capability.

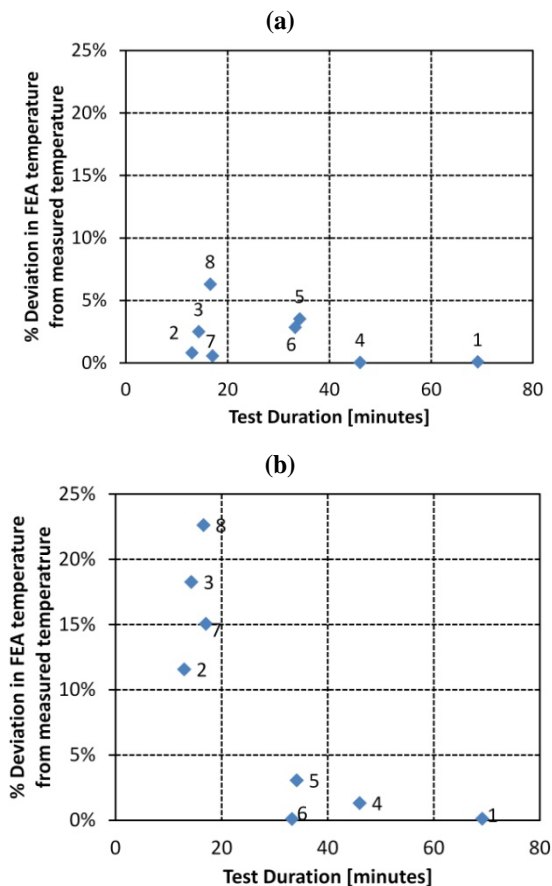


Figure V - 96: IPM motor model comparison against test data showing the model temperature relative to the test temperature, (a) end-winding temperature, (b) case temperature.

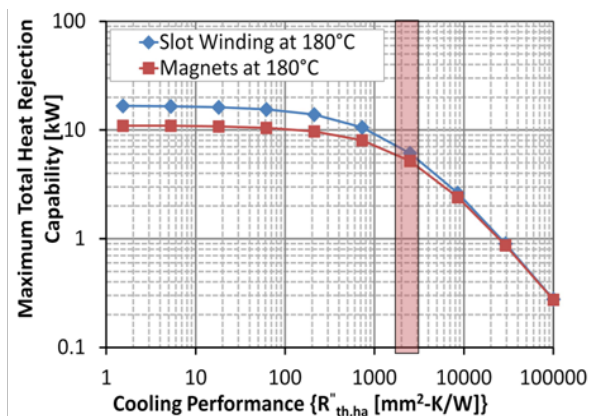


Figure V - 97: Cooling performance sensitivity analysis for the selected IPM motor. The graph shows the total heat that can be removed from the motor versus cooling performance applied to the motor for the maximum component temperature constraints shown. The vertical band represents the baseline cooling performance for the model validation.

Next, a sensitivity study around the material properties was performed on the IPM model. Figure V - 98 summarizes the results of the material sensitivity study.

The figure shows the percent increase in power output (assuming fixed efficiency and temperature constraints) as each of the listed component's thermal conductivity is increased by 20%. Each of the figures compares two operating conditions. The first is a high-speed, low-torque operating point where higher losses are expected within the rotor, as seen in Table V - 7. The second operating point is a low-speed, high-torque operating point where higher losses are expected within the stator. Figure V - 98a compares the results at the baseline cooling condition, while Figure V - 98b provides the same comparison but at a more aggressive cooling condition (lower thermal resistance) where the slope of the curve in Figure V - 97 approaches zero. For the high-speed, low-torque condition, the conductivity properties within the rotor have the most impact, while at the low-speed, high-torque operating condition, the thermal properties associated with the stator in general have more of an effect. The differences between Figure V - 98a and Figure V - 98b emphasize the interactions between cooling performance and the internal heat spreading performance within the motor. If the convective cooling performance improves the effective thermal conductivities within the motor have a larger impact on overall heat removal.

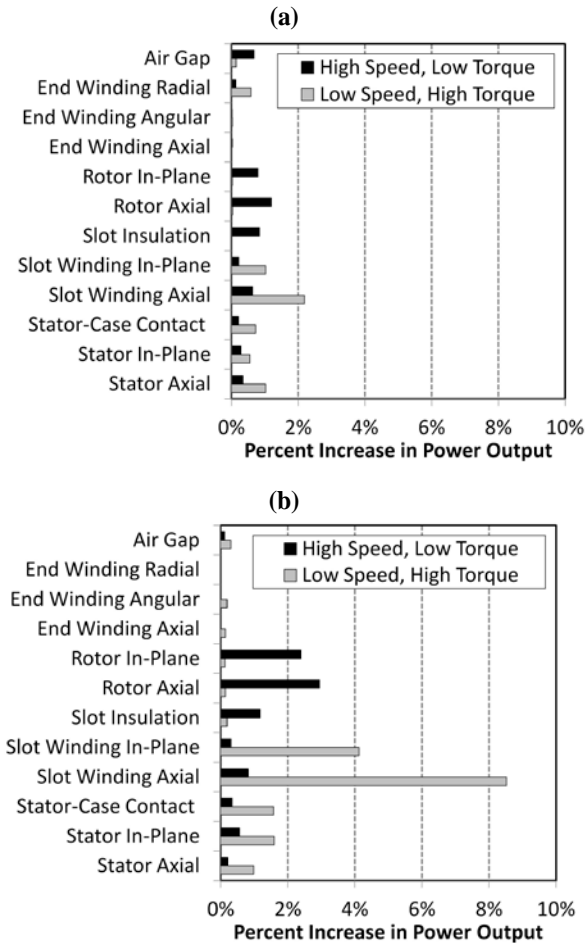


Figure V - 98: IPM model parameter sensitivity analysis for a 20% increase in component thermal conductivity. This impact is measured in terms of increased motor output power. The results compare two heat distributions (high-speed, low-torque and low-speed, high-torque) for two different cooling conditions, (a) baseline cooling condition, (b) aggressive low-thermal-resistance cooling condition.

This study compared how variations in motor cooling parameters affect motor thermal performance. The analysis was performed on multiple permanent magnet configurations to validate modeling assumptions and identify common thermal improvements not specific to a single motor design. Variations in the motor heat load distribution were incorporated into the analysis to account for the impact of different motor operating points causing the loss distribution to change within the motor. Additional thermal parameters in the sensitivity study included heat transfer coefficients, cooling locations, material orthotropic thermal conductivity values, and interface contact resistances. The large number of design factors required the creation of a MATLAB-based graphical user interface that was capable of running unattended simulations to drive batch runs of ANSYS.

The thermal models were validated against available test data for the selected electric motor prior to performing

the thermal sensitivity study. The sensitivity study quantified the impact of thermal improvements within the motor. The results showed that improvements to both internal heat spreading within the motor and convective heat transfer at the solid-fluid interface in the electric motors can significantly improve the output power capability of electric motors. The internal heat spreading within the electric motor is dependent on the thermal conductivity of materials and the internal thermal contact resistances between materials. The impact of improvements depends on the operating conditions of the electric motor. The electric motor for an electric vehicle traction drive system may be expected to operate over a wide torque and speed range. For this reason, improvements in motor thermal management are needed in multiple areas within electric motor traction drive applications.

Identifying the areas of greatest impact provided information on what effective material properties need particular attention in motor thermal models. In addition, the sensitivity study highlighted the potential impact of improved convective heat transfer. The optimal convective heat transfer performance is linked to the internal heat spreading resistance of the electric motor. As convective heat transfer at the solid-liquid interface improves, the effective thermal conductivities within the motor have a larger impact on overall heat removal. The analysis and results from this work identified areas within the motor that could improve thermal performance by reducing internal heat spreading resistance or enable improved convective heat transfer. While the work focused on IPM motors, the results could also support other motor configurations, and a similar analysis approach could be applied to specific motor designs.

Material and Interface Thermal Properties

As illustrated in Figure V - 98, the thermal properties of materials and interfaces within the motor have a significant effect on the heat transfer in electric motors. During FY12 we also completed initial material and thermal interface measurements for the lamination materials. The measurement results support efforts to quantify the thermal contact resistance between lamination materials used in the stator and rotor core. The measured material properties for a range of lamination steels are shown in Figure V - 99 through Figure V - 102. The error bars represent the range of measurement results.

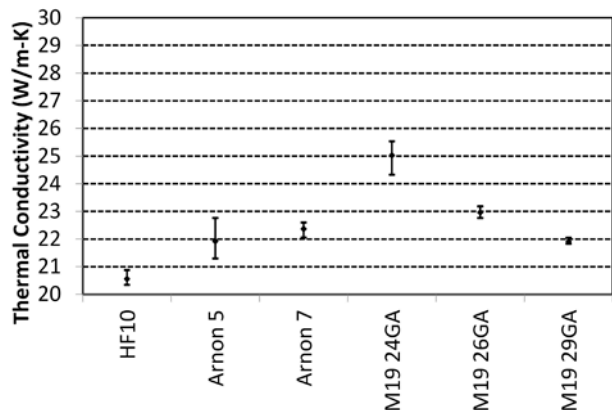


Figure V - 99: Thermal conductivity of the bulk material.

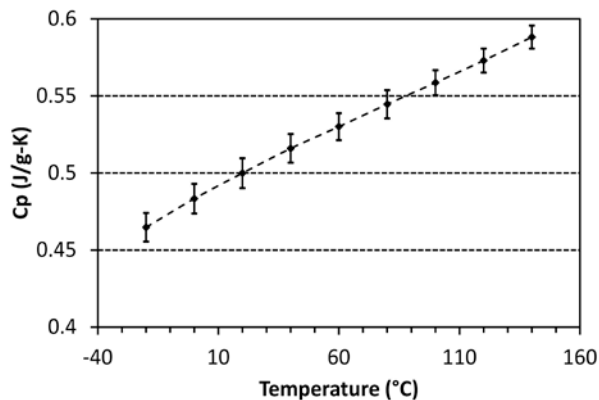


Figure V - 101: Specific heat measurement of Arnon.

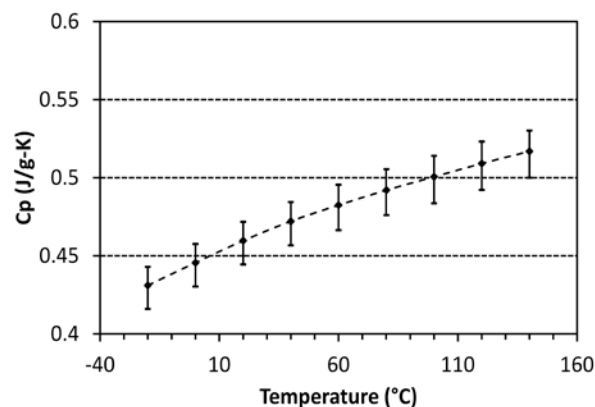


Figure V - 100: Specific heat measurement of M19.

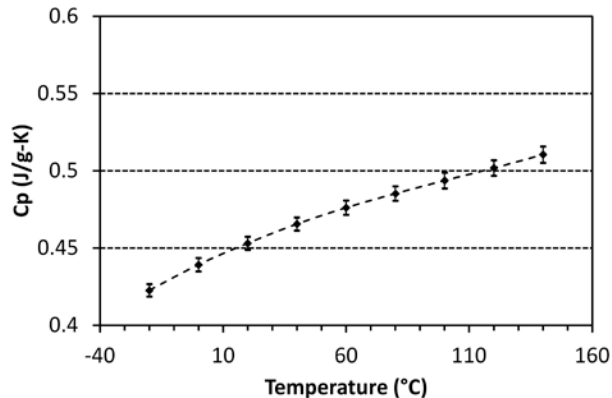


Figure V - 102: Specific heat measurement of HF10.

Figure V - 99 displays the measured bulk material thermal conductivity across a range of material samples. We obtained results for specific materials, and the results agreed with general data available for silicon steels which list the thermal conductivity to be between 20-30 W/m-K [9]. The variability between the tested M19 thicknesses or gauges (GA) is partly expected because M19 is a specific grade, but there may be some variation in the material. Each of the laminations had a C-5 insulation coating.

Figure V - 100 through Figure V - 102 display the measured bulk material specific heat against temperature. The results for each of the M19 gauges are shown in Figure V - 100. The results for the two Arnon materials are shown in Figure V - 101, and the results for the HF10 material are shown in Figure V - 102. The measurement results provide data for specific materials, and the results agreed with general data available for silicon steels, which list the specific heat for silicon steel to be 0.49 J/(g-K) [9].

In addition to the bulk material properties, another critical parameter is the axial or through-stack effective conductivity through the stack of laminations in the stator or rotor. The effective axial conductivity is dominated by the thermal contact resistance between the lamination layers. For this reason the inter lamination thermal contact resistance over a range of pressures was quantified. To quantify the contact resistance between laminations, tests were performed using NREL's ASTM thermal interface material test stand as shown in Figure V - 103a. The test stand provides accurate measurements of thermal interface and contact resistances. As shown in Figure V - 103b and Figure V - 103c, a stack of laminations was placed between the measurement meter blocks, and the effective thermal resistance was measured across the stack of laminations. The process was repeated over a range of stack thicknesses or number of stacked laminations. All of the laminations contained a C-5 insulation coating. The top surface of the top lamination in contact with the meter block had the C-5 insulation coating sanded off, and the bottom surface of the bottom lamination in contact with the meter block also had the C-5 insulation coating sanded off.

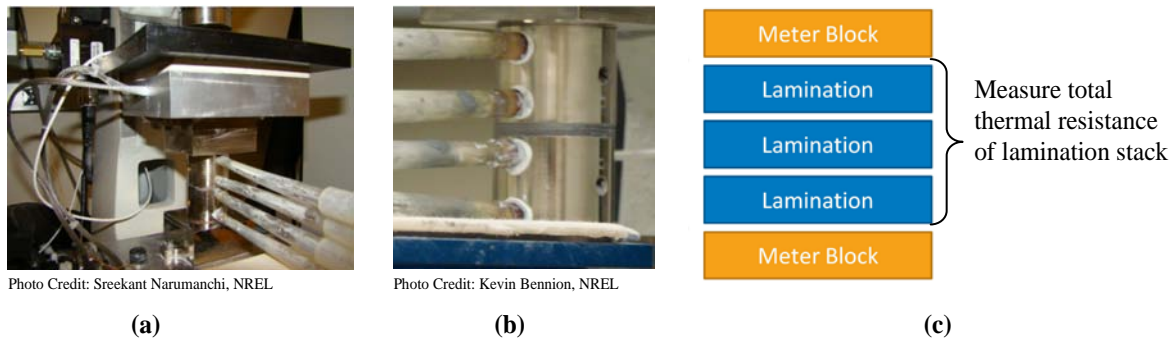


Figure V - 103: Through stack lamination thermal resistance measurement: (a) ASTM interface test stand, (b) lamination stack under test, (c) schematic of stack total thermal resistance measurement.

Using the measurement results of the effective stack thermal resistance over a range of stack heights and combining this with the bulk material data it was possible to quantify the average contact resistance between laminations. The measurements were repeated over a range of pressures to quantify the impact of pressure on the effective contact resistance between laminations. The results for the thermal contact resistance between lamination materials are shown in Figure V - 104. As seen in the figure, most of the data show good agreement between the different materials. The results for the M19 24-gauge material show a slightly higher thermal contact resistance. Future work is necessary to quantify the uncertainty of the thermal contact resistance measurement.

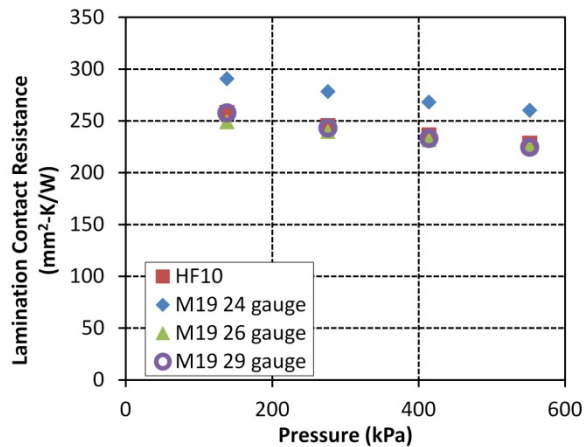


Figure V - 104: Thermal contact resistance between lamination materials with C-5 insulation coating as a function of pressure.

Conclusion

The goal of this research project is to improve thermal management of electric motors to impact the achievable continuous power density. Work during FY12 resulted in analysis results quantifying the sensitivity of passive thermal design parameters and convective cooling on

motor performance. The results not only quantified the impact but also provided guidance on future research priorities to enable enhanced motor performance through improved thermal management. With the emphasis on reducing or eliminating rare-earth materials such as dysprosium, increasing motor speed, or increasing motor stack length, the impact of thermal management increases. The thermal sensitivity analysis was completed on multiple motor configurations in collaboration with the University of Wisconsin – Madison. Applying the analysis to multiple motor configurations provided results that could be broadly applied to a range of motor configurations with or without permanent magnet or rare-earth materials.

In addition to the thermal sensitivity analysis, work was completed in FY12 to complete testing on the thermal properties of lamination materials and measurements of the thermal contact resistance between lamination materials as a function of pressure. The contact resistance between lamination materials significantly reduces the effective thermal conductivity of the stator or rotor core in the axial direction. The results not only support motor thermal modeling efforts, but the results also provide baseline data when comparing the impact of potential improvements to the internal heat spreading or the passive thermal design of the motor.

Future work will build on work started in FY12 to transition from modeling and analysis to an experimental emphasis using thermal test capabilities at NREL. Work in FY13 will involve development of baseline data from fundamental heat transfer experiments with oil jets, which builds on NREL’s previously developed experimental and analytical capabilities for jet cooling as applied to power electronics. The experimental capabilities will also enable investigating concerns associated with wire insulation degradation effects of oil impingement. In addition to using NREL’s thermal experimental capabilities for oil impingement characterization, work will also utilize NREL’s ASTM thermal test stand to perform tests of slot winding structures to obtain baseline data and evaluate

alternative slot winding methods and materials. Despite the emphasis on experimental data in FY13, analytical work will continue to investigate strategies to mitigate the impact of thermal interfaces within motors and enhance the passive thermal design or internal heat spreading within the motor.

Publications

1. K. Bennion and J. Cousineau, "Sensitivity Analysis of Traction Drive Motor Cooling," in *2012 IEEE Transportation Electrification Conference and Expo (ITEC)*, 2012, pp. 1–6.

Acknowledgments

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- Tim Burress (Oak Ridge National Laboratory)

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VI. Small Business Innovation Research Grants (SBIR)

VI.1 Small Business Innovative Research (SBIR) Projects

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Objectives

- Use the resources available through the Small Business Innovation Research (SBIR) and Small Business Technology Transfer (STTR) programs to conduct research and development of technologies that can benefit the Advanced Power Electronics and Electric Motors (APEEM) effort within the Vehicle Technologies Program.
- Achieve the four SBIR objectives: (1) to stimulate technological innovation; (2) to increase private sector commercialization of innovations; (3) to use small business to meet federal research and development needs; and (4) to foster and encourage participation by minority and disadvantaged persons in technological innovation.

Approach

- The Small Business Innovation Research (SBIR) program was created in 1982 through the Small Business Innovation Development Act. Eleven federal departments participate in the SBIR program and five departments participate in the STTR program, awarding a total of \$2billion to small high-tech businesses.
- A 1982 study found that small businesses had 2.5 times as many innovations per employee as large businesses, while large businesses were nearly three times as likely to receive government assistance. As a result, the SBIR Program was established to provide funding to stimulate technological innovation in small businesses to meet federal agency research and development needs. After more than a decade, the STTR program was launched. The major difference is that STTR projects must involve substantial (at least 30%) cooperative research collaboration between the small business and a non-profit research institution.

- Small Business Innovation Research (SBIR) and Small Business Technology Transfer (STTR) are U.S. Government programs in which federal agencies with large research and development (R&D) budgets set aside a small fraction of their funding for competitions among small businesses only. Small businesses that win awards in these programs keep the rights to any technology developed and are encouraged to commercialize the technology.
- Each year, DOE issues a solicitation inviting small businesses to apply for SBIR/STTR Phase I grants. It contains technical topics in such research areas as energy production (Fossil, Nuclear, Renewable, and Fusion Energy), Energy Use (in buildings, vehicles, and industry), fundamental energy sciences (materials, life, environmental, and computational sciences, and nuclear and high energy physics), Environmental Management, and Nuclear Nonproliferation. Grant applications submitted by small businesses MUST respond to a specific topic and subtopic during an open solicitation.
- SBIR and STTR have three distinct phases. Phase I explores the feasibility of innovative concepts with typical awards up to \$150,000 for 9 months. Only Phase I award winners may compete for Phase II, the principal R&D effort, with awards up to \$1,000,000 over a two-year period. There is also a Phase III, in which non-Federal capital is used by the small business to pursue commercial applications of the R&D. Also under Phase III, Federal agencies may award non-SBIR/STTR-funded, follow-on grants or contracts for products or processes that meet the mission needs of those agencies, or for further R&D.

Phase I Topics for 2012

Under the SBIR/STTR process, companies with Phase I awards from FY 2012 are eligible to apply for a Phase II award in FY 2013. The FY 2012 Phase I subtopic summaries are below:

Release 2

Power electronic inverters and converters are essential for electric drive vehicle operation, and currently add significant cost to these vehicles, therefore limiting their commercialization potential. Improvements in their performance can lead to cost reduction or better utilization

of their capabilities in vehicles, as outlined in the U.S. DRIVE partnership Electrical and Electronics Technical Team Roadmap.

Grant applications are sought to develop subcomponent-level improvements to power electronic inverters or converters which would support commercialization of micro, mild, and full HEVs, PHEVs, and EVs. Some specific improvements which are of interest include: small, lightweight low loss magnetic materials for passive inductors; low cost, high-temperature capable packaging materials for power semiconductor modules; improved direct-bond copper materials; and improved die attachment methods.

Release 3

New materials for automotive traction drive motor laminations, cores, or structures that could achieve significant cost savings and contribute to achieving the DOE motor cost target of \$4.7/kW in 2020 are needed. Applications should propose specific material innovations in one of these three areas and address how they can lead to reduced costs with respect to currently available materials.

Phase I Awards Made in 2012

Five Phase I awards were made in FY 2012 and resulted in the following projects:

Low-Cost Integrated Package and Heat Sink for High-Temperature Power Modules

Advanced Thermal Technologies LLC
Dr. James Connell, jconnell@charter.net

Project Summary:

The proposed packaging and heat sink technology will support increased heat dissipation that will lead to improved efficiency and reliability for HEV power conversion systems as well as a range of other industrial and commercial power electronics systems. The technology will support enabling packaging solutions for more efficient next generation semiconductor materials that will provide benefits to society in the form of more efficient products that consume less energy and contribute to improved environmental quality by reducing greenhouse gas emissions.

Statement of the Problem:

There is a growing demand for power electronics that can operate under the high temperature and high power conditions that will be encountered in Hybrid Electric Vehicles (HEVs). As the coolant temperature used to dissipate heat from electronics increases, the operation of power semiconductor devices becomes severely limited in

order that the safe operating temperature limit of the semiconductors not be exceeded. There is a need for low-cost, high efficiency heat sink technology to support next generation high power, high reliability HEV power modules.

How this Problem is Being Addressed:

The proposed project is focused on the development of a novel, low-cost integrated package and heat sink assembly for use in high-temperature power module packaging and thermal management. This integrated package and heat sink is enabled by a unique integrated ceramic-graphite-copper composite material technology and a highly effective compact heat transfer technology. The integrated assembly provides for electrical isolation of the power module's electronic components and circuitry, and minimizes the thermal resistance between the power semiconductor devices and the heat sink coolant. Further, the assembly provides for the minimization of the coefficient of thermal expansion (CTE) mismatch between the different material layers of the assembly in order to minimize thermal stresses resulting from cyclic power and temperature operation – key to achieving a reliable product with a long life. The primary research objectives of this project are the development of a low-cost unique integrated package and heat sink assembly and the establishment of the fabrication processes required to support its manufacture. There is a critical need for advanced packaging and active cooling solutions capable of meeting the thermal management requirements of emerging power module applications which include: (1) hybrid electric vehicle (HEV) power inverters and converters; (2) power converters for renewable energy systems (e.g., solar arrays, wind generators); and (3) power supplies for a wide variety of electronic systems (DC power supplies and inverters).

Commercial Applications and Other Benefits:

The unique integrated package and heat sink technology will provide lower thermal resistance and thus enable thermal management solutions that improve the operating range and efficiency for a wide variety of power electronic systems. The commercial applications of the proposed package and heat sink technology include silicon-based and silicon carbide-based power modules; RF power amplifiers used in communication systems; high brightness light emitting diodes used in solid state lighting and power electronics for harsh environment operation.

High Performance Thermal Packaging Substrate

Applied Nanotech Inc.

Dr. James Novak, jnovak@appliednanotech.net

Project Summary:

Thermal management is a critical part of hybrid electric vehicle technology and in particular represent a difficult and costly area for power electronics production. The proposed research will exploit recent advances in nanotechnology to provide increased thermal and electrical conductivity for power electronic materials by develop CarbAI™-based advanced dielectric thermal management materials. The proposed solution has application for increasing lifetime and reliability in all power electronic devices including solid-state lighting (LEDs) and displays.

Statement of the Problem:

Thermal Transfer is a critical part of power electronics application. Power electronics are being utilized with greater frequency in today's modern world. The power electronics market segments include high current carrying semiconductor devices such as IGBTs, MOSFETs, power transistors, and modules. These devices require high performance thermal management materials both in the packaging of the discrete devices as well as for the packaging of modules consisting of several or arrays of these devices. The market for power electronic thermal management products is projected to be \$3.0B by 2015 with a compound annual growth rate (CAGR) of 1.6%.

How this Problem is Being Addressed:

The overall objective of this program (Phase I and Phase II) was to develop CarbAI-based advanced dielectric thermal management substrates for HEV power electronic and packaging applications, leading to better automotive performance and ecology economy.

The proposed Phase I program is a continuation of the materials development completed internally at ANI. Choosing a polymer dielectric coating with the proper specifications provides ease of manufacture and eliminates two thermal interfaces compared to a bonded inorganic plate. We also have increased control over material thickness and superior thermal performance while continuing to meet our targets for dielectric voltage breakdown.

The Phase I will focus on die attachment to the novel thermal management substrates. After initial substrate fabrication the samples will be screened for thermal management and electrical performance. After suitable materials and procedures are identified test boards for an Hybrid Electric Vehicle (HEV) power electronics module will be fabricated and sent to a major automotive manufacturer for testing.

Commercial Applications and Other Benefits:

If successful, the technology developed through this project will provide an accurate, robust, reliable and cost effective method for increasing the thermal capacity of power electronic devices. There is a critical and growing market need for this technology in hybrid electric vehicles as well as solid state lighting applications. The SBIR project team will share results of this program with commercial companies to accelerate commercialization of the technology in a marketable product form. While this program will not be the single solution, it will assist in the reduction of American and global energy consumption.

Hybrid Electric Vehicles (HEVs) utilize a high efficiency internal combustion engines to drive electronic generators. HEV technology can be used for automobiles, trucks, rail and ship materials. The generators charge battery systems that provide propulsion through electric drive motors. The electronics that control power delivery between the battery and the drive motor generate a large amount of heat. This heat can cause problems with the reliability of the electronic components. The growth rate for hybrid vehicle technologies in the U.S. has grown 3700% in the past 10 years.² This represents one of the single largest growing forms of alternative transportation. In fact, Global automakers have produced nearly 12 new models in the past two years alone (2008-2009). This represents tremendous opportunity for market penetration of new technology related to the hybrid gas/electric propulsion systems. This vehicle data is just part of the growing trend for the application of power electronics.

High Performance Low-Cost IGBT Power Module Thermal Management for HEV/EV Applications

Metal Matrix Cast Composites LLC

Dr. James Cornie, jcornie@mmccinc.com

Project Summary:

This project will provide a low cost high performance power module packaging solution for advanced HEVs/EVs "green" automobiles buses trucks construction mining traction vehicles and military armored vehicles and trucks. Enhanced power module technologies will increase fuel efficiency and reduce the cost of HEV/EV for the consumer.

Statement of the Problem:

This proposal addresses a critical need to develop low cost packaging solutions to reduce size, weight, and increase performance in hybrid electric vehicle (HEV) and electric vehicle (EV) motor drive power electronics. IGBT (integrated gate bipolar transistor) and inverter/converter devices for HEV/EV's currently use silicon as the primary switching element where junction temperatures cannot exceed ~150C. Power modules operating in the harsh

environment of an engine compartment must maintain acceptable junction temperatures and require large actively cooled heat sinks which add significant cost and weight to vehicles.

How this Problem is Being Addressed:

MMCC proposes to advance IGBT power module packaging technology by demonstrating that Al₂O₃ and AlN dielectric substrates can be in-situ cast into lightweight CTE (coefficient of thermal expansion) matched copper graphite composite heat sinks together with the copper metallization layer that effectively becomes a direct bonded copper process (DBC). In addition to providing a low cost net shape casting, the proposed process will feature: 1) a CTE matched high thermal conductivity (2x that of current materials) copper graphite composite base plate; 2) capture a ceramic dielectric substrate, effectively creating a DBC dielectric and eliminating a high thermal impedance interface as well as a manufacturing process step; 3) capture cast-in cooling channels during pressure infiltration casting, thus eliminating a second high thermal impedance interface layer and providing for high efficiency cooling, and finally as an option, 4) enable the migration from Si to SiC IGBT semiconductors which can accommodate higher power and junction temperatures.

Commercial Applications and Other Benefits:

The proposed technology will be applied to hybrid electrical vehicles, plug-in hybrid electric vehicles and electrical powered vehicles as well as traction and utility vehicles. Other applications could be for RF power amplifiers for the telecommunications industry as well as advanced microwave and radar applications. This technology will increase the cooling capacity and enable the migration from Si to higher power capacity SiC and GaN semiconductors.

High Coercivity, High Energy Product Nd-Fe-B Magnets with Less or No Dysprosium

Electron Energy Corporation
Dr. Melania Marinescu, mmarinescu@electronenergy.com

Project Summary:

To mitigate the rare earth supply chain vulnerability and reduced availability of dysprosium in the earth crust, Electron Energy Corporation will employ new technologies to develop dysprosium-free and, alternatively, dysprosium-lean "Neo" magnets for high-performance motors and generators. These magnets will have immediate implementation, without the need of machine structural changes.

Statement of the Problem:

High performance motors, like those in hybrid electric vehicles, use high performance Nd-Fe-B magnets that contain up to 12 wt% of dysprosium (Dy) in order to increase the coercivity, and avoid demagnetization at elevated temperatures. However, the global rare earth elements (Nd, Dy, etc) supply chain risk combined with predicted supply shortages for dysprosium which DOE has deemed critical has become a grave concern for the healthy development of all green technologies operating with permanent magnets. Recently, efforts have been directed towards new designs of permanent magnet motors which allow the use of lower energy product magnets, or the use of induction motors; however, they have resulted in lower performances compared to rare earth permanent magnet motors, and will have critical implementation problems.

How this Problem is Being Addressed:

The proposed project will develop a methodology for the production of high-performance, high-coercivity Nd-Fe-B permanent magnets with less or no dysprosium, based on (i) control of Dy atoms distribution at grain boundaries through a newly discovered phenomenon beyond the current research on "grain boundary diffusion" concept, in order to minimize their usage in Nd-Dy-Fe-B magnets and (ii) microstructure engineering aimed at grain size refinement and new methods for intergranular phase control in Dy-free Nd-Fe-B magnets. The proposed technologies will demonstrate 30% higher coercivity values for magnets with Dy contents equivalent to those of their current commercial counterparts (i.e., the new Dy-free magnets will have 30% higher coercivity than existing ones). Correspondingly, the amount of Dy needed to reach a higher level of coercivity will be decreased by 30% in the new Dy-lean Nd-Fe-B magnets. Moreover, a reduced or eliminated Dy content will lead to a higher maximum energy product for these magnets throughout their entire operating temperature range.

Commercial Applications and Other Benefits:

The cost of the magnets to be developed with the proposed technologies is expected to be reduced substantially compared to the price of the current commercial counterparts with the same level of coercivity.

Computational Design and Development of Low Cost, High Strength, Low Loss Soft Magnetic Materials for Traction Drive Motor Applications

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Project Summary:

This project will design and develop low cost, high strength, low core loss soft magnetic core materials at the prototype scale that show promise to provide cost savings in traction drive motor applications.

Statement of the Problem:

QuesTek proposes to apply its Materials By Design® approach to design a high performance, low cost soft magnetic material capable of achieving significant cost savings to approach the DOE motor cost target of \$4.7/kW in 2020. In order to meet the ambitious motor targets, traction motors in electric vehicles (EV) must become even more compact, light-weight, and highly efficient. For a compact design, EV motors must operate at high speed, which in turn places the rotor under high mechanical stresses. Materials used for rotor cores thus require high strength in order to withstand the centrifugal forces generated during high speed revolution. Additionally, motors operating at high frequencies must demonstrate low core losses as well as high strength because core losses increase exponentially with increasing frequency. The conflicting microstructures required for high strength and low electrical losses makes the simultaneous achievement of high strength, low loss soft magnetic materials very difficult.

How this Problem is Being Addressed:

The idea of this Phase I is to design and develop a high strength, low cost soft magnetic Fe-Si alloy by utilizing strengthening precipitates that are designed to be small enough not to significantly impede the motion of the domain walls, but of the desired length scale to impede dislocation motion to increase mechanical strength. A material that could satisfy both the high yield strength requirements for the rotor of higher speed EV motors and the low core losses, which are important for the stator during high frequency operation of the motor, would lead to significant cost savings to help achieve the DOE motor cost targets.

One of the critical limitations in the design of the high speed interior permanent magnet (IPM) motors used in current hybrid electric vehicles is the mechanical strength of the rotor. Thus, there is a pressing need for a high strength, low cost, low core loss, and easily processable soft magnetic alloy for use in the rotor core of EV electric motors. The design of a high performance electrical steel

sheet for the core of the motor plays a large role in the traction performance and fuel efficiency of an EV. Electrical steels used in rotor cores require high strength without sacrificing magnetic properties to contribute significant cost savings to meet the DOE motor cost targets. QuesTek will utilize its systematic and integrated computational materials engineering (ICME) approach to design and develop a low cost, high strength, low core loss soft magnetic alloy that will enable a more compact, lighter motor for significant cost savings.

Commercial Applications and Other Benefits:

QuesTek's proposed Fe-Si soft magnetic alloy material development efforts will leverage our previous development efforts on Fe-Co soft magnetic alloys. Our previous experience designing precipitation strengthened Fe-Co soft magnetic materials and mapping out the processing steps to form thin-rolled sheets, which are assembled and stacked into laminates will be extremely valuable in the development of high strength, low loss Fe-Si alloys. With this background, QuesTek will explore alloy design concepts that may focus on incorporating nano-scale precipitates (<10 nm diameter), maximizing resistivity, controlling grain size, and controlling grain texture. QuesTek will utilize its expertise in computational materials design and in-house models to design both the alloy composition and processing steps to create the structure that delivers the desired mechanical and magnetic properties. Utilizing a computational materials design approach, QuesTek is prepared to design and develop low cost, high strength, low core loss soft magnetic core materials at the prototype scale that show promise to provide cost savings in traction drive motor applications.

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