Final Scientific Report for DOE/EERE

Project Title: "High efficiency (> 20%) heterojunction solar cell on 30µm thin crystalline Si substrates using a novel exfoliation technology"

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Cost-Sharing Partners: N/A

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I. Executive Summary

To achieve grid parity, photovoltaic (PV) technologies must reduce the production cost of PV modules to well below $0.50/Wp (peak Watt of power produced). In crystalline Si PV modules, which account for over 80% of all the PV modules in production world-wide, the cost of raw Si wafers is over 40% of the module cost. Therefore, there is an industry wide effort to reduce crystalline Si wafer thickness and improve efficiency. However, conventional wafer sawing technologies suffer from significant kerf losses and also are limited due to constraints on handling of free standing wafers that are thinner than 150µm. .

This project aims to develop low cost high efficiency crystalline Si solar cells using ultra thin (~ 30µm) layers of monocrystalline Silicon fabricated using a metal backed exfoliation technology. These exfoliated Si foils are backed by metal and rugged and flexible, which help in overcoming the yield losses and handling issues that are a problem for traditional thin Si wafers. The metal backing of the exfoliated foils poses new challenges in processing of such thin wafers and limits the temperature of processing to below 300C.

The project develops further understanding of thin crystalline Si based cell architectures and potential processing issues involved in making high efficiency cells with metal backed monocrystalline Si foils. A 13.5% efficiency cell was demonstrated during this project and the individual components of surface passivation (Voc) and fill factor needed to obtain higher efficiency (16%) have also been shown. It is believed that with some changes to the cell manufacturing process and access to industrial quality passivation films, should enable high efficiency cells with this technology. The cost model indicates that with high efficiency cells in volume production, this technology can meet the Sunshot goals of < $0.50/Wp for PV module production.

This project was run as a collaboration between AstroWatt, University of Texas, Austin, National Renewable Energy Laboratories, University of Florida, Gainesville and Georgia Institute of Technology with additional contributions from Institute for Energy Conversion, Delaware. The project has resulted in several conference publications and presentations during 2012.

II. Comparison of Actual Accomplishments with Goals and Objectives:

The following table provides a summary of accomplishments during the project on each of the goals set at the beginning of the project.

Task #	Description	Goal	Accomplishment
I.1	Develop optimal BSF and rear heterojunction structure for cells	Voc > 0.65V on thin exfoliated cells	Demonstrated Voc of 0.662V
I.2.1.1	Demonstrate optimal handling of thin exfoliated cells	Demonstrate functional 3” x 3” exfoliated cells	3” x 3” functional thin exfoliated cells were demonstrated
I.2.1.2	Develop device model for cell performance projection	Model of exfoliated cell performance	Model developed and presented
I.2.1.3	Metallization Optimization	Demonstrate repatable fill factor > 75%.	Repeatable fill factor > 75% demonstrated with improvements in process.
I.2.2	Demonstrate 16% efficiency exfoliated cell	Completed exfoliated cell with 16% efficiency	13.5% champion exfoliated cell demonstrated.

III. Technical Narrative:

Project Objective: This project seeks to fabricate high efficiency (> 20%) solar cells on 30µm thin monocrystalline Si substrates using a novel Semiconductor on Metal (SOM®) exfoliation technology. Specifically, this project will develop robust processes for (a) making 30µm thin c-Si film backed by a metal foil (b) forming an optimal light trapping structure to enable high J_{SC} (> 36mA/cm^2) in the SOM cells (c) optimal surface passivation of the SOM substrates to enable high V_{OC} (> 0.72V) and (d) optimal metallization of the front and back contacts and screen printing on SOM substrates to enable high fill factors (> 78%).

Background: In solar cells using crystalline Si (c-Si) wafers, which account for over 80% of all the PV modules in production, the cost of raw Si wafers is over 40% of the module cost. There is an industry wide push to reduce the active Si content of the cell through a combination of thinner wafers and increased cell efficiency. However, cell manufacturers are struggling to reduce the wafer thickness below 150µm as there are no economically viable technologies for manufacturing very thin Si wafers and such thin silicon wafers impose stringent handling requirements as wafer breakage and yield loss impact final module cost

We have demonstrated a kerfless exfoliation process to fabricate 20-40µm thin monocrystalline Si substrates backed by metal. These exfoliated Si foils are rugged and flexible which help in overcoming the yield losses and handling issues that are a problem for traditional thin Si wafers. Previously, we demonstrated a 12.5% efficient cell with a locally diffused back surface field and an amorphous Si based front heterojunction. This device architecture takes advantage of the higher V_{OC} enabled by thin Si. Our device simulations indicate that peak cell efficiencies can be obtained when the crystalline Si wafer thickness is in the 20-50µm regime. With surface passivation in the range of 10 cm/sec and with optimal internal light reflection, it is expected that the 25µm SOM cell will reach an efficiency of 21%. The kerfless exfoliation technique dramatically reduces the amount of Si consumed in fabricating the cell. This together with the proposed low cost process flow can reduce the final module cost to below $0.50/Wp.

Two different cell architectures are explored in this project. In both architectures, the light facing side has a a-Si based heterojunction emitter and Indium Tin Oxide transparent conductor for light absorption and carrier collection, fabricated at UT-Austin. The rear side junction is different for the two architectures. In one case, a diffused Phosphorous doped back surface field structure fabricated at Georgia Tech was used on the rear side and in the other case a rear side heterojunction deposited at either NREL or one of our industrial partners was used. The rear side processing is completed when the Si is still in wafer form. After the rear side processing is complete, a metal is deposited on the rear of the wafer and a 30um thick Si layer including the rear side junction is exfoliated from the rear of the wafer. The thin exfoliated Si is then processed into a complete solar cell using front side heterojunction stack deposition.

Significant Accomplishments During This Project:

Task I.1: Develop optimal local BSF and rear heterojunction structure for high efficiency SOM cell: A BSF structure using a phosphorous doping process and nitride passivation has been developed at Georgia Institute of Technology. Wafers with this doping and passivation have been exfoliated to form the rear BSF of SOM cells. The nitride passivation can act as an etch barrier as well as phosphorous diffusion barrier as needed for forming a local BSF structure and provide a backside SRV of ~ 10 cm/s (Fig. 1.) This structure has been exfoliated to produce 13.5% efficient cells.

Exfoliated cells with rear heterojunction structures have been fabricated and we have obtained Voc > 0.65V with cells fabricated at UT, NREL and IEC. The amorphous Si films from NREL and IEC were evaluated on test wafers to verify passivation quality. Float zone high lifetime wafers passivated with films from both NREL and IEC show implied Voc > 700 mV and effective lifetime of > 1msec. Dual heterojunction cells fabricated with front side heterojunction deposited at UT-Austin, NREL and IEC show Voc > 0.65V (as shown in Fig. 2).

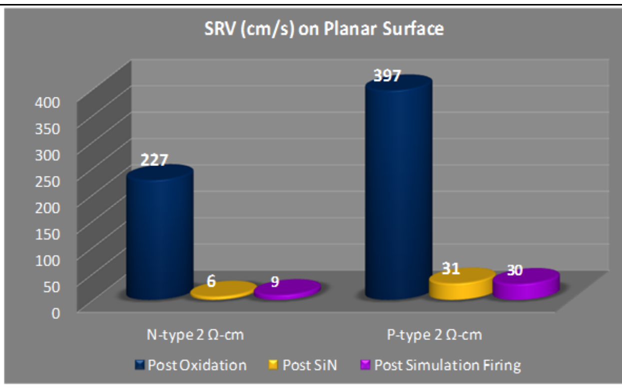

Fig. 1: Measured SRV at different stages of cell process on N & P type planar wafers with SiN passivation on both surfaces

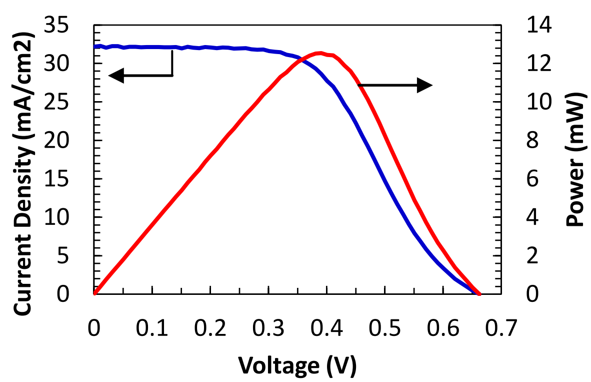

Fig. 2: Measured I-V plot on a 1cm x 1cm area cell formed on an exfoliated foil with industrial quality rear heterojunction and RPCVD front heterojunction.

Task I.2.1.1: Demonstrate optimal handling to enable processing of foils through wet cleans, vacuum deposition processes and screen printing:
Functional 3" x 3" cells have been fabricated to verify that there are no shunts across large area exfoliated cells and also to demonstrate that such large area cells can be handled and processed through standard solar cell processes such as wet cleans, heterojunction deposition and screen printing (Fig.3). We have evaluated a few different options – magnetic holders, mechanical clamps, vacuum chucks and adhesives - to process curled exfoliated foils through wet cleans, film deposition and screen printing. Mechanical holders coated with inert materials are the best choice for processing the foils. We have successfully processed several foils as large as 5-inch pseudosquare through the each of the wet cleans, film deposition and screen printing steps using the mechanical clamp holders. We have used metal holders which have

been coated with an inert material as well as uncoated glass/teflon holders to process exfoliated foils. The design allows for industrial scale batch processing of multiple foils in trays to mimic current wafer level processing on industry standard tool sets.

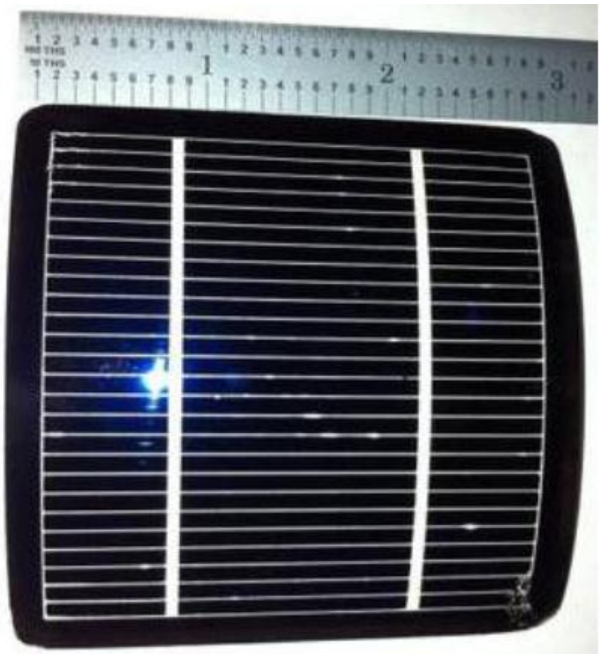

Figure 3. Picture of completed 3" x 3" exfoliated cell

Task I.2.1.2: Develop a model for optimal process based design and cell performance projection:

2-D numerical simulations were setup and carried out in FLOODS under AM1 (92.5mW/cm^2) sunlight to define the optimal cell design and to project the ultimate one-sun performance. These simulations have identified optimum BSF design and local back contact pitch to improve V_{OC} for a range of different back surface passivations. The model predicts an intrinsic cell efficiency of greater than 20% with 25µm thin Si if bulk lifetime is greater than 160µs assuming a surface passivation of ~ 10cm/sec (Fig. 4). The simulated BSF design will be implemented on bulk wafer and exfoliated SOM cells in the second phase of this DOE Sunshot project. This work formed a critical chapter in the dissertation work for a Ph.D. student from University of Florida and has also been published at the IEEE PhotoVoltaics Conference this year in Austin, TX.

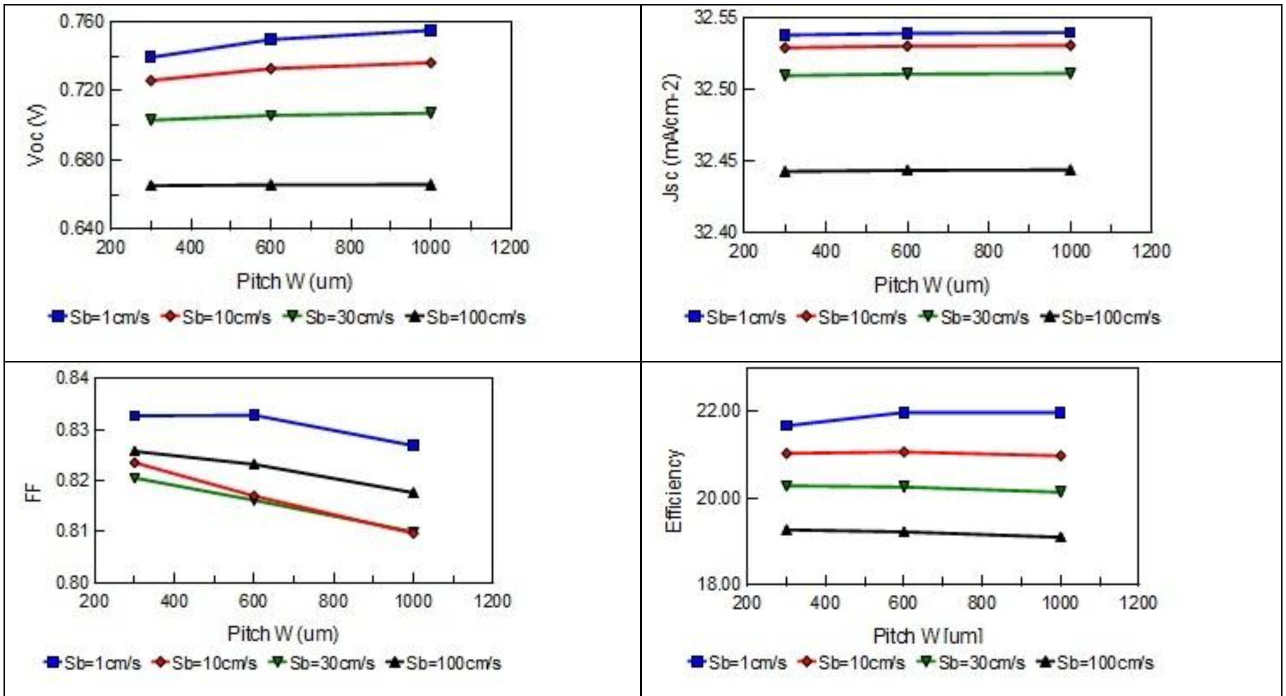

Figure 4: FLOODS predicted local BSF cell performance versus pitch and S_b; with τ_p=1ms, t_{Si}=25µm, back N_s=3e20.cm^{-3},contact width w_m=2µm, no internal reflection at AM1(92.5mW/cm^2) sunlight.

Task I.2.1.3: ITO optimization and metallization improvement to demonstrate fill factor > 75%:

The ITO process has been improved at UT-Austin by monitoring the target aging and use conditions and controlling the chamber condition prior to ITO deposition. In addition the screen printing process has also been improved with new screens and better alignment between the screen and the cell. Figure 5 shows a chart of fill factors obtained on a set of wafers run through the improved ITO and screen printing process. As seen in the chart, FF > 75% have been consistently obtained on wafers. On exfoliated cells, champion fill factor of 76% has been obtained with typical fill factors in the 60-75% range. The wider range of fill factors on exfoliated cells is believed to be due to a combination of (a) non-optimal cleans before a-Si deposition (b) non-optimal a-Si films on exfoliated cells.

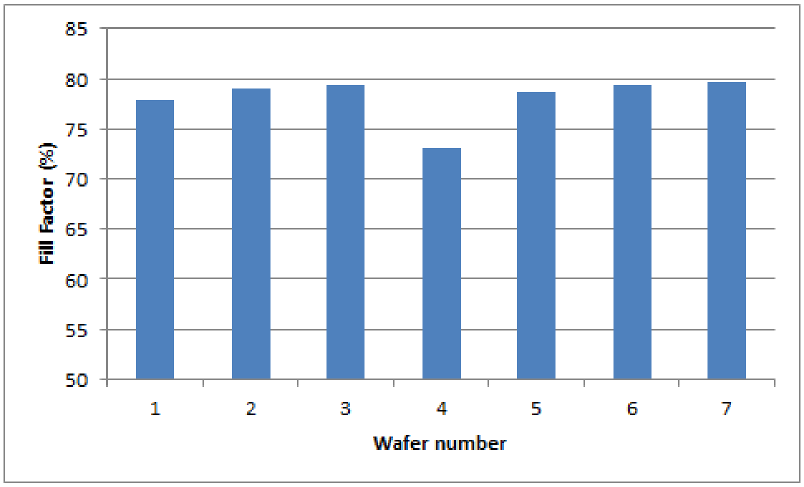

Figure 5. Chart showing measured fill factor on thick wafer based cells with front heterojunction using improved ITO process and screen printing at UT-Austin .

We have also evaluated shadow mask sputter deposition of metal as an alternative to screen printing to improve fill factor. The shadow mask metal deposition processes were carried out at NREL and IEC. The cells completed at both sites showed lower fill factors (60-70%) compared to screen printed cells at AstroWatt.

<u>*Task I.2.2: Demonstrate champion exfoliated cell with efficiency of 16%:*</u>
Our champion cell data to date is shown in Fig. 6 for both cell architectures. In both cases, we have demonstrated cell efficiencies of ~ 13.3 – 13.5% with fill factor greater than 72% using optimized a-Si and ITO process. However, the Voc of the cells was lower than the champion Voc demonstrated so far (~ 660mV).

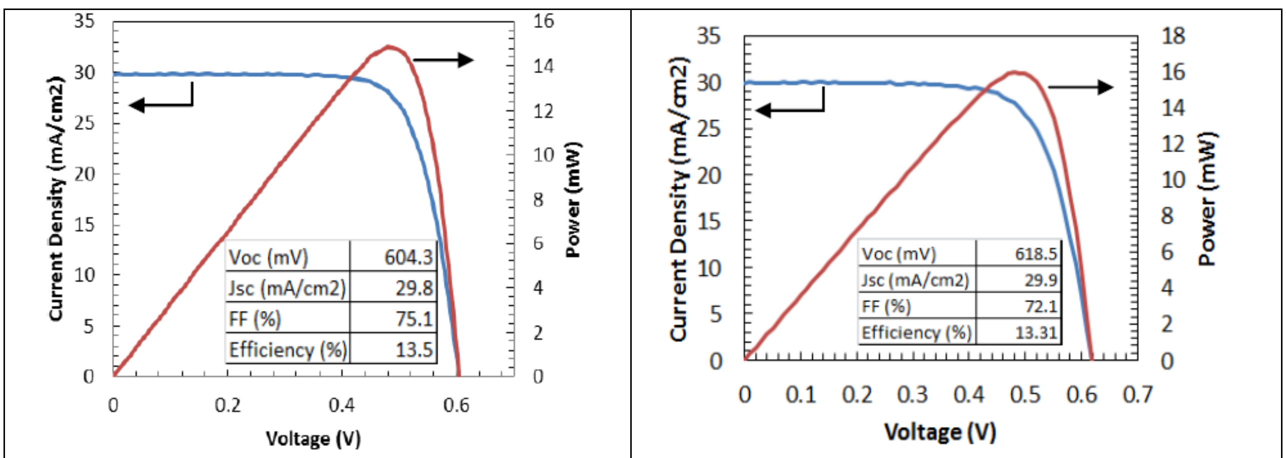

Figure 6: I-V characteristics of champion exfoliated cells using front heterojunction with rear BSF (left) and dual heterojunction (right) architectures.

Previously, we have demonstrated high Voc of 650mV but with lower fill factors (< 60%). It is believed that the Voc and the fill factor of the cell could be limited by metal contamination at the a-Si/c-Si interface as discussed below.
Table I below shows the measured lifetime on 180um thick control wafers, which were processed along with metal foils in the wet cleans. As can be seen from Table I, the lifetime of the wafer (MC1315-03) is degraded when exposed to a piranha solution that also has an exfoliated foil in it. It is believed that trace amounts of Ni residue from the metal backed foil in solution get deposited on the wafer, which then degrades the a-Si/c-Si interface resulting in potentially lower fill factors and lower Voc of cells.

Table I: Lifetime tests showing degraded passivation on wafer exposed to metal in piranha cleans.

Wafer	Sample #	Exfoliated Si on Ni foil in piranha bath	Lifetime (us)
IEC n.Cz (Tex)	MC1315-03	Yes	723
IEC n.Cz (Tex)	MC1315-04	No	2265

It is believed that the metal contamination problem is limiting the Voc and fill factor attainable with the exfoliated cells. The following mitigation strategies were identified during the project:

(1) Protecting the metal with a sacrificial oxide film in the piranha cleans: After exfoliation, a sacrificial PECVD oxide will be deposited on the metal side before the foil is introduced in the piranha clean. The final HF clean before a-Si deposition will remove this PECVD oxide.
(2) Change the pre amorphous Si clean chemistry to not attack the metal: We will evaluate if an alternate chemistry which does not attack the metal can be used to clean the Si surface before a-Si deposition

IV. Collaborations fostered during this project

This project was run as a collaboration between AstroWatt, University of Texas, Austin, National Renewable Energy Laboratories, University of Florida, Gainesville and Georgia Institute of Technology with additional contributions from Institute for Energy Conversion, Delaware.

V. Publications/Presentations:

The work carried out in this first phase of the project led to the following publications and presentations:

1. A low-cost kerfless exfoliation technology for 25 µm thin monocrystalline silicon solar cells, - D. Jawarani et. al, presented at **5th International Workshop on**

Science and Technology of Crystalline Silicon Solar Cells (CSSC-5) , Boston, MA, Nov 2011

2. Integration and Reliability of Ultrathin Silicon Solar Cells and Modules Fabricated using SOM® Technology – D. Jawarani et. al., **invited talk at the IEEE PhotoVoltaic Specialists Conference,** Austin, TX June 2012

3. A Low-Cost Kerfless Thin Exfoliated Si Solar Cell Technology – R. Rao, et. al, presented at **IEEE PhotoVoltaic Specialists Conference,** Austin, TX June 2012

4. Remote Plasma Chemical Vapor Deposition for High-Efficiency Ultra-Thin ~25-Microns Crystalline Si Solar Cells **–** D. Sarkar et.al **(Nominated for Best Paper)** presented at **IEEE PhotoVoltaic Specialists Conference,** Austin, TX June 2012

5. Exfoliated 15-micron Thin-Crystalline Germanium Heterojunction Solar Cells **–** E. Onyegam et al**, (Nominated for Best Paper) ,** presented at **IEEE PhotoVoltaic Specialists Conference,** Austin, TX June 2012

6. A Novel Low-Cost ~25µm-Thin Monocrystalline Silicon Bifacial Solar Cell Technology with Flexible and Rigid Form-Factor and Electroplated Contacts – L. Mathew et. al, **(Nominated for Best Paper)** , presented at **IEEE PhotoVoltaic Specialists Conference,** Austin, TX June 2012

7. A Low-Cost Kerfless Thin Exfoliated Si Solar Cell Technology – R. Rao, et. al, presented at the Symposium on Advanced Photovoltaics – Ultra High Efficiency Technologies, InterSolar NA, San Francisco, CA, July 2012.