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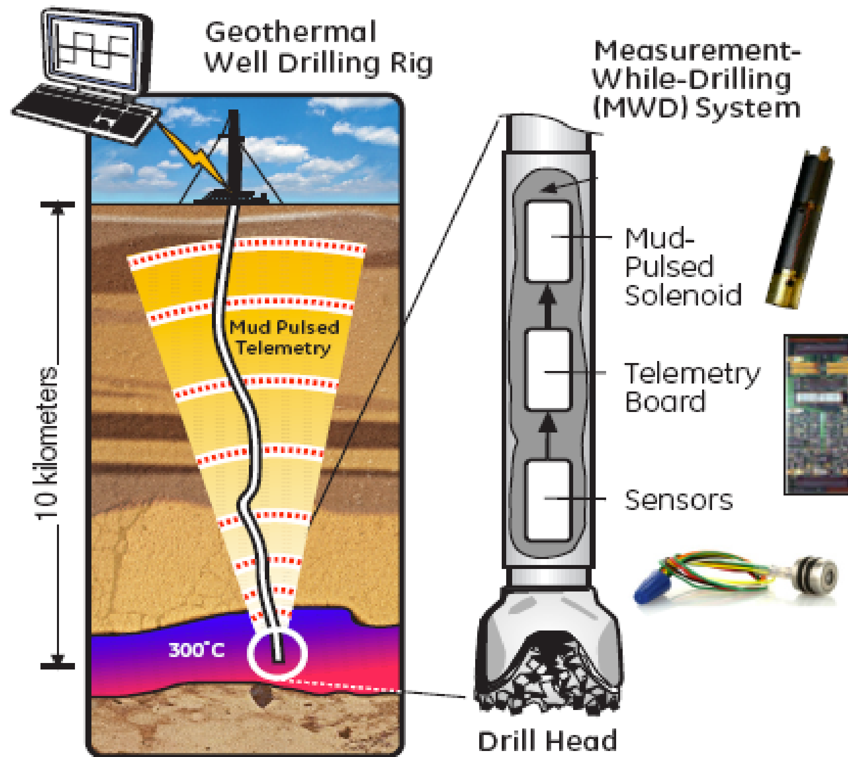

Pressure sensor and Telemetry methods for measurement while drilling in geothermal wells

May 19, 2010

Vinayak Tilak
GE Global Research

High Temperature Tools and Sensors,
Down-hole Pumps and Drilling

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Overview

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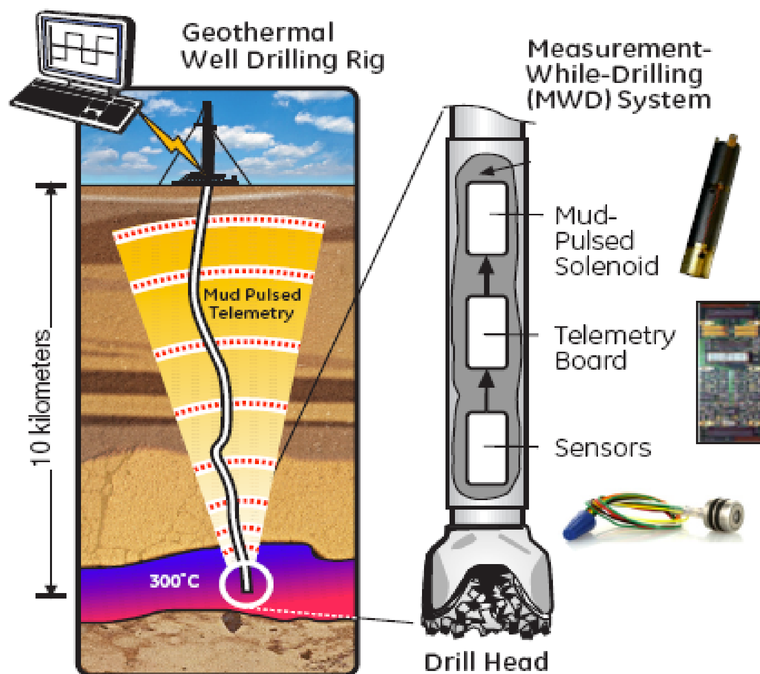


Program Objective:
- Develop electronics for sensors and telemetry for measurement while geothermal drilling
- Demonstrate multiple sensor systems multiplexed through a telemetry system

Budget
- Total budget - $4.3MM
- DOE share - $3.4MM
- GE share - $0.9 MM
- Funding planned for 2010 - $1.3MM

Timelines
- Project start date – Dec 29, 2009
- Project end date – Dec 28, 2012
- Percentage completed – 0%

Partners
- Auburn University (Prof. Wayne Johnson) – high temperature electronics packaging

GTP Barrier addressed by this technology
- Development of high temperature (300ºC) logging tools and sensors to enable economic well construction and reservoir characterization

Impact of Research

Project Objective

Develop telemetry electronics and pressure sensor system for operation at 300ºC and demonstrate the operation of multiple pressure sensor systems at 300ºC

Benefits to Geothermal industry

- Enable high temperature well construction – MWD using this technology can enable economic drilling
- Better reservoir characterization through long term reservoir monitoring – sensors based on this technology will be designed to operate at high temperatures for months

Key innovations

- Silicon carbide based digital and analog integrated circuits used for active electronics – The integrated circuits on silicon carbide attempted in this project will be the most complex till date
- Ceramic based packaging and board materials that are rated to operate at 300ºC and with high shock and vibration specs – Traditional organic based boards and lead based solders are not used in this approach

Impact of Research

2010 Objectives

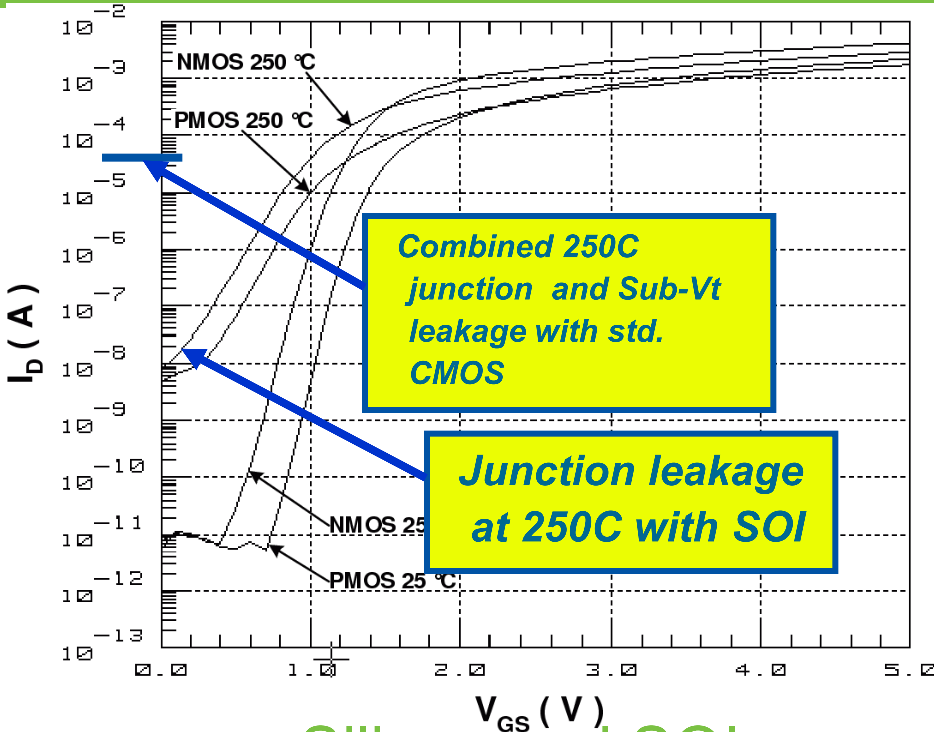
• Demonstrate simple digital electronics – complexity of shift registers – on silicon carbide

• Design the sensor system architecture and telemetry module based on silicon carbide capability

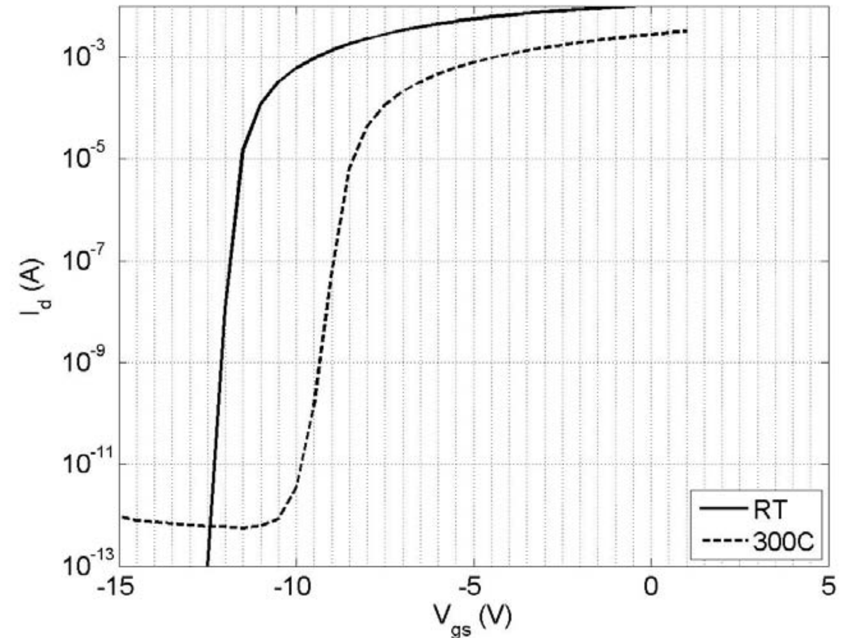
•Design and fabricate silicon carbide based analog electronics chip sets for pressure sensor system

• Define process for chip-level and board level packaging for 300ºC operation while meeting the shock and vibration specification

Scientific Approach – Why SiC ?



Silicon and SOI,
(source Honeywell)

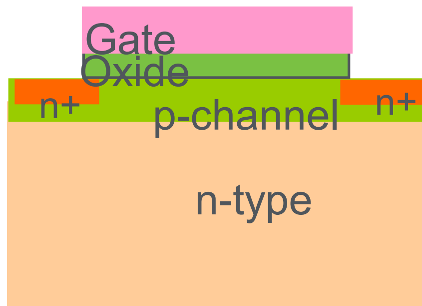


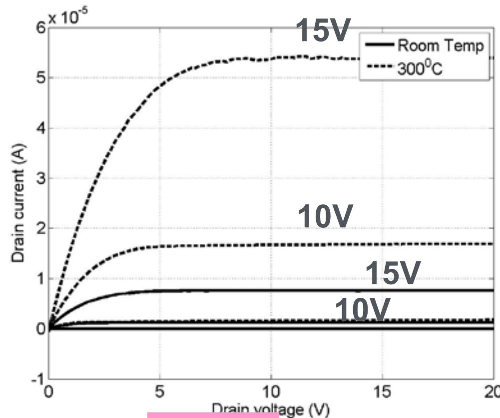
Silicon Carbide

The band gap of SiC (3.26 eV) compared to the band gap of Si (1.12eV) is the reason for the low leakage of p-n junctions at high temperatures

Objective: For optimum performance we want to have ratio of "ON' current to "Off" current

Technical Approach – SiC MOSFETs





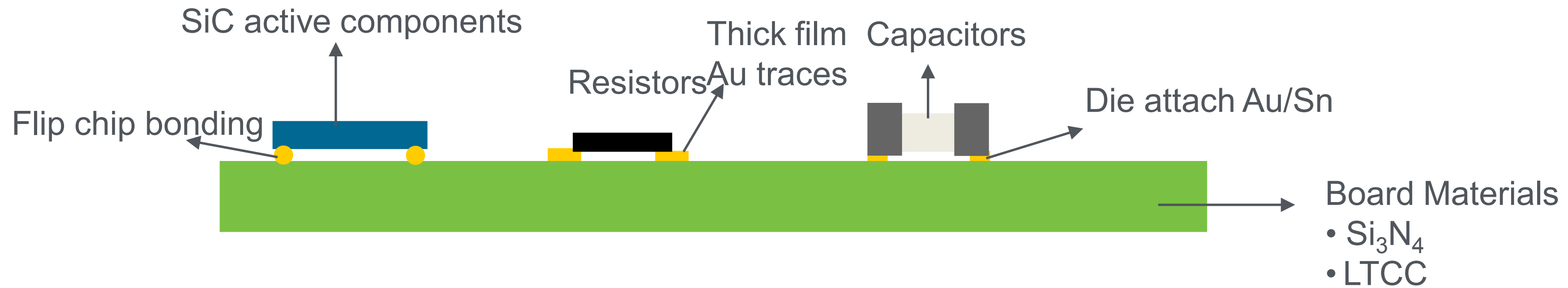
Enhancement-mode MOSFET

- **Normally off – Efficient use of semiconductor real estate, ease of scaling**
- **P-MOS devices not ready for circuits and therefore NMOS logic is used**
- **Low mobility due to poor oxide carbide interface leads to poor performance, operate only in saturation region**
- **Threshold voltage temperature coefficient is much larger (~15 mV/ºC) than in silicon devices (2 mV/ ºC) making analog design more complicated**
- **Current increases with increasing temperature – conventional silicon modeling tools cannot be used**
- **Load resistor may have a different temperature coefficient compared to the drive transistor**

Depletion-mode MOSFET

- **Normally on – inefficient use of real estate**
- **Low Efield intensity in drain region – Higher reliability of gate oxide**
- **High mobility of channel electrons and can be operated in linear region**

Technical Approach - Packaging

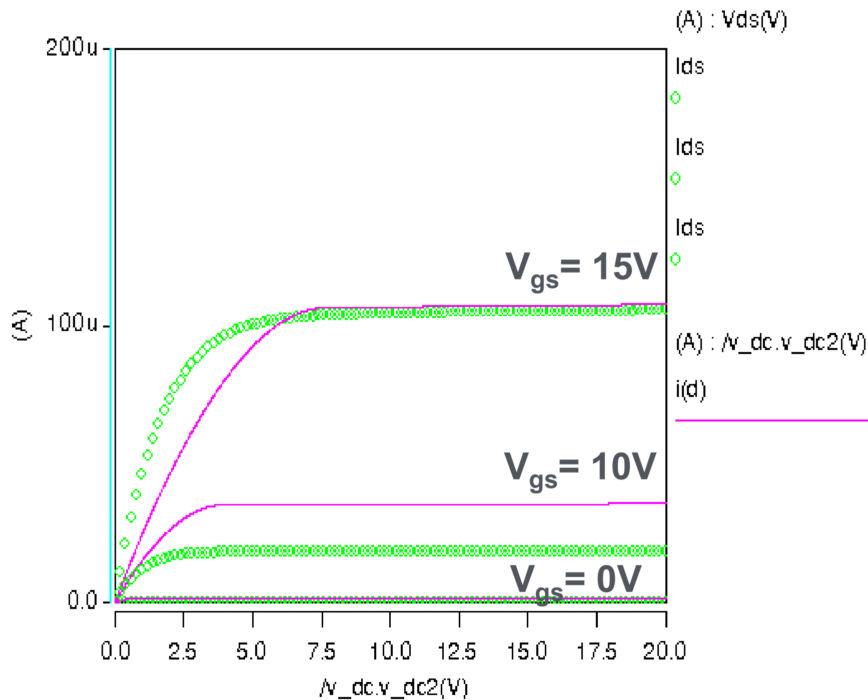


- Passives to be sourced from vendors
- SiN/LTCC substrate to be used as the electronics board substrate to minimize Coefficient of thermal expansion (CTE) mismatch between SiC and substrate.
- Au thick film for gold traces – explore multi layers
- AuSn is the preferred attach material for passives
- Au Flip chip bonding bonding for electrical connections

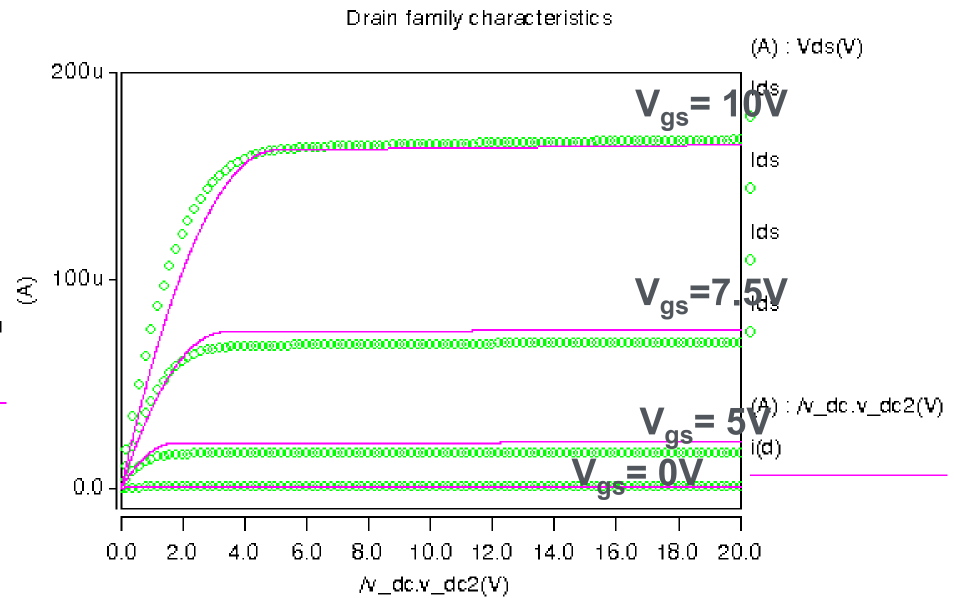
Mechanical Test	Specification
Sine Sweep Vibration	30G, 10-2000Hz, each axius
Random Vibration	20Grms, 10-80Hz 6dB/oct, 80-1000Hz flat, 4 hrs each axis
Mechanical Shock	1000G, 1mSec, ½ sine pulse, each axis

Test conditions for shock and vibration testing

Accomplishments – Device models



Room temperature experimental data and SPICE model



300^0C experimental data and SPICE model

- We have developed a temperature independent level 2 SPICE model for use at room temperature and 300^oC – need to ensure that the circuit works with two different models
- Plan to build a temperature dependence in the model – Dec 2010

Accomplishments - Planned

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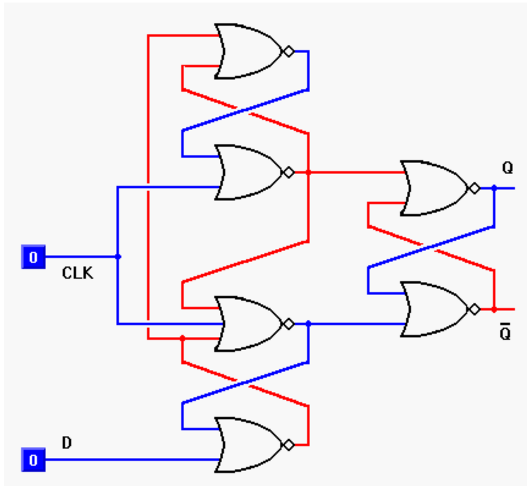
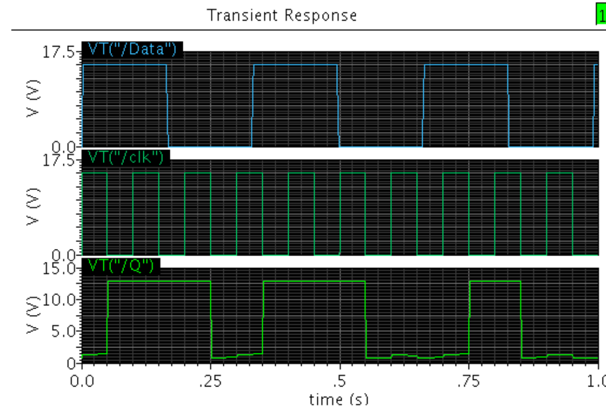
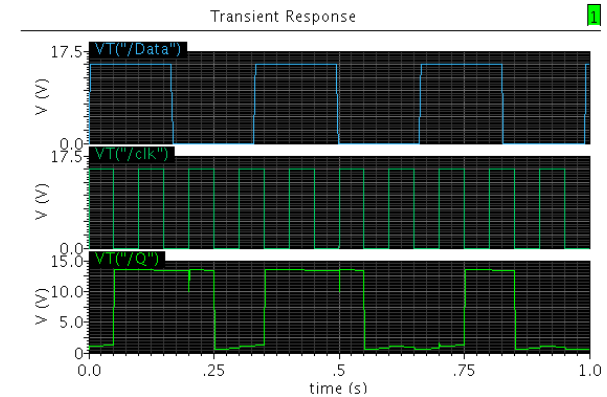


D-type Flip flop design



D-type flip flop output waveforms – 27°C



D-type flip flop output waveforms – 300°C

- Circuit design for simple gates, combinatorial logic and shift registers to be completed – June 2010
- Fabricate and test ICs – September 2010
- Sensor and telemetry architecture preliminary design – August 2010
- Pressure sensor electronics design and fab – September 2010

Project Management – Gantt chart

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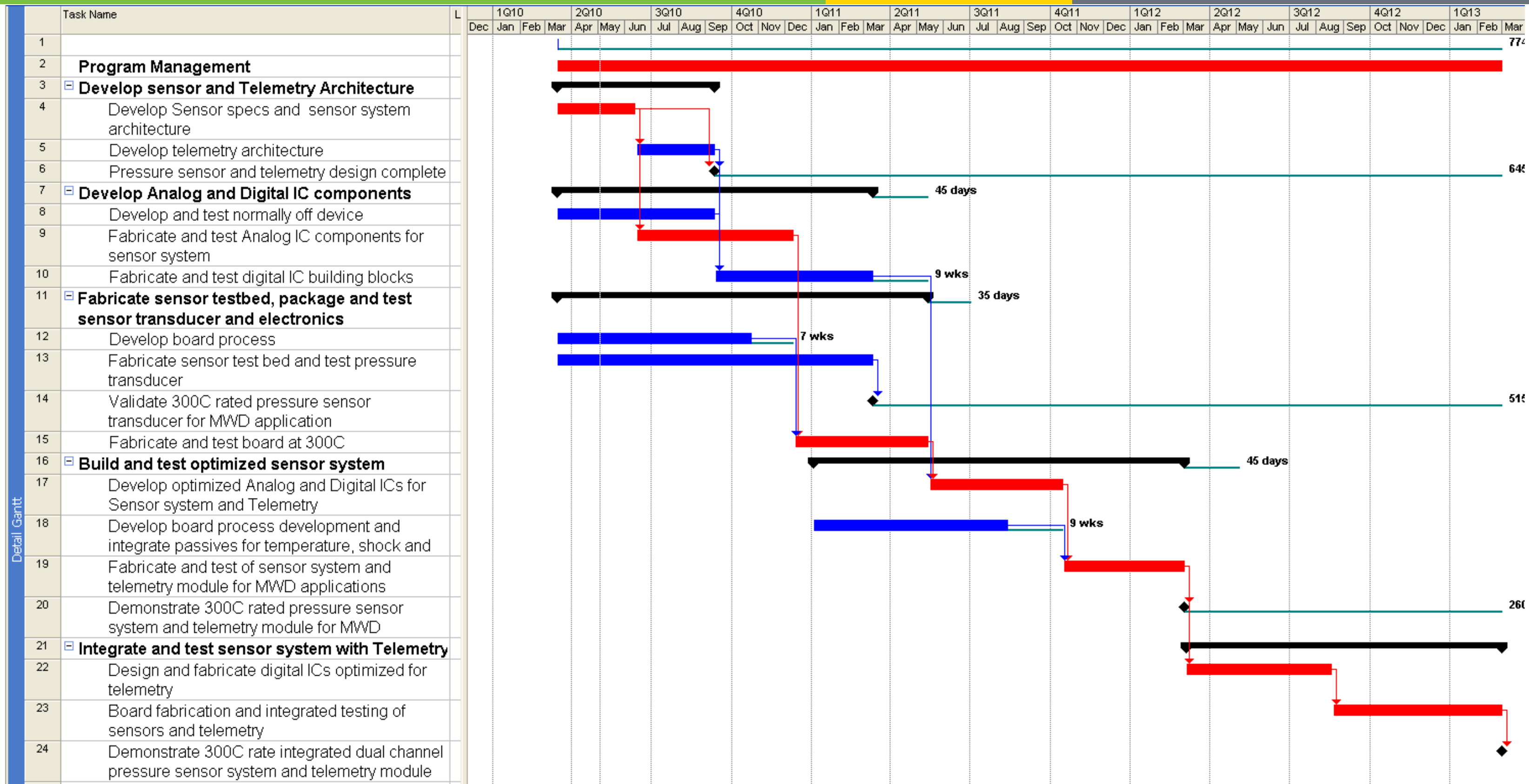

FY 2010 milestones – Planned spend $1.3MM

- Complete pressure sensor and telemetry module design – September 2010
- Demonstrate simple SiC digital ICs at 300^{0}C - October 2010
- Validate pressure sensor transducer for MWD operation at 300^{0}C – November 2010
- Develop board level packaging process for 300^{0}C - October 2010

Project management – FY 2011, 2012 milestones

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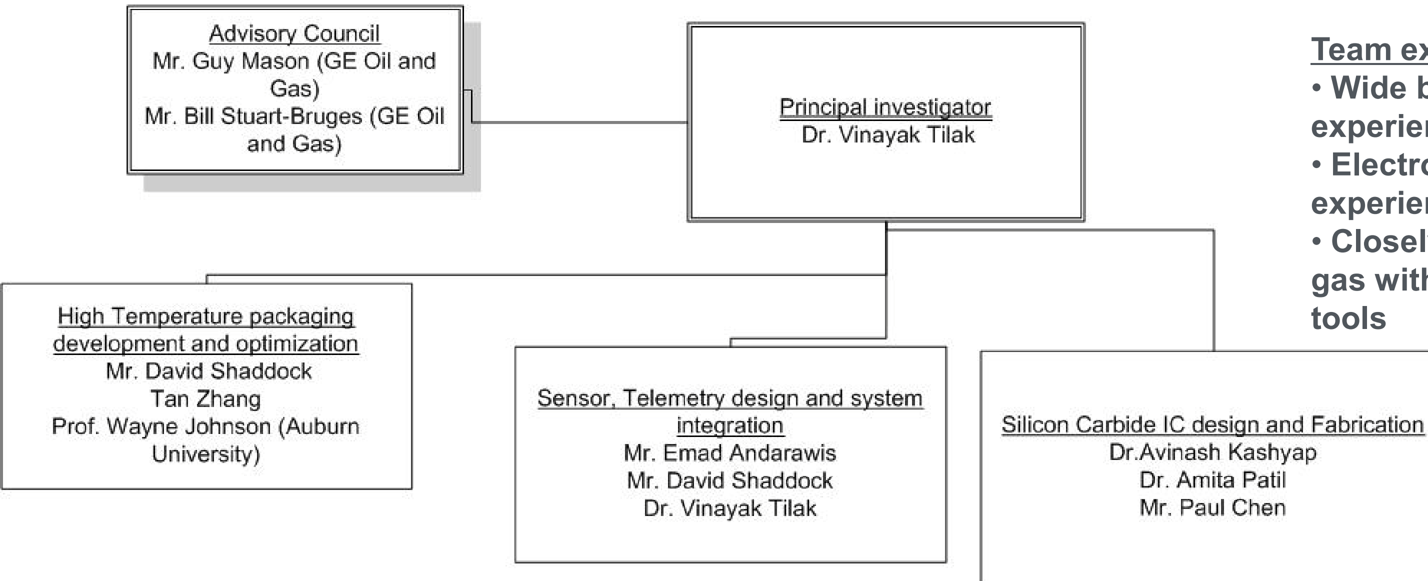
FY 2011 milestones – Planned spend $1.5MM

- Fabricate and test at 300^{0}C chip set for pressure sensor system – March 2011
- Fabricate and test at 300^{0}C board for pressure sensor system – May 2011
- Fabricate and test chip set for telemetry module – May 2011
- Fabricate and test at 300^{0}C chip set for telemetry module – June 2011
- Fabricate board and test at 300^{0}C board for telemetry module – August 2011

FY 2012 milestones – Planned spend $1.5MM

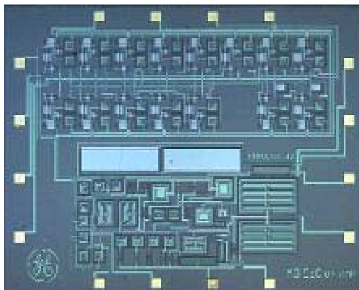
- Fabricate and test optimized chipset for 300^{0}C pressure sensor system and telemetry module – March 2012
- Fabricate and test at 300^{0}C integrated pressure sensor systems and telemetry module – August 2012

Program management - Team

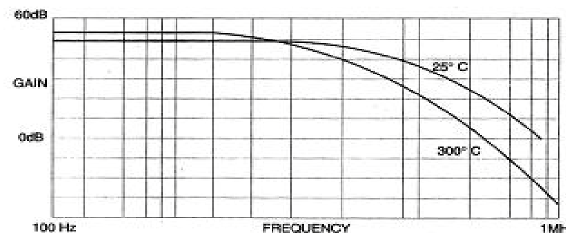


Team experience

- **Wide band gap semiconductor experience – 20 years**
- **Electronics packaging experience – 50 years**
- **Closely working with GE oil and gas with expertise in down hole tools**



GE fabricated Silicon Carbide based op amp IC



T (°C)	Gain (dB)	Bandwidth (kHz)
25	49	724
160	54	501
210	54	447
250	53	380
300	53	269

Long experience in Silicon carbide MOSFETs

- World's first Silicon carbide based op-amp IC fabricated at GE in 1994
- Current active program that has demonstrated a 1.2 kV, 30 Amp SiC MOSFET with world record on resistance of 7 mΩ-cm^2

Future Directions

- FY 2010 – digital building block chips demonstrated, analog sensor system chips fabricated, board process for 300^0C shock and vibration specs identified
- FY 2011 – digital telemetry board fabricated, analog board fabricated and tested individually
- FY 2012 – all pieces of electronics demonstrated working in consort
- Future research
  - Gamma at 300^0C
  - Field test of the electronics and sensor system

Summary Slide

- Most complex digital electronics on SiC to be attempted – if successful, we will open > 300ºC temperature regime for electronics
- Packaging that meets both temperature, shock and vibration specifications
- Boards that operate at 300ºC, 30 g vibration and 1000 g shock to be demonstrated
- Electronics should enable the transmission of multi-sensor data to the surface using a mud pulse solenoid

Supplemental Slides

Scientific Approach – Gate oxidation

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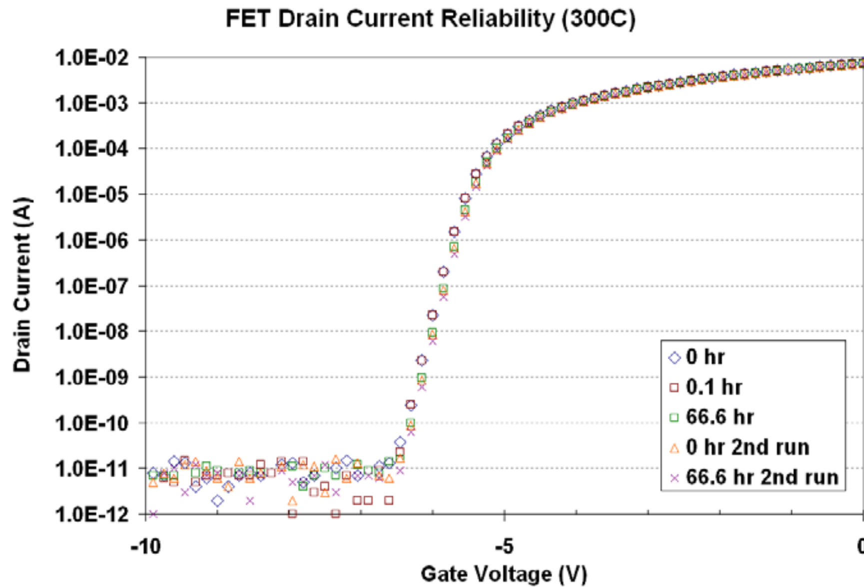
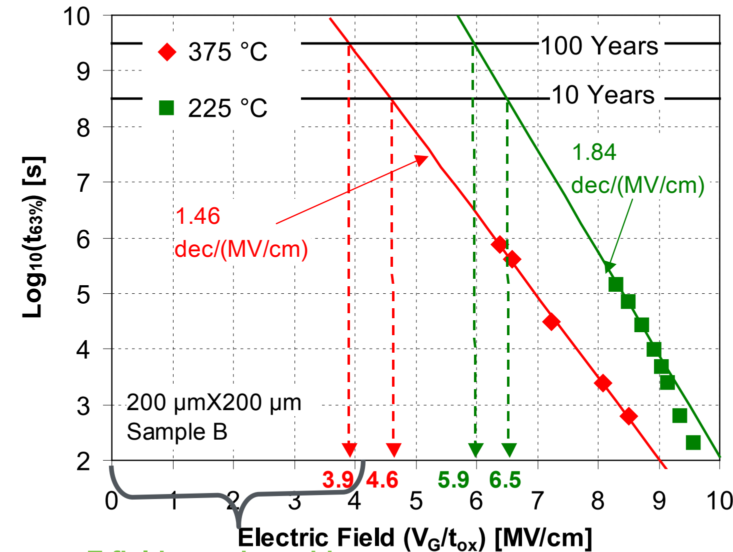


Stability of SiC MOSFET at 300°C

Data from L.C. Yu et al., "Oxide Reliability of SiC MOS Devices", IEEE International Integrated Reliability Workshop Final Report, pp. 141-144 (2008)

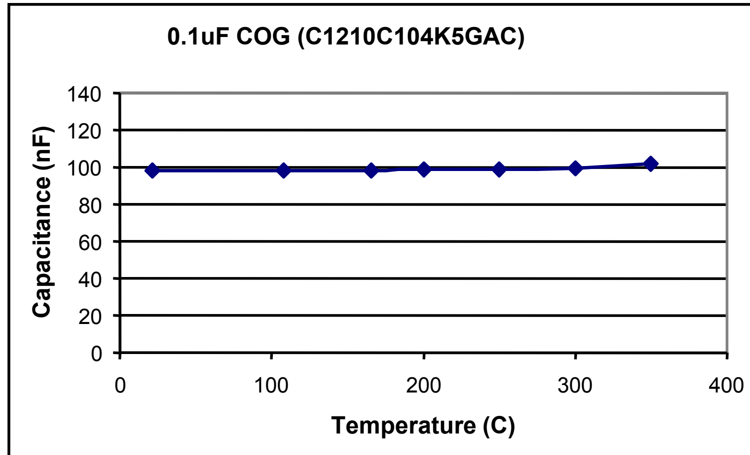


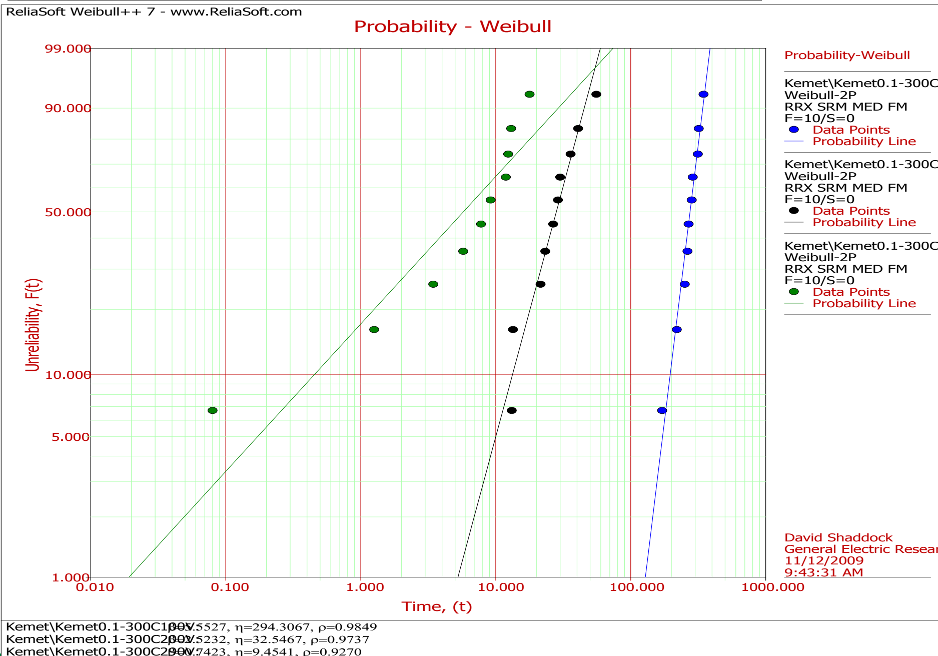
E field seen by oxide during operation

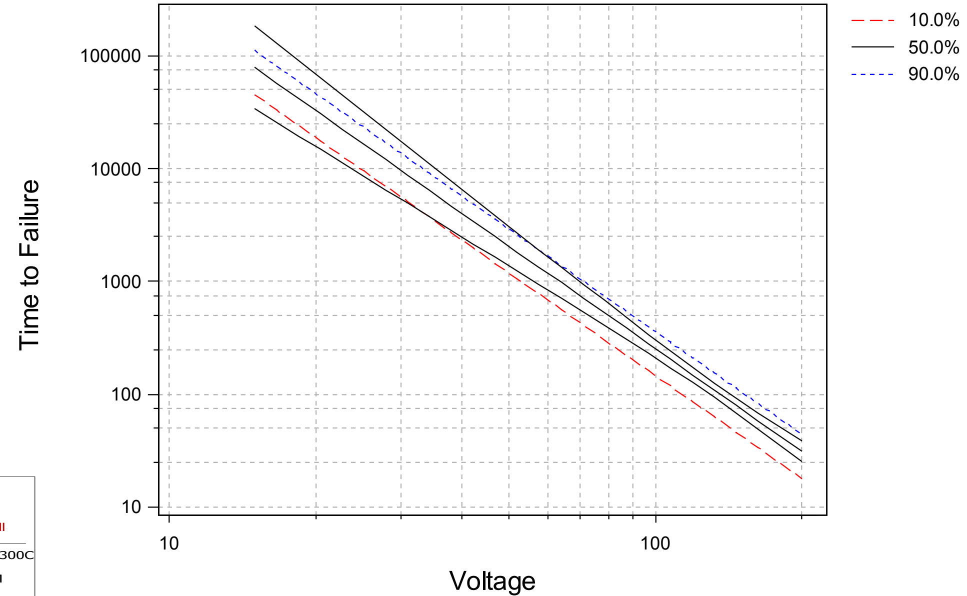
Lifetime of gate oxide in SiC MOSFET

- NO based post oxidation anneals used to fabricate all the gate oxides in the project
- Reliability of gate oxide has improved at high temperature to MTTF of 100 years at 375°C
- Stability of SiC MOSFET after 132 hours at 300°C is a dramatic improvement on pervious generation MOSFETs

Scientific approach - capacitors





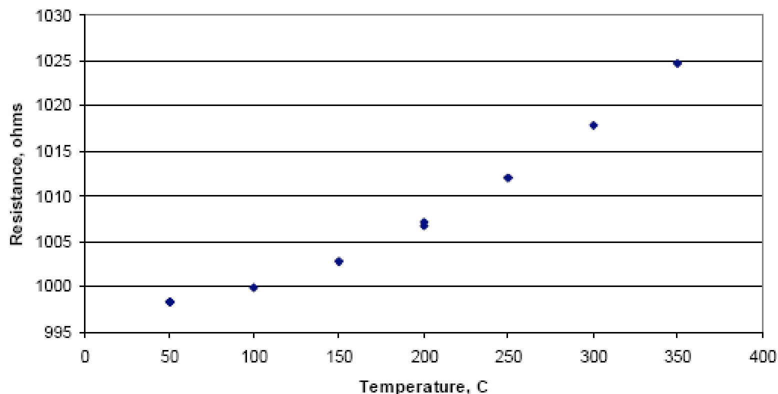


Value: 0.10uF, 50V, H dielectric
Temperature: 300C
Voltage Bias: 290, 200, 100
Model parameters: n=3.67 using 100 and 200V
Estimated Life: 17254 hrs at 25V

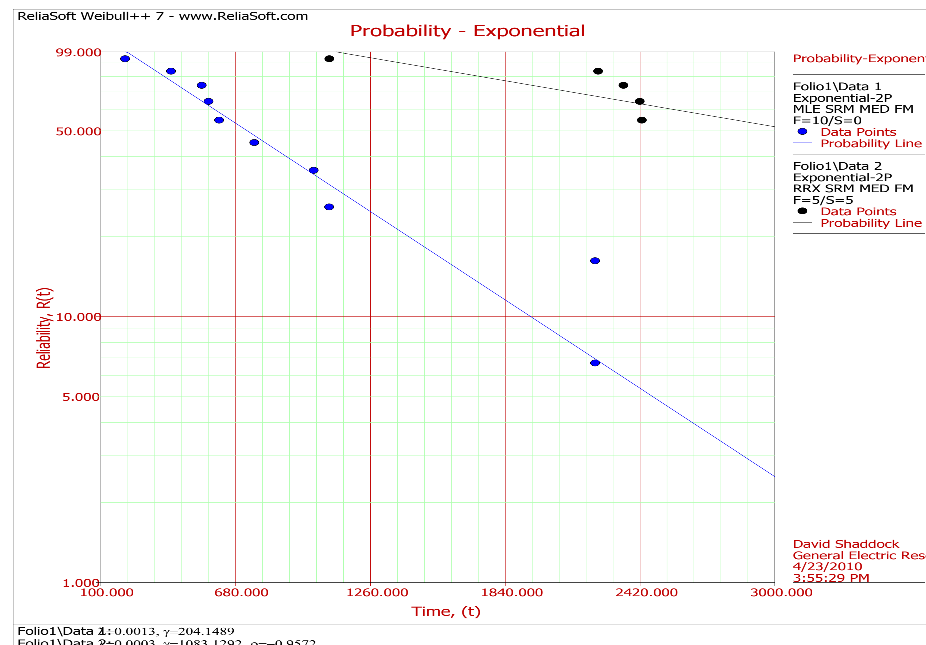
Work performed for the DOE Geothermal Technologies Program under DE-FG-GO3608GO18181

Scientific Approach - Resistors

1 kΩ thick film resistor



Temp=350C, 16V across DUT, 0.25W (at rating)
3529 hrs, 7 failures



Mean life
962.3558 hours @ 1 % degradation
3994.9697 hours @ 2% degradation

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