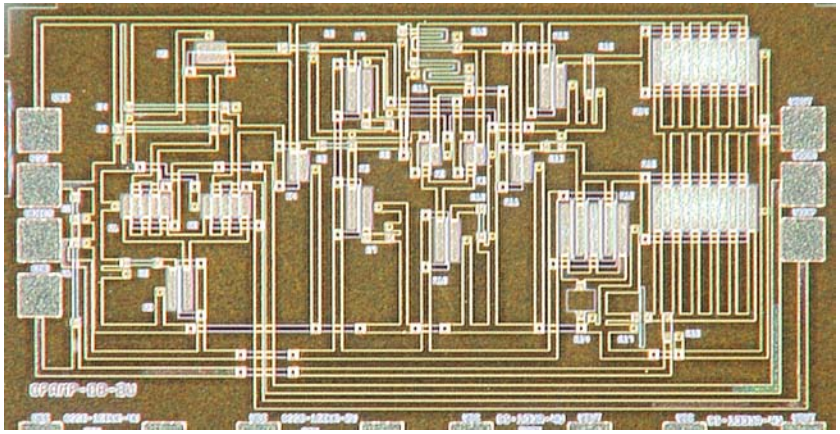
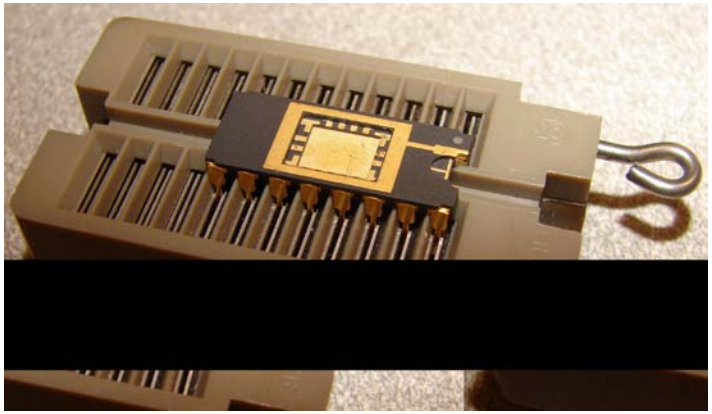


Silicon Carbide Integrated Circuit



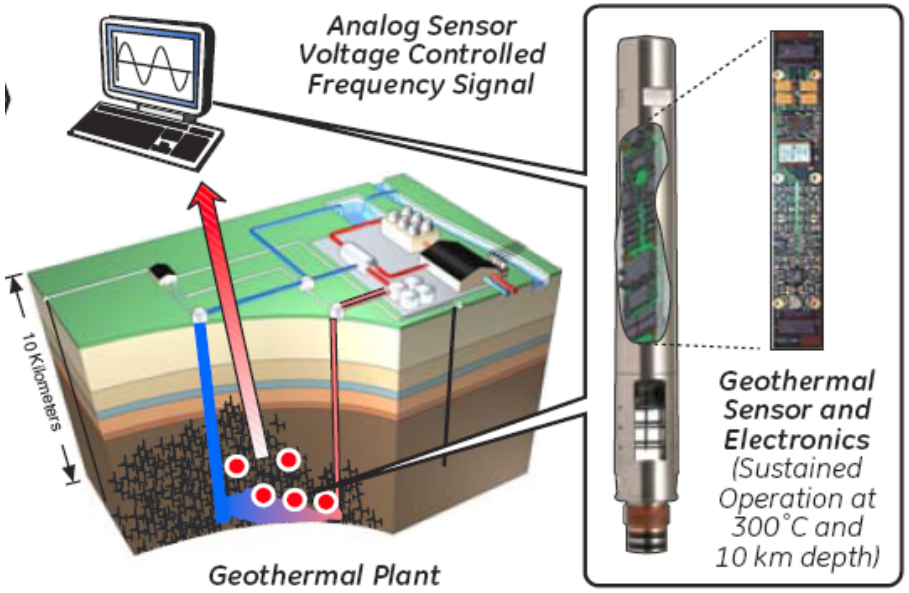
300° C Capable Electronics Platform and Temperature Sensor System For Enhanced Geothermal Systems

May 18, 2010

Vinayak Tilak
GE Global Research

High Temperature tools and drilling

Overview



Program Objective:

- Enable geothermal wellbore monitoring through the development of SiC based electronics and ceramic packaging capable of sustained operation at temperatures up to 300˚C and 10 km depth.
- Demonstrate the technology with a temperature sensor system

Budget

- Total budget - $2MM
- DOE share - $1.6MM
- GE share - $0.4 MM
- Funding received in 2009 - $0.92MM
- Funding planned for 2010 - $0.8MM

Timelines

- Project start date – Dec 29, 2008
- Project end date – Dec 28, 2011
- Percentage completed - 40%

Partners

- Auburn University (Prof. Wayne Johnson) – high temperature electronics packaging

GTP Barrier addressed by this technology

- Development of high temperature (300ºC) logging tools and sensors to enable economic well construction and reservoir characterization

Impact of Research

Project Objective

Develop electronics platform technology for operation at 300ºC and demonstrate a temperature sensor system

Benefits to Geothermal industry

• Enable high temperature well construction – logging tools developed using this technology can enable economic drilling

• Better reservoir characterization through long term reservoir monitoring – sensors based on this technology will be designed to operate at high temperatures for months

Key innovations

• Silicon carbide based integrated circuits used for active electronics – The integrated circuits attempted in this project is one of the most complex till date on silicon carbide

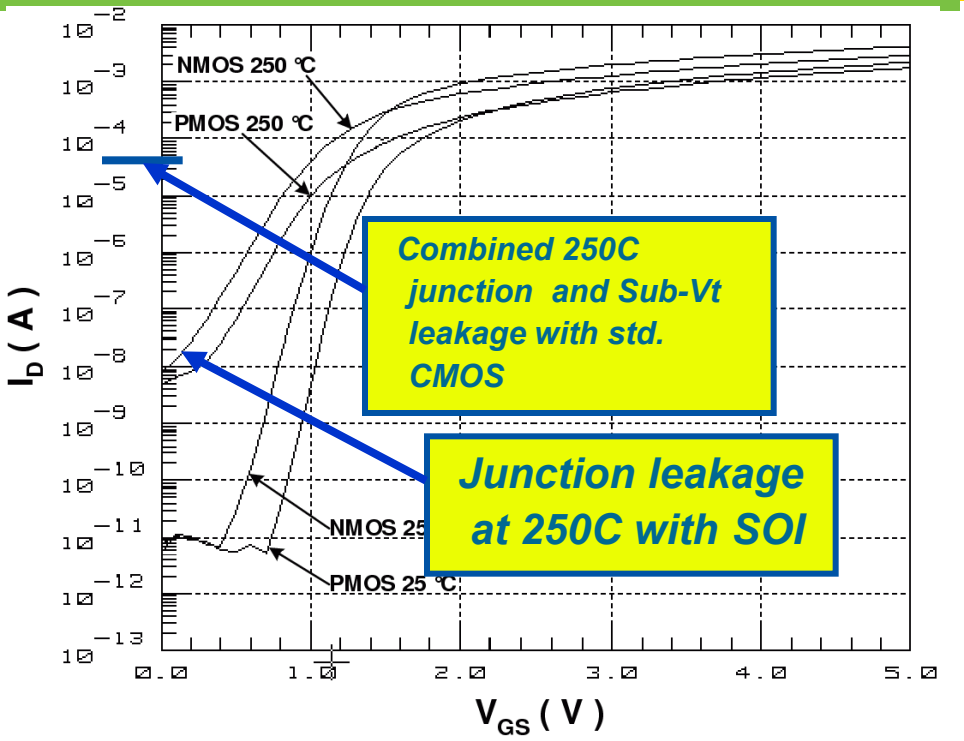
• Ceramic based packaging and board materials that are rated to operate at 300ºC – Traditional organic based substrates or lead based packaging materials will not be used

Impact of research

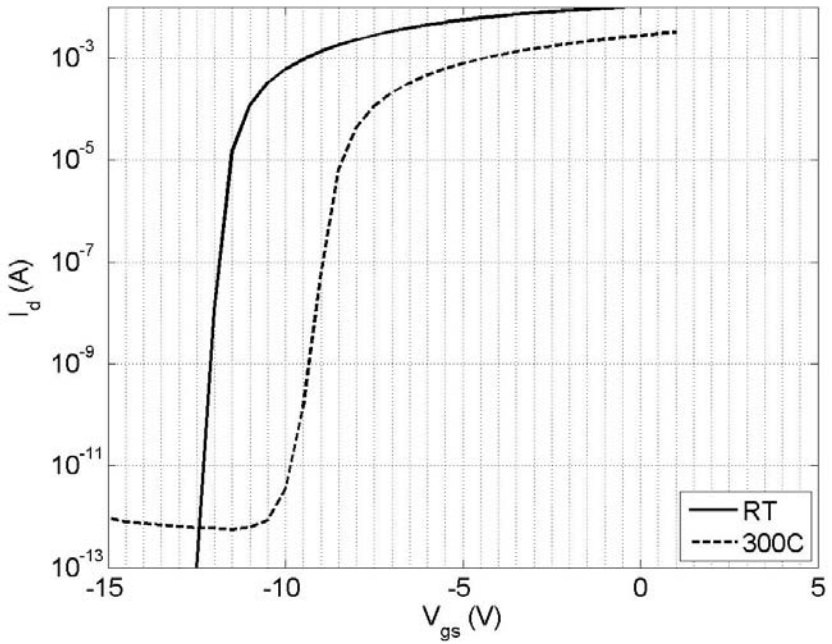
2009 objectives

- Develop temperature sensor system architecture and flow down specifications of the silicon carbide integrated circuit
- Finalize silicon carbide active device
- Demonstrate a silicon carbide based integrated circuit operating at 300ºC
- Validate resistors and capacitors for 300ºC operation
- Develop a high temperature capable packaging process for silicon carbide

Scientific approach – choice of substrate



Silicon and SOI

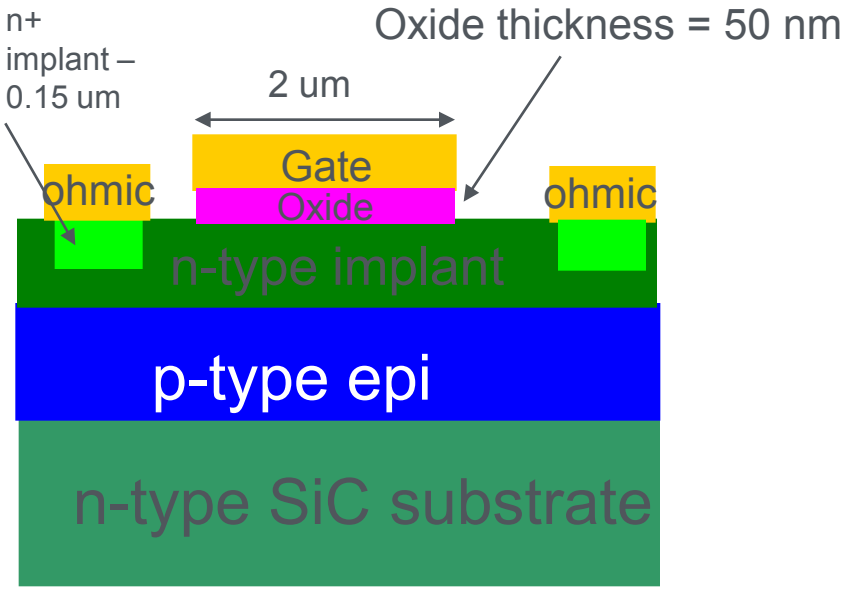


Silicon Carbide

The band gap of SiC (3.26 eV) compared to the band gap of Si (1.12eV) is the reason for the low leakage of p-n junctions at high temperatures

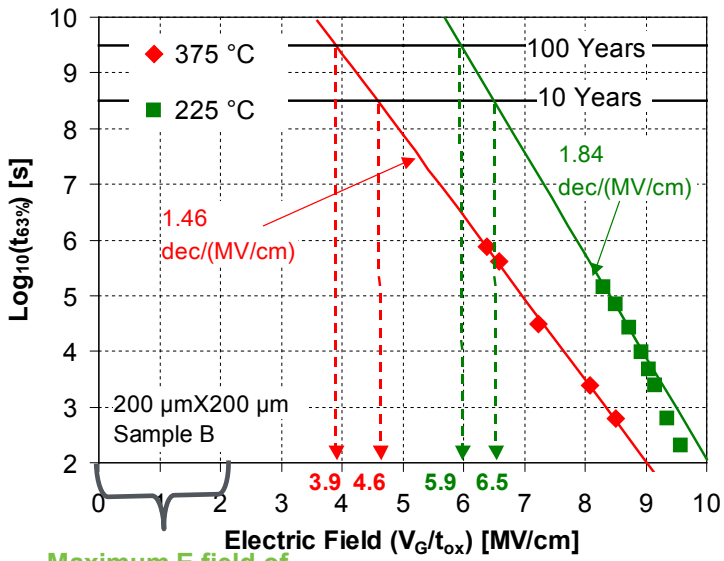
Objective: For optimum performance we want to have ratio of "ON' current to "Off" current

Scientific approach – SiC MOSFETs



Depletion mode – SiC MOSFETs

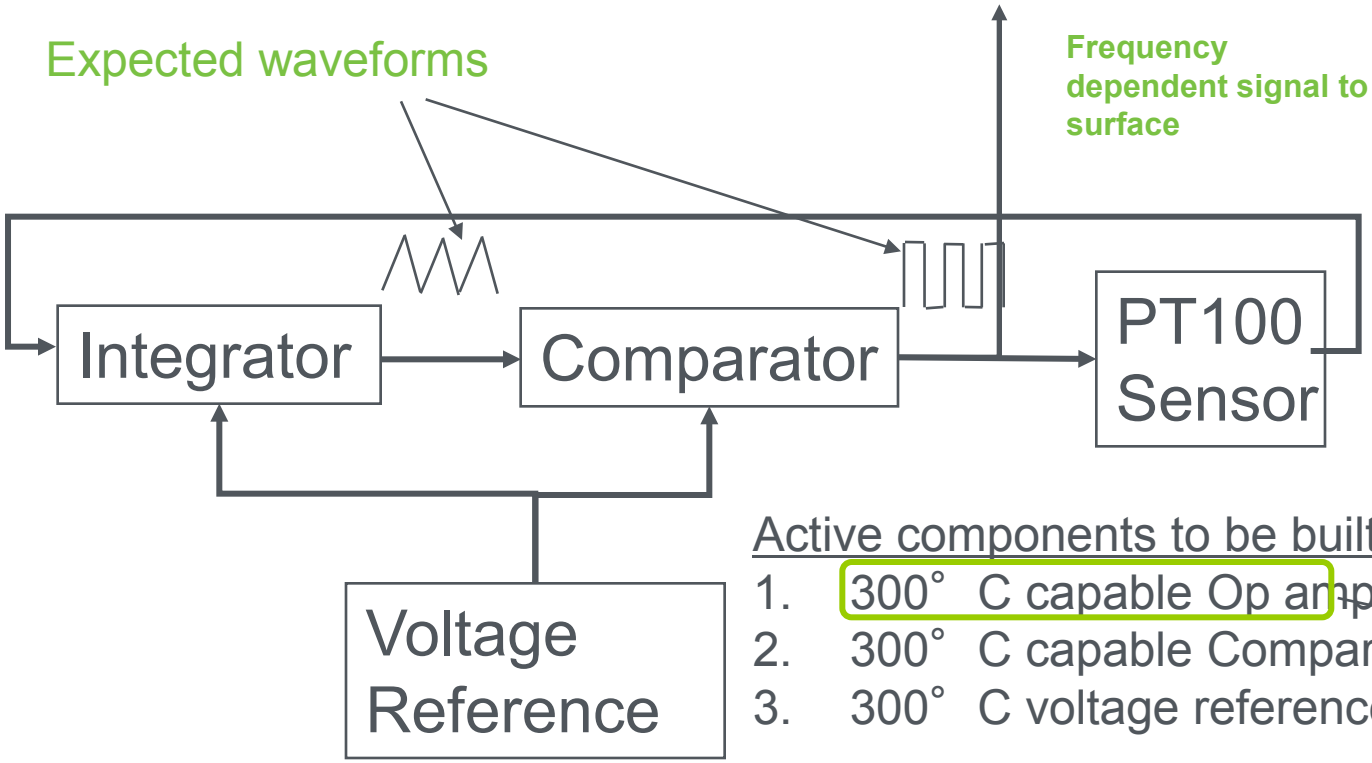
Data from L.C. Yu et al., "Oxide Reliability of SiC MOS Devices", IEEE International Integrated Reliability Workshop Final Report, pp. 141-144 (2008)



Maximum E field of normally on device

- Normally-on transistor used as a basic building block of circuit ($V_{threshold}$<0)
- n-type implant tailored to provide the appropriate threshold voltage
- SiC based gate oxidation performed using N_2O precursor and followed by a NO post oxidation anneal – Leads to higher reliability and stability of the gate compared to previous generation devices and circuits
- Ni used for ohmic contacts and gold used as bond pad metal

Scientific approach – Board design

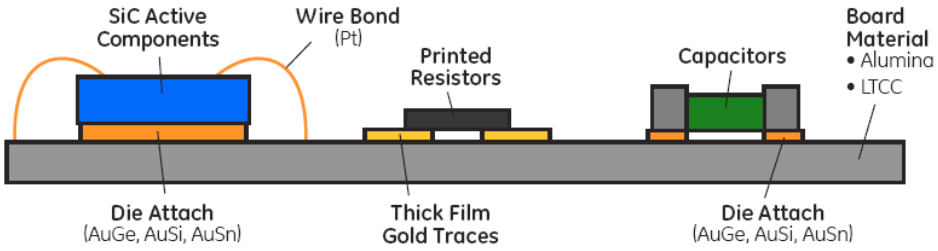


Active components to be built in the program

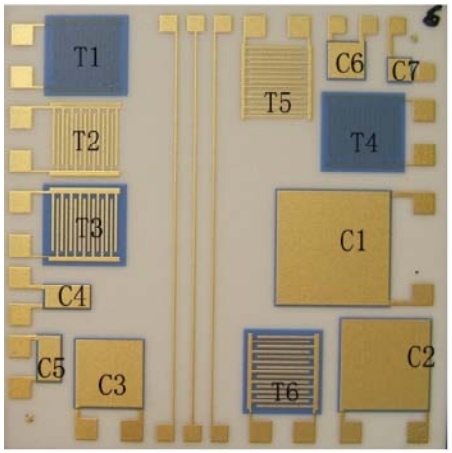
1. 300° C capable Op amp → Lot 1 build
2. 300° C capable Comparator
3. 300° C voltage reference

- This circuit can be configured to convert different sensor signals to different frequencies so that we can transmit the signals on a single channel
- A similar board can be built for converting pressure, fluid flow, orientation information into frequency and transmitted to the surface

Scientific approach – packaging



SiC high temperature packaging approach



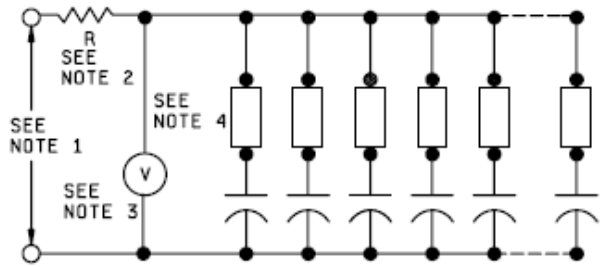
Alumina based electrical test pattern

Packaging approach in collaboration with Auburn University

- Alumina substrate to be used as the electronics board – no organics
- Au thick film for gold traces
- AuSn off-eutectic is the preferred Die attach material, expected to operate at temperatures close to 400° C
- Au Wire bonding for electrical connections
- Ni Clad Moly Tabs used for wire attach
- Alumina dielectric is used to form multi-layers

The targeted form factor of the board is 6”(Length)x1”(width)

Scientific approach – Passive component validation

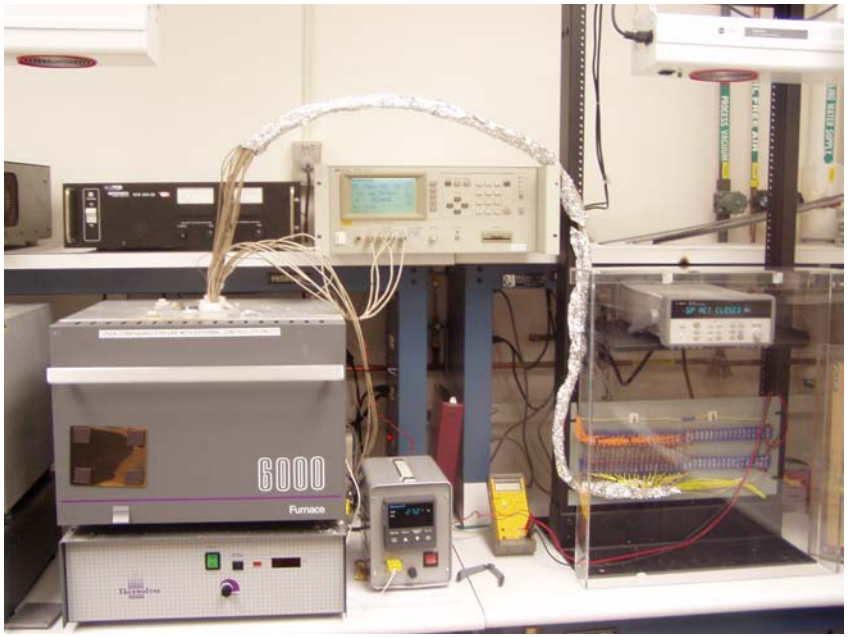


NOTES:

1. The power supply shall be capable of supplying the required test voltage.
2. The current limiting device shall be a resistor and/or a fuse. The current shall be limited to no less than 30 milliamperes (mA) and no more than 10 A.
3. There shall be a voltage monitor that will trigger an alarm and shut off the test if the applied voltage drops by more than 5 percent.
4. Fuses and resistors are optional. The value of the resistors and fuses shall be such that they do not restrict the power supply's ability to provide the required test voltage to the device under test (±5 percent).
5. The capacitor bank shall be no less than 10 capacitors.

Component Type	Supplier	Value	Voltage	Dielectric	Rated Temp
Capacitor	A	0.1 μf	50	HT-300	300
Capacitor	A	1.0 μf	50	HT-300	300
Capacitor	B	0.1 μf	10	NBT, Class II	230
Capacitor	C	0.1 μf	50	Class I	250
Capacitor	C	0.47 μf	50	Class I	250

Component Type	Supplier	Value	Precision	Wattage	Rated Temp
Wire wound	D	1K	1%	2	275
Wire wound	D	1K	3%	0.5	250
Wire wound	D	1K	3%	5.5	350
Wire wound	D	10K	3%	5.5	350
Thick Film	E	1K	1%	0.25	150
Thick Film	E	10K	1%	0.25	150
Thick Film	E	100K	1%	0.25	150
Thick Film	E	1M	10%	0.25	150

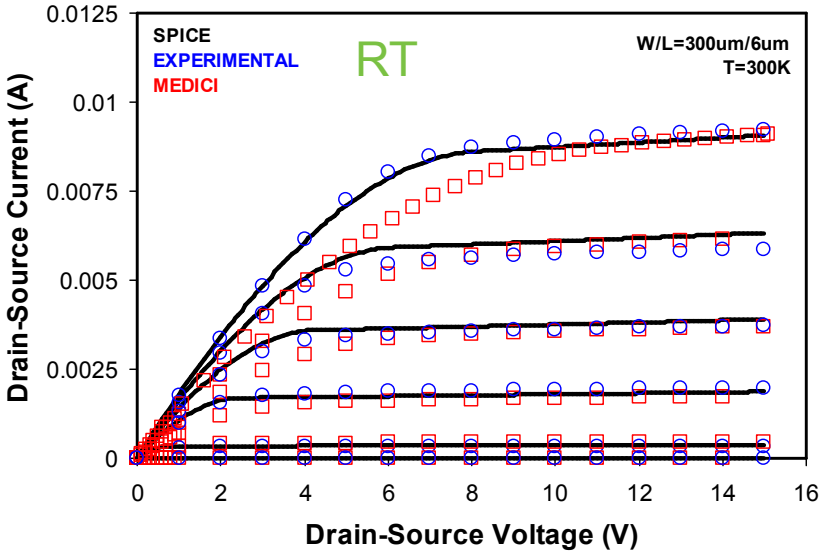


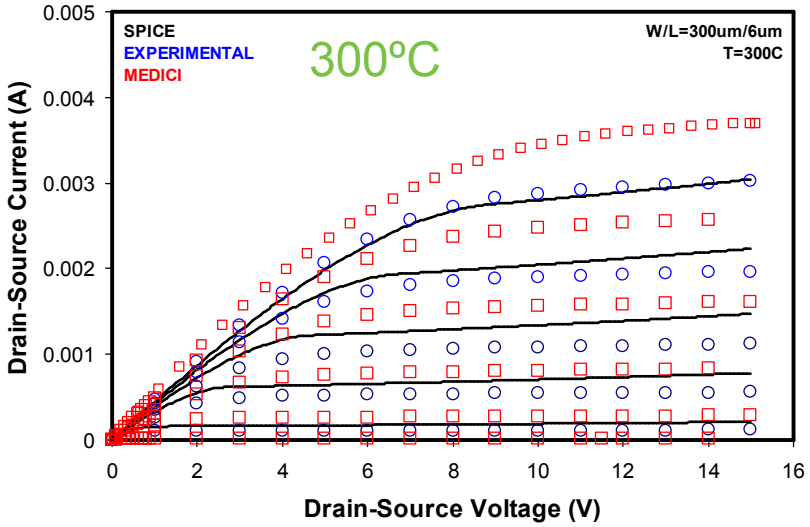
- Highly accelerated life testing (HALT) methodologies were employed with both voltage and temperature as acceleration factors to determine lifetime at 300° C

$$\frac{t_1}{t_2} = \left(\frac{V_2}{V_1}\right)^n \exp\left[\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$$

Accelerated model equation

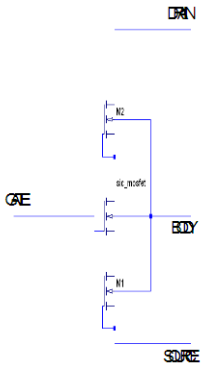
Key accomplishments – SiC MOSFET 300ºC operation





Key MOSFET parameters at RT and 300C

Parameters	300K	573K
$V_{threshold}$	-9V	-8.5V
I_{dsat}	30 mA/mm	10 mA/mm
G_m	4.6 mS/mm	1.7mS/mm
R_{sheet}(resistor)	11.8 kΩ/sq	41.8 kΩ/sq



Model features

- Scalable by setting the values of W and L
- Body effect on Drain and Source series resistance modeled with M1 and M2 FETs
- DC model (no capacitances included)
- Predictive of on-state I-V, does not model off-state leakage current

Key accomplishments – SiC op amp operation at 300ºC

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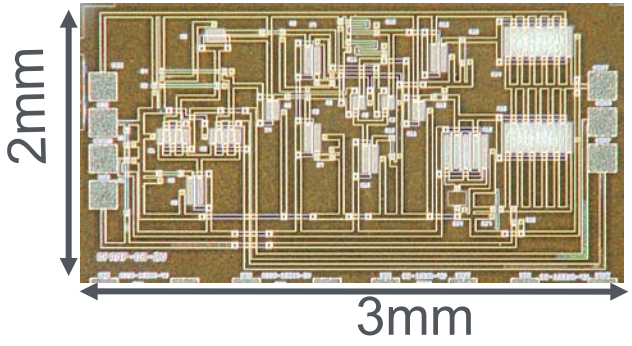
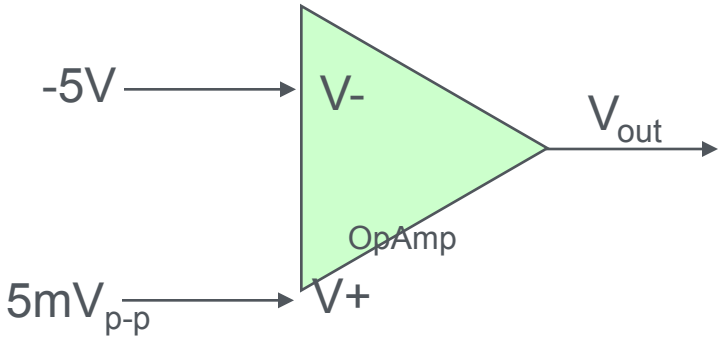
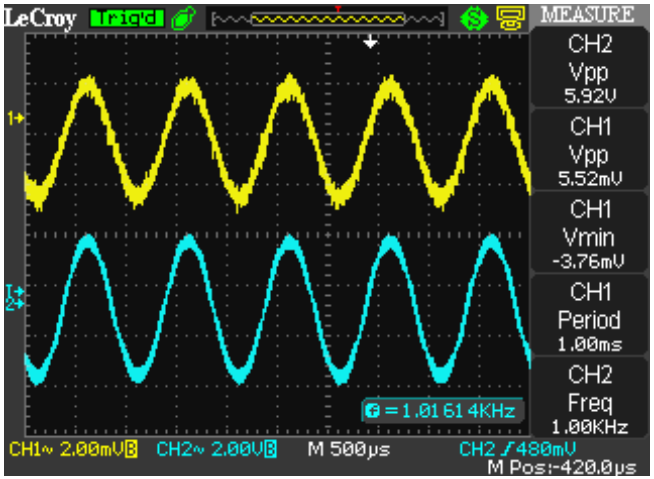
Picture of SiC op amp



The op amp circuit consists of 15 transistors and 17 resistors



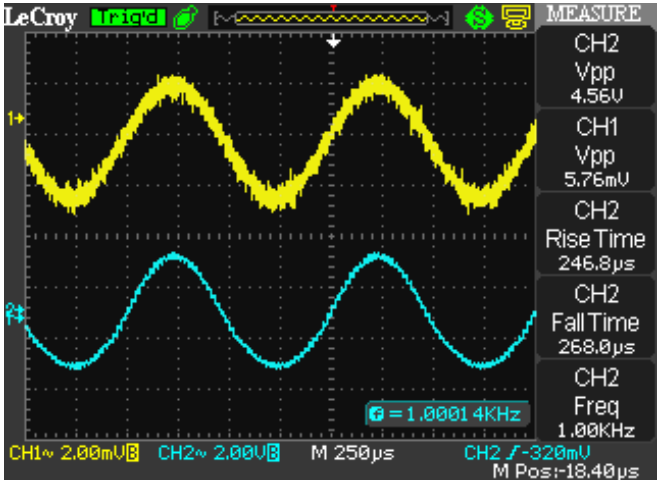
Room Temperature



input

output

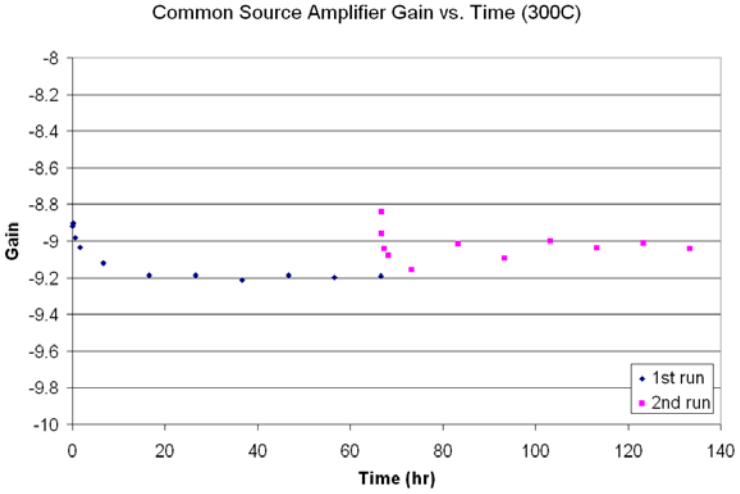
300C



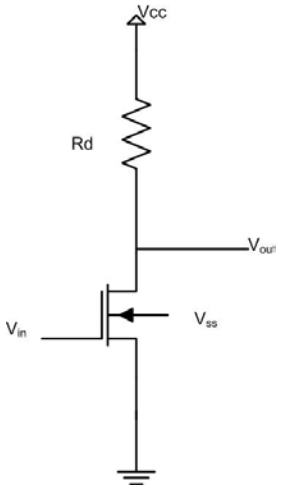
60dB gain @ 1kHz

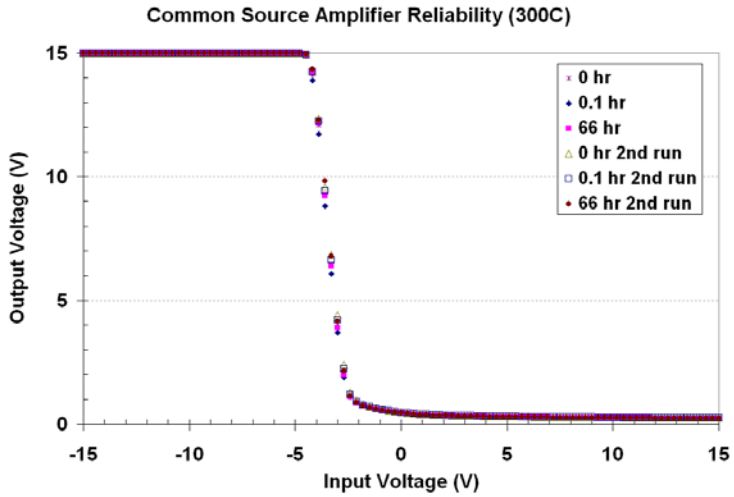
57.9dB gain @ 1kHz

Key accomplishments – SiC high temperature circuit stability



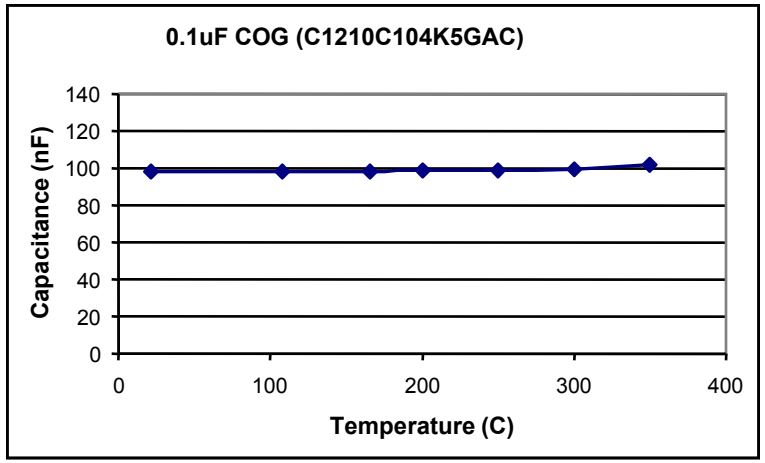
Common-source amplifier

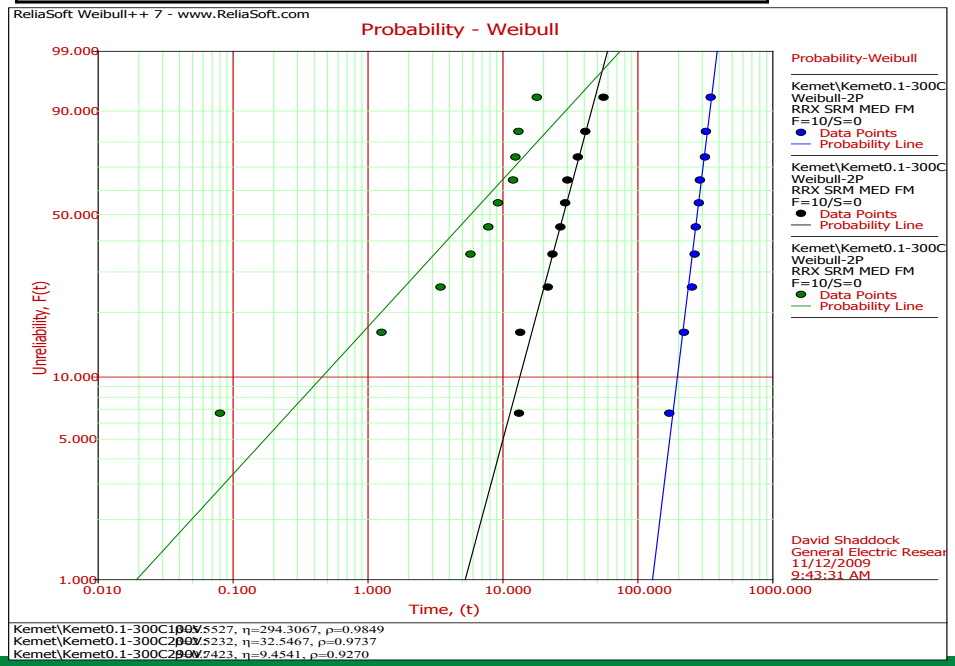


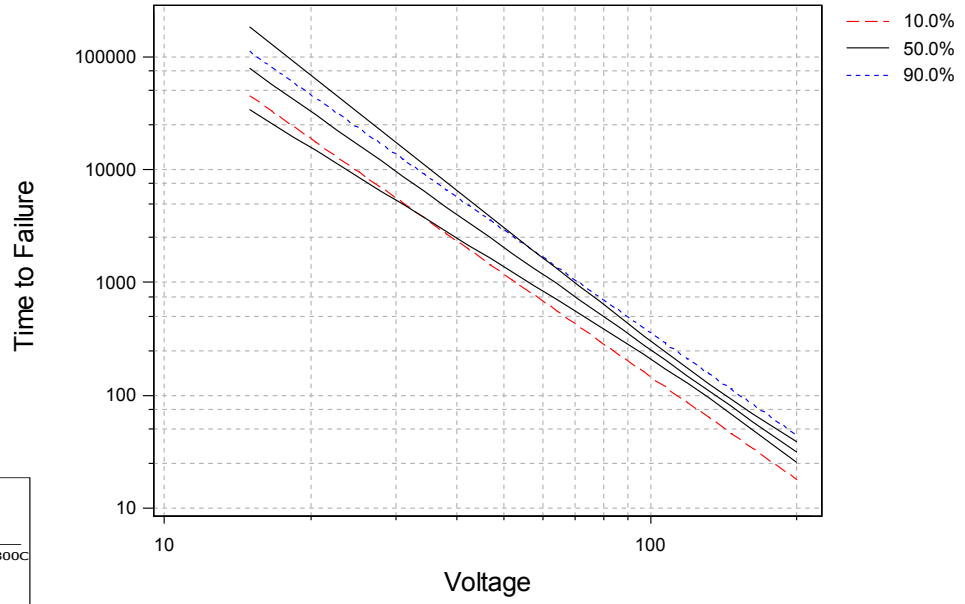


- The circuits were stressed so that maximum current flows through the transistor at 300ºC
- Very little drift of gain and input-output curves seen at 300ºC
- The dramatic improvement in stability and reliability compared to previous generations of SiC ICs is attributed to the improvement in the SiC gate oxidation process

Key accomplishments – lifetime of capacitors



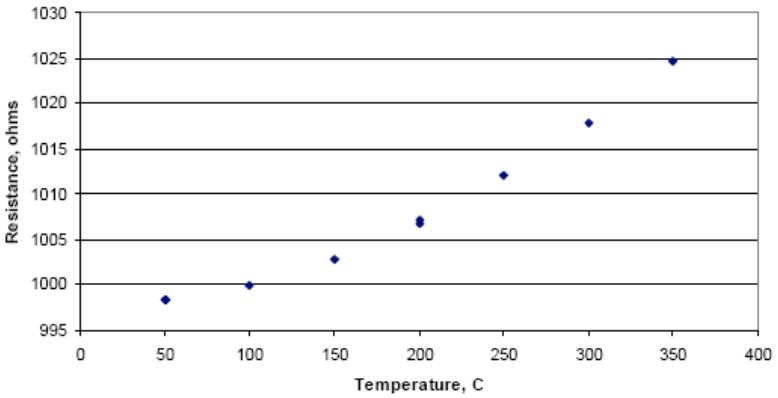




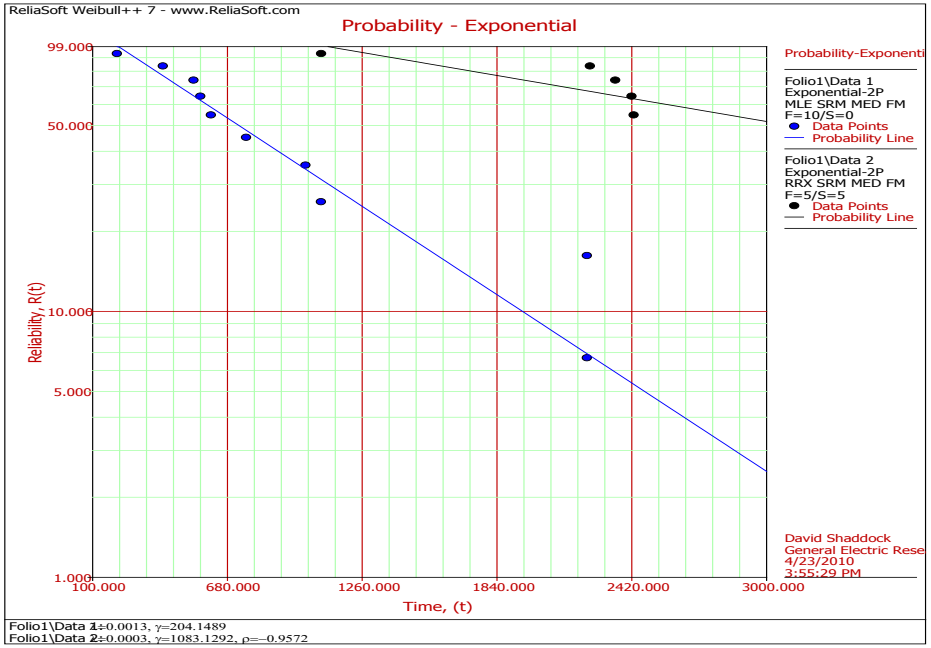
Value: 0.10uF, 50V, H dielectric
Temperature: 300C
Voltage Bias: 290, 200, 100
Model parameters: n=3.67 using 100 and 200V
Estimated Life: 17254 hrs at 25V

Key accomplishments – lifetime of resistors

1 kΩ thick film resistor

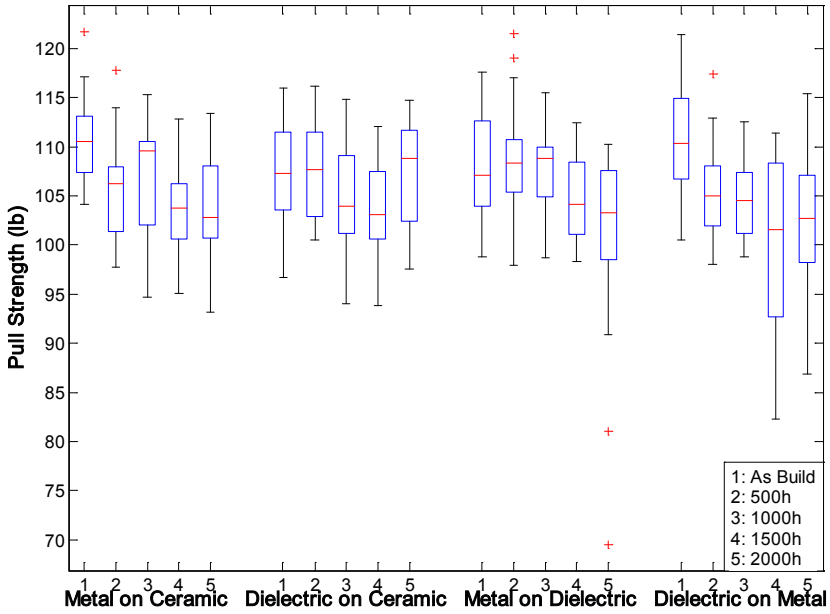


Temp=350C, 16V across DUT, 0.25W (at rating)
3529 hrs, 7 failures

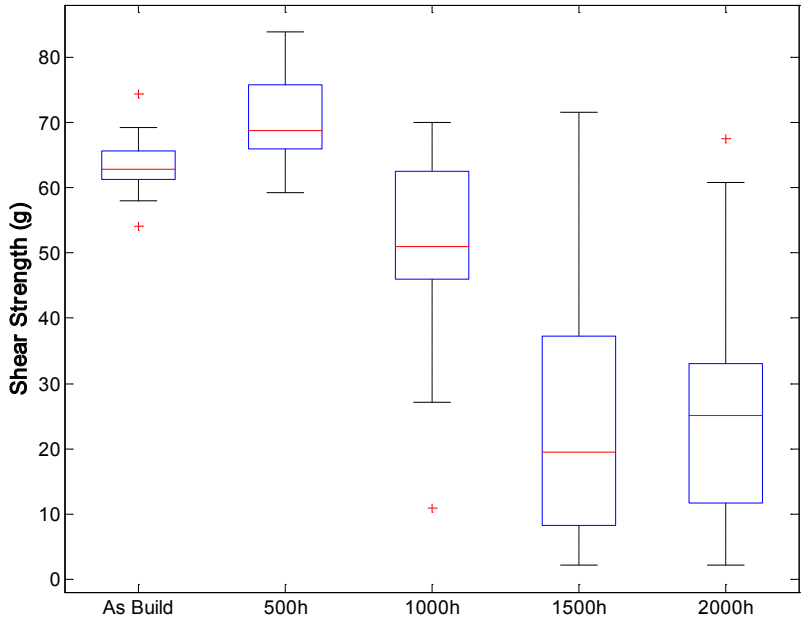


Mean life
962.3558 hours @ 1 % degradation
3994.9697 hours @ 2% degradation

Key accomplishments – 300C packaging process



Adhesion of dielectric(5951), metal(5771) and alumina substrate shows very little degradation at 300C

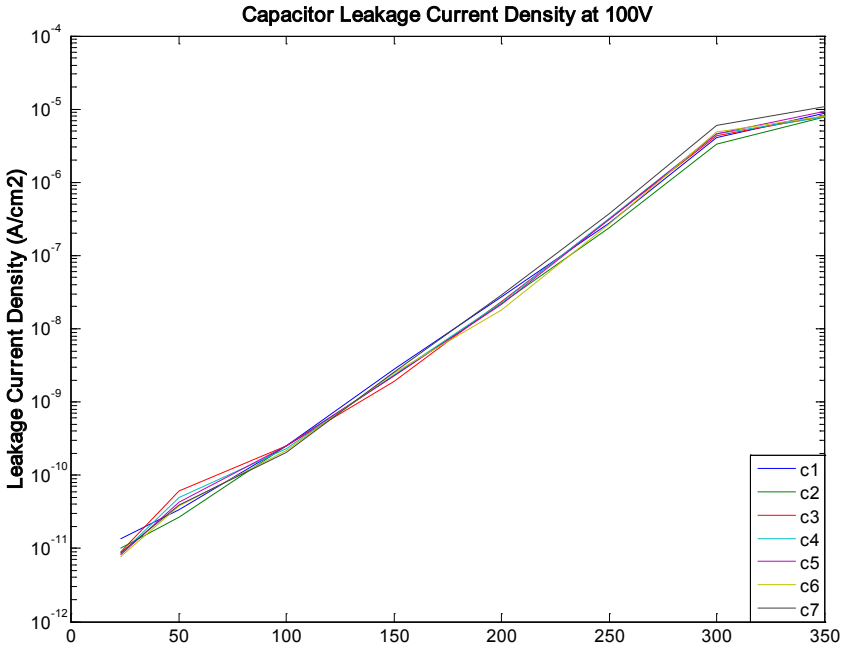


Ball bond shear strength decreases after 1500 hours at 300C – The decrease is related to diffusion of Ti into Au in the bond pads

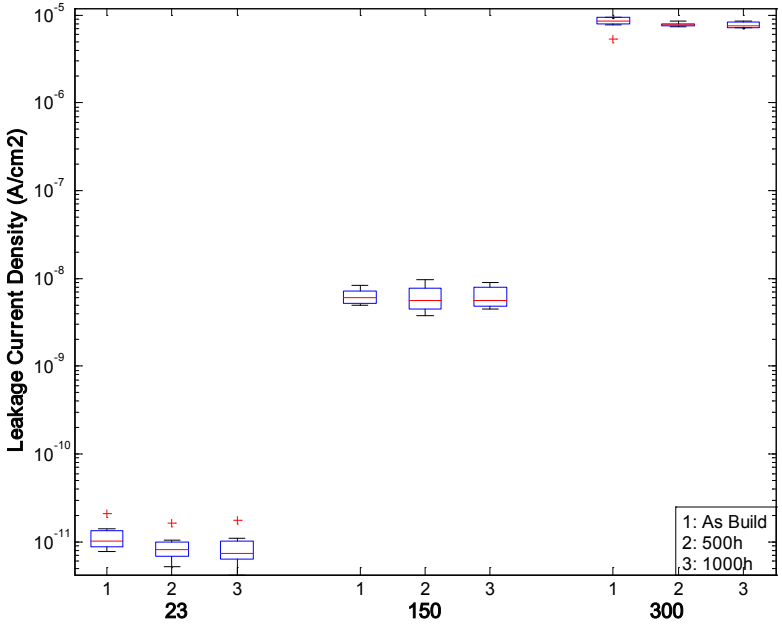
Key packaging steps

- Deposition of dielectric and conductor on alumina substrates
- Wire bonding of SiC die for electrical connection
- Attachment of SiC die and passive dies on alumina substrates and dielectric
  - Initial die attach strength was 11.3 kg/mm^2
  - 500 hour, 320ºC die attach strength was 3.7 kg/mm^2 – Sn diffusion is suspected as reason for reduction in die attach strength

Key accomplishments – 300C packaging process



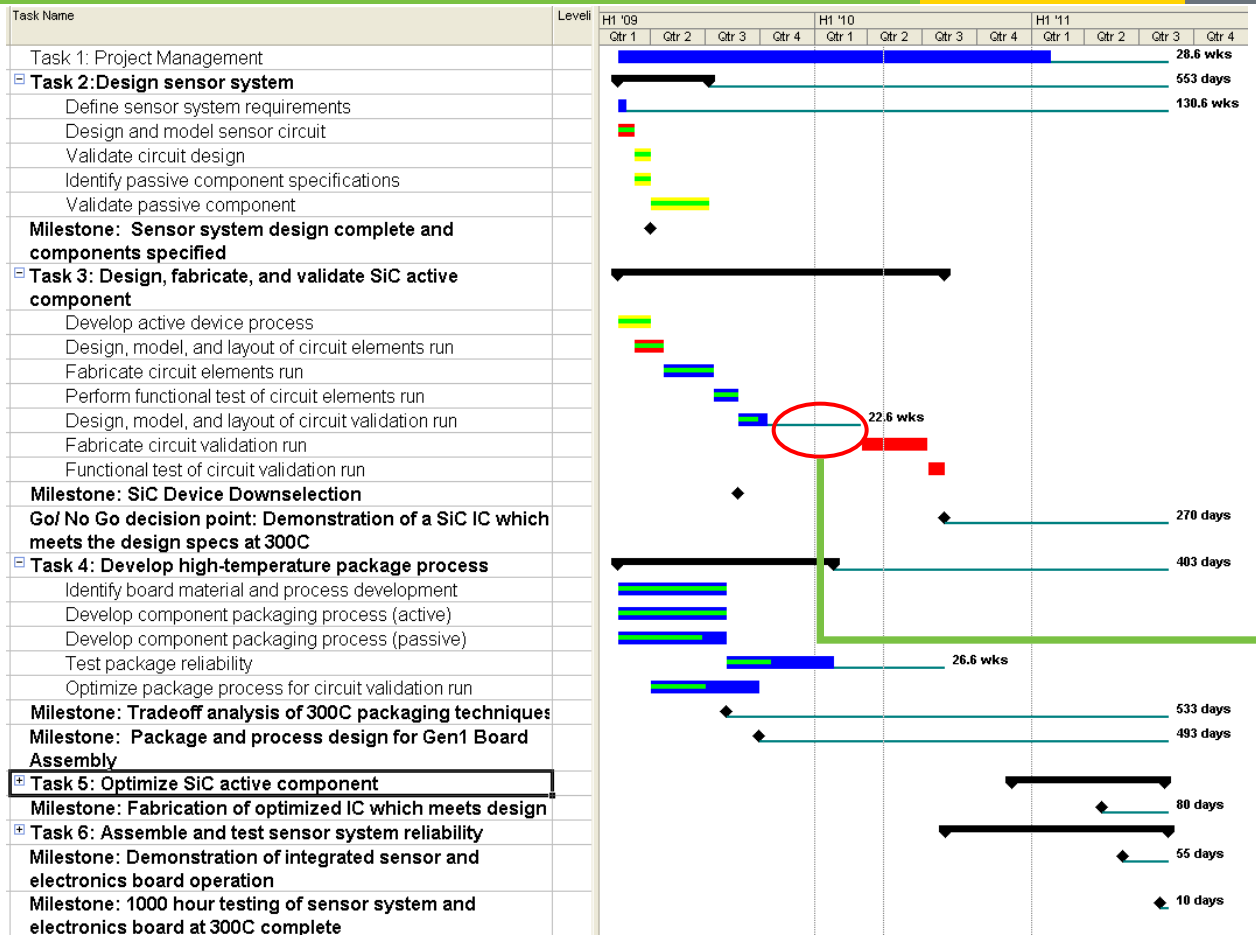
Leakage of alumina substrate as a function of temperature



Leakage of alumina substrate at different times and temperatures

- Leakage of alumina substrates are in the pA range, when scaled with area at 300ºC
- Leakage of alumina substrates does not increase significantly with time at 300ºC

Project schedule



2009 Spending profile

Q1 2009 - $184K
Q2 2009 - $258K
Q3 2009 - $190K
Q4 2009 - $289K

Delay in starting second lot because of a wafer breakage incident and long lead times from SiC suppliers (see supplemental information)

- Key milestones met so far
  - Sensor system design complete and components specified
  - SiC device selected
  - Package and process for Gen 1 board finalized

Project management – external collaborations and reporting

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- The high temperature electronics project so far has yielded 3 publications (see supplemental slide for reference)
- The results from this work will be presented at the High temperature electronics conference (HiTEC 2010)
- The boards developed under the program will be tested at Sandia National Labs under a supplementary program funded by DOE
- A second project for the development of telemetry module to multiplex multiple sensor inputs and to demonstrate a sensor system that consists of multiple pressure and temperature sensors operating at 300ºC has been funded by DOE through recovery act funding

Future directions

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Plans for FY 2010

- Complete fabrication of second lot of ICs and demonstrate op amps, comparators and voltage reference operating at 300ºC – July 2010
- **Fabricate a high temperature board that converts temperature to frequency** (Go/No-Go decision point) – August 2010
- Based on results of high temperature board, design optimized SiC ICs for operation at 300ºC –November 2010

Plans for FY 2011

- Complete fabrication of third lot of ICs – February 2011
- Fabricate optimized high temperature board – April 2011
- Complete 1000 hour testing of high temperature board – July 2011

Future Research

This project will demonstrate the feasibility of using SiC electronics at 300ºC in a **lab** environment.

If successful, the electronics will need to be field tested and is the next logical step in raising the technology readiness level (TRL).

Summary

- Geothermal drilling requires high temperature sensors and tools for well construction and reservoir characterization
- A key technology gap for high temperature tools us the electronics and packaging technology
- Silicon carbide IC technology and ceramic packaging technology can bridge that gap

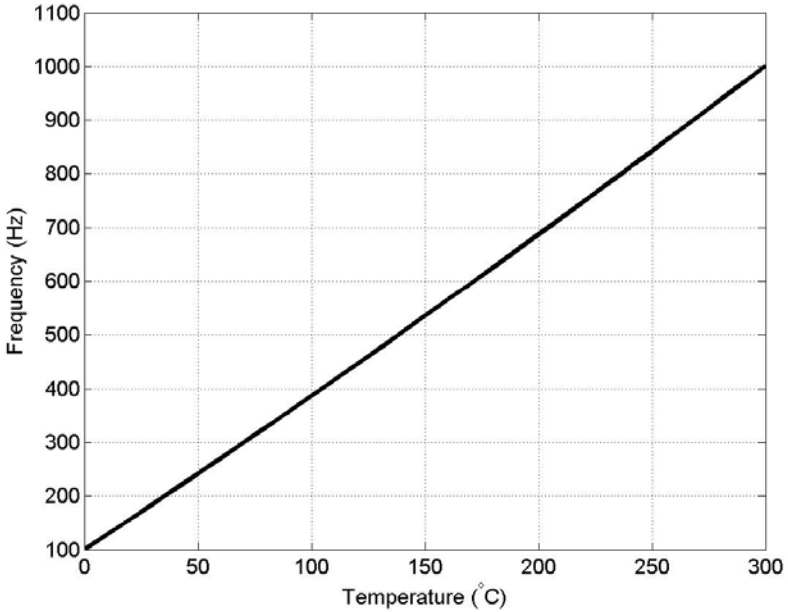
Year	Key technical results
2009	1. Designed a sensor system suitable for operation at 300ºC 2. Demonstrated SiC based op amp operating at 300ºC with open loop gain of 58 dB at 1 kHz – one of the most complicated ICs fabricated on SiC till date. 3. Identified and validated passive components for operation at 300ºC for 1000 hours 4. Developed a ceramic based packaging process for building an electronics board for 300ºC operation
2010	1. Fabricate a board that converts temperature to frequency based on SiC ICs and ceramic packaging 2. Design optimized SiC ICs based on results of board performance

Supplemental Slides

Publications

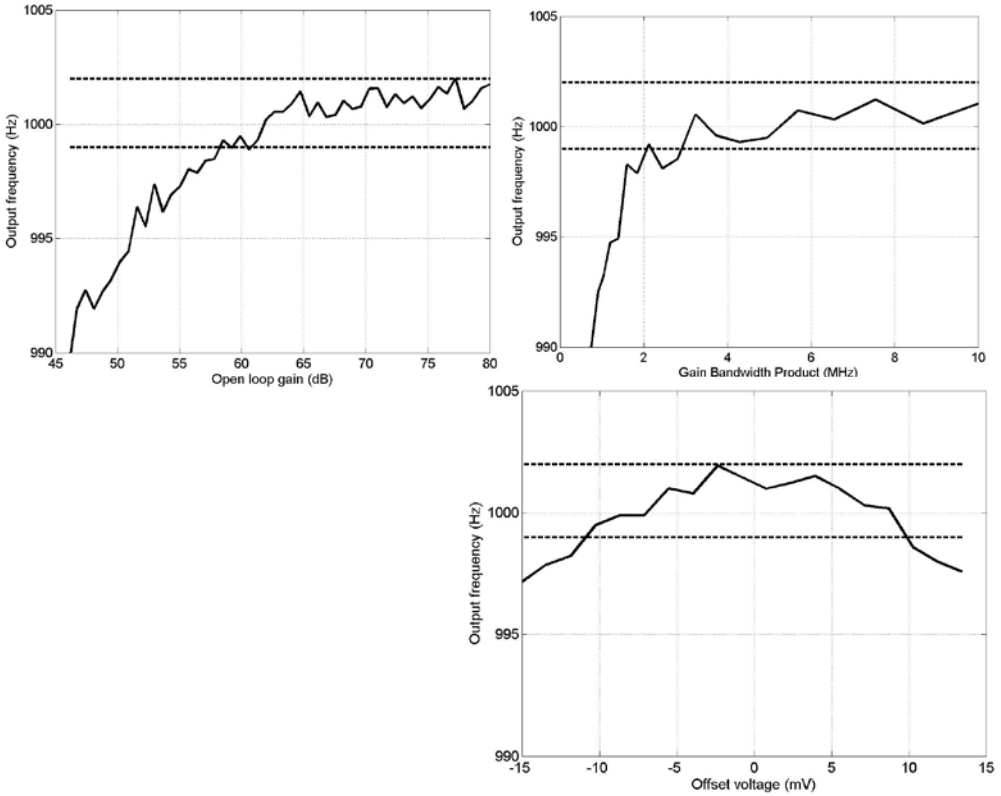
- V. Tilak, C-P Chen, P. Losee, E. Andarawis and Z. Stum, “Development of a 300ºC capable SiC based operational amplifier”, accepted for publication in the Proc. High Temperature Electronics Conf., Albuquerque, NM, May 11-13, 2010
- D. Shaddock, V. Tilak, T. Zhang, R. Zhang and R. Wayne Johnson, “Reliability assessment of passives for 300ºC using HALT”, accepted for publication in the Proc. High Temperature Electronics Conf., Albuquerque, NM, May 11-13, 2010
- R. Zhang, R. Wayne Johnson, V. Tilak, T. Zhang and D. Shaddock, “Characterization of Thick Film Technology for 300ºC Packaging”, accepted for publication in the Proc. High Temperature Electronics Conf., Albuquerque, NM, May 11-13, 2010

Scientific approach – board level simulations



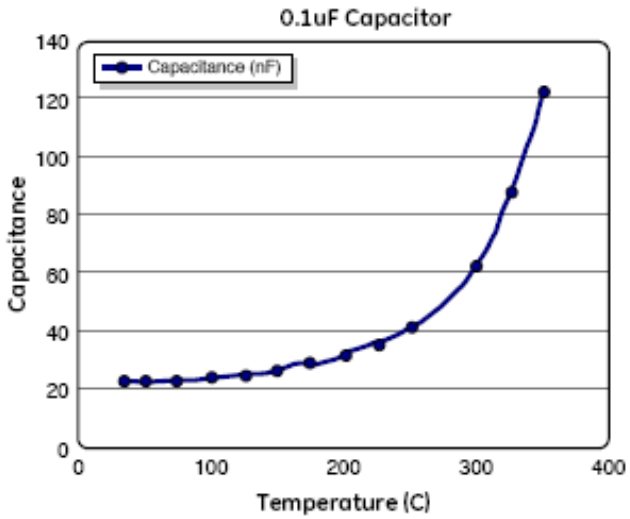
Frequency versus temperature

Error budget



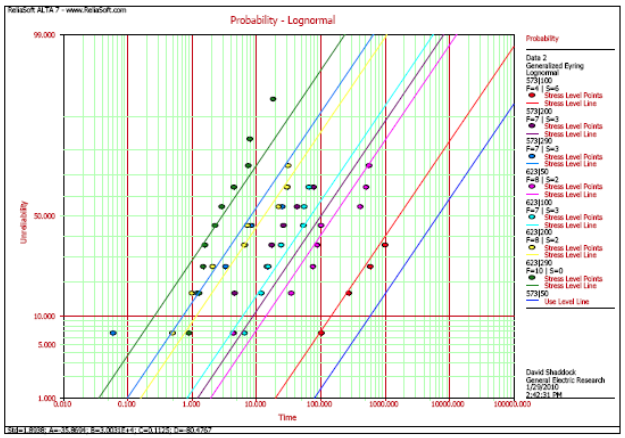
Targeting 1° C error in temperature from active components

Accomplishments – capacitors

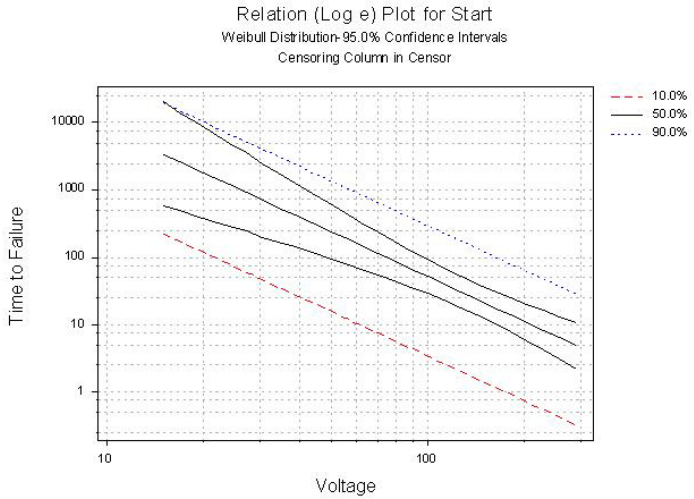


Large temperature coefficient of capacitance > 100%

Group	N	E_a	Mean
SiSc	1.85	3.5 eV	48454
$CaZrO_3$	3.67	NA	17254

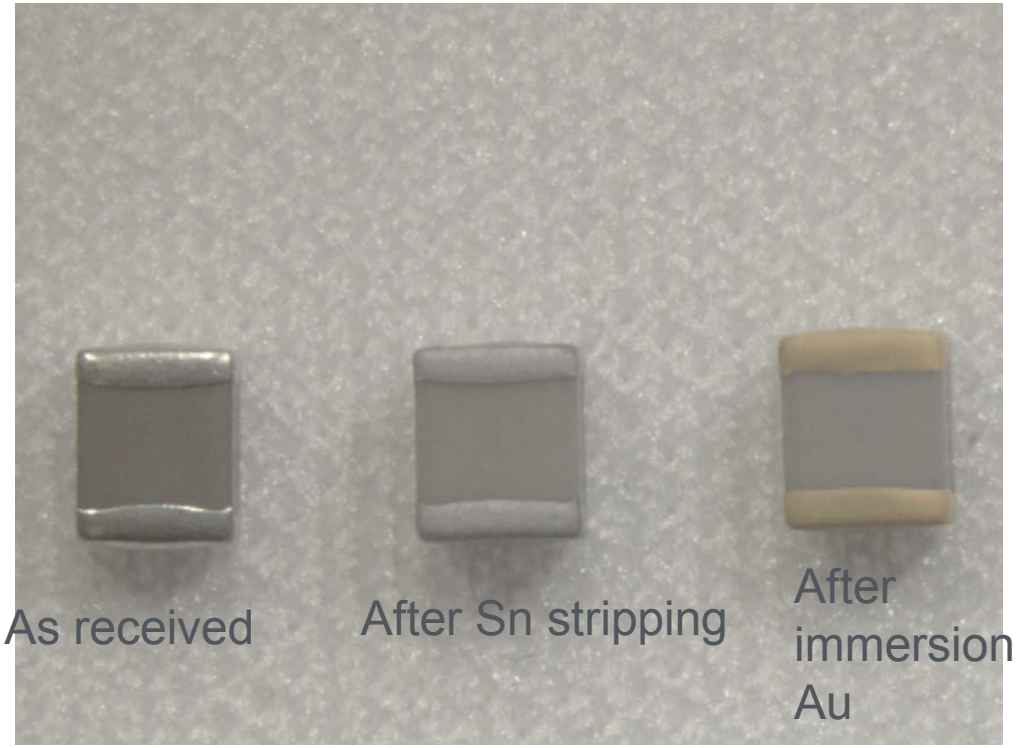


SiSc 0.1 uF capacitor HALT data (100V, 200V, 290V; 300ºC, 350ºC)



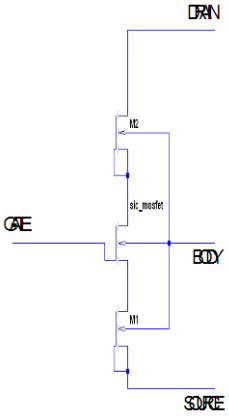
Projected lifetime of TRS capacitor at 15V is excess of 1000 hours at 350C

Accomplishments- capacitor termination



- Commercial off-the shelf (COTS) parts use Sn termination or AgPd termination and are therefore unsuitable for operation at 300C
- GE has developed a process for stripping the Sn and plating it with Au. The immersion gold is intended to preserve the solderability of the nickel surface until soldering using a high temperature solder. Nickel will diffuse through the gold at the use temperature and form a limiting oxide.

Accomplishments – Transistor SPICE models



Model features

- Does not include temperature coefficients (two models, one for RT and one for 300°C)
- Level 2 SPICE model
- Scalable by setting the values of W and L
- Body effect on Drain and Source series resistance modeled with M1 and M2 FETs
- DC model (no capacitances included)
- Predictive of on-state I-V, does not model off-state leakage current

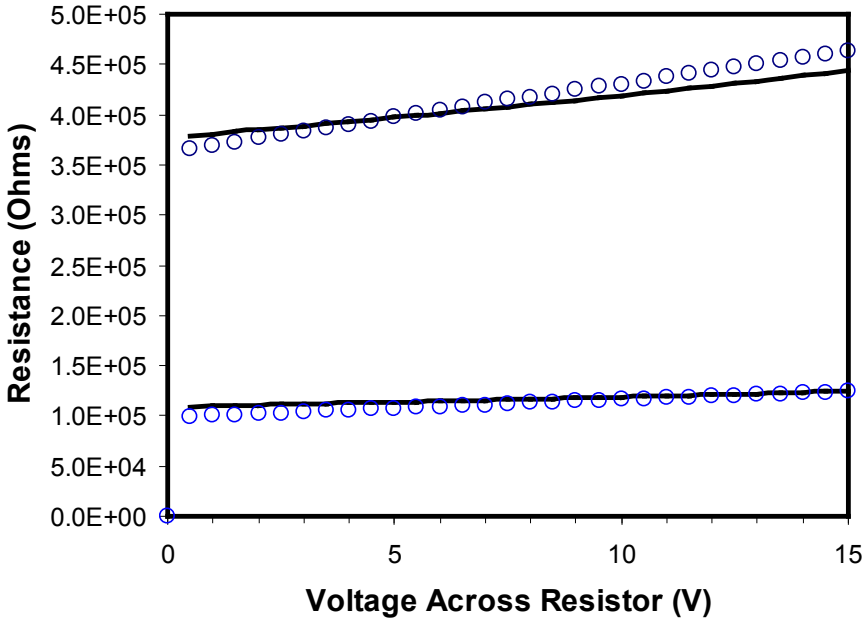
T= RT

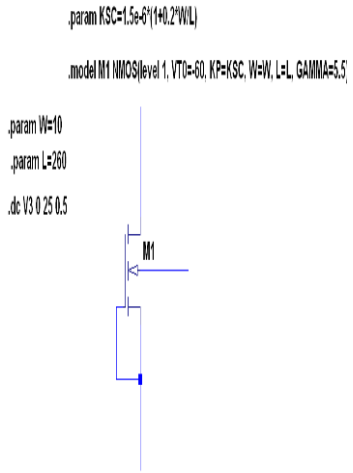
```
.model sic_mosfet NMOS (level 2,
Gamma=1.375, PHI=3, LAMBDA=LSC, VT0=-
9.2, KP=35e-6, UCRIT=3.8e4, Uexp=0.605,
Utr=0.5, TOX=0.5e-7, RD=RSC, RS=RSC,
W=200u, L=4u)
.model M1 NMOS(level1, VT0=-60, KP=KSC,
GAMMA=5.5, W=W, L=L)
.param W=200
.param L=4
.param LSC=8e-3*sqrt(6/L)
.param RSC=150
.param KSC=3e-6*(W/L)
```

T= 300ºC

```
.model sic_mosfet NMOS (level 2,
Gamma=1.375, PHI=3, LAMBDA=LSC, VT0=-
9.2, KP=12.4e-6, UCRIT=3.0e4, Uexp=0.58,
Utr=0.5, TOX=0.5e-7, RD=RSC, RS=RSC,
W=200u, L=4u)
.model M1 NMOS(level1, VT0=-60, KP=KSC,
GAMMA=5.5, W=W, L=L)
.param W=200
.param L=4
.param LSC=12e-3*sqrt(6/L)
.param RSC=584
.param KSC=1.1e-6*(W/L)
```

Accomplishments – Resistor SPICE models



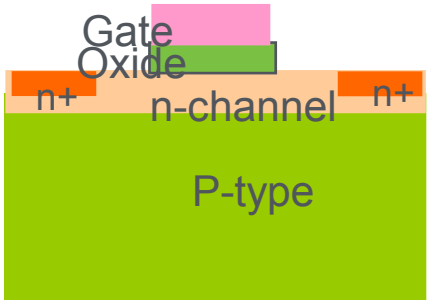



```
.para KSC=1.5e-6*(1+0.2*W/L)
.model M1 NMOS(level 1, VT0=-60, KP=KSC,
W=W, L=L, GAMMA=5.5)
.param W=10
.param L=260
.dc V3 0 25 0.5
```

Resistors are modeled as a transistor with gate and source shorted

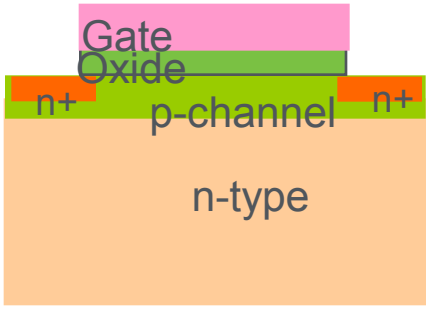
Resistor behavior depends on geometry and need standard geometry to better predict behavior

Scientific approach – SiC JFETs vs SiC MOSFETs



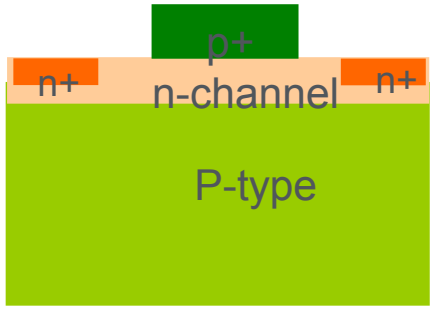
Depletion-mode MOSFET

- Normally on
- Low Efield intensity in drain region – Potentially higher reliability of gate oxide
- Can be driven in accumulation mode to increase the performance
- High mobility and performance due to the ease in scaling the device
- Electron trapping may cause drift issues



Enhancement-mode MOSFET

- Normally off
- Low power and more efficient use of semiconductor real estate
- Can be scaled easily to improve performance
- Low mobility due to poor oxide carbide interface leads to poor performance
- Threshold voltage temperature coefficient is much larger than in other devices making analog design more complicated



JFET

- Normally on
- Low Gate Voltage Operation
- No gate oxide – higher gate oxide reliability and low drift due to electron trapping
- Design is more challenging as the need to ensure gate does not turn on

Program management – broken wafers

- Wafers broken by SIMS vendor – broken wafers cannot run on Stepper lithography system and hence useless for the program
- New wafers were ordered and are in house
- Lot was started on March 22 and is expected to be completed by June